PM8316

TEMUX-84

HIGH DENSITY 84 T1/63 E1 FRAMER WITH INTEGRATED VT/TU MAPPERS AND M13 MULTIPLEXERS

TECHNICAL OVERVIEW

PROPRIETARY AND CONFIDENTIAL

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1 PURPOSE AND SCOPE OF THIS DOCUMENT

The PM8316 TEMUX-84 is a third-generation PMC-Sierra broadband access technology offering unparalleled density and flexibility ideal for Metro Optical access, Multi-Service switches and Edge router equipment. The PM8316 84/63 Channel T1/E1 Framer with Integrated VT/TU Mappers and M13 Multiplexers substantially simplifies the design of the following systems:

- High density multiplexers, multi-service switches, routers and digital modems
- Frame Relay switches and access devices (FRADS)
- SONET/SDH Add Drop and Terminal Multiplexers
- Optical Access Equipment
- Digital Access Cross-Connect Systems

By taking advantage of its Scaleable Bandwidth Interconnect (SBI) bus, the TEMUX-84 streamlines the design of access service architectures by providing seamless interconnect to PMC-Sierra's FREEDM packet processors and AAL1gator AAL1 SAR products. TEMUX-84 also supports H-MVIP bus to interconnect to MECA-4A Voice over ATM processor or to the MECA-4I voice over IP Processor.

This document provides an overview of PM8316 TEMUX-84, covering TEMUX-84's operational modes, key applications, functions, principle data paths, available diagnostics and finally the migration path from PM8315 TEMUX to this next-generation device. Full details of the PM8316 TEMUX-84 are available in the PMC-1991437 TEMUX-84 datasheet. In the event that there are contradictions between this document and the datasheet, the datasheet takes precedence.

2 DEVICE OVERVIEW

2.1 Operational Modes

The TEMUX-84 provides framing and multiplexing for 84 T1 channels or 63 E1 channels into three channelized DS-3's or alternatively maps the T1/E1 channels directly into a SONET/SDH OC-3. For higher line rate applications, four TEMUX-84's will support a channelized OC-12 data stream, 16 TEMUX-84 devices will support a channelized OC-48 data stream. DS3 and E3 unchannelized mode is also supported through a clock and data interface. Figure 1 provides a high-level view of TEMUX-84's various operational modes.

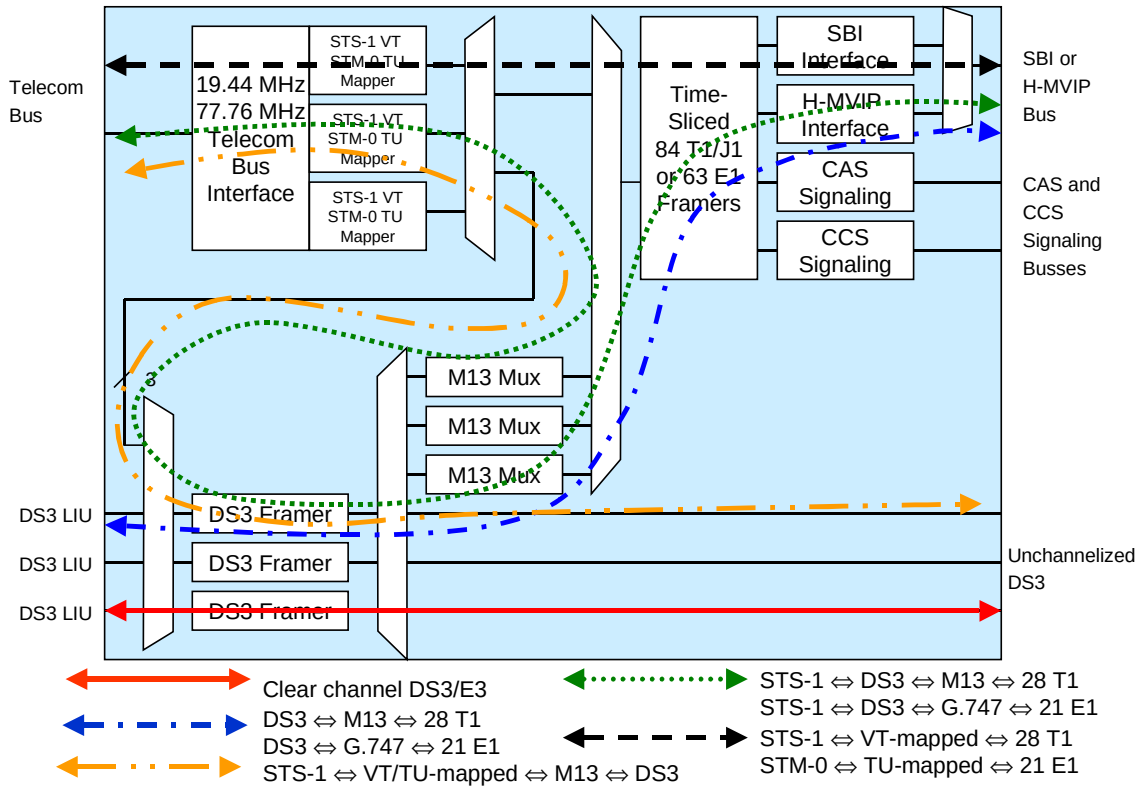

Figure 1 TEMUX-84 Operational Modes

TEMUX-84 supports various framing and mapping formats and standards that make it ideal for global applications. TEMUX-84's flexibility is illustrated below in Table 1, where TEMUX-84's broad range of supported standards is highlighted.

Table 1 PM8316 Flexible Functionality

FUNCTIONALITY	RATE			
	T1 (1.544 Mbits/s)	E1 (2.048 Mbits/s)	DS3 (44.736 Mbit/s)	E3 (34.368 Mbps)
Framing	√ SF √ SLC-96 √ ESF	√ ITU-T G.704 basic √ CRC-4 multiframe (ITU-T G.706 framing)	√ M23 √ C-bit parity formats	√ G.751 √ G.832 E3
Mapping – Bit asynchronous/Byte synchronous	√ VT1.5->STS-1 SPE √ TU-11->STM-1/VC3 √ TU-11->TUG3->STM-1/VC4 √ TU-12->STM-1/VC3 √ TU-12->TUG3->STM-1/VC4	√ VT-2->STS-1 SPE √ TU-12->STM-1/VC3 √ TU-12->TUG3->STM-1/VC4	√ DS3->VC3->AU3->STS-1 SPE	———
Multiplexing	M13	G.747	———	———

Along with supporting T1 and E1 framing and mapping, TEMUX-84 also supports TTC JT-G.704 multiframe formatted J1 framing. The alternate CRC-6 calculation is also available in PM8316 for Japanese applications.

2.2 Line-Side Interfaces

2.2.1 Telecom Bus

The TEMUX-84 offers either a 19.44 MHz or 77.76 MHz Telecom bus for direct interface to the SPECTRA Payload Extractor/Aligner product family. The Telecom Bus is an 8-bit parallel bus. Clocked at 19.44 MHz, the Telecom Bus can move up to 155 Mbit/s, at 77.76 Mbit/s this bus can add and drop up to 622 Mb/s. The 77.76 MHz high speed Telecom bus allows up to four TEMUX-84s to interface to a single SPECTRA-622, offering a full OC-12 data stream through a single bus.

2.2.2 Line Side Interface Summary

Table 2 shows the line side interface options supported by TEMUX-84.

Table 2 Line Side Interfaces

Line Rate	Telecom Bus (19.44 or 77.76 MHz)	DS3 clock and data	E3 clock and data
T1 (1.544 Mbit/s)	✓	✓	
E1 (2.048 Mbit/s)	✓		
J1 (1.544 Mbit/s)	✓		
DS3 (44.736 Mbit/s)	✓	✓	
E3 (34.368 Mbit/s)			✓

2.3 System-Side Interfaces:

2.3.1 H-MVIP bus

The 8 Mbit/s High-Density Multi-Vendor Interface Protocol (H-MVIP) bus simplifies interfaces between TEMUX-84 and the link layer devices connected to it. TEMUX-84 provides 21 H-MVIP data interfaces for synchronous access to all the DS0s of all 84 T1 links or all the timeslots of all 63 E1s. TEMUX-84 also provides 21 H-MVIP interfaces for access to the channel associated signaling (CAS) bits for all T1 DS0s or E1 timeslots along with three 8 Mbit/s H-MVIP interfaces for common channel signaling (CCS) channels and V5.1 and V5.2 control channels. H-MVIP access for CAS is also available as an optional replacement for CAS access over the SBI bus.

2.3.2 Scaleable Bandwidth Interconnect (SBI) Bus

The TEMUX-84 also supports Scaleable Bandwidth Interconnect (SBI) Bus on the system side for access to multiple devices on a common bus. The SBI bus is based on TELECOMBUS. It is also an 8-bit-wide parallel bus offering either a 19.44 MHz or 77.76 MHz clock rate, allowing it to move up to 622 Mbits/s of data. The 77.76 MHz bus can support up to four TEMUX-84s and several link layer devices.

System Side Interface Summary Table 3 shows TEMUX-84's system side interface alternatives.

Table 3 System Side Interfaces

Line Rate	SBI Bus (19.44 or 77.76 MHz)	DS3 serial clock and data	H-MVIP	E3 serial clock and data
T1 (1.544 Mbit/s)	✓		✓	
E1 (2.048 Mbit/s)	✓		✓	
J1 (1.544 Mbit/s)	✓		✓	
DS3 (44.736 Mbit/s)	✓	✓		✓
E3 (34.368 Mbit/s)				
Arbitrary Data Streams	✓			

2.4 Device Description

The TEMUX-84 provides jitter attenuation in the T1/E1 tributary receive and transmit directions, as well as providing three independent de-jittered T1 or E1 recovered clocks for system timing and redundancy. PM8316 also provides PRBS generators and detectors at DS3 and E3 rates and on each tributary for error testing at T1, E1 and NxDS0 rates as recommended in ITU-T 0.151, 0.152. The TEMUX-84 has a generic 8-bit microprocessor bus interface for configuration, control and status monitoring. It supports a standard five signal P1149.1 JTAG test port for boundary scan board test purposes. The TEMUX-84 is implemented using low power 1.8 V/3.3 V CMOS technology with 5V tolerant pins. It is available in a high-density 324-pin fine pitch Plastic Ball Grid Array Package (PBGA) with dimensions of 23mm x 23mm.

3 APPLICATION EXAMPLES

TEMUX-84's mapping function coupled with PMC-Sierra's SPECTRA SONET/SDH product family is ideal for Optical Access Equipment. Through the SONET/SDH Telecom Bus, either at 19.44 MHz or 77.76 MHz, optical scalability is achieved from OC-3 to OC-48. For lower speed applications DS3 LIUs are interfaced to TEMUX-84 directly through clock and data. The ability to scale from DS3 to OC-48 with PMC-Sierra's TEMUX-84 is illustrated in Figure 2.

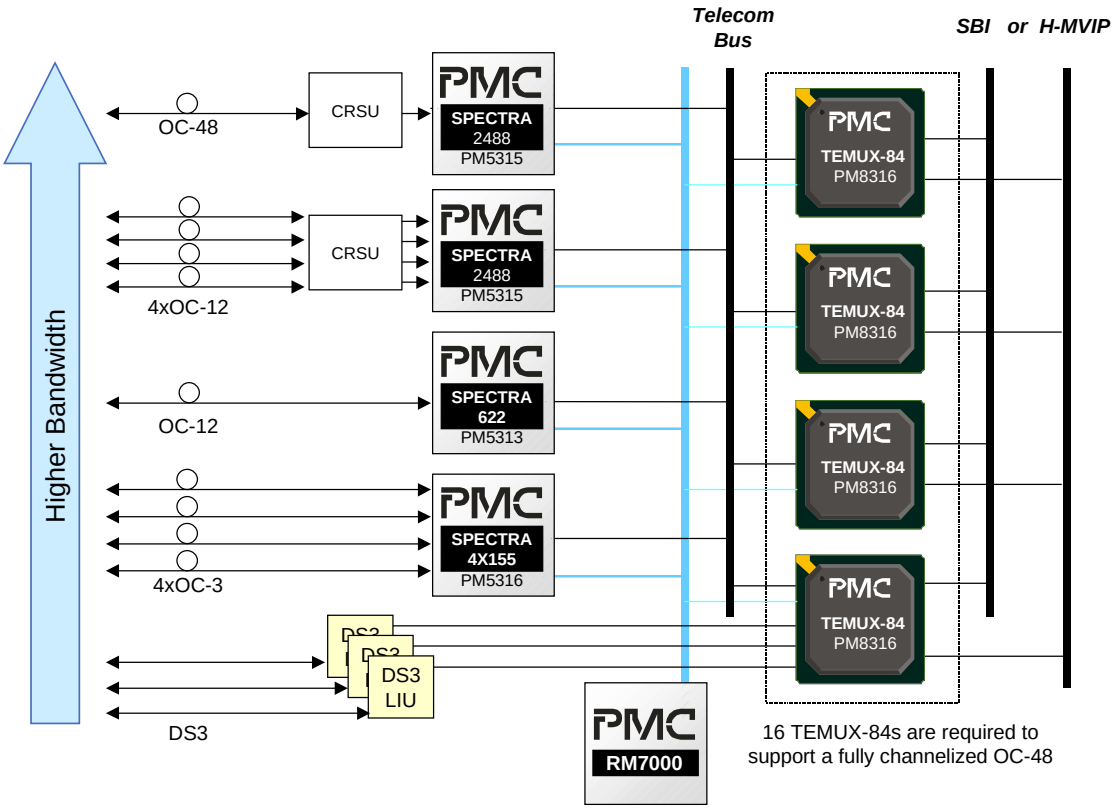

Figure 2 Scalability from DS3 to OC-48 in single port card designs with TEMUX-84

TEMUX-84 is also ideal for multi-service applications. By leveraging its seamless interface to PMC's broad range of link layer products through the SBI bus, TEMUX-84 enables Any-Service Any-Port architectures as shown in Figure 3. In this application PMC's FREEDM products provide High Density HDLC packet processing. PMC's AAL1gator product family provides line interface access to ATM Adaptation Layer 1 (AAL1) Constant Bit Rate (CBR) ATM networks, enabling a broad range of circuit emulation services. The Voice over ATM and Voice over IP application space is addressed with PMC's MECA-4A and MECA-4I devices respectively.

On the system side of this architecture the S/UNI ATLAS and S/UNI-APEX together provide per-VC ATM buffering, scheduling, policing and OA&M for all traffic. PMC's RM7000A microprocessor is ideally suited as the controller for both applications illustrated in Figure 2 and Figure 3.

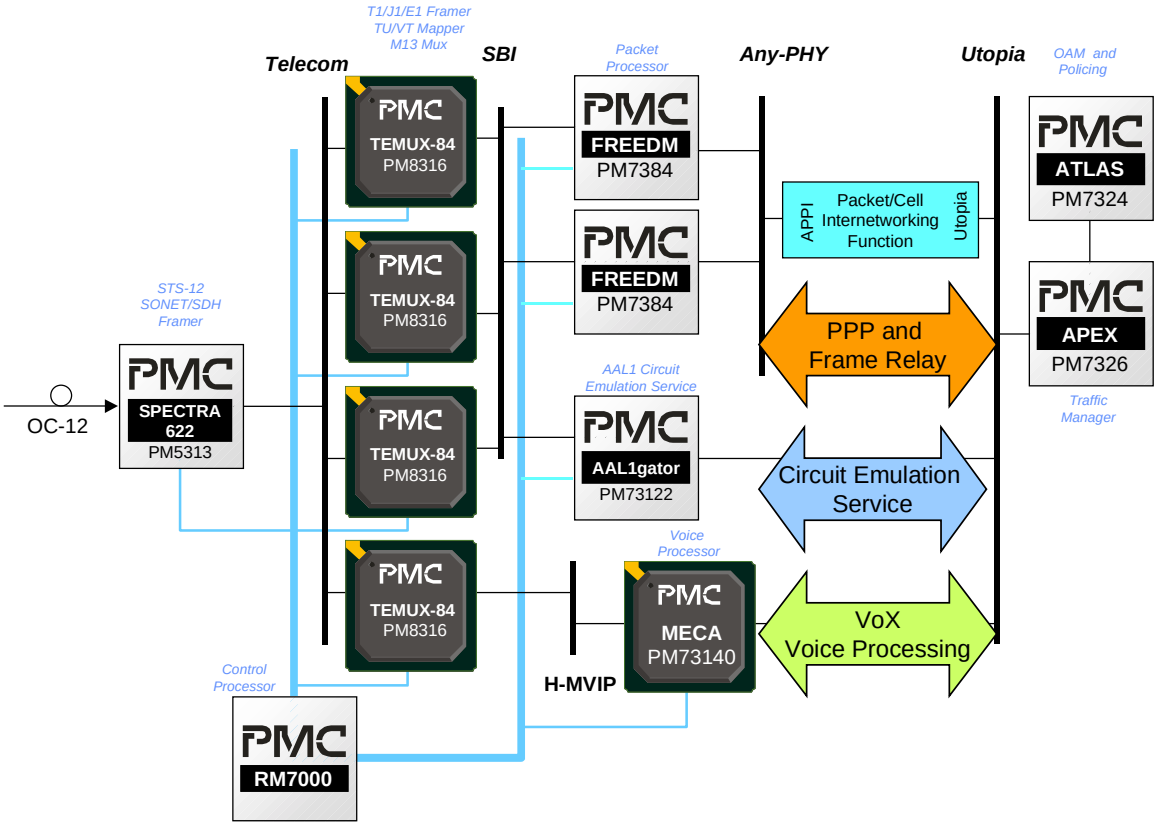

Figure 3 Any-Service Any Port Applications enabled with the SBI Bus

4 FUNCTIONAL OVERVIEW

4.1 Major Functional Blocks

This section describes the major functional blocks of TEMUX-84. A simplified block diagram of the complete TEMUX-84 is shown below in Figure 4. PM8316 enables T1 links to be multiplexed into the DS3s, mapped into the telecom bus as SONET VT1.5 virtual tributaries or mapped as SDH TU-11 or TU-12 tributary units. E1 links can be mapped into the telecom bus as SONET VT2 virtual tributaries or as SDH TU-12 tributary units.

System-side access to the T1s and E1s is available through the Synchronous H-MVIP interfaces or the SBI bus. DS3 line-side access is provided via the clock and data interface for line interface units (LIUs), or as DS3s mapped into the SONET/SDH Telecom bus. Unchannelized DS3 system-side access is available through the SBI bus. TEMUX-84 offers four major functions –T1 and E1 framing, M13 Multiplexing, DS3 and E3 Framing and SONET/SDH Mapping.

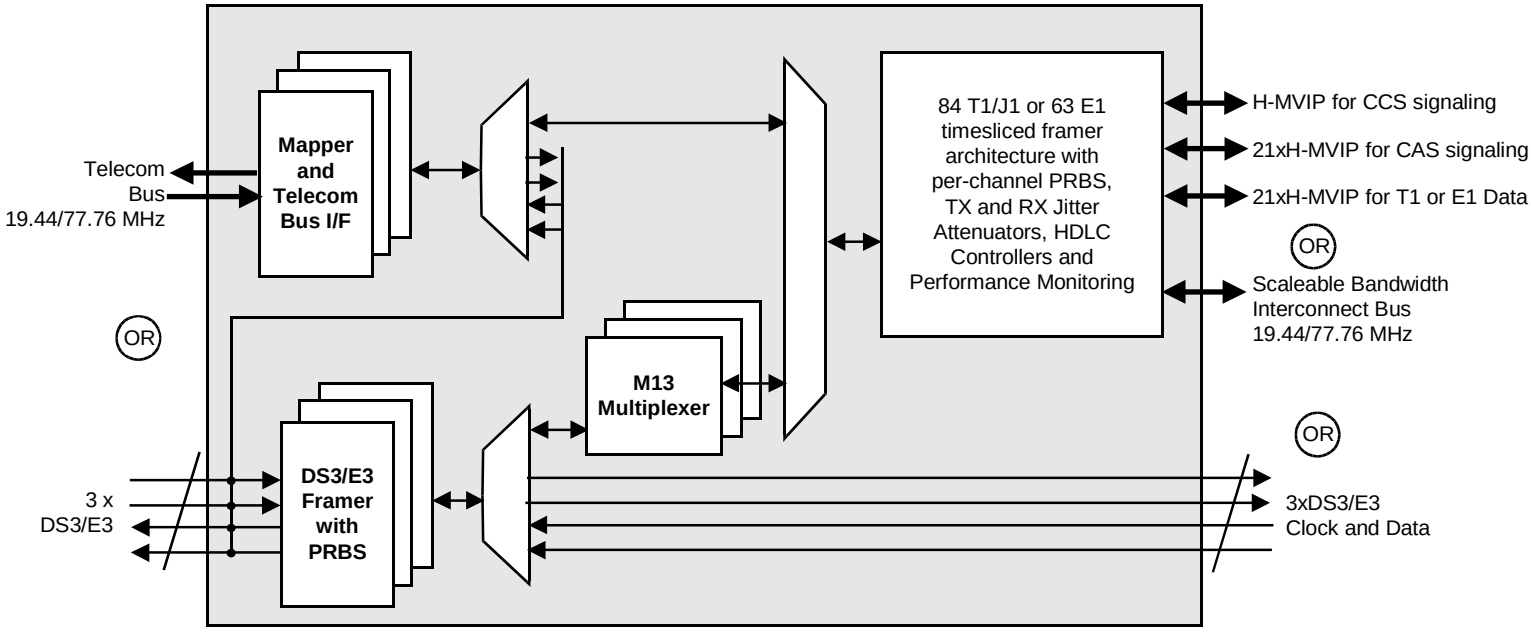

Figure 4 TEMUX-84 Block Diagram

4.2 T1/J1 Framer Functions

TEMUX-84 uses a time-sliced framer architecture to frame up to 84 T1 channels. In the ingress direction, each of the 84 T1 framers is either demultiplexed from a channelized DS3, or extracted from a SONET VT1.5, TU-11 or TU-12 mapped bus. The TEMUX-84 can be configured to either frame each T1 signal using Super Frame (SF), Extended Super Frame (ESF) or Subscriber Loop Carrier –96 (SLC-96) or to bypass each T1 framer (unframed mode). Each of the T1 framers and transmitters is independently software configurable, allowing timing master and feature selection without changes to external wiring.

Each T1 framer detects and indicates the presence of Yellow and AIS patterns. They also integrate Yellow, Red, and AIS alarms.

The TEMUX-84 offers T1 performance monitoring, with accumulation of:

- CRC-6 errors
- Framing bit errors
- Out-of-frame events
- Changes of frame alignment

The TEMUX-84 also detects the presence of ESF bit-oriented codes, and detects and terminates HDLC messages on the ESF data link. A 128 byte FIFO terminates the HDLC messages.

The TEMUX-84 offers an elastic store, which optionally supports slip buffering and adaptation to backplane timing. A signaling extractor supports signaling debounce, signaling freezing, and interrupt on signaling state change on a per-DS0 basis. The TEMUX-84 also offers:

- Idle code substitution and detection
- Digital milliwatt code insertion
- Data extraction
- Trunk conditioning
- Data sign and magnitude inversion
- Pattern generation or detection on a per-DS0 basis

In the transmit direction, the TEMUX-84 generates framing for 84T1s into either three channelized DS3s or a SONET/SDH mapped add bus. Each T1 transmitter frames to SF, ESF or SLC-96 DS1 formats. Optionally, T1 framing can be disabled. The TEMUX-84 supports:

- Signaling insertion
- Idle code substitution
- Data insertion
- Line loopback
- Inband Code Loopback
- Data inversion
- Zero-code suppression on a per-DS0 basis

The TEMUX-84 offers PRBS generation or detection on a framed and unframed T1 basis.

The TEMUX-84 can generate a low jitter transmit clock. It also offers jitter attenuation in the receive path. Three low-jitter recovered T1 clocks can be routed outside the TEMUX-84 for network timing applications.

In synchronous backplane systems, the TEMUX-84 offers 8 Mb/s H-MVIP interfaces for:

- Access to 2016 DS0 channels
- Channel associated signaling (CAS) for all 2016 DS0 channels
- Common channel signaling (CCS) for all 84 T1s

The TEMUX-84 multiplexes the DS0 channel H-MVIP interface and CAS H-MVIP interface with the SBI interface. The CCS signaling H-MVIP interface is independent of the DS0 channel and CCS H-MVIP interface. The use of any of the H-MVIP interfaces requires the use common clock and frame pulses along with T1 slip buffers.

For J1 applications, TEMUX-84 supports TTC JT-G.704 multiframe formatted J1 framing. The alternate CRC-6 calculation is also available in PM8316 for Japanese applications.

4.3 E1 Framer Functions

TEMUX-84 time-sliced architecture also frames up to 63 E1 channels. In the ingress direction, the TEMUX-84 extracts each of the 63 E1 signals from the SONET/SDH VT2 or TU-12 mapped bus and frames them to the E1 signals. Each of the E1 framers and transmitters is independently software configurable, allowing timing master and feature selection without changes to external wiring. E1 tributaries may be mixed at a VC-3/TUG-3/DS3 granularity. Each E1 framer detects and indicates the presence of remote alarm and AIS patterns. They also integrate Red and AIS alarms.

The E1 framers offer detection of various alarm conditions, such as loss of frame, loss of signaling multiframe and loss of CRC multiframe. The E1 framers also support reception of the following alarm signals:

- Remote alarms
- Remote multiframe alarms
- Alarm indications
- Time slot 16 alarm indications

The TEMUX-84 offers E1 performance monitoring, with accumulation of:

- CRC-4 errors
- Far-end block errors
- Framing bit errors

The TEMUX-84 offers a receive HDLC controller for the detection and termination of messages on the national use bits. The TEMUX-84 offers detection of the 4-bit Sa-bit code words (defined in ITU-T G.704 and ETSI 300-233) and V5.2 link ID signals. The TEMUX-84 can generate an interrupt on any change of state of the 4 bit Sa code words.

The TEMUX-84 offers an ingress elastic store for slip buffering and rate adaptation to backplane timing. The TEMUX-84 offers receive-side data and signaling trunk conditioning. It also offers a signaling extractor that supports:

- Signaling debounce
- Signaling freezing
- Idle code substitution
- Digital milliwatt tone substitution
- Data inversion
- Signaling bit fixing on a per-channel basis

In the egress direction, the TEMUX-84 generates framing for 63 E1s and maps the signals into a SONET/SDH add bus. Each E1 transmitter generates framing for a basic G.704 E1 signal. Optionally, the signaling multiframe alignment structure and the CRC multiframe structure can be inserted. In addition, framing can be disabled. The TEMUX-84 supports transmission of the 4-bit Sa code words (defined in ITU-T G.704 and ETSI 300-233). In addition, it offers PRBS generation or detection on a framed and unframed E1 basis.

4.4 M13 Multiplex/DS3 Framer

TEMUX-84 can be used as a M13 Multiplexer as well as a DS3 framer. When the TEMUX-84 is configured as a DS3 multiplexer/demultiplexer or DS3 framer, it accepts and outputs one or both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.

In the DS3 receive direction, the TEMUX-84 frames to DS3 signals with a maximum average reframe time of 1.5 ms in the presence of 10^{-3} bit-error-rate. It also detects the following problems:

- Line code violations
- Loss of signal
- Framing bit errors
- Parity errors
- C-bit parity errors
- Far-end block errors
- AIS
- Far end receive failure
- Idle code

The DS3 framer is an off-line framer, indicating both out-of-frame (OOF) and change-of-frame-alignment (COFA) events. The error events (such as C-bit, FEBE) are still indicated while the framer is OOF, based on the previous frame alignment.

When in C-bit parity mode, the TEMUX extracts the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels. The TEMUX-84 HDLC receivers support Path Maintenance Data Link. In addition, the TEMUX-84 detects the valid bit-oriented codes in the FEAC channels. It makes them available through the microprocessor port.

The TEMUX-84 offers DS3 error event accumulation, which accumulates:

- Framing bit errors
- Line code violations
- Excessive zeros occurrences
- Parity errors
- C-bit parity errors
- Far-end block errors

Error accumulation continues even while the off-line framers are indicating OOF. The counters are intended to be polled once per second, and are sized so as not to saturate at a 10^{-3} bit-error-rate. The transfer of count values to holding registers is initiated through the microprocessor interface.

In the DS3 transmit direction, the TEMUX-84 inserts DS3 framing, X, and P bits. When enabled for C-bit parity operation, the TEMUX offers bit-oriented code transmitters and HDLC transmitters. These transmitters insert the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals, Far End Receive Failure, and idle signals can be inserted using internal registers. TEMUX-84 can also be configured for automatic insertion when errors arrive.

When M23 operation is selected, the TEMUX-84 forces the C-bit Parity ID bit (the first C-bit of the first M sub-frame) to toggle. Thus, downstream equipment will not confuse an M23-formatted stream with stuck-at-1 C-bits for C-bit Parity application. Transmit timing is from an external reference or from the receive-direction clock.

Configured as a DS3 framer, the unchannelized payload of the DS3 link is available to an external device.

4.5 E3 Framer

TEMUX-84 can also be used as a high-density unchannelized E3 framer. In the receive direction TEMUX-84 frames to G.751 and G.832 E3 unchannelized framing formats. For G.832 the Trail Trace and either the Network Requirement or the General Purpose data link is terminated.

In the transmit direction, TEMUX-84 provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion and diagnostic features. For G.832, the Trail Trace is inserted and an integral HDLC transmitter is provided to insert either the Network requirement or the General Purpose data link.

4.6 SONET/SDH Mapper Operation

The SONET/SDH line-side interface processes and generates:

- STS-1 SPEs (Synchronous Payload Envelopes)
- TUG3 tributary unit groups within a VC4 virtual container
- VC3 virtual containers

The payload processor aligns and monitors the performance of SONET virtual tributaries (VTs) or SDH tributary units (TUs). Maintenance functions per tributary include detection of the following problems:

- Loss of pointer
- AIS alarms
- Tributary path signal label mismatch
- Tributary path signal label unstable alarms

Optionally, interrupts can be generated from the assertion and removal of any of the above alarms.

The TEMUX-84 accumulates counts for tributary-path BIP-2 errors on a block or bit basis and FEBE indications. The synchronous-payload envelope generator generates all tributary pointers. Then it calculates and inserts tributary path BIP-2. The generator also inserts FEBE, RDI, and auxiliary RDI in the V5 byte. Software can force AIS insertion on a per tributary basis. As well the TEMUX-84 processes the tributary trace messages of all the tributaries in an STS-1 stream.

A SONET/SDH mapper bit asynchronously maps and demaps up to 84 T1s, 63 E1s, or three DS3s into three STS-1 SPEs, TUG3s or VC3s. The fixed stuff (R) bits are all set to zeros or ones under microprocessor control. The bit asynchronous demapper performs majority vote C-bit decoding to detect stuff requests for T1, E1, and DS3 asynchronous mappings. The VT1.5/VT2/TU-11/TU-12 mapper uses an elastic store and a jitter attenuator capability to minimize jitter introduced via bit stuffing.

5 KEY DATA PATHS

The TEMUX-84 is a flexible device that can be used in many modes. The TEMUX-84 can be configured as a:

- DS3 or E3 framer, providing external access to the full DS3 or E3 payload
- VT/TU mapper, providing access to unframed 1.544 Mb/s and 2.048 Mb/s links
- SONET/SDH VT/TU mapper and M13 Multiplexer
- M13 Multiplexer with performance monitoring
- Transmultiplexer - up to 84 DS3 multiplexed T1 streams are mapped as bit asynchronous VT1.5 virtual tributaries or TU-11 tributary units

These key data paths are shown in Figures 5 through 10.

Figure 5 shows the TEMUX-84 configured as a DS3 or E3 framer. In this mode the TEMUX-84 provides access for up to three full DS3/E3 unchannelized payloads. The payload access (right side of figure) has two clock and data interfacing modes, one utilizing a gapped clock to mask out the DS3/E3 overhead bits, while the second utilizes an ungapped clock with overhead indications on a separate overhead signal. The SBI bus can also be used to provide access to the unchannelized DS3/E3.

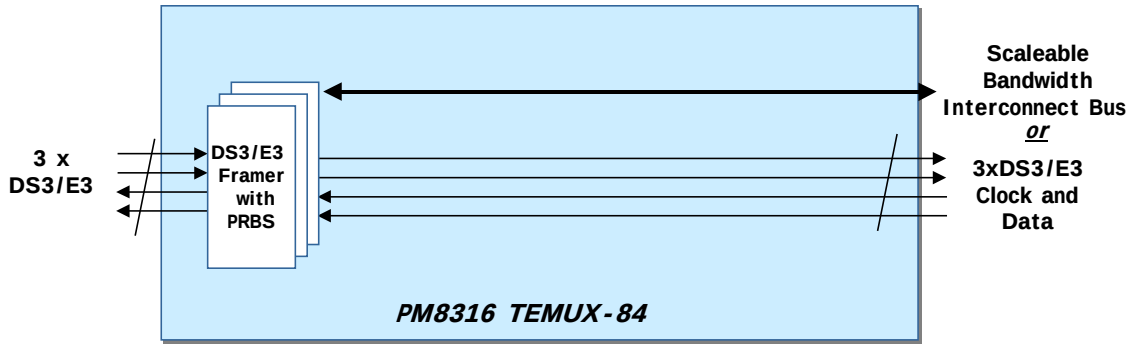

Figure 5 DS3/E3 framer only mode

Figure 6 illustrates PM 8316's VT/TU Mapping Only Mode. In this mode, the TEMUX-84 bypasses the T1 and E1 framers and provides access for up to 84 independent unframed 1.544 Mbit/s streams or 63 independent unframed 2.048 Mbit/s streams. The 1.544 Mbit/s and 2.048 Mbit/s streams can be accessed on the system side via the SBI bus or in byte-synchronous mode via H-MVIP. The T1 or E1 framing architecture can be used to monitor the passing traffic in either the ingress or egress direction.

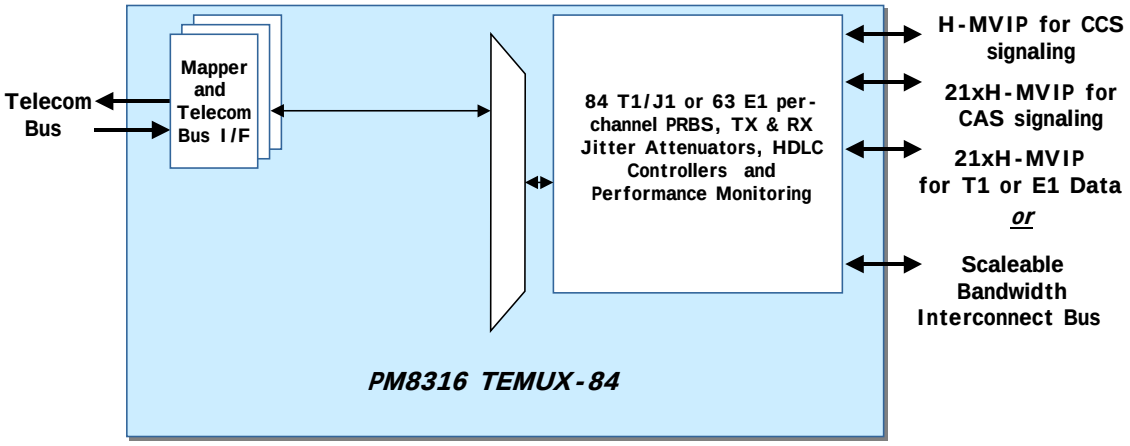

Figure 6 VT/TU Mapper Mode

Figure 7 shows the SONET/SDH mapping and M13 Multiplexing mode. In this mode SONET mapped DS3's are demapped, DS3 deframed and then M13 demultiplexed. T1 or E1s are then framed and can be accessed from either the H-MVIP or SBI interface.

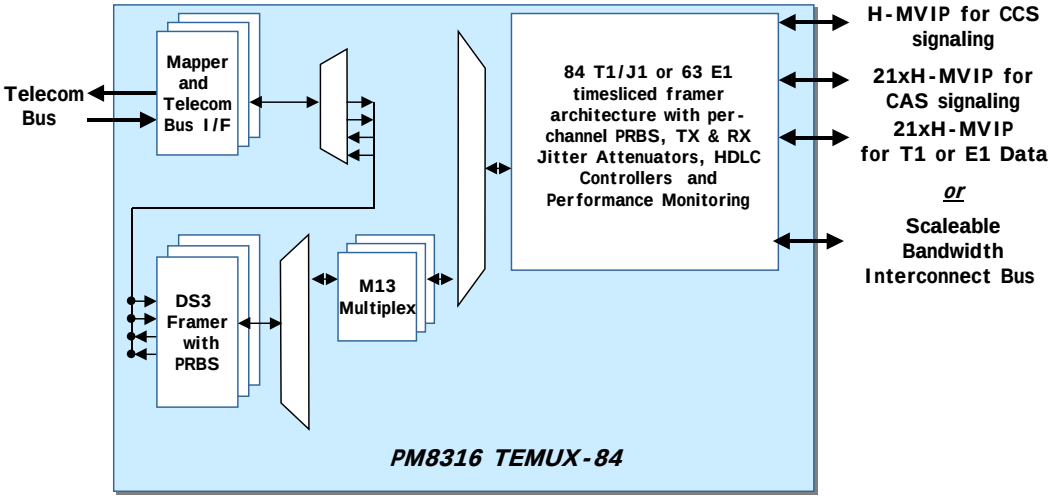

Figure 7 SONET/SDH Mapper and M13 Multiplexer

Figure 8 shows TEMUX-84's M13 Multiplexer Mode. In this example, the TEMUX-84 provides synchronous access to the fully channelized T1s (access to all DS0s)

multiplexed into the DS3 from either the H-MVIP or SBI interface. Both SBI and H-MVIP provide access to all channel-associated signaling channels (CAS). Although common channel signaling (CCS) access is provided within the data H-MVIP signals, when using SBI or as an alternative when using H-MVIP, CCS access can be provided through the additional H-MVIP interfaced.

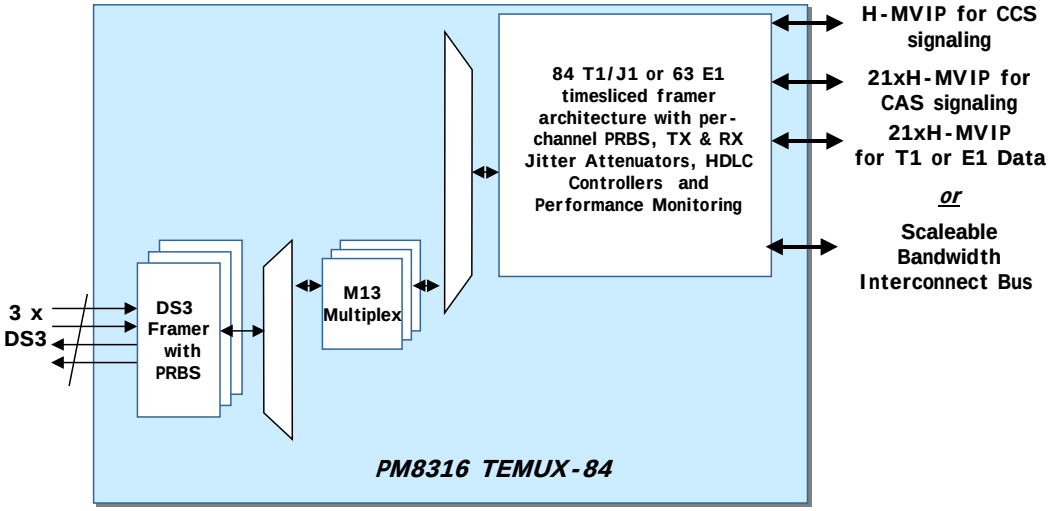

Figure 8 M13 Multiplexer Mode

Figure 9 shows TEMUX-84 configured in Transmultiplexing Mode. In this configuration TEMUX-84 VT/TU maps up to 84 DS3 multiplexed T1s into a SONET/SDH data stream.

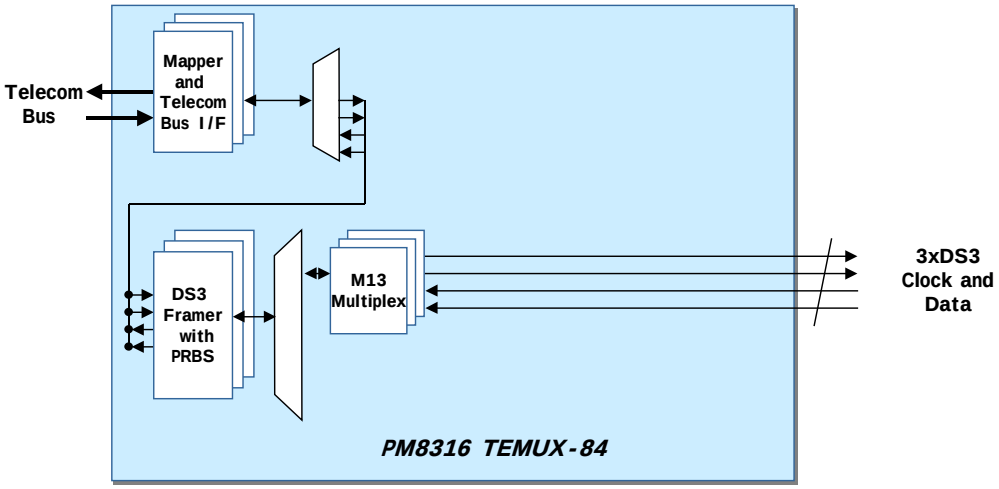

Figure 9 Transmux Mode

6 DIAGNOSTICS

The TEMUX-84 offers a suite of diagnostic tools that include different types of loopbacks and various pseudo-random bit sequences. These diagnostic tools enable more extensive system and board diagnostics, not only at DS3, T1, and E1 line rates, but also at N x DS0 rates. Without any external logic or test equipment, these diagnostics even support in-service testing on any of the tributaries.

6.1.1 Loopback Modes

To enhance device diagnostics, the TEMUX-84 includes:

- Three types of loopback at the DS3 level
- Two types of loopback at the E3 level
- Two loopbacks at the tributary level
- Two loopbacks at the mapper level

At the DS3 level, these loopbacks include:

- **DS3 and E3 Diagnostic Loopback** allows the transmitted DS3 or E3 to be looped back into the receive DS3 or E3 path. These loopbacks override the DS3 or E3 streams received on the inputs. This loopback mode can be used when PM8316 is configured as a M13 multiplexer, DS3 framer or E3 framer only.
- **DS3 and E3 Line Loopbacks** allows the received DS3/E3 streams to be looped back into the transmit DS3/E3 paths. These loopbacks override the DS3/E3 streams created internally , allowing the DS3 or E3 streams to loop back at the line-side before going through the TEMUX.
- **DS2 Demultiplex Loopbacks** loop each of the seven demultiplexed DS2 streams internal to the DS3 into the line and multiplex it up into the transmit DS3. This mode supports in-service testing of the DS3 using only one out of the seven DS2s worth of data for diagnostics.

At the tributary level, the following loopback modes are available within each of the T1/E1 framer slices:

- **T1/E1 line loopback**, connects the received data stream after the jitter attenuator back to the transmit T1/E1 output. The stream then goes to the SONET/SDH mappers or DS3 M13 multiplexers.
- Per **T1/E1 diagnostic loopback**, which connects the transmit T1/E1 output data-steam back into the receive framer.

When using the TEMUX-84 in its SONET/SDH Mapper/Demapper mode, the following loopback modes are available:

- A **Telecom Bus diagnostic loopback**, which allows the transmitted telecom bus data stream to be looped back into the receive SONET/SDH path, overriding the data stream received on the telecom drop bus inputs.
- A **Telecom line loopback**, which loops the received STS-1 back into the transmit path.

6.1.2 Pseudo-Random Bit Sequence (PRBS) Support

The TEMUX-84 offers pseudo-random binary sequence (PRBS) generation and detection. By providing PRBS independently at different levels, the TEMUX-84 can support bit-error-rate testing at the following rates:

- DS3 and E3 rates – includes support for patterns recommended in ITU-T O.151.
- DS1, E1 and NxDS0 rates as recommended in ITU-T O.151 and O.152.

At the DS3 level, the TEMUX-84 offers PRBS pattern generation and detection, which is programmable up to 2^{32}-1 bit length sequences (conforming to ITU-T O.151 standards). It can also offer generation and detection of any repeating pattern up to 32 bits. Diagnostic abilities include not only single bit error insertion, but also error insertion of bit error rates ranging from 10^{-1} to 10^{-7}.

At the tributary (T1 or E1) level, the TEMUX-84 offers PRBS pattern generation and detection. This is user-selectable from bit sequence lengths of 2^7 –1, 2^{11} –1, 2^{15} –1 or 2^{20} –1 (conforming to ITU-T O.151 and ITU-T O.152 standards). You can detect these patterns in either the receive or transmit directions. The sequence can be the entire T1 or E1 any combination of DSOs or timeslots within a framed T1/E1.

7 MIGRATING FROM TEMUX TO TEMUX-84

TEMUX-84 is a follow-on product to PMC-Sierra's successful PM8315 TEMUX product. TEMUX-84 is ideal for higher density applications as it integrates three TEMUX devices into a single package. TEMUX is a good fit for applications from DS3 to OC-3, while TEMUX-84 allows designs to scale more effectively up to OC-48. TEMUX-84 introduces a time-sliced framing architecture to enable its higher density. As well, several features have been added in this next-generation product. A significant portion of the software code written for TEMUX should be easily used with TEMUX-84. Table 4 summarizes the similarities and differences of the two products.

Table 4 Comparison of TEMUX and TEMUX-84

	PM8316 TEMUX-84	**PM8315 TEMUX**
DS3 Framers and M13 Multiplexers	3 DS3/**E3** framers 3 M13 Muxes	1 DS3 framer 1 M13 Mux
Aggregate Bandwidth	STS-3/STM-1	STS-1/STM-0
VT-mapper	Bit-asynchronous and **byte synchronous** mappers	Bit-asynchronous mapper
T1/J1 Framers	84 SF, ESF and **SLC96**	28 SF and ESF
E1 Framers	63 E1 framers	21 E1 framers
Clock and data interfaces	N/A	28 T1 and 21 E1
Telecom Bus Support	**77.76 MHz (STS-12)** and 19.44 MHz (STS-3)	19.44 MHz
Scaleable Bandwidth Interconnect	**77.76 MHz (STS-12)** and 19.44 MHz (STS-3)	19.44 MHz
H-MVIP	21 H-MVIP (8MHz)	7 H-MVIP (8 MHz)
Package	**324 PBGA (23 mm x 23mm)**	324 PBGA (23 mm x 23mm)
Worst Case Power Dissipation	**1.4 Watt**	1.4 Watt
Supply Power	**1.8V** Core 3.3V I/O	2.5V Core 3.3V I/O

NOTES

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