Digital Correction Signal Processor

FEATURES

- Digitial Adaptive Pre-Distortion for wideband linearization of power amplifiers in wireless basestations.
- Digitial Correction for Analog Quadrature Modulation Distortion.
- Digital Soft Pre-compression for efficiency management.
- Input Signal Bandwidth up to 10 MHz. Sample rate up to 80 MHz.
- Programmable, variable input data rate.
- 16-bit microprocessor bus interface for adaptive control processor compensation engine.
- Serial interface (configurable to SPI or I2C operation) for update of power and carrier values.
- 48 general-purpose IO pins, eight of which are edge-triggered interrupt sources.
- Standard five-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

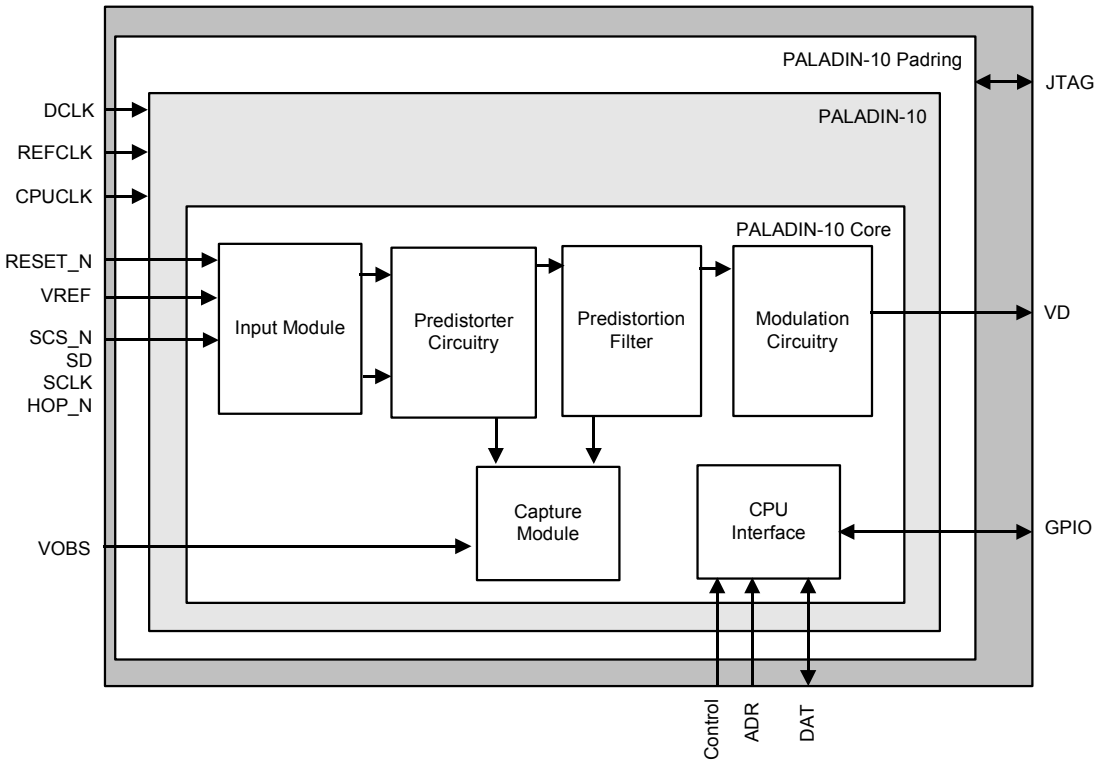
PACKAGING

- Low-power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs.
- Industrial temperature range (-40 °C to +85 °C).
- 304-pin SBGA with a body size of 31mm x 31mm.

APPLICATIONS

- Multi-carrier WCDMA Base Transceiver Subsystems (BTS).
- CDMA2000 BTS (requires firmware upgrade).
- GSM/TDMA/EDGE BTS (requires firmware upgrade).

BLOCK DIAGRAM



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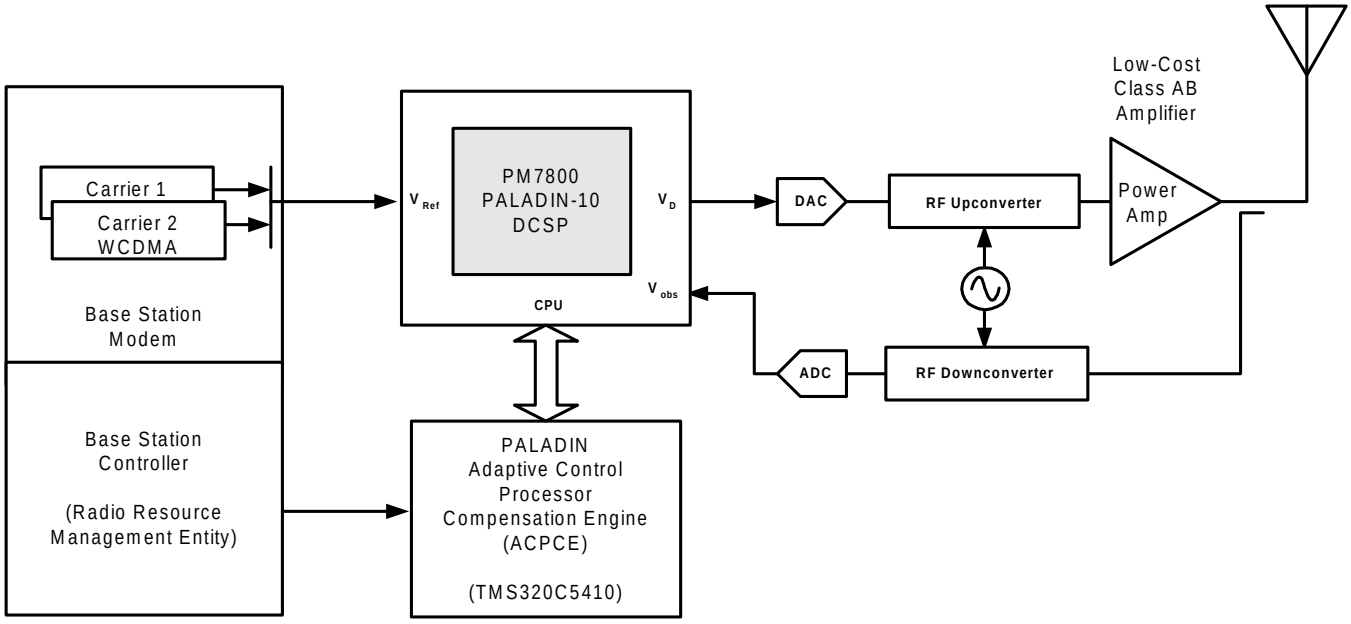
TYPICAL APPLICATIONS

PALADIN-10 MCPA-EQUIPPED BTS



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