XN01214 (XN1214)

Silicon NPN epitaxial planer transistor

For switching/digital circuits

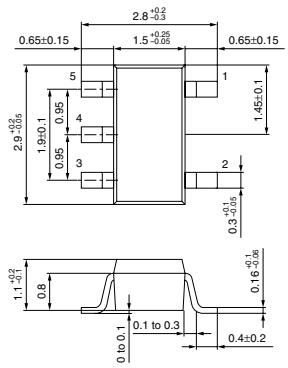
Features

- Two elements incorporated into one package.
  (Emitter-coupled transistors with built-in resistor)
- Reduction of the mounting area and assembly cost by one half.

Basic Part Number of Element

- UNR1214(UN1214) × 2 elements

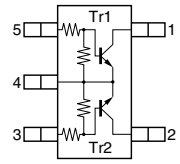
Unit: mm



1 : Collector (Tr1)
2 : Collector (Tr2)
3 : Base (Tr2)
4 : Emitter
5 : Base (Tr1)
EIAJ : SC–74A
Mini Type Pakage (5–pin)

Marking Symbol: 9H

Internal Connection



Absolute Maximum Ratings (Ta=25˚C)

Parameter		Symbol	Ratings	Unit
Rating of element	Collector to base voltage	V_{CBO}	50	V
	Collector to emitter voltage	V_{CEO}	50	V
	Collector current	I_C	100	mA
Overall	Total power dissipation	P_T	300	mW
	Junction temperature	T_j	150	˚C
	Storage temperature	T_{stg}	–55 to +150	˚C

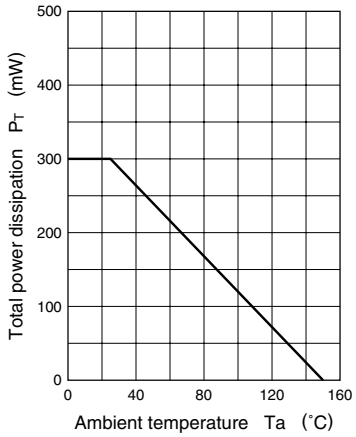
Electrical Characteristics (Ta=25˚C)

Parameter	Symbol	Conditions	min	typ	max	Unit
Collector to base voltage	V_{CBO}	I_C = 10μA, I_E = 0	50			V
Collector to emitter voltage	V_{CEO}	I_C = 2mA, I_B = 0	50			V
Collector cutoff current	I_{CBO}	V_{CB} = 50V, I_E = 0			0.1	μA
	I_{CEO}	V_{CE} = 50V, I_B = 0			0.5	μA
Emitter cutoff current	I_{EBO}	V_{EB} = 6V, I_C = 0			0.2	mA
Forward current transfer ratio	h_{FE}	V_{CE} = 10V, I_C = 5mA	80			
Forward current transfer h_{FE} ratio	h_{FE} (small/large)*1	V_{CE} = 10V, I_C = 5mA	0.5	0.99		
Collector to emitter saturation voltage	$V_{CE(sat)}$	I_C = 10mA, I_B = 0.3mA			0.25	V
Output voltage high level	V_{OH}	V_{CC} = 5V, V_B = 0.5V, R_L = 1kΩ	4.9			V
Output voltage low level	V_{OL}	V_{CC} = 5V, V_B = 2.5V, R_L = 1kΩ			0.2	V
Transition frequency	f_T	V_{CB} = 10V, I_E = –2mA, f = 200MHz		150		MHz
Input resistance	R_1		–30%	10	+30%	kΩ
Resistance ratio	R_1/R_2		0.17	0.21	0.25	

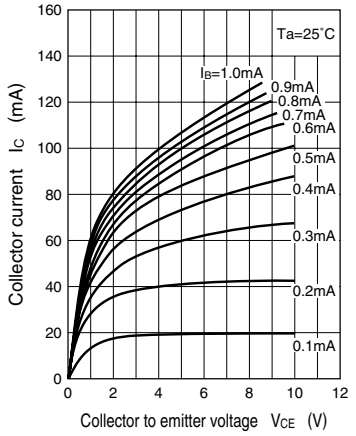
*1 Ratio between 2 elements

Note.) The Part number in the Parenthesis shows conventional part number.

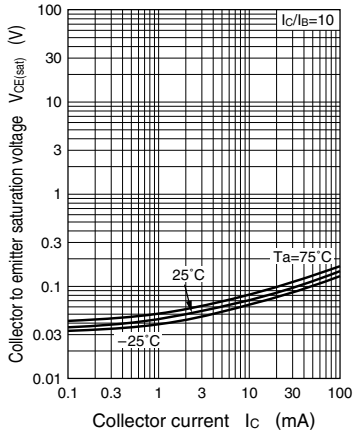
P_T — Ta



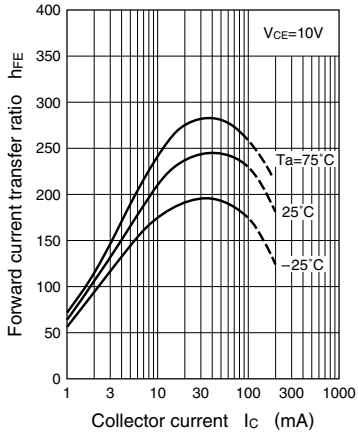
I_C — V_{CE}



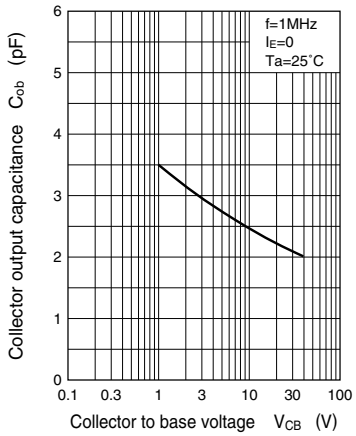
$V_{CE(sat)}$ — I_C



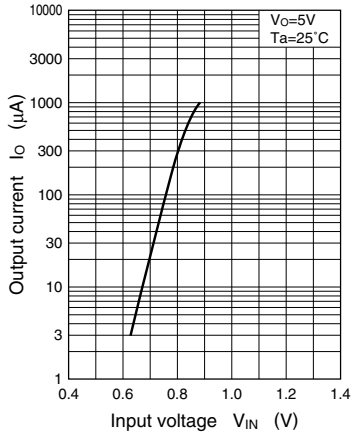
h_{FE} — I_C



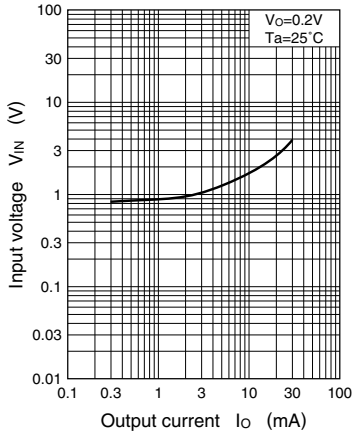
C_{ob} — V_{CB}



I_O — V_{IN}



V_{IN} — I_O



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