TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

65,536-WORD BY 18-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V1864J/FT is a 1,179,648-bit high-speed static random access memory (SRAM) organized as 65,536 words by 18 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, and low-voltage operation it operates from a single 3.3 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. Data byte control signals (LB, UB) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V1864J/FT is available in plastic 44-pin SOJ and TSOP packages (400 mil width) for high density surface assembly.

FEATURES

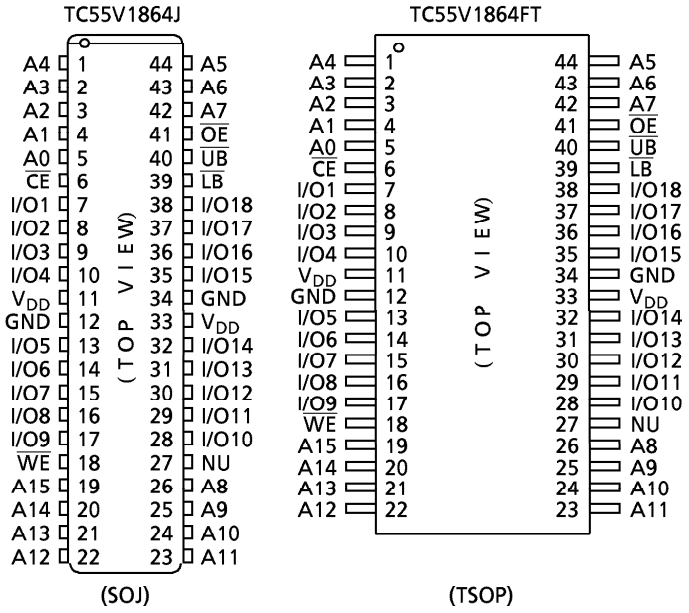
- Fast access time of 15 ns (maximum)
- Low-power dissipation
  (the following are maximum values)

Cycle Time	15	20	30	ns
Operation (max)	200	180	150	mA

  Standby: 2 mA

- Single power supply voltage of 3.3 ± 0.3 V.
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using $\overline{OE}$
- Data byte control using $\overline{LB}$ (IO1 to IO9) and $\overline{UB}$ (IO10 to IO18)
- Packages:
  SOJ44-P-400-1.27 (J) (Weight: 1.64 g typ)
  TSOP II 44-P-400-0.80 (FT) (Weight: 0.45 g typ)

PIN ASSIGNMENT

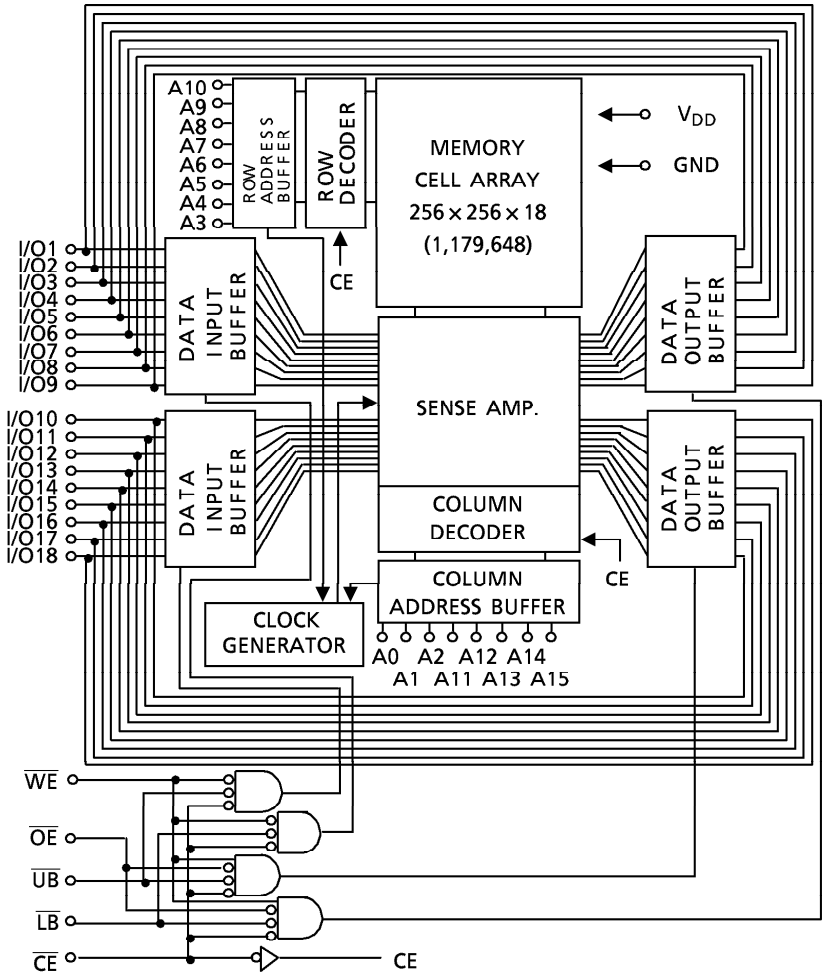


PIN NAMES

A0 to A15	Address Inputs
I/O1 to I/O18	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+ 3.3 V)
GND	Ground
NU	Not Used (Input)

961001EBA1

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	− 0.5~4.6	V
V_{IN}	Input Terminal Voltage	− 0.5 * ~4.6	V
$V_{I/O}$	Input / Output Terminal Voltage	− 0.5 * ~VDD + 0.5**	V
P_D	Power Dissipation	1.2	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{strg}	Storage Temperature	− 65~150	°C
T_{opr}	Operating Temperature	− 10~85	°C

* : −1.5V with a pulse width of 20% · tRC min (4ns max)
** : V_{DD} + 1.5V with a pulse width of 20% · tRC min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Suply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	–	V_{DD} + 0.3**	V
V_{IL}	Input Low Voltage	– 0.3 *	–	0.8	V

* : −1.0V with a pulse width of 20% · tRC min (4ns max)
** : V_{DD} + 1.0V with a pulse width of 20% · tRC min (4ns max)

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current (Except NU pin)	V_{IN} = 0~V_{DD}		– 1	–	1	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0~VDD		– 1	–	1	μA
$I_{I(NU)}$	Input Current (NU pin)	V_{IN} = 0~0.8V		– 1	–	20	μA
		V_{IN} = 0~0.2V		– 1	–	1	
V_{OH}	Output High Voltage	I_{OH} = – 2mA		2.4	–	–	V
		I_{OH} = – 100μA		V_{DD} – 0.2	–	–	
V_{OL}	Output Low Voltage	I_{OL} = 2mA		–	–	0.4	
		I_{OL} = 100μA		–	–	0.2	
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH} / V_{IL}	tcycle = 15ns	–	–	200	mA
			tcycle = 20ns	–	–	180	
			tcycle = 30ns	–	–	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH} / V_{IL}		–	–	20	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} – 0.2V Other Inputs = V_{DD} – 0.2V or 0.2V		–	–	2	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~I/O9	I/O10~I/O18	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* : H or L

NOTE : N.U. pin must be kept open electrically or pulled down to GND level or less than 0.8V. Applying a voltage more than 0.8V to N.U. pin is prohibited.

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 3.3V ± 0.3V)

READ CYCLE

SYMBOL	PARAMETER	TC55V1864J/FT - 15		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	ns
t_{ACC}	Address Access Time	–	15	
t_{CO}	$\overline{CE}$ Access Time	–	15	
t_{OE}	$\overline{OE}$ Access Time	–	8	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	8	
t_{OH}	Output Data Hold Time from Address Change	3	–	
t_{COE}	Output Enable Time from $\overline{CE}$	3	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	

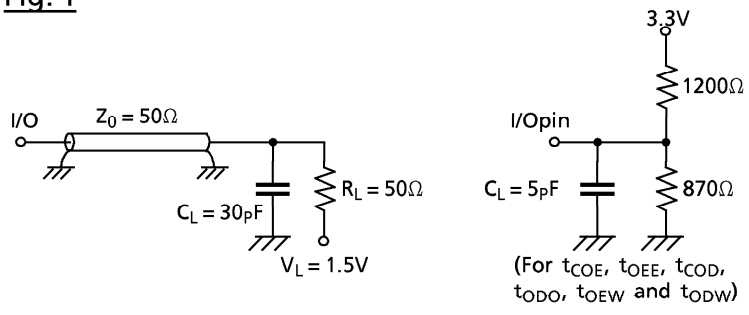
WRITE CYCLE

SYMBOL	PARAMETER	TC55V1864J/FT - 15		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	ns
t_{WP}	Write Pulse Width	9	–	
t_{CW}	Chip Enable to End of Write	12	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	11	–	
t_{AW}	Address Valid to End of Write	11	–	
t_{AS}	Address Set Up Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{DS}	Data Set Up Time	8	–	
t_{DH}	Data Hold Time	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	

AC TEST CONDITIONS

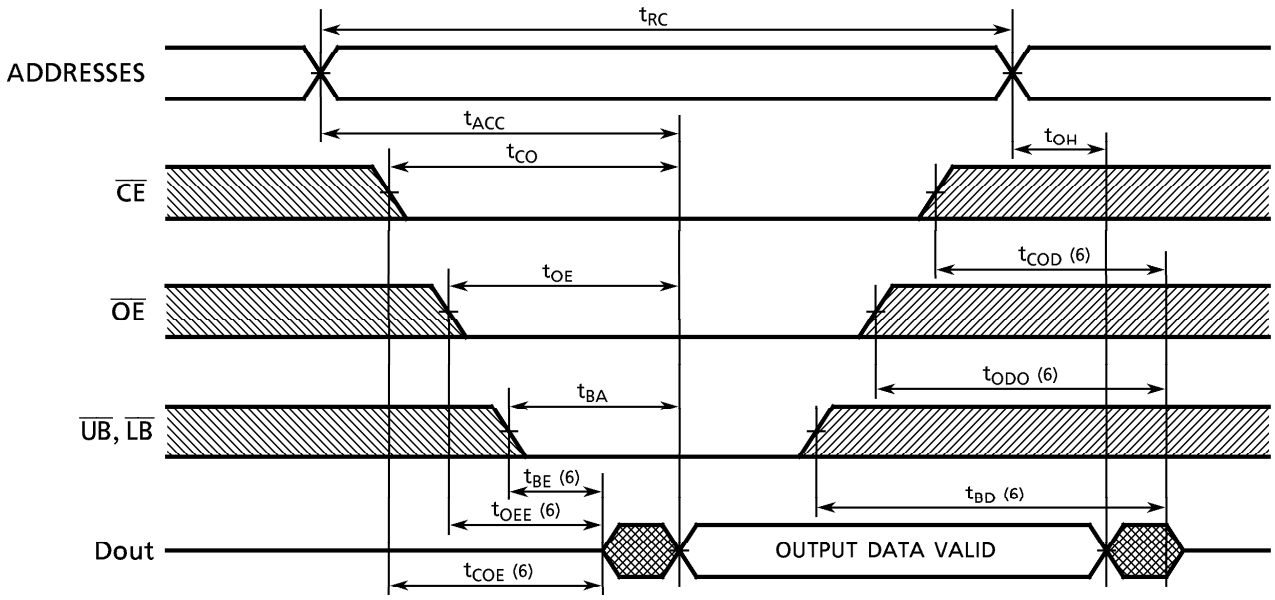
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

Fig. 1

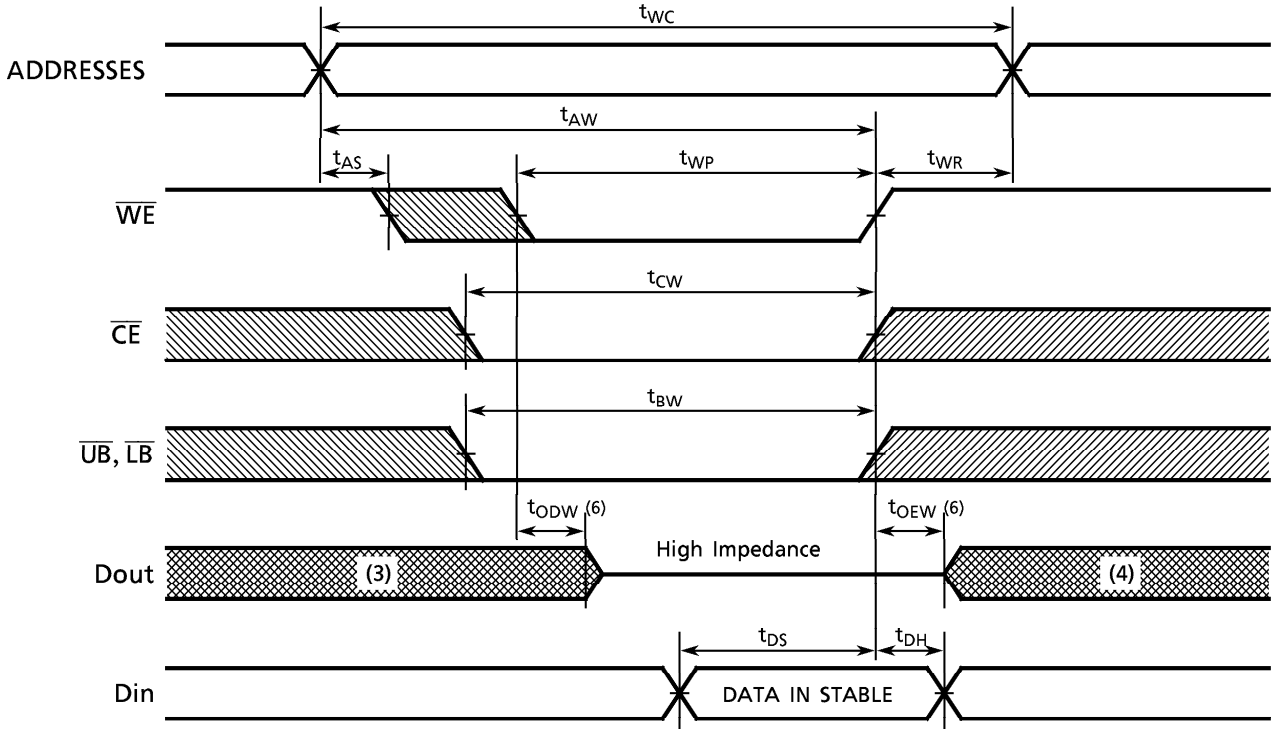


TIMING WAVEFORMS

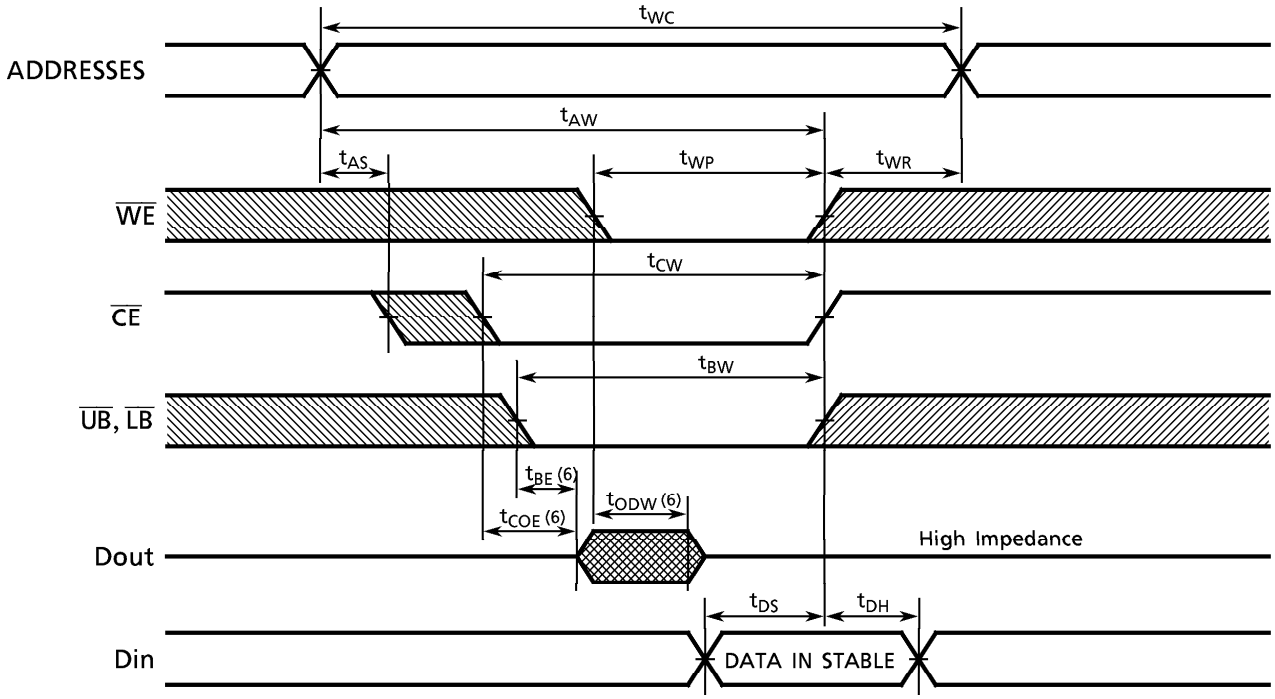
READ CYCLE (2)



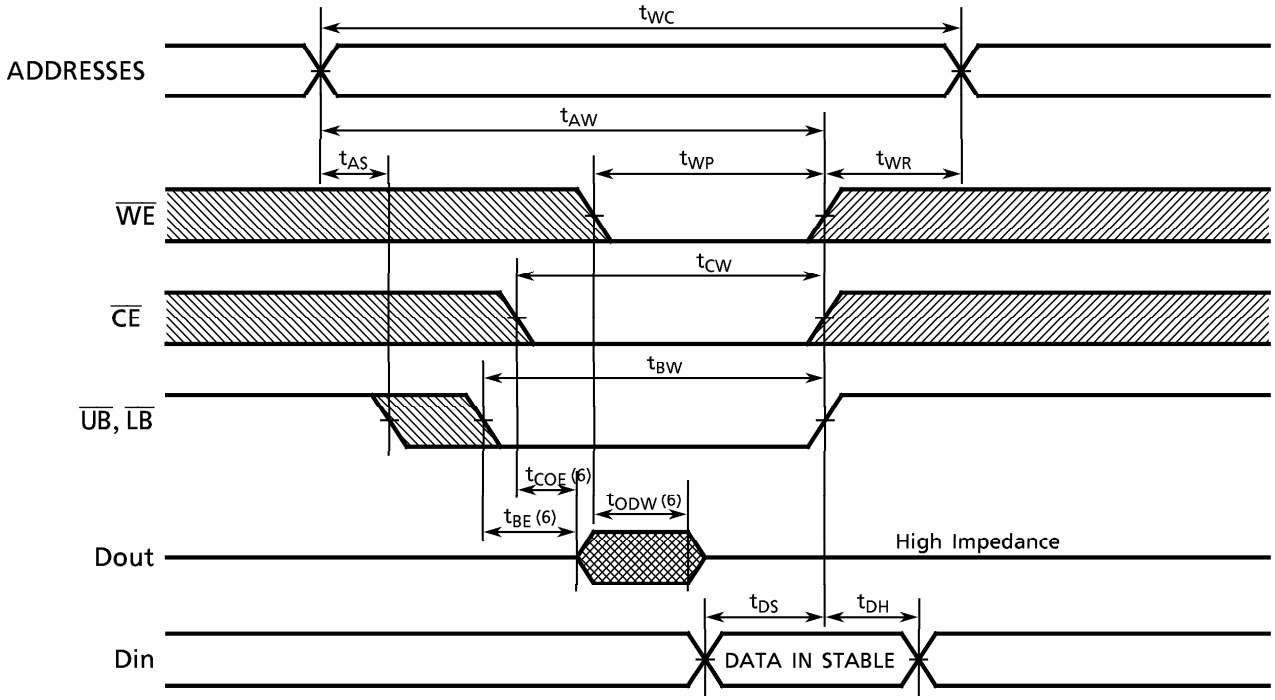
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled)



WRITE CYCLE 3 (5) ($\overline{UB}$, $\overline{LB}$ Controlled)

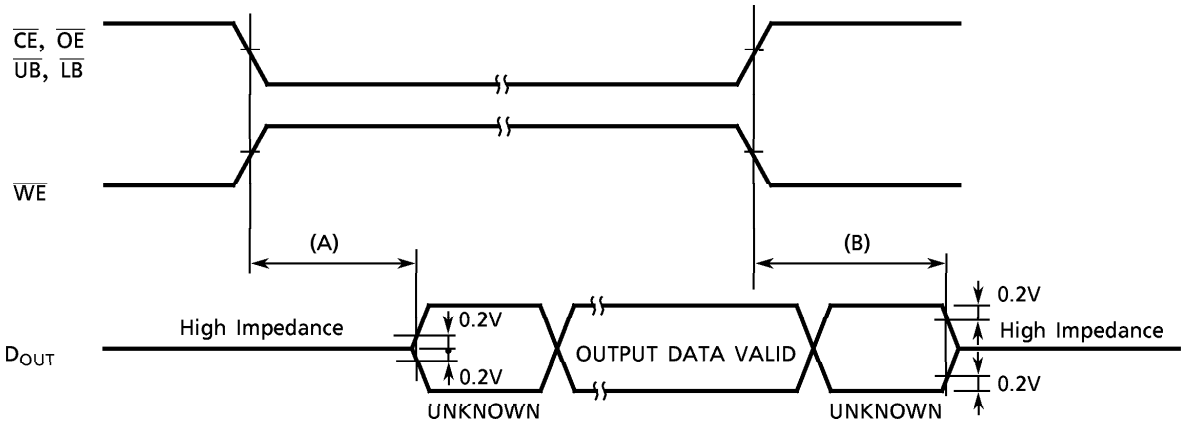


NOTE :

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. $\overline{WE}$ is High for Read Cycle.
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.
6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{BE}, t_{OEW} ····· Output Enable Time

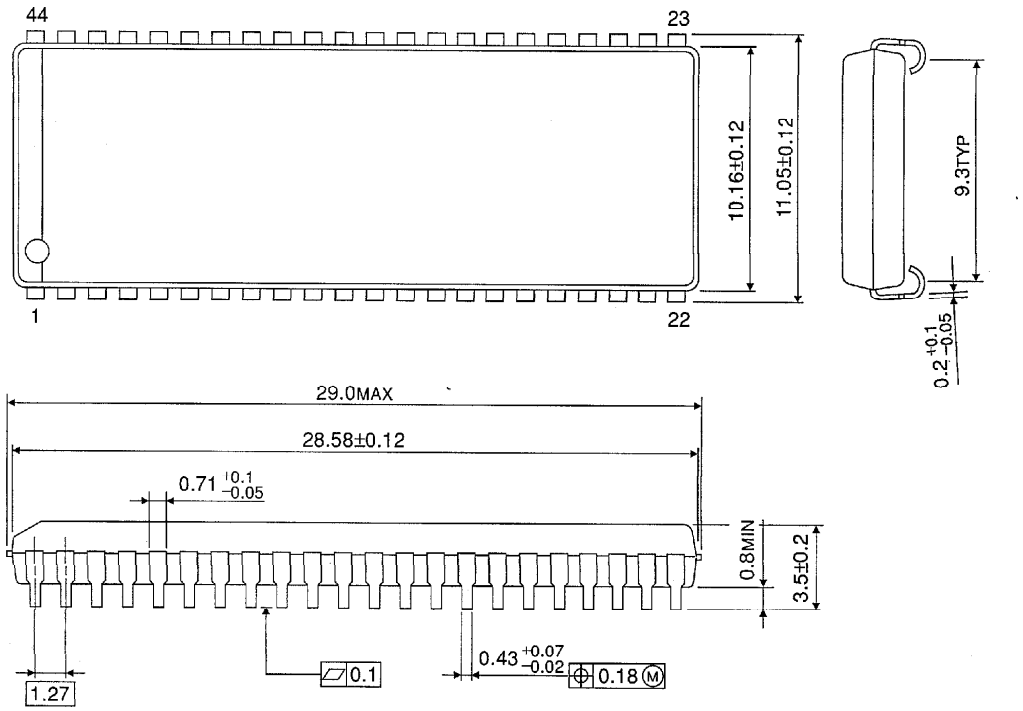
   (B) t_{COD}, t_{ODO}, t_{BD}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic SOJ (SOJ44-P-400-1.27)

Unit in mm

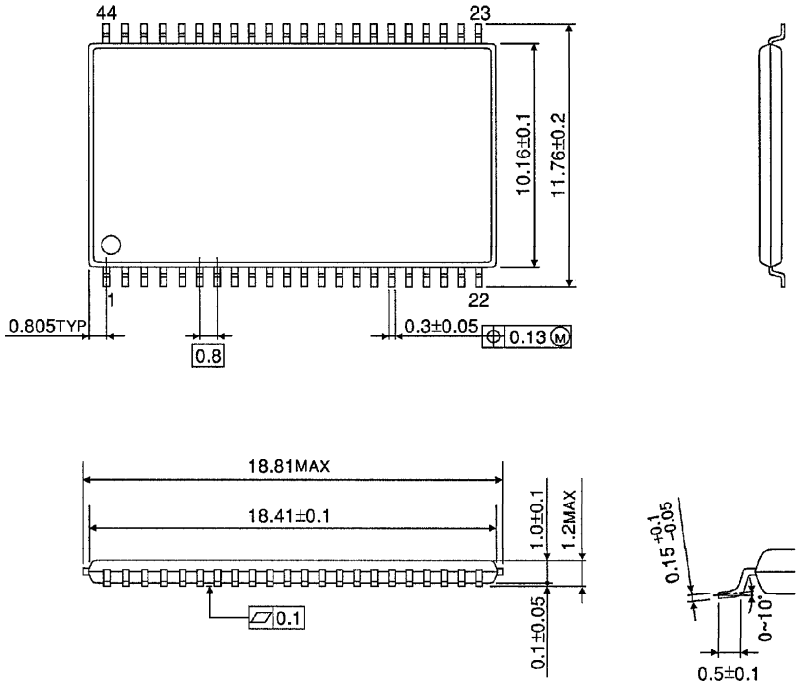


Weight : 1.64g (Typ.)

OUTLINE DRAWINGS

Plastic TSOP (TSOP II 44-P-400-0.80)

Unit in mm



Weight : g (Typ.)