



# STS1C1S250

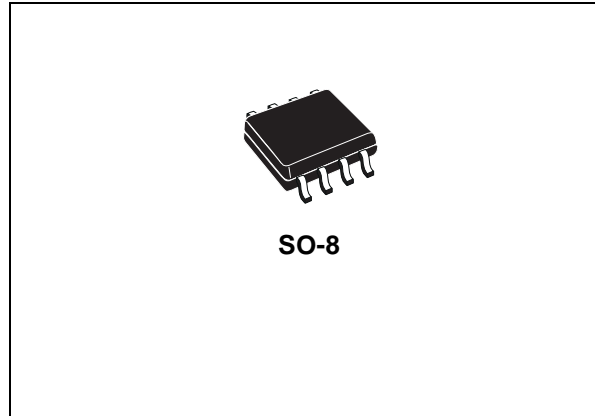
N-CHANNEL 250V - 0.9Ω - 0.75A SO-8

P-CHANNEL 250V - 2.1Ω - 0.6A SO-8

MESH OVERLAY POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS1C1S250(N-Channel)	250 V	<1.4Ω	0.80 A
STS1C1S250(P-Channel)	250 V	<2.8Ω	0.60 A

- TYPICAL R<sub>DS(on)</sub> (N-Channel) = 0.9 Ω
- TYPICAL R<sub>DS(on)</sub> (P-Channel) = 2.1 Ω
- GATE-SOURCE ZENER DIODE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

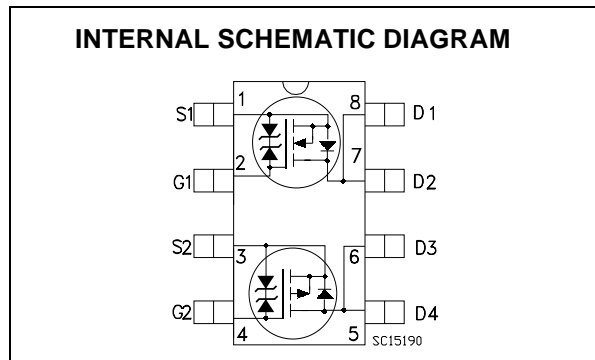


## DESCRIPTION

This complementary pair uses the Company's proprietary high voltage MESH OVERLAY™ process based on advanced strip layout and efficient edge termination. Designed for high volume manufacturing capability, it is ideal in lighting converters such as CFL supplied from 120V mains.

## APPLICATIONS

- LIGHTING



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		N-CHANNEL	P-CHANNEL	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	250	250	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	250	250	V
V <sub>GS</sub>	Gate- source Voltage	±25		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	0.75	0.60	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	0.47	0.38	A
I <sub>DM</sub> (1)	Drain Current (pulsed)	3	2.4	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C Single Operation Total Dissipation at T <sub>C</sub> = 25°C Dual Operation	1.6 2		W
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

(1)Pulse width limited by safe operating area

# STS1C1S250

## THERMAL DATA

Rthj-amb (2)	Thermal Resistance Junction-ambient Max (Single Operating) (Dual Operating)	62.5 78	°C/W
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(2) Mounted on 0.5 in<sup>2</sup> pad of 2oz. copper.

## ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	<b>N-CHANNEL</b> I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 <b>P-CHANNEL</b> I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	n-ch	250			V
			p-ch	250			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C	n-ch			1	μA
			p-ch			1	μA
			n-ch			10	μA
			p-ch			10	μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V	n-ch			±10	μA
			p-ch			±10	μA

## ON (1)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	<b>N-CHANNEL</b> V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA <b>P-CHANNEL</b> V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	n-ch	2	3	4	V
			p-ch	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	<b>N-CHANNEL</b> V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.40A <b>P-CHANNEL</b> V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.30A	n-ch		0.9	1.4	Ω
			p-ch		2.1	2.8	Ω

## DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input Capacitance	<b>N-CHANNEL</b> V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0 <b>P-CHANNEL</b> V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0	n-ch		325		pF
			p-ch		260		pF
C <sub>oss</sub>	Output Capacitance	<b>N-CHANNEL</b> V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0 <b>P-CHANNEL</b> V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0	n-ch		51		pF
			p-ch		52		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	<b>N-CHANNEL</b> V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0 <b>P-CHANNEL</b> V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0	n-ch		24		pF
			p-ch		25.5		pF
R <sub>g</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain	n-ch		6		Ω
			p-ch		6		Ω

(3) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**  
SWITCHING ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	<b>N-CHANNEL</b> $V_{DD} = 125V, I_D = 1.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$	n-ch p-ch		9 12		ns ns
$t_r$	Rise Time	<b>P-CHANNEL</b> $V_{DD} = 125V, I_D = 1.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (Resistive, see Figure 3)	n-ch p-ch		11 22		ns ns
$Q_g$	Total Gate Charge	<b>N-CHANNEL</b> $V_{DD} = 200V, I_D = 1.5A,$ $V_{GS} = 10V$	n-ch p-ch		15 16	20 21	nC nC
$Q_{gs}$	Gate-Source Charge	<b>P-CHANNEL</b> $V_{DD} = 200V, I_D = 1.5A,$ $V_{GS} = 10V$	n-ch p-ch		1.9 1.4		nC nC
$Q_{gd}$	Gate-Drain Charge	$V_{DD} = 200V, I_D = 1.5A,$ $V_{GS} = 10V$	n-ch p-ch		7 7.6		nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	<b>N-CHANNEL</b> $V_{DD} = 125V, I_D = 1.5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$	n-ch p-ch		31 29.5		ns ns
$t_f$	Fall Time	<b>P-CHANNEL</b> $V_{DD} = 200V, I_D = 1.5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)	n-ch p-ch		11 7		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current		n-ch p-ch			0.75 0.6	A A
$I_{SDM(4)}$	Source-drain Current (pulsed)		n-ch p-ch			3 2.4	A A
$V_{SD(5)}$	Forward On Voltage	$I_{SD} = 3A, V_{GS} = 0$ $I_{SD} = 3A, V_{GS} = 0$	n-ch p-ch			1.5 1.5	V V
$t_{rr}$	Reverse Recovery Time	<b>N-CHANNEL</b> $I_{SD} = 0.8A, di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$	n-ch p-ch		127 143		ns ns
$Q_{rr}$	Reverse Recovery Charge	<b>P-CHANNEL</b> $I_{SD} = 0.60A, di/dt = 100A/\mu s,$ $V_{DD} = 40V, T_j = 150^\circ C$ (see test circuit, Figure 5)	n-ch p-ch		450 806		nC nC
$I_{RRM}$	Reverse Recovery Curren		n-ch p-ch		7 11		A A

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{gs} = \pm 500 \mu A$ (Open Drain)	$\pm 25$			V

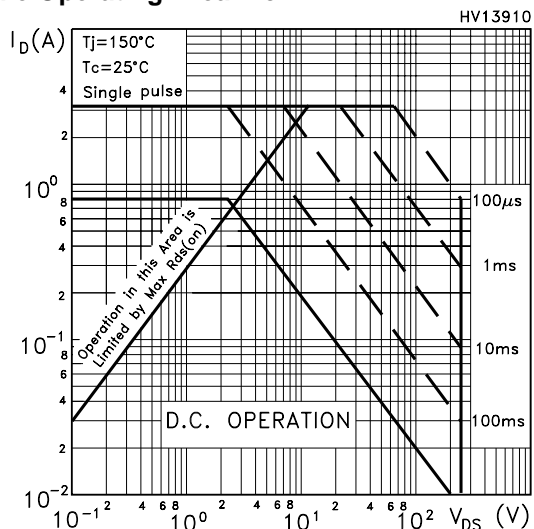
(4) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(5) Pulse width limited by safe operating area

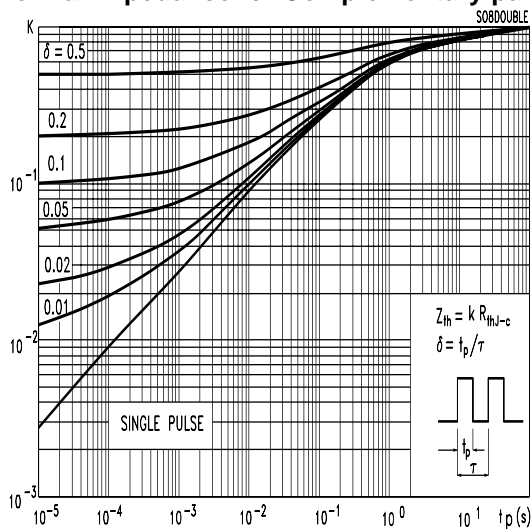
**PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES**

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

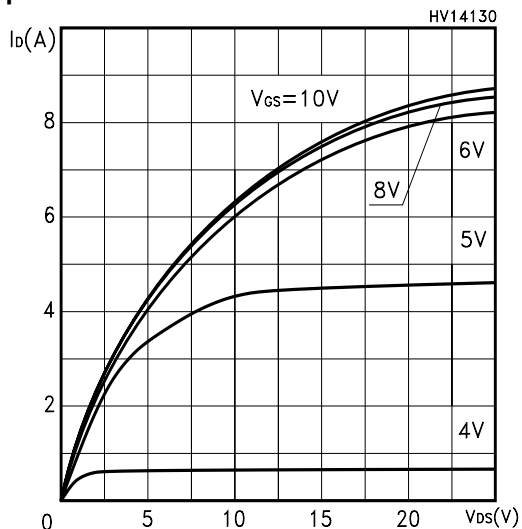
Safe Operating Area n-ch



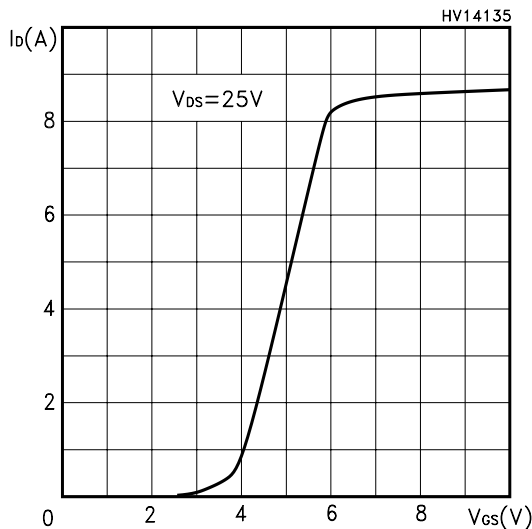
Thermal Impedance for Complementary pair



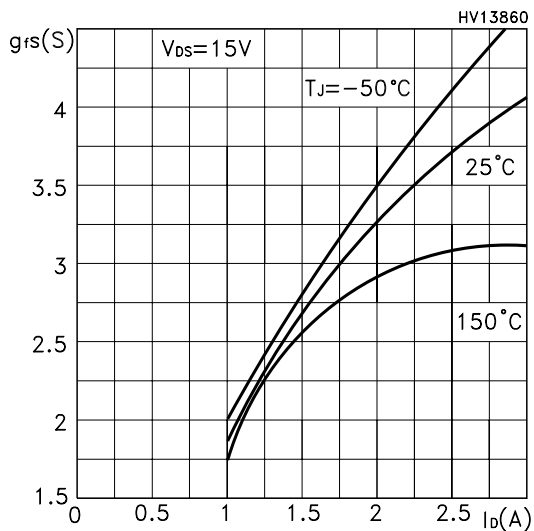
Output Characteristics n-ch



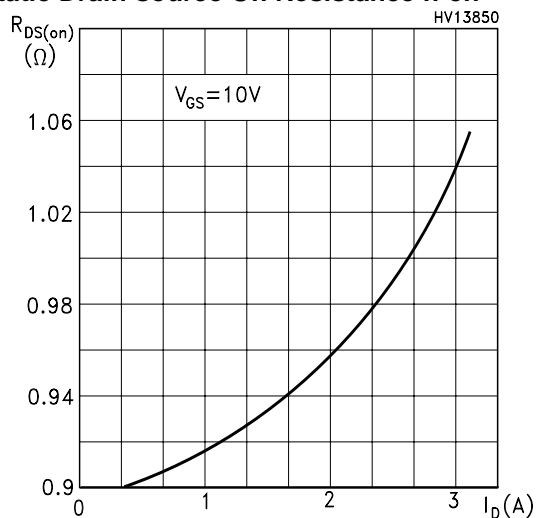
Transfer Characteristics n-ch



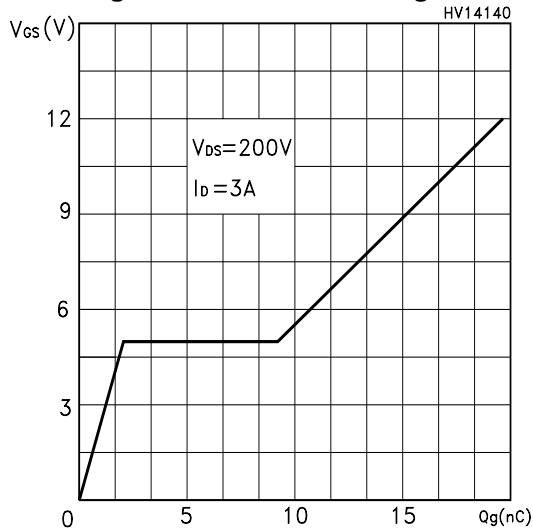
Transconductance n-ch



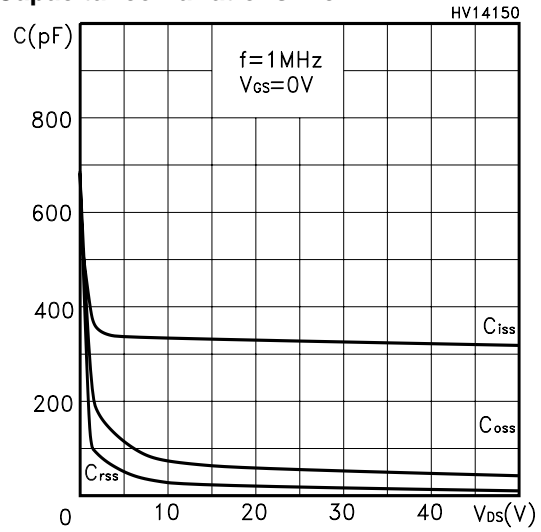
Static Drain-source On Resistance n-ch



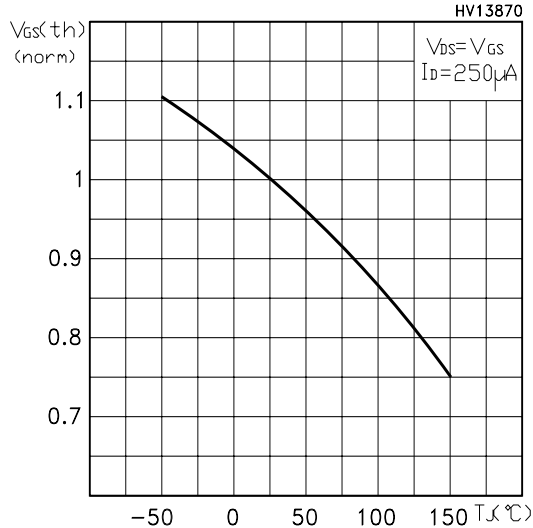
Gate Charge vs Gate-source Voltage n-ch



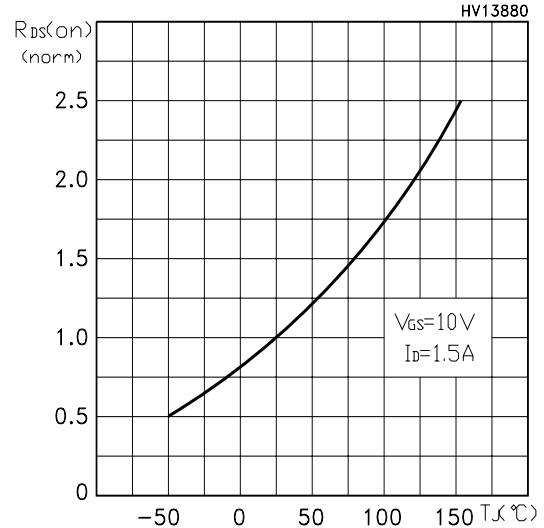
Capacitance Variations n-ch



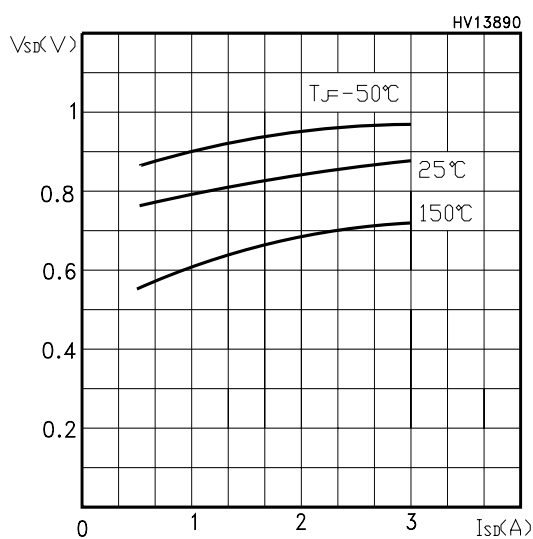
Norm. Gate Threshold Voltage vs Temp n-ch



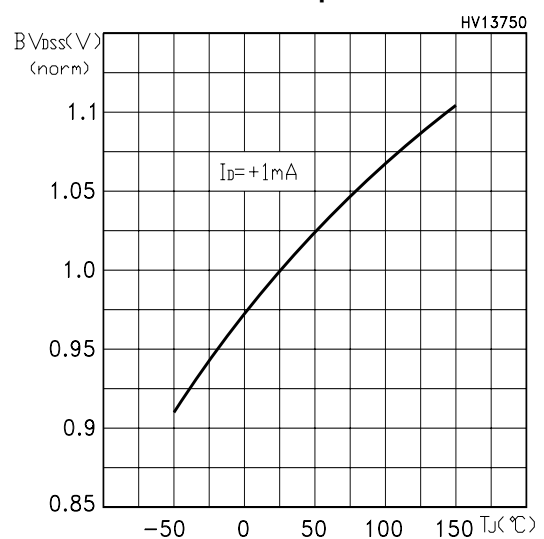
Norm. On Resistance vs Temperature n-ch



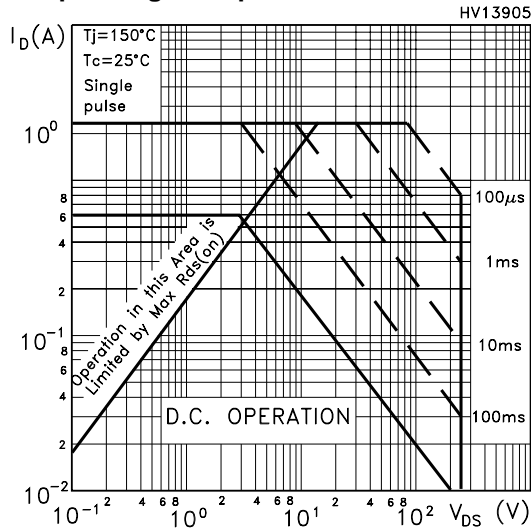
Source-drain Diode Forward Characteristics n-ch



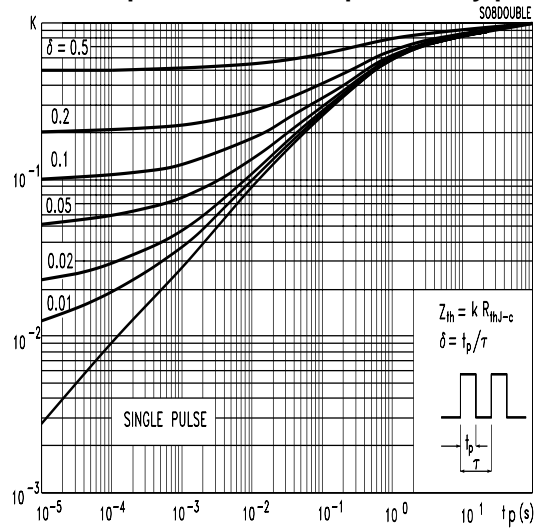
Normalized BVDS vs Temperature n-ch



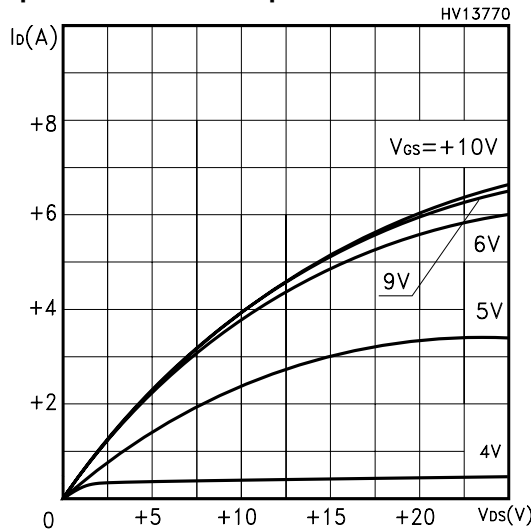
Safe Operating Area p-ch



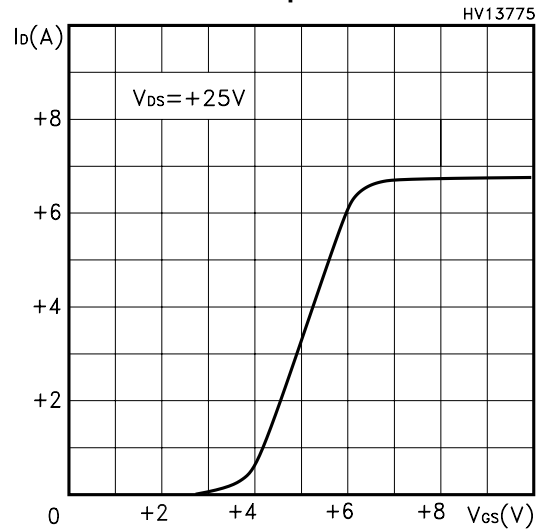
Thermal Impedance for Complementary pair



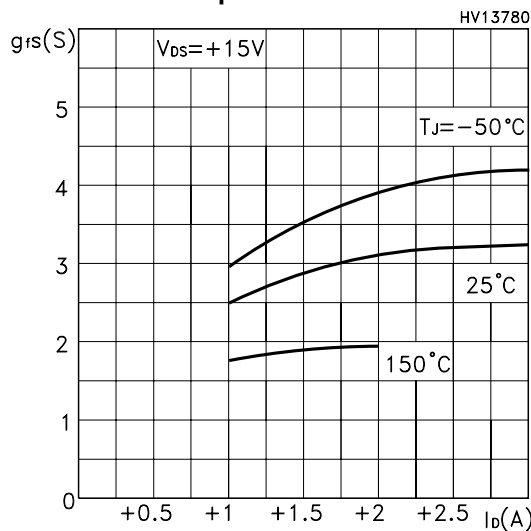
Output Characteristics p-ch



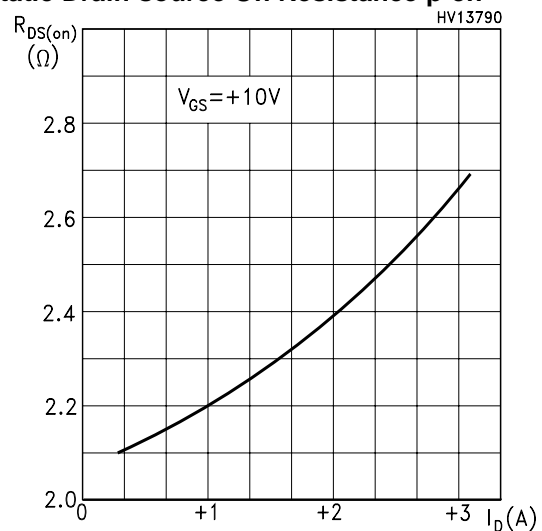
Transfer Characteristics p-ch



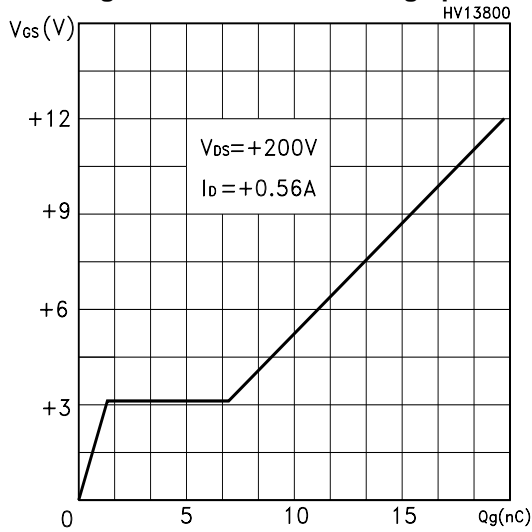
Transconductance p-ch



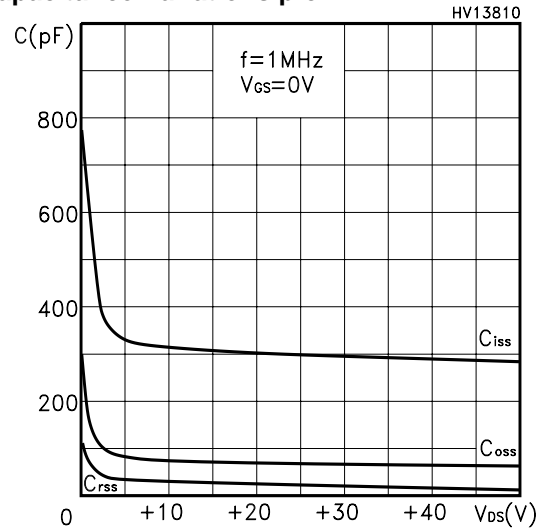
Static Drain-source On Resistance p-ch



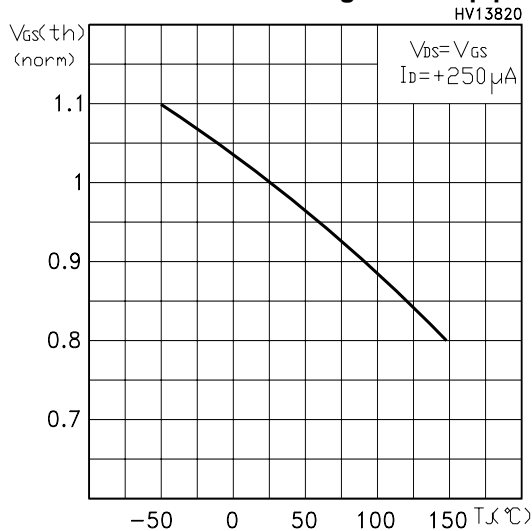
**Gate Charge vs Gate-source Voltage p-ch**



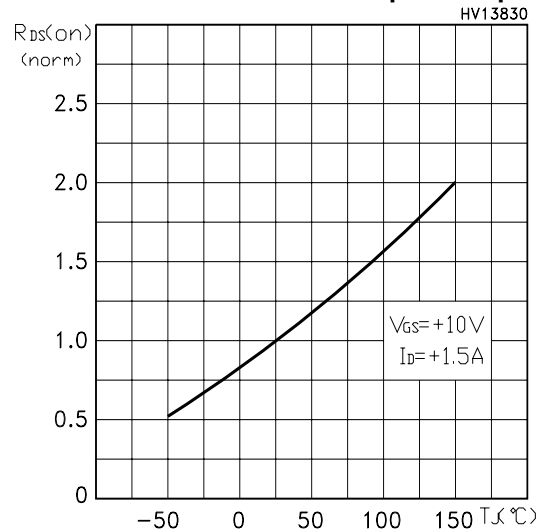
**Capacitance Variations p-ch**



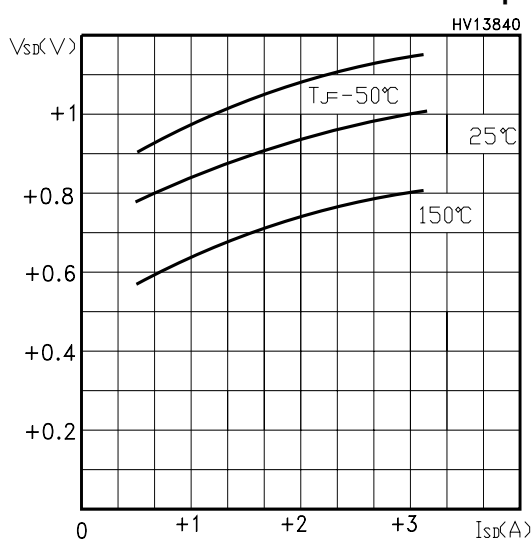
**Norm. Gate Threshold Voltage vs Temp p-ch**



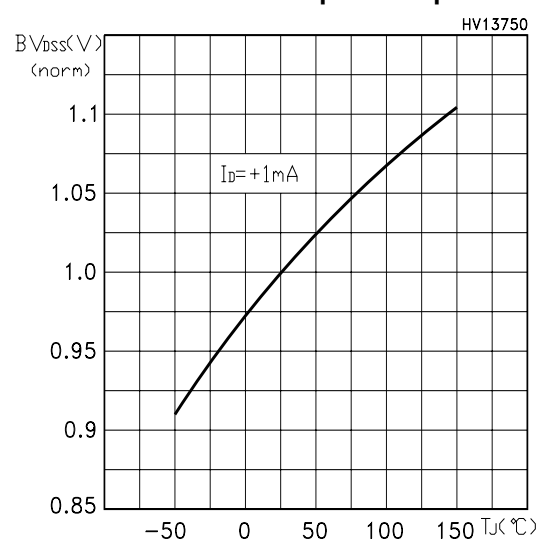
**Normalized On Resistance vs Temperature p-ch**



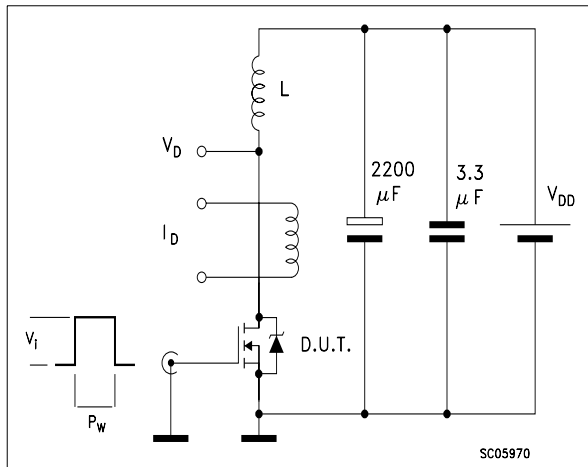
**Source-drain Diode Forward Characteristics p-ch**



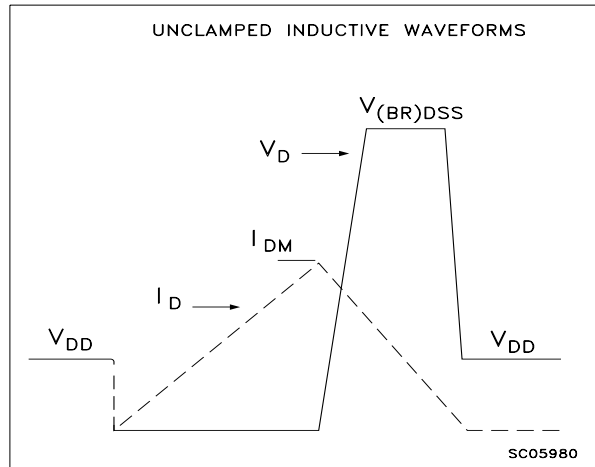
**Normalized BVDSS vs Temperature p-ch**



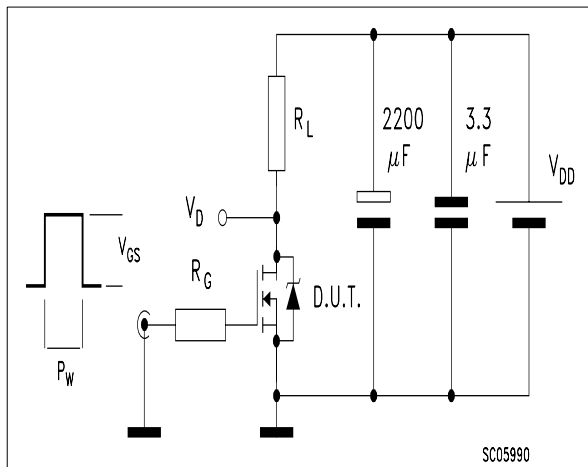
**Fig. 1: Unclamped Inductive Load Test Circuit**



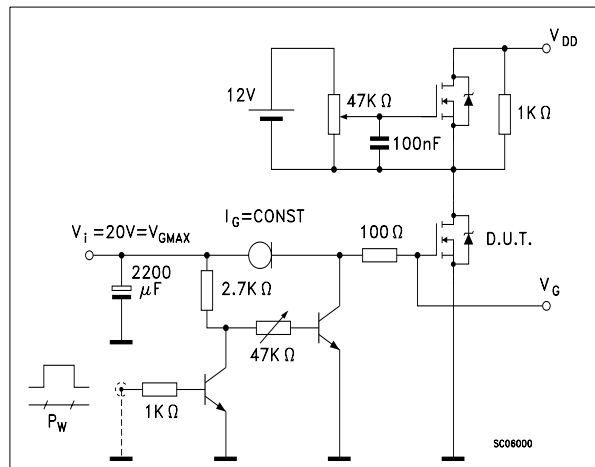
**Fig. 2: Unclamped Inductive Waveform**



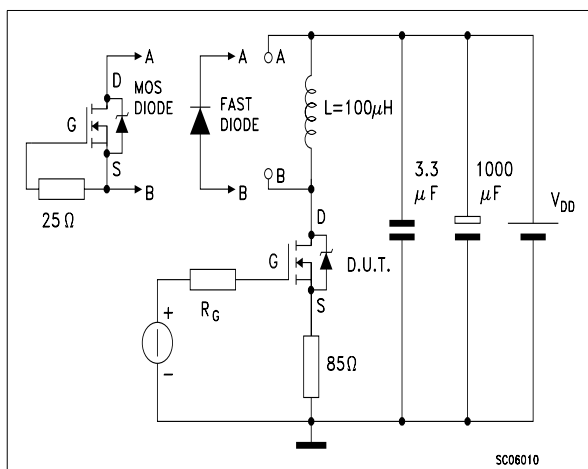
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**



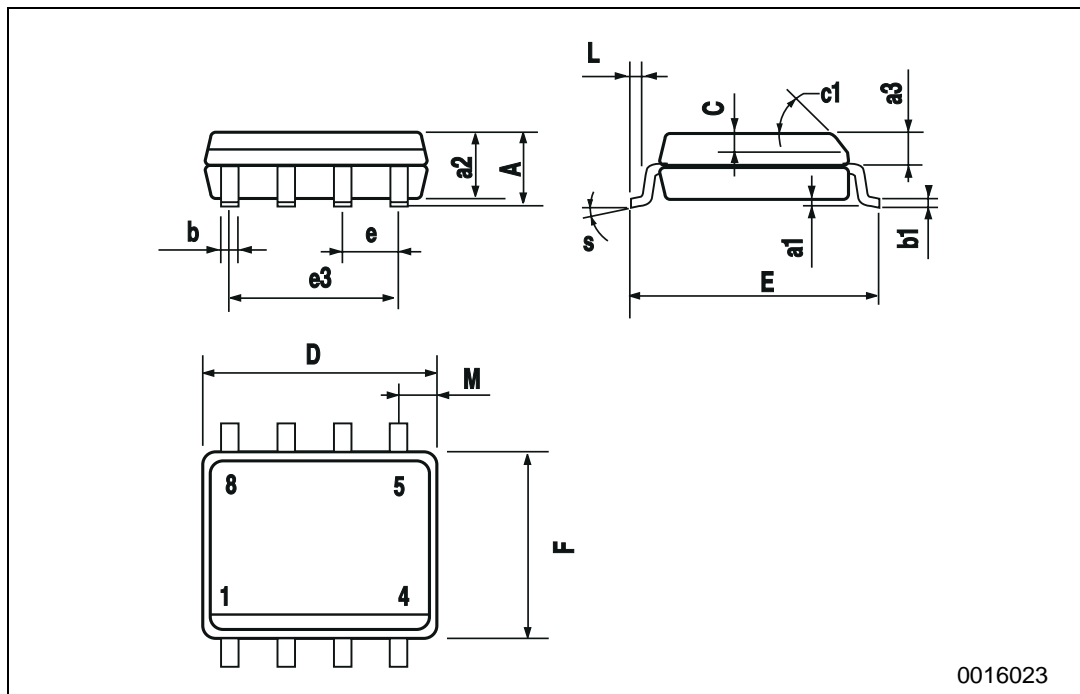
**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**





**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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