SP5768

3.0GHz Low Phase Noise Frequency Synthesiser

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Features

- Complete 3.0GHz single chip system
- Optimised for low phase noise, with comparison frequencies up to 4 MHz
- No RF prescaler
- Selectable reference division ratio
- Reference frequency output
- Selectable charge pump current
- Integrated loop amplifier
- Four switching ports
- Low power replacement for SP5658 and 5668
- Downwards software compatible with SP5658
- ESD protection, (Normal ESD handling procedures should be observed)

Applications

- TV, VCR and Cable tuning systems
- Communications systems

Ordering Information

SP5768/KG/MP1S (Tubes)
SP5768/KG/MP1T (Tape and Reel)
SP5768/KG/QP1S (Tubes)
SP5768/KG/QP1T (Tape and Reel)

Description

The SP5768 is a single chip frequency synthesiser designed for tuning systems up to 3.0GHz and is optimized for low phase noise with comparison frequencies up to 4 MHz.

The RF programmable divider contains a front end dual modulus 16/17 functioning over the full operating range and allows for coarse tuning in the upconverter application and fine tuning in the downconverter.

Comparison frequencies are obtained either from a crystal controlled on-chip oscillator or from an external source. A buffered reference frequency output is also available to drive a second SP5768.

The device also contains 4 switching ports.

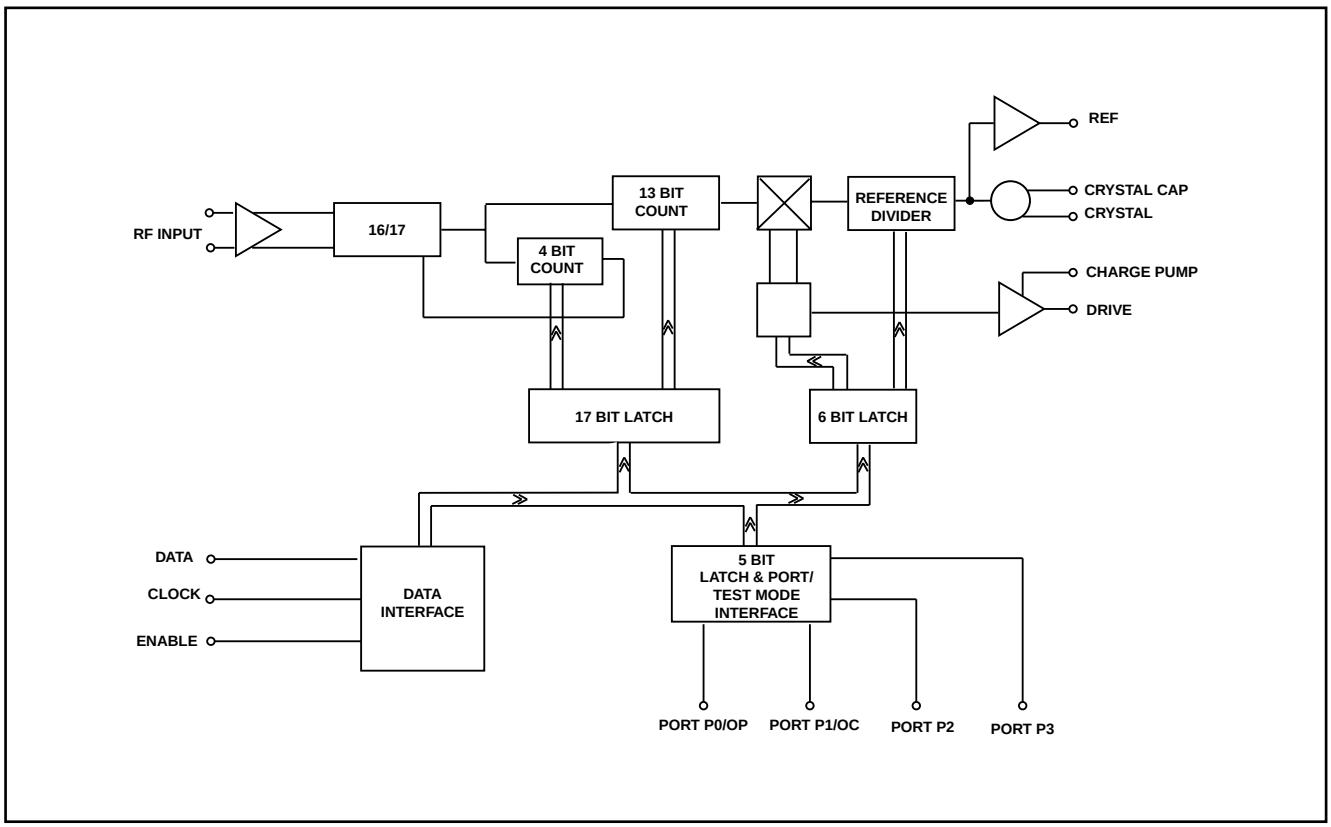
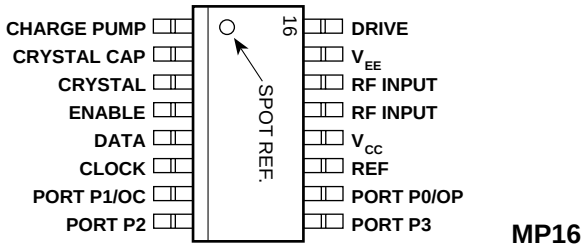


Figure 1 - SP5768 block diagram



MP16
QP16

Figure 2 - Pin Connections Diagram

Electrical Characteristics

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. T_{AMB} = -40°C to 80°C, V_{CC} = +4·5V to +5·5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	12		18	25	mA	
RF input frequency range	13,14	100		3000	MHz	
RF input voltage	13,14	100		300	mV rms	100 - 200MHz
	13, 14	30		300	mVrms	See Figure 6
RF input impedance	13,14					See Figure 3
Data, clock & enable	5,6,4					
input high voltage		3		Vcc	V	
input low voltage		0		0.7	V	
input current		-10		10	µA	All input conditions
hysterysis			0.8		V	
Clock rate		6			500	kHz
Bus timing -	5,6,4					
data set up		300			ns	
data hold		600			ns	
enable set up		300			ns	
enable hold		600			ns	
clock to enable		300			ns	

Electrical Characteristics (continued)

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Tamb = -40°C to 80°C, Vcc = +4·5V to +5·5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Charge pump output current	1					See Table 1 Vpin1 = 2V
Charge pump output leakage	1		±3	±10	nA	Vpin1=2V, Vcc = +5.0V, Tamb = 25°C
Charge pump drive output current	16	0.5			mA	Vpin 16=0.7V
Crystal frequency	2,3	2		20	MHz	See Figure 5 for application
External reference input frequency	3	2		20	MHz	Sinewave coupled through 10F blocking capacitor
External reference drive level	3	0.2		0.5	V_{pp}	Sinewave coupled through 10nF blocking capacitor
Buffered reference frequency output	11					AC coupled, See note 1
output amplitude			0.35		Vpp	2-20MHz
output impedance			250		Ω	
Comparison frequency				4	MHz	
Equivalent phase noise at phase detector		-148			dBc/Hz	At 10 kHz, SSB, with 2 MHz comparison from 4 MHz crystal reference
RF division ratio		240		131071		
Reference division ratio		2		320		See Table 2
Output ports P0-P3	7,8,9,10					See Note 2
sink current			2		mA	Vport = 0.7V
leakage current				10	µA	Vport = Vcc

1 Reference output disabled by connecting to Vcc if not required

2 Output ports high impedance on power up, with data, clock and enable at logic 0

Absolute Maximum Ratings

All voltages are referred to Vee at 0V

Characteristic	Pin	Min	Typ	Max	Units	Conditions
Supply voltage, Vcc	12	-0.3		7	V	
RF input voltage	13,14			2.5	V_{p-p}	Differential
RF input DC offset	13,14	-0.3		V_{cc}+0.3	V	
Port voltage	7,8,9,10	-0.3		V_{cc}+0.3	V	
Charge pump DC offset	1	-0.3		V_{cc}+0.3	V	
Varactor drive DC offset	16	-0.3		V_{cc}+0.3	V	
Crystal DC offset	2,3	-0.3		V_{cc}+0.3	V	
Buffered ref output	11	-0.3		V_{cc}+0.3	V	
Data, clock & enable DC offset	5,6,4	-0.3		V_{cc}+0.3	V	
Storage temperature		-55		+125	°C	
Junction temperature				+150	°C	
MP16 thermal resistance, chip to ambient chip to case				 80 20	 °C/W °C/W	
Power consumption at V_{cc}=5.5V				138	mW	All ports off
ESD protection		2			kV	Mil-std 883B latest revision method 3015 cat.1.

Functional description

The SP5768 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with excellent phase noise performance, even with high comparison frequencies.

The package and pin allocation is shown in Figure 1 and the block diagram in Figure 2.

The SP5768 is controlled by a standard 3-wire bus comprising data, clock and enable inputs. The programming word contains 28 bits, four of which are used for port selection, 17 to set the programmable divider ratio, four bits to select the reference division ratio, bits RD & R0-R2, see Table 2, two bits to set charge pump current, bit C0 and C1, see Table 1, and the remaining bit to access test modes, bit T0, see Table 3. The programming format is shown in Figure 4.

The clock input is disabled by an enable low signal, data is therefore only loaded into the internal shift registers during an enable high and is clocked into the controlling buffers by an enable high to low transition. This load is also synchronised with the programmable divider so giving smooth fine tuning.

The RF signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier is fed to the 17 bit fully programmable counter, which is of MN+A architecture. The M counter is 13 bit and the A counter 4
The output of the programmable counter is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into1 of 16 ratios as descried in Table 2.

The output of the phase detector feeds the charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter integrates the current pulses into the varactor line voltage. The charge pump current setting is described in Table 1,
A buffered crystal reference frequency suitable for driving further synthesisers is available from Pin 11. If not required this output can be disabled by connecting to Vcc

The programmable divider output divided by 2, Fpd/2 and comparison frequency, Fcomp can be switched to ports P0 and P1 respectively by switching the device into test mode. The test modes are described in Table 3.

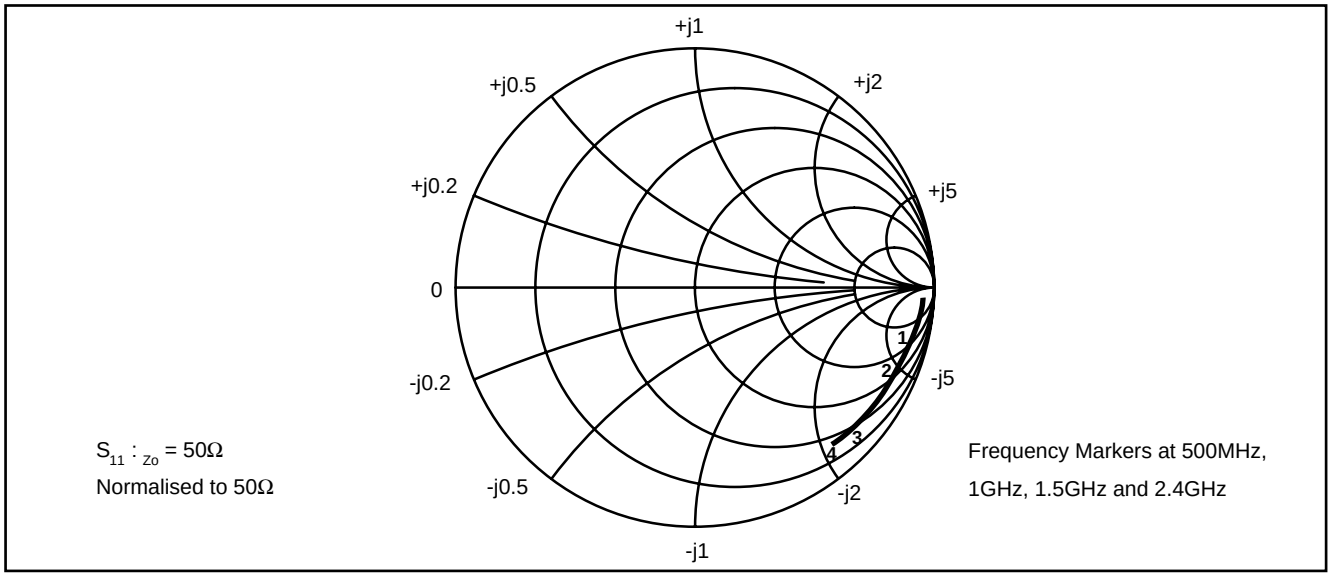
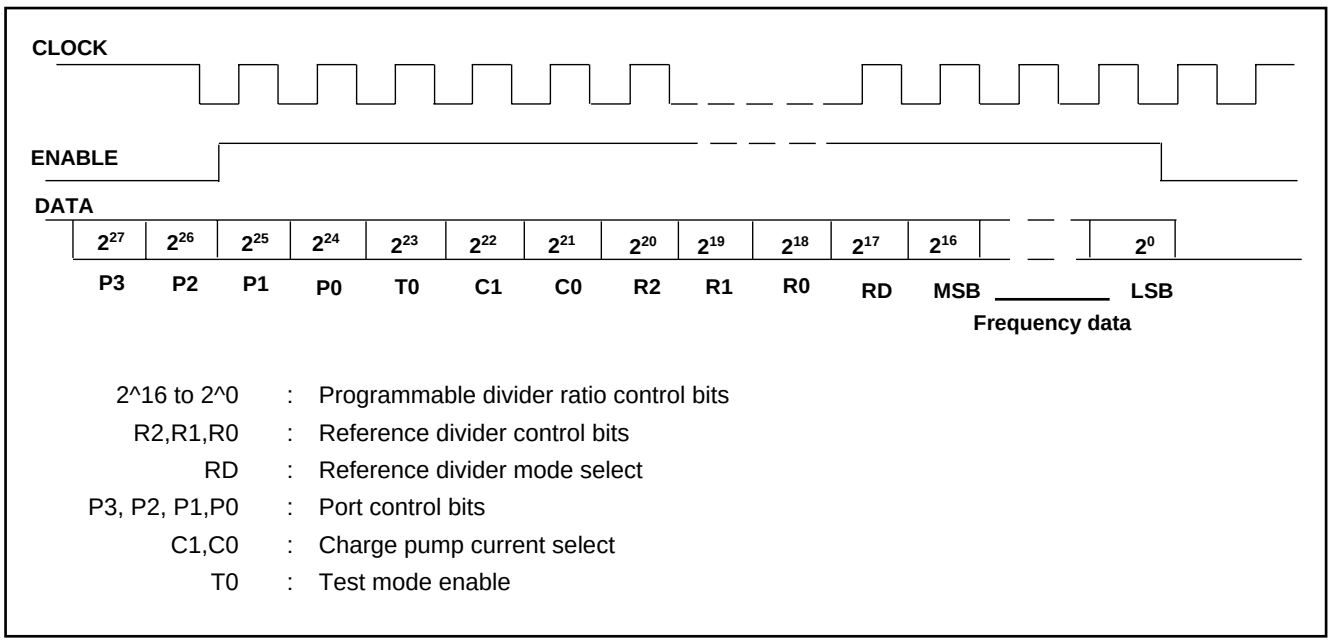


Figure 3 - RF input impedance



2^16 to 2^0	:	Programmable divider ratio control bits
R2,R1,R0	:	Reference divider control bits
RD	:	Reference divider mode select
P3, P2, P1,P0	:	Port control bits
C1,C0	:	Charge pump current select
T0	:	Test mode enable

Figure 4 - Data format

C1	C0	Current (in μA)
0	0	230
0	1	1000
1	0	115
1	1	500

Table 1 - Charge pump current

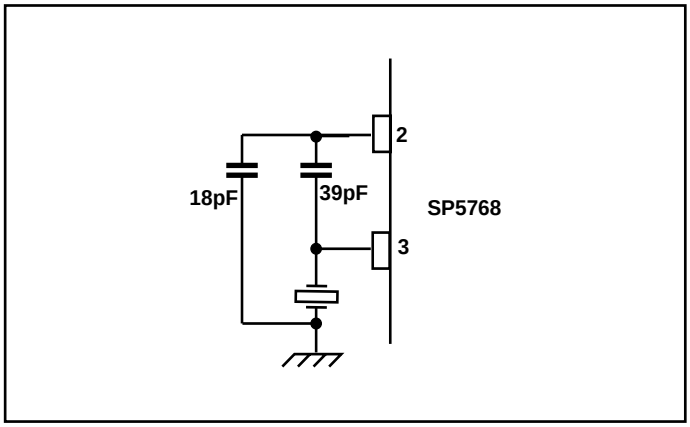


Figure 5 - Crystal oscillator application

RD	R2	R1	R0	RATIO
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	3
1	0	0	1	5
1	0	1	0	10
1	0	1	1	20
1	1	0	0	40
1	1	0	1	80
1	1	1	0	160
1	1	1	1	320

Table 2 - Reference division ratio

P1	P0	T0	FUNCTIONAL DESCRIPTION
X	X	0	Normal operation
0	0	1	Charge pump sink
0	1	1	Charge pump source
1	0	1	Charge pump disable
1	1	1	Port P1 = Fcomp, P0 = Fpd/2

X = don't care

Table 3 - Test modes

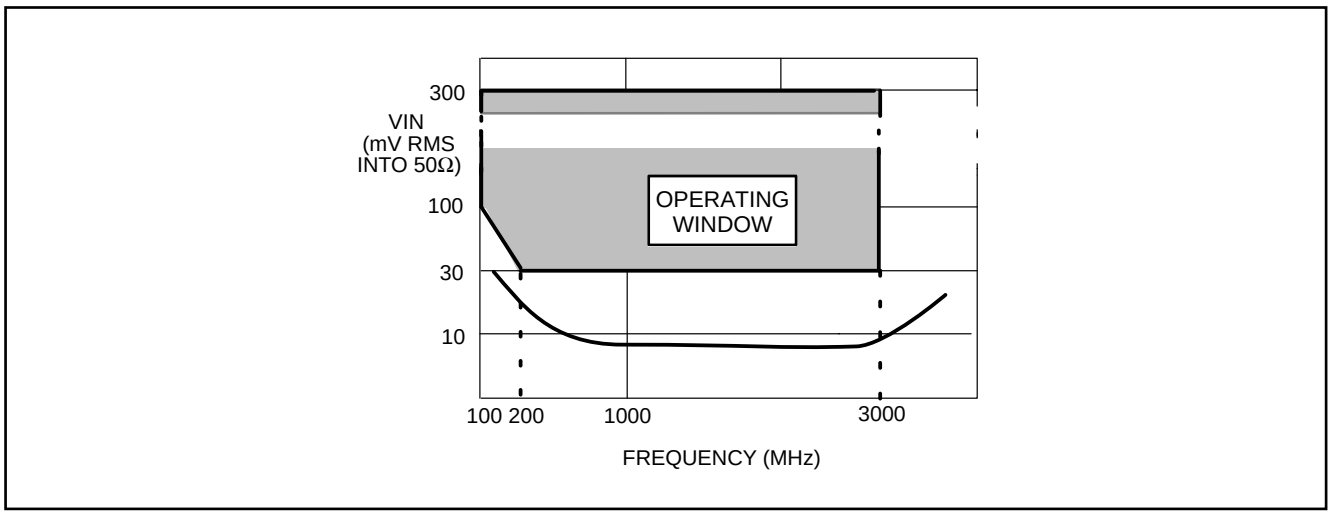


Figure 6 - Typical input sensitivity

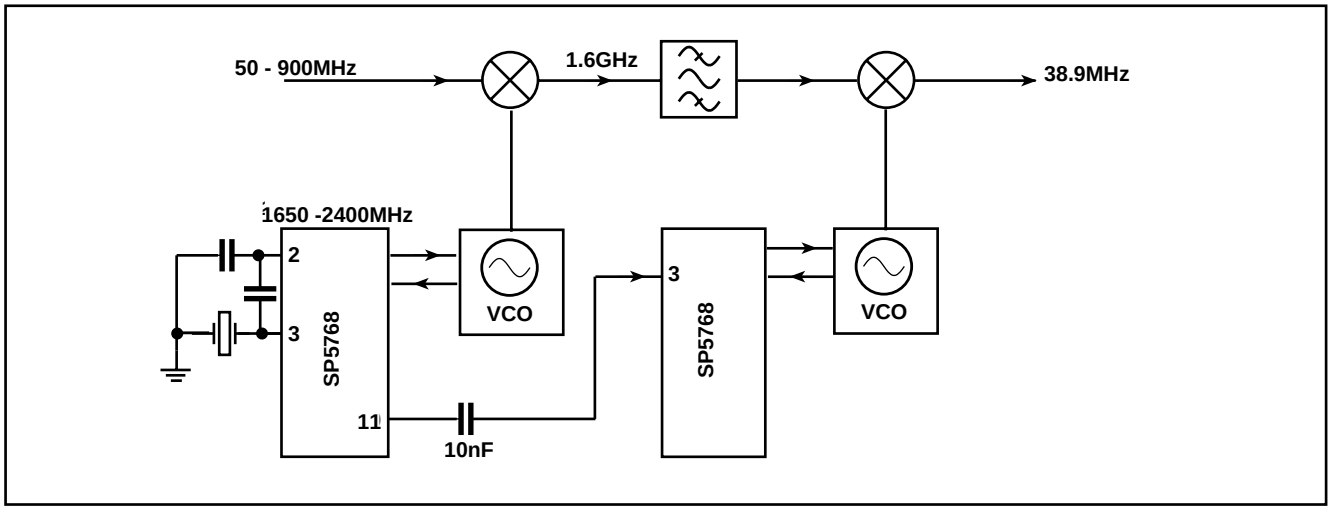


Figure 7 - Example of double conversion from VHF/UHF frequencies to TV IF

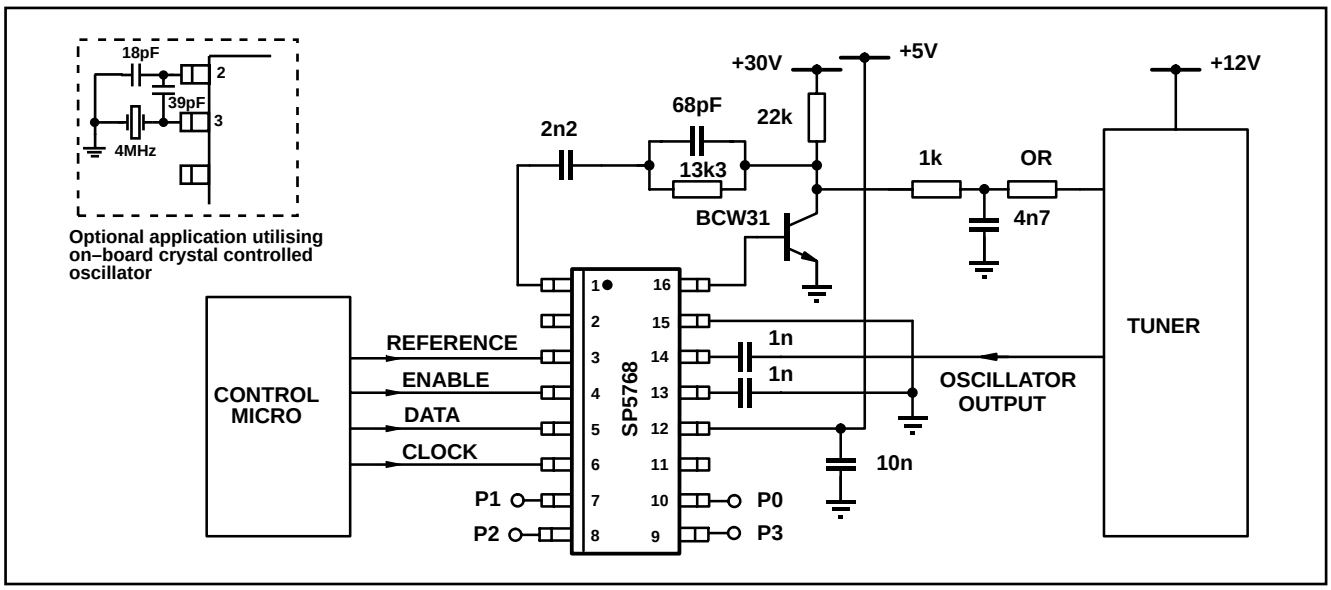


Figure 8 - Typical application SP5768

Application Notes

A generic set of application notes AN168 for designing withsynthesisers such as the SP5768 has been written. This covers aspects such as loop filter design and decoupling. This application note is also featured in the Media Data Book, or refer to the Zarlink Semiconductor Internet Site http://www.zarlink.com.

Reference Source

The SP5768 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase noise within the loop bandwidth is:

$$\text{phase comparator noise floor} + 20 \log_{10} \left(\frac{\text{LO frequency}}{\text{phase comparator frequency}} \right)$$

Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO to phase comparator division ratio is a minimum.

There are two ways of achieving a higher phase comparator sampling frequency:–

A) Reduce the division ratio between the reference source and the phase comparator

B) use a higher reference source frequency.

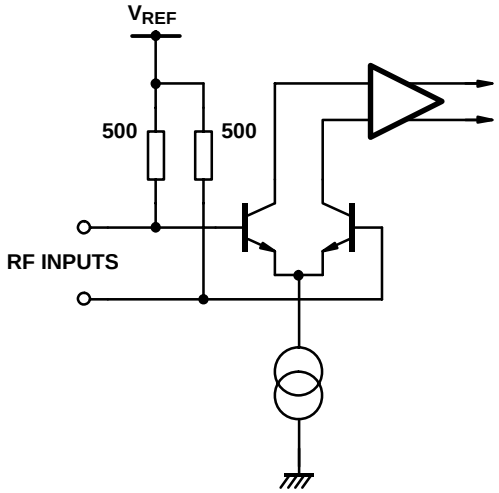
Approach B) may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.

Loop Bandwidth

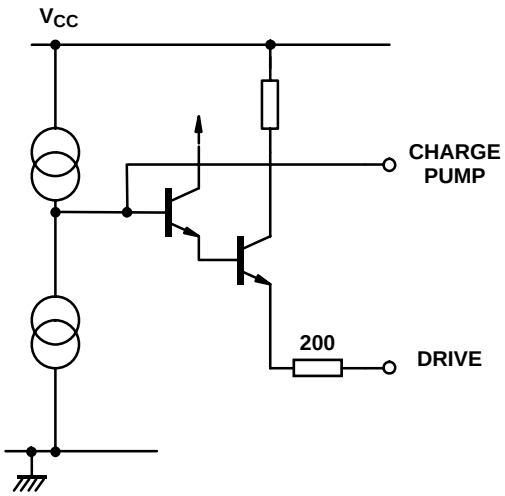
The majority of applications for which the SP5768 is intended require a loop filter bandwidth of between 2kHz and10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

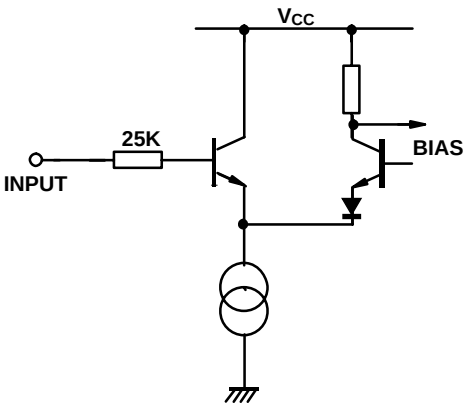
The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.



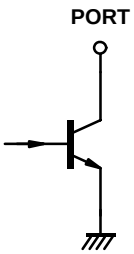
RF inputs



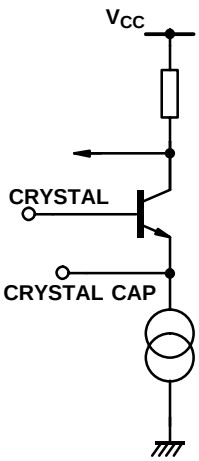
Loop amplifier



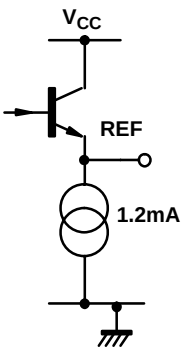
Disable, Enable, Data and Clock inputs



Output Ports



Reference oscillator



Reference output

Figure 9 - Input/Output interface circuits

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