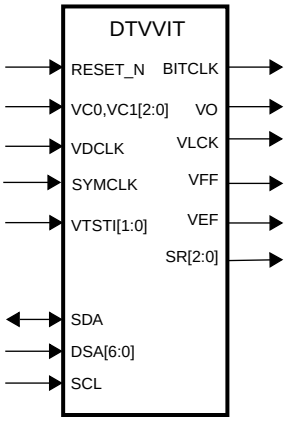
MC92300

Product Preview

VITERBI Decoder for Digital TV

This product preview describes a high performance device, a Viterbi Decoder, for Digital-TV applications according to the EBU defined DVB transmission standard for satellite and cable Set-Top systems.



Viterbi Decoder - Capability Specification

- Operates at max. 50MBits/s output rate to work with all present DVB channels
- Implements K=7, (171_8,133_8) Viterbi decoder for rates 1/2, 2/3, 3/4, 5/6 and 7/8 with a survivor depth of 96
- Code rate and synchronization control programmable via I^2C standard serial bus
- Automatic rate selection and signal quality output (qval)
- Full/empty flag generation of input FIFO for system monitoring of VDCLK/BITCLK ratio
- Simplified system design with internal PLL for the generation of output BITCLK from the incoming VDCLK for all depuncturing modes
- Available in a 128QFP package

Ordering Information	
Device	**Package**
MC92300CG	128QFP

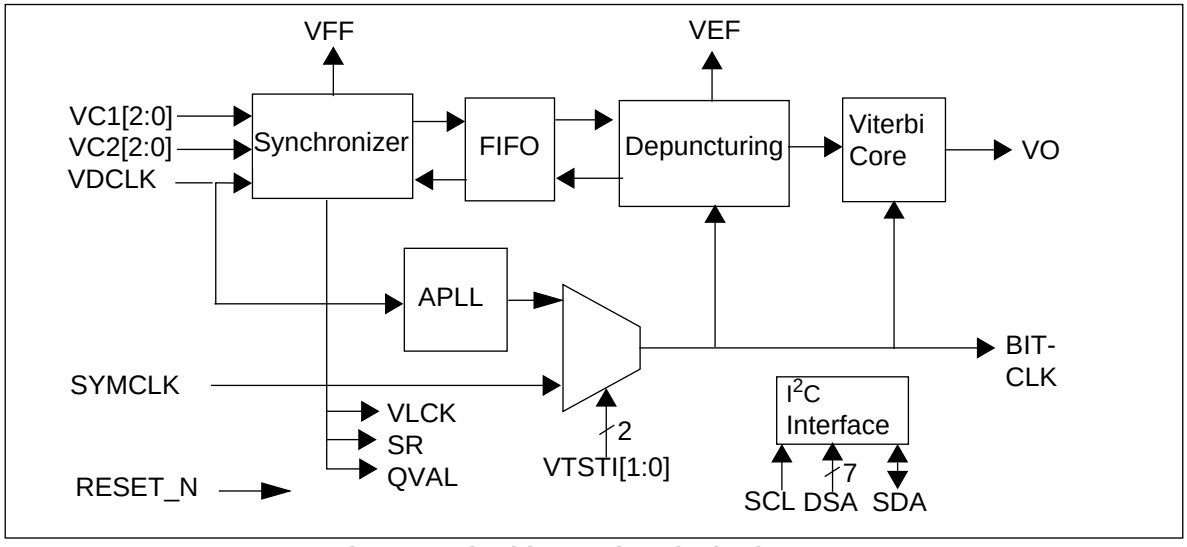


Figure 1. Viterbi Decoder Block Diagram

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

Product Description

The Viterbi Decoder contains the Viterbi core logic, which operates the K=7 convolutional code and generates a lock indication after successful acquisition. The core works with the main clock BITCLK, which provides the output data VO (output of the Viterbi). This clock is generated by the integrated bit clock generator circuit and is adjusted according to the programmed depuncturing rate.

The input to the chip are 3 bit soft decision data VC0/1 from the QPSK demodulator together with the associated demodulator clock VDCLK. Rate adjustment in accordance with the several depuncturing rates is achieved with the input FIFO. The data is read into the depuncturing logic with the internally generated BITCLK.

Generator Polynomials

The Viterbi decoder is designed to decode bit streams encoded using the DVB standard generator polynomials (171_8, 133_8).

Punctured Codes

The Viterbi Decoder is able to decode a basic rate 1/2 convolutional code and the “standard” punctured codes for a k=7 constraint length. The punctured codes are shown in the table below. Specific bits of the original rate 1/2 code sequence are periodically deleted prior to transmission according to the entries in the table, where a 0 means that the bit is deleted and a 1 means that the bit is transmitted.

Table 1 Deletion Map For Punctured Rate 1/2 Codes

Coding Rate	Puncture Map
1/2	1 1
2/3	11 10
3/4	110 101
5/6	11010 10101
7/8	1111010 1000101

Synchronization

Prior to outputting valid data the Viterbi decoder block must synchronize to the input data stream, i.e. remove any phase ambiguity in the received symbols and determine the punctured code rate transmitted

The Viterbi block employs a method known as Syndrom Based Node Synchronization to achieve both I & Q symbol and punctured rate synchronization.
The theory of the Syndrom Based Node Synchronization is based on the observation that the product of the incoming data and a syndrom is zero if there are no errors If errors are present in the data, the probability of 0’s and 1’s in the product increases.
The possible states that the synchronizer has to deal with are a combination of the following factors:

1. The phasing of the received symbols.
   I & Q input streams can either be processed as-is or can be rotated 90^o to account for constellation rotation in the receiver.
2. Determination of the framing of the I and Q bit streams so as to extract the correct symbol. There are four possible ways to frame the two bit stream and the synchronizer must determine the correct one.

I^2C Interface

The internal registers of the VITERBI are accessible via the I^2C interface. After reset, default values are preprogrammed, so that no more configuration is necessary.

APLL

In order to allow a simple system design, a Analogue PLL is integrated for generation of the output Bit Clock. The following output frequencies R_o are generated for a given DVB transponder Bandwidth TBW respectively for a given input symbol rate R_s .

TBW[MHz]	R_s[MHz]	R_o[MHz] for rates 1/2	2/3	3/4	5/6	7/8
36	38.3	28.3	37.7	42.4	47.2	49.5
33						
30						
27						
26	20.5	20.5	27.3	30.7	34.2	35.9
R_s/R_o		1	4/3	3/2	5/3	7/4

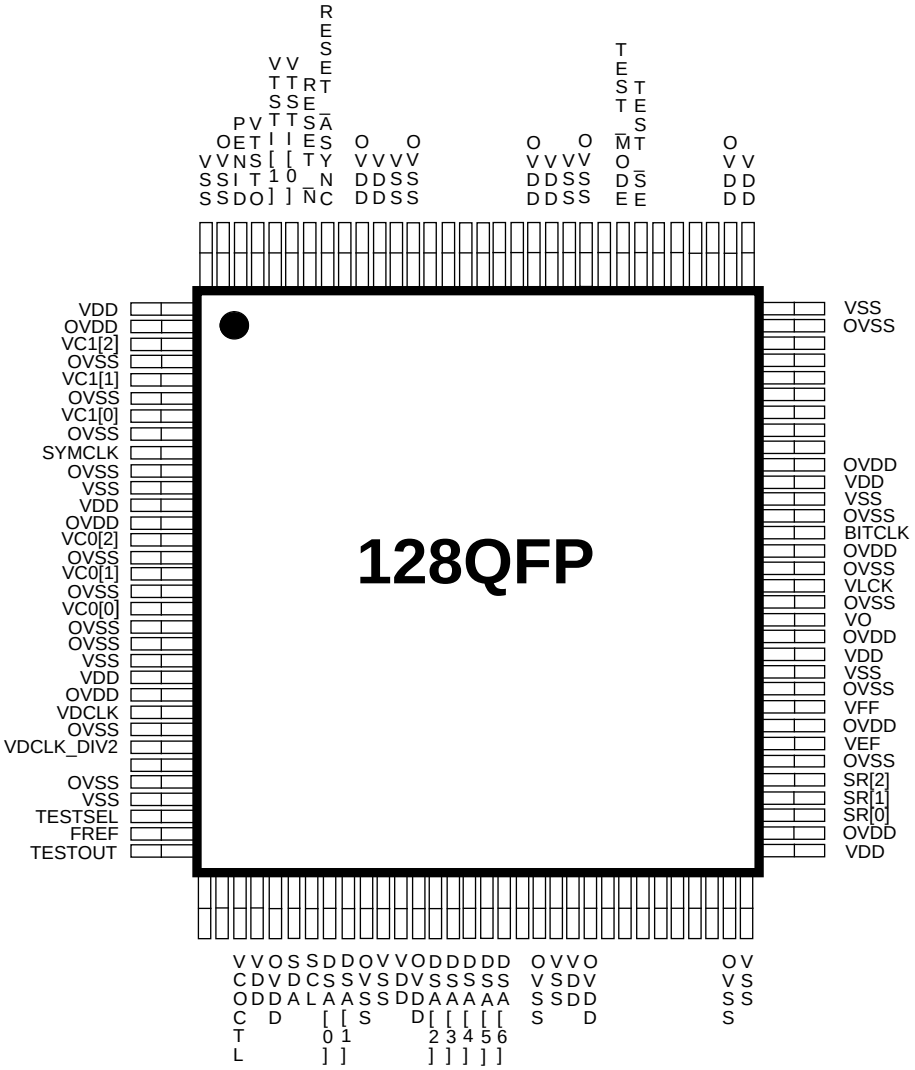
Application

The MC92300 is used in satellite receiver implementation for DVB.

Packaging

The MC92300 is available in a 128-pin Plastic Quad Flat Pack (128QFP) package.

Viterbi Decoder Pin Description



SYMCLK	- System Clock (input clock)
BITCLK	- System Clock (output clock)
VDCLK	- Input Clock
VDCLK_DIV2	- VDCLK/2
RESET_N	- Asynchronous Reset
VLCK	- Viterbi Decoder in Lock
VFF	- FIFO Full Flag
VEF	- FIFO Empty Flag
SR[2:0]	- Selected Rate
VO	- Viterbi Decoder Output
VC0,VC1[2:0]	- Soft Decision Input
SDA	- Data Bus of I^2C-interface
DSA[6:0]	- Slave Address of I^2C-interface
SCL	- Clock Line of I^2C-interface
TESTSEL, FREF, TESTOUT, VCOCTL	- APLL pins
VTSTI[1:0]	- Test pins
VTSTO	- Test output
RESET_ASYNC	- Teset for Scan Test
TEST_SE	- Test pin for Scan Mode
TEST_MODE	- Test pin for Scan Mode

MOTOROLA Device Test Pins:
51, 56-62, 105, 110-115, 120
(don't connect these pins)

NOT CONNECTED Pins:
27, 33, 34, 88-94, 99-102

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