FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12530-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89650AR Series

MB89653AR/655AR/656AR/657AR/P657A
MB89PV650A

■ DESCRIPTION

The MB89650AR series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, timers, PWM timers, a serial interface, an A/D converter, external interrupts, an LCD controller/driver, and a watch prescaler.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8L family CPU core
- Dual-clock control system
- Maximum memory space: 64 Kbytes
- Minimum execution time: 0.4 µs/10 MHz
- Interrupt processing time: 3.6 µs/10 MHz
- I/O ports: max. 64 channels
- 21-bit time-base counter
- 8-bit PWM timers: 2 channels (A maximum of 4 channels can be used for output.)
- 8/16-bit timer/counter: 4 channels (16 bits × 2 channels)
- 8-bit serial I/O: 1 channel
- 8-bit A/D converter: 8 channels

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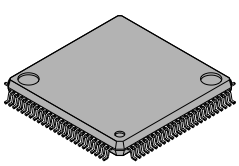
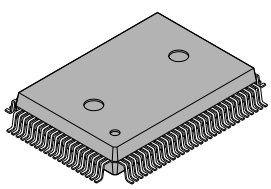
■ PACKAGE

100-pin Plastic SQFP



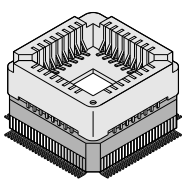
(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

100-pin Ceramic MQFP



(MQP-100C-P02)

MB89650AR Series

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- External interrupt 1
  Four independent channels with edge detection function
- External interrupt 2 (wake-up function)
  Twelve “L” level-interrupt channels
- Watch prescaler
- LCD controller/driver: 16 to 32 segments × 2 to 4 commons
- Power-on reset function
- Low-power consumption modes (subclock mode, watch mode, sleep mode, and stop mode)
- SQFP-100 and QFP-100 packages

■ PRODUCT LINEUP

Parameter \ Part number	MB89653AR	MB89655AR	MB89656AR	MB89657AR	MB89P657A	MB89PV650A
Classification	Mass production products (mask ROM products)				One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits	768 × 8 bits	1 K × 8 bits		
LCD display RAM	16 × 8 bits					
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs/10 MHz to 6.4 µs/10 MHz, 61.0 µs/32.768 kHz Interrupt processing time: 3.6 µs/10 MHz to 57.6 µs/10 MHz, 549.3 µs/32.768 kHz					
Ports	Input ports: 8 (All also serve as peripherals.) Output ports: 8 (All also serve as peripherals.) I/O ports: 48 (All also serve as peripherals.) Total: 64					
8-bit timer 1, 8-bit timer 2	8-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 µs) 16-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 µs) 2 output channels are enabled when operating as an 8-bit timer.					
8-bit timer 3, 8-bit timer 4	8-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 µs) 16-bit timer operation (toggled output capable, operating clock cycle: 0.8 to 12.8 µs) 2 output channels are enabled when operating as an 8-bit timer.					
Clock timer	21 bits × 1 (in main clock mode)/15 bits × 1 (at 32.768 kHz)					
8-bit PWM timer 1, 8-bit PWM timer 2	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 3.3 ms) 8-bit resolution PWM operation (conversion cycle: 102 µs to 839 ms) Both 8-bit PWM timer 1 and 8-bit PWM timer 2 can output 2 channels.					

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Parameter \ Part number	MB89653AR	MB89655AR	MB89656AR	MB89657AR	MB89P657A	MB89PV650A
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)					
8-bit A/D converter	8-bit resolution × 8 channels A/D conversion mode (conversion time: 18 µs) Sense mode (conversion time: 5 µs) Continuous activation by an internal timer capable Reference voltage input					
External interrupt 1	4 independent channels (edge selection) Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)					
External interrupt 2 (wake-up function)	"L" level interrupt × 12 channels					
Standby mode	Subclock mode, sleep mode, watch mode, and stop mode					
Process	CMOS					
Operating voltage*	2.2 V to 6.0 V				2.7 V to 6.0 V	
EPROM for use						MBM27C256A-20TVM

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
In the case of the MB89PV650A, the voltage varies with the restrictions of the EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89653AR MB89655AR MB89656AR MB89657AR MB89P657A	MB89PV650A
FPT-100P-M05	○	×
FPT-100P-M06	○	×
MQP-100C-P02	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

MB89650AR Series

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89653AR, the upper half of the register bank cannot be used.
- On the MB89P657A, the program area starts from address 8006_H but on the MB89PV650A and MB89657AR starts from 8000_H.

  (On the MB89P657A, addresses 8000_H to 8005_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV650A and MB89657A, addresses 8000_H to 8005_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P657A.)
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV650A, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

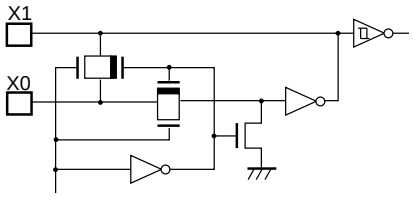
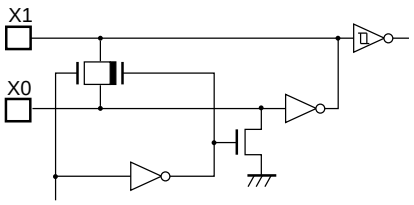
Take particular care on the following points:

- A pull-up resistor cannot be set for P70 to P75 on the MB89P657A. On this product, a pull-up resistor must be selected in a group of four bits for P14 to P17, P40 to P43, and P44 to P47.
- A pull-up resistor is not selectable for P30 to P37 and P40 to P47 if they are used as LCD pins.
- Options are fixed on the MB89PV650A.

4. Differences between the MB89650A and MB89650AR Series

- Electrical specifications/electrical characteristics
  Electrical specifications of the MB89650AR series are the same with that of the MB89650A series.
  Electrical characteristics of both series are much the same.
- Oscillation circuit type
  In the MB89650A series, the circuit type of using an external clock differs from that of using a crystal or ceramic resonator as follows.
  Circuit type of the MB89650AR series is a circuit type in using external clock even when crystal or ceramic resonator is selected.
- Memory access area and other specifications of both the MB89650A and MB89650AR series are the same.

- **I/O circuit type**

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) MB89PV650A and MB89P657A, external clock input selection versions of MB89653A/655A/656A/657A At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
		• Crystal or ceramic oscillation type (main clock) Crystal or ceramic oscillation selection versions of MB89653A/655A/656A/657A At an oscillation feedback resistor of approximately 1 MΩ/5.0 V

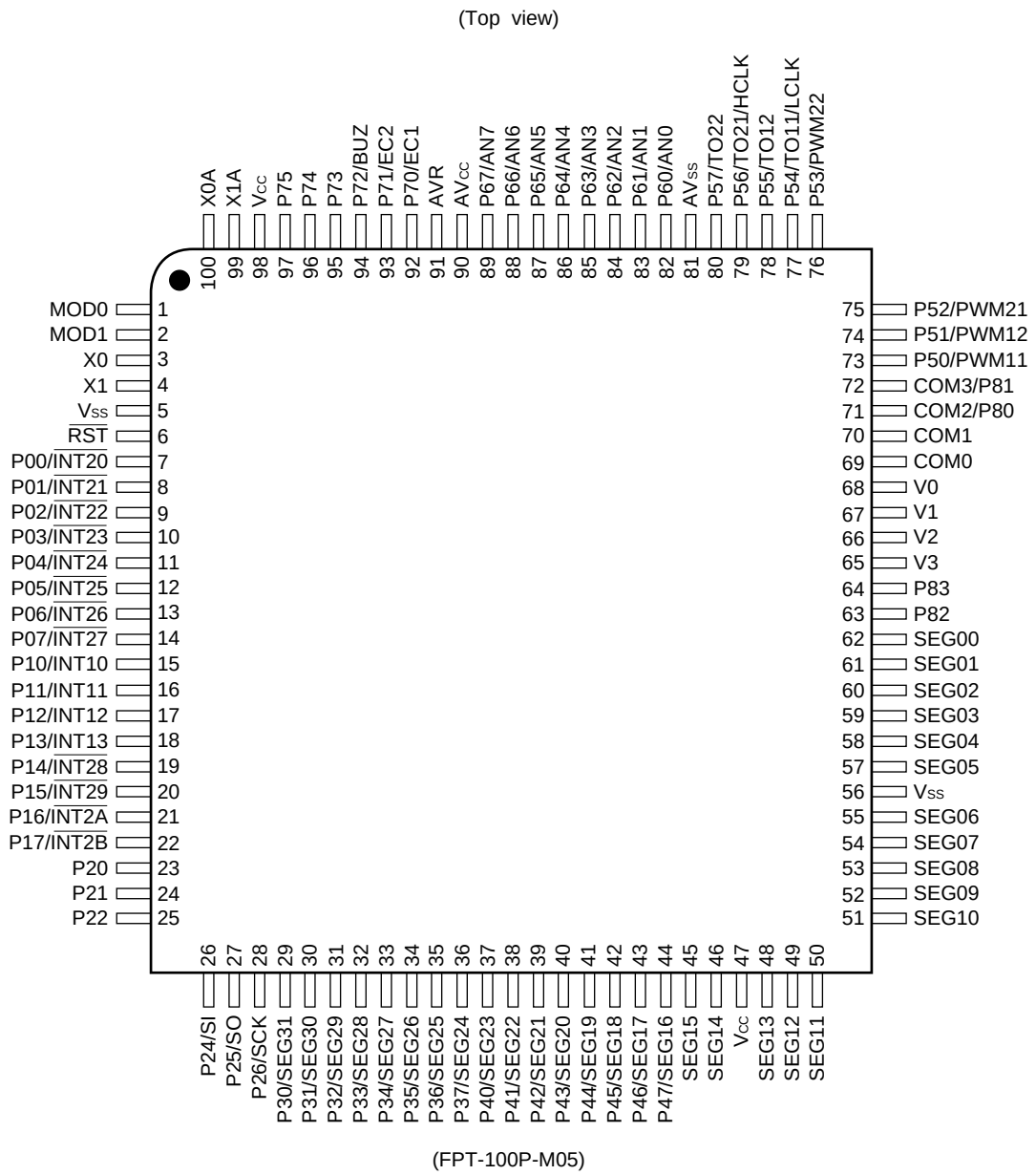
■ CORRESPONDENCE BETWEEN THE MB89650A AND MB89650AR SERIES

- The MB89650AR series is the reduction version of the MB89650A series.
- The MB89650A and MB89650AR series consist of the following products:

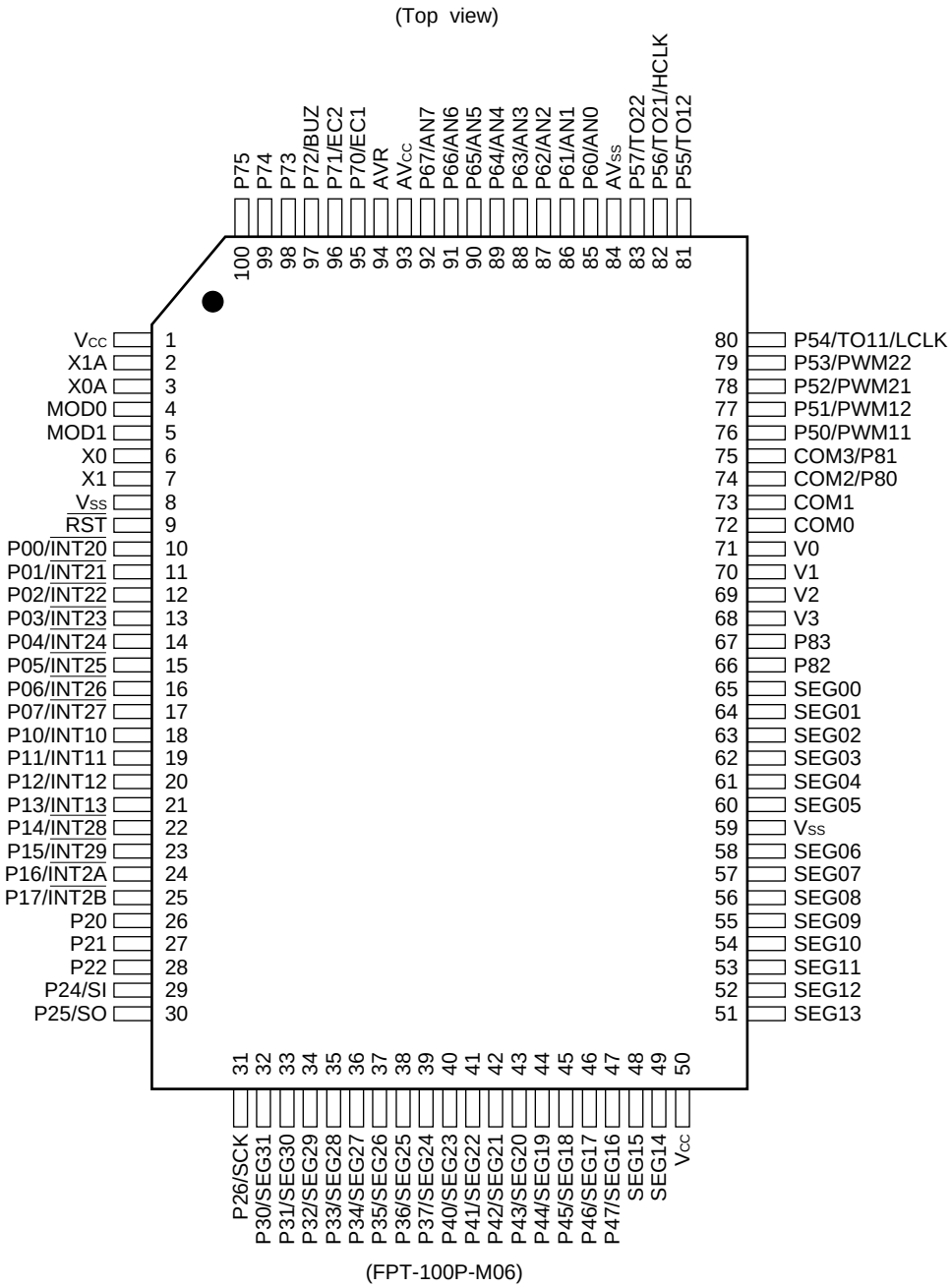
MB89650A series	MB89653A	MB89655A	MB89656A	MB89657A	MB89P657A	MB89PV650A
MB89650AR series	MB89653AR	MB89655AR	MB89656AR	MB89657AR		

MB89650AR Series

■ PIN ASSIGNMENT



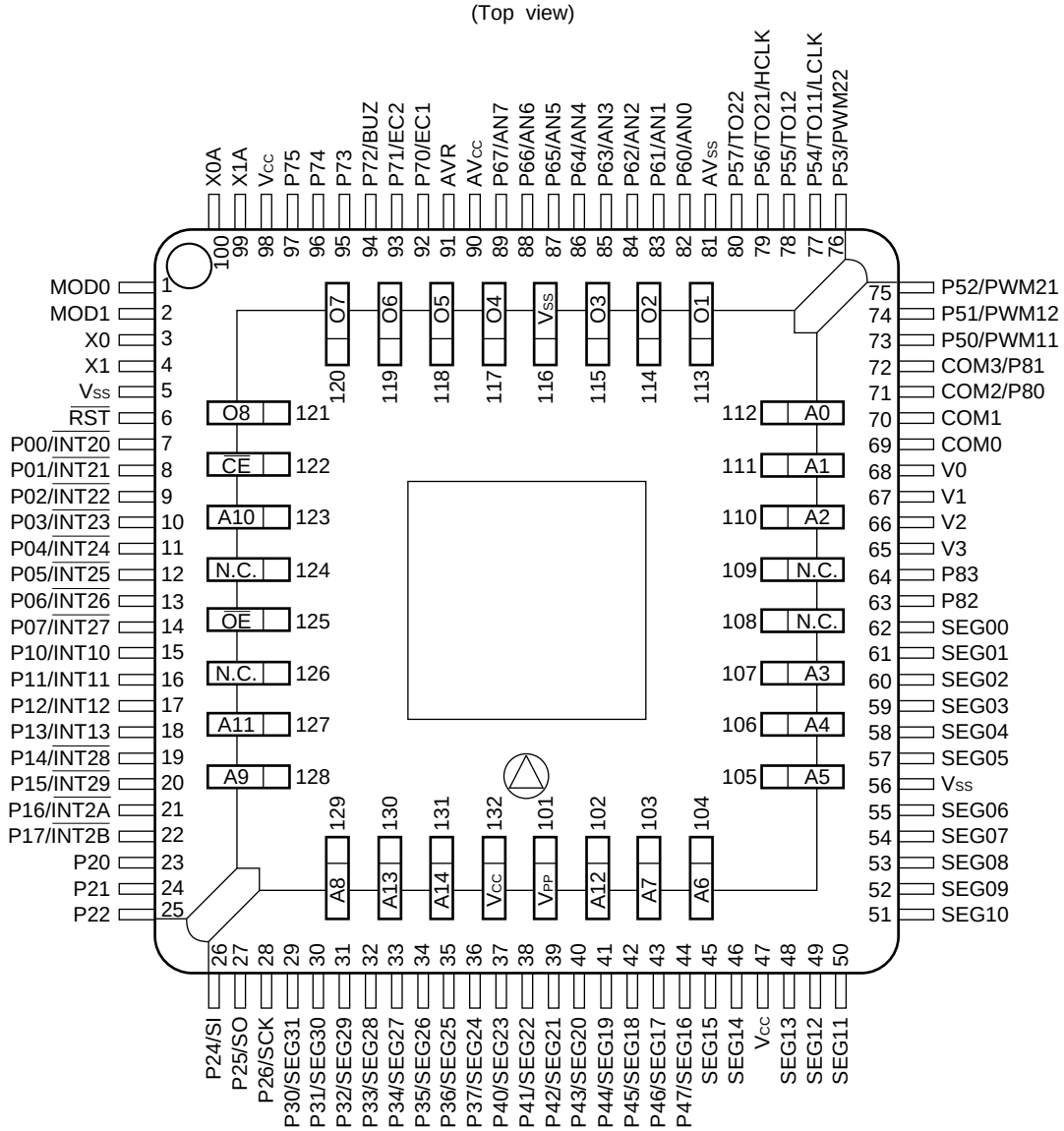
(FPT-100P-M05)


(Top view)
P75 100
P74 99
P73 98
P72/BUZ 97
P71/EC2 96
P70/EC1 95
AVR 94
AVCC 93
P67/AN7 92
P66/AN6 91
P65/AN5 90
P64/AN4 89
P63/AN3 88
P62/AN2 87
P61/AN1 86
P60/AN0 85
AVSS 84
P57/TO22 83
P56/TO21/HCLK 82
P55/TO12 81
VCC 1
X1A 2
X0A 3
MOD0 4
MOD1 5
X0 6
X1 7
VSS 8
RST 9
P00/INT20 10
P01/INT21 11
P02/INT22 12
P03/INT23 13
P04/INT24 14
P05/INT25 15
P06/INT26 16
P07/INT27 17
P10/INT10 18
P11/INT11 19
P12/INT12 20
P13/INT13 21
P14/INT28 22
P15/INT29 23
P16/INT2A 24
P17/INT2B 25
P20 26
P21 27
P22 28
P24/SI 29
P25/SO 30
80 P54/TO11/LCLK
79 P53/PWM22
78 P52/PWM21
77 P51/PWM12
76 P50/PWM11
75 COM3/P81
74 COM2/P80
73 COM1
72 COM0
71 V0
70 V1
69 V2
68 V3
67 P83
66 P82
65 SEG00
64 SEG01
63 SEG02
62 SEG03
61 SEG04
60 SEG05
59 VSS
58 SEG06
57 SEG07
56 SEG08
55 SEG09
54 SEG10
53 SEG11
52 SEG12
51 SEG13
31 P26/SCK
32 P30/SEG31
33 P31/SEG30
34 P32/SEG29
35 P33/SEG28
36 P34/SEG27
37 P35/SEG26
38 P36/SEG25
39 P37/SEG24
40 P40/SEG23
41 P41/SEG22
42 P42/SEG21
43 P43/SEG20
44 P44/SEG19
45 P45/SEG18
46 P46/SEG17
47 P47/SEG16
48 SEG15
49 SEG14
50 VCC

(FPT-100P-M06)

MB89650AR Series

(Top view)



(MQP-100C-P02)

- **Pin assignment on package top (MB89PV650A only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
101	V_{PP}	109	N.C.	117	O4	125	$\overline{OE}$
102	A12	110	A2	118	O5	126	N.C.
103	A7	111	A1	119	O6	127	A11
104	A6	112	A0	120	O7	128	A9
105	A5	113	O1	121	O8	129	A8
106	A4	114	O2	122	$\overline{CE}$	130	A13
107	A3	115	O3	123	A10	131	A14
108	N.C.	116	V_{SS}	124	N.C.	132	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2 SQFP*3			
4	1	MOD0	J	Operating mode selection pins Connect to V_{SS} (GND) when using.
5	2	MOD1		
6	3	X0	A	Main clock crystal oscillator pins (max. 10 MHz)
7	4	X1		
8	5	V_{SS}	—	Power supply (GND) pin
9	6	$\overline{RST}$	J	Reset input pin
10 to 17	7 to 14	P00/$\overline{INT20}$ to P07/$\overline{INT27}$	F	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input ($\overline{INT20}$ to $\overline{INT27}$) is hysteresis input while port input (P00 to P07) is CMOS input.
18 to 21	15 to 18	P10/INT10 to P13/INT13	F	General-purpose I/O ports Also serve as an external interrupt 1 input. External interrupt 1 input (INT10 to INT13) is hysteresis input while port input (P10 to P13) is CMOS input.
22 to 25	19 to 22	P14/$\overline{INT28}$ to P15/$\overline{INT2B}$	F	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input ($\overline{INT28}$ to $\overline{INT2B}$) is hysteresis input while port input (P14 to P17) is CMOS input.
26 to 28	23 to 25	P20 to P22	C	General-purpose I/O ports
29, 30, 31	26, 27, 28	P24/SI, P25/SO, P26/SCK	F	General-purpose I/O ports The output type can be switched between N-ch open-drain and CMOS. These ports also serve as an 8-bit serial I/O. The P26/SCK pin is a CMOS input type when it functions as the port input (P26) while the pin is a hysteresis input type when it functions as the serial clock input (SCK).
32 to 47	29 to 44	P36/SEG31 to P47/SEG26	H	General-purpose I/O ports Also serve as an LCD controller/driver segment output.
48, 49	45, 46	SEG15, SEG14	I	LCD controller/driver segment output pins

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*1: FPT-100P-M06
*2: FPT-100P-M05
*3: MQP-100C-P02

MB89650AR Series

(Continued)

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2 SQFP*3			
50	47	V_{CC}	—	Power supply pin
51 to 58	48 to 55	SEG13 to SEG06	I	LCD controller/driver segment output pins
59	56	V_{SS}	—	Power supply (GND) pin
60 to 65	57 to 62	SEG05 to SEG00	I	LCD controller/driver segment output pins
66, 67	63, 64	P82, P83	C	General-purpose I/O ports
68 to 71	65 to 68	V3 to V0	—	LCD driving power supply pins
72, 73	69, 70	COM0, COM1	I	LCD controller/driver common output pins
74, 75	71, 72	COM2/P80, COM3/P81	H	General-purpose I/O ports Also serve as an LCD controller/driver common output.
76 to 79	73 to 76	P50/PWM11 to P53/PWM22	G	General-purpose output ports Also serve as an 8-bit PWM timer.
80, 81, 82, 83	77, 78, 79, 80	P54/TO11/LCLK, P55/TO12, P56/TO21/HCLK, P57/TO22	G	General-purpose output ports Also serve as an 8/16-bit timer. P54 and P56 also serve as a 32.768 kHz oscillation output/10 MHz divide-by-two output.
84	81	AV_{SS}	—	A/D converter power supply (GND) pin
85 to 92	82 to 89	P60/AN0 to P67/AN7	E	General-purpose input ports Also serve as an analog input.
93	90	AV_{CC}	—	A/D converter power supply pin
94	91	AVR	—	A/D converter reference voltage input pin
95, 96	92, 93	P70/EC1, P71/EC2	K	General-purpose N-ch open-drain I/O ports Also serve as an 8/16-bit timer to input hysteresis.
97, 98 to 100	94, 95 to 97	P72/BUZ, P73 to P75	D	General-purpose N-ch open-drain I/O ports P72 also serves as a buzzer output.
1	98	V_{CC}	—	Power supply pin
2	99	X1A	B	Subclock crystal oscillator pins (32.768 kHz)
3	100	X0A		

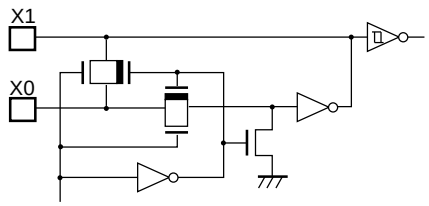
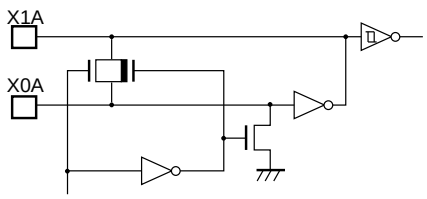
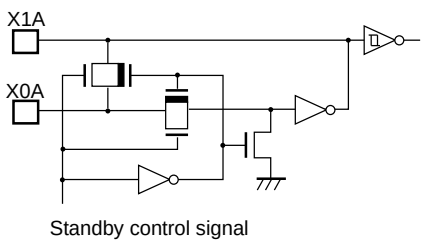
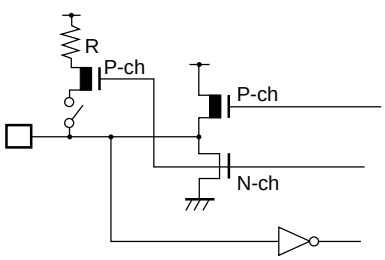
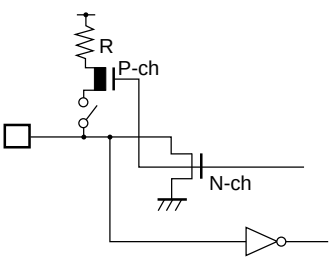
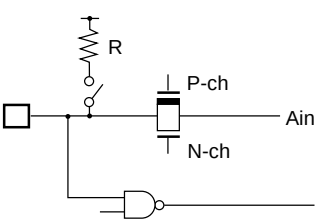
*1: FPT-100P-M06
*2: FPT-100P-M05
*3: MQP-100C-P02

- **External EPROM pins (MB89PV650A only)**

Pin no.	Pin name	I/O	Function
101	V_{PP}	O	“H” level output pin
102 103 104 105 106 107 110 111 112	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
113 114 115	O1 O2 O3	I	Data input pins
116	V_{SS}	O	Power supply (GND) pin
117 118 119 120 121	O4 O5 O6 O7 O8	I	Data input pins
122	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
123	A10	O	Address output pin
125	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
127 128 129	A11 A9 A8	O	Address output pins
130	A13	O	Address output pin
131	A14	O	Address output pin
132	V_{CC}	O	EPROM power supply pin
108 109 124 126	N.C.	—	Internally connected pins Be sure to leave them open.

MB89650AR Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) MB89PV650A and MB89P657A, external clock input selection versions of MB89653AR/655AR/656AR/657AR At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		• Crystal or ceramic oscillation type (subclock) MB89PV650A, MB89P657A At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
		• Crystal or ceramic oscillation type (subclock) MB89653AR/655AR/656AR/657AR At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
C		• CMOS I/O • Pull-up resistor optional (except P82 and P83)
D		• N-ch open-drain I/O • CMOS input • Pull-up resistor optional
E		• A/D converter input • CMOS input • Pull-up resistor optional

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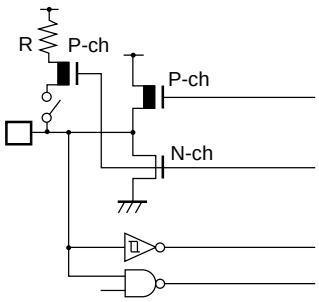
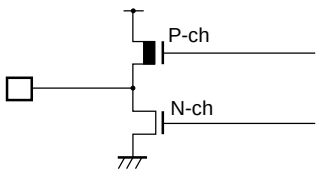
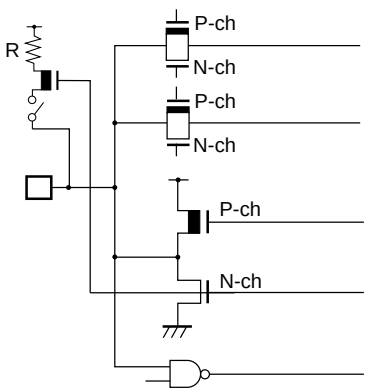
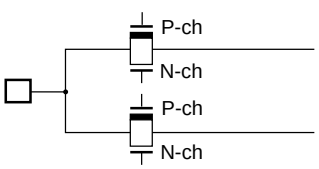
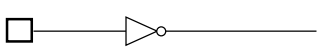
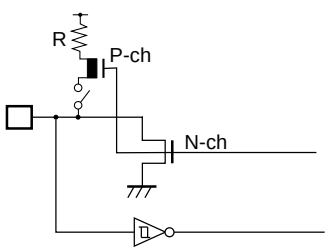
Type	Circuit	Remarks
F		• CMOS I/O (when selected as general-purpose ports) P24 to P26 outputs can be switched between CMOS and N-ch open-drain. • When toggled as hysteresis input peripherals. However, SI input excluded. • Pull-up resistor optional
G		• CMOS output
H		• LCD controller/driver output • CMOS I/O • Pull-up resistor optional
I		• LCD controller/driver output
J		
K		• Hysteresis input • N-ch open-drain output • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P657A

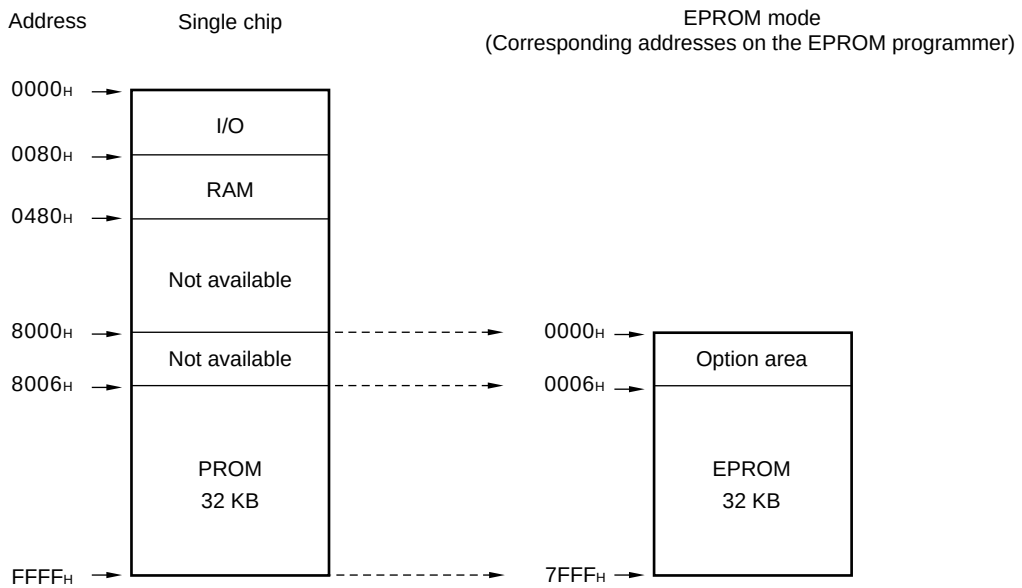
The MB89P657A is an OTPROM version of the MB89650A series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P657A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 32 Kbytes (8006H to FFFFH) the PROM can be programmed as follows:

- **Programming procedure**

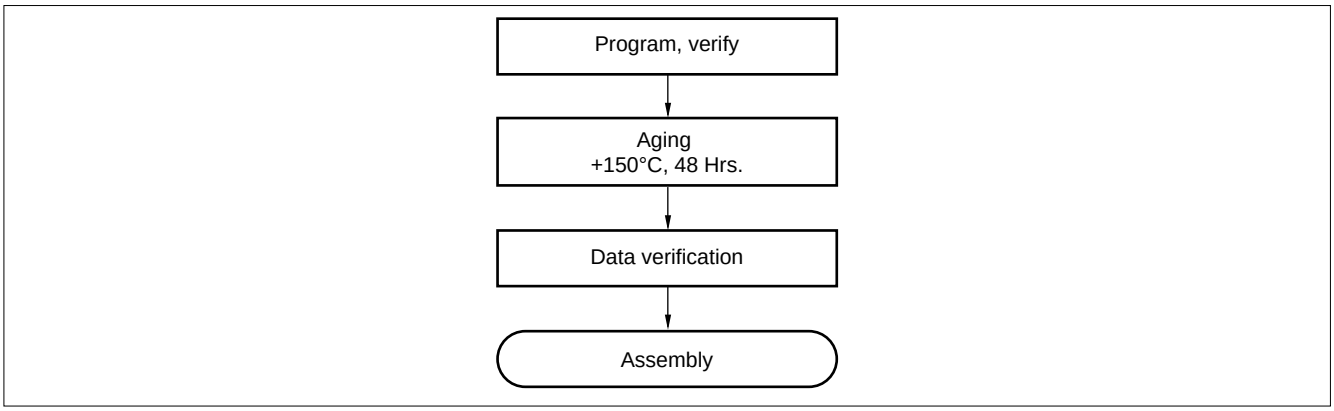
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0006H to 7FFFH (note that addresses 8006H to FFFFH while operating as a single chip assign to 0006H to 7FFFH in EPROM mode).
Load option data into addresses 0000H to 0005H of the EPROM programmer. (For information about each corresponding option, see “7. Setting OTPROM Options.”)

(3) Program to 0000H to 7FFFH with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-100P-M05	ROM-100SQF-28DP-8L
FPT-100P-M06	ROM-100QF-28DP-8L2

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: Connect the ROM-100SQF-28DP-8L jumper pin to V_{SS} when using.
Depending on the EPROM programmer, inserting a capacitor of about 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes	Single/dual-clock system 1: Dual clock 2: Single clock
0001_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0003_H	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
0004_H	P47 to P44 Pull-up 1: No 0: Yes	P43 to P40 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
0005_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P17 to P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes

Notes: • Set each bit to 1 to erase.
• Do not write 0 to the vacant bit.
The read value of the vacant bit is 1, unless 0 is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adapter

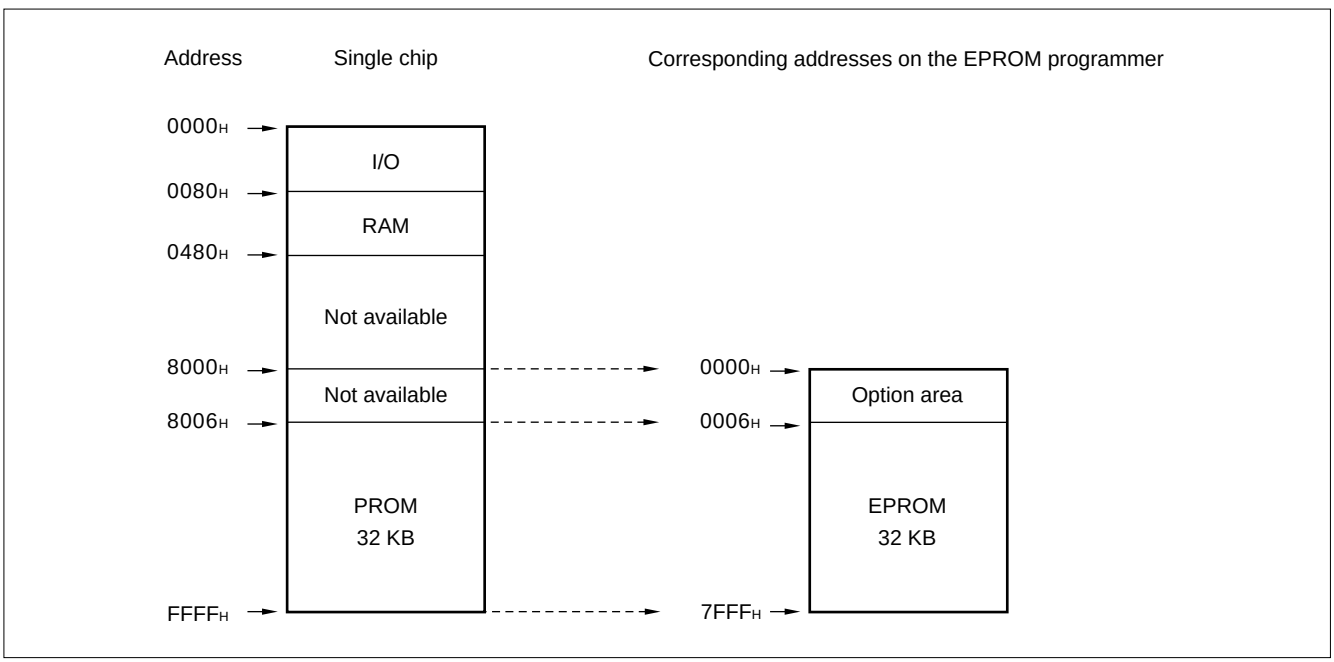
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



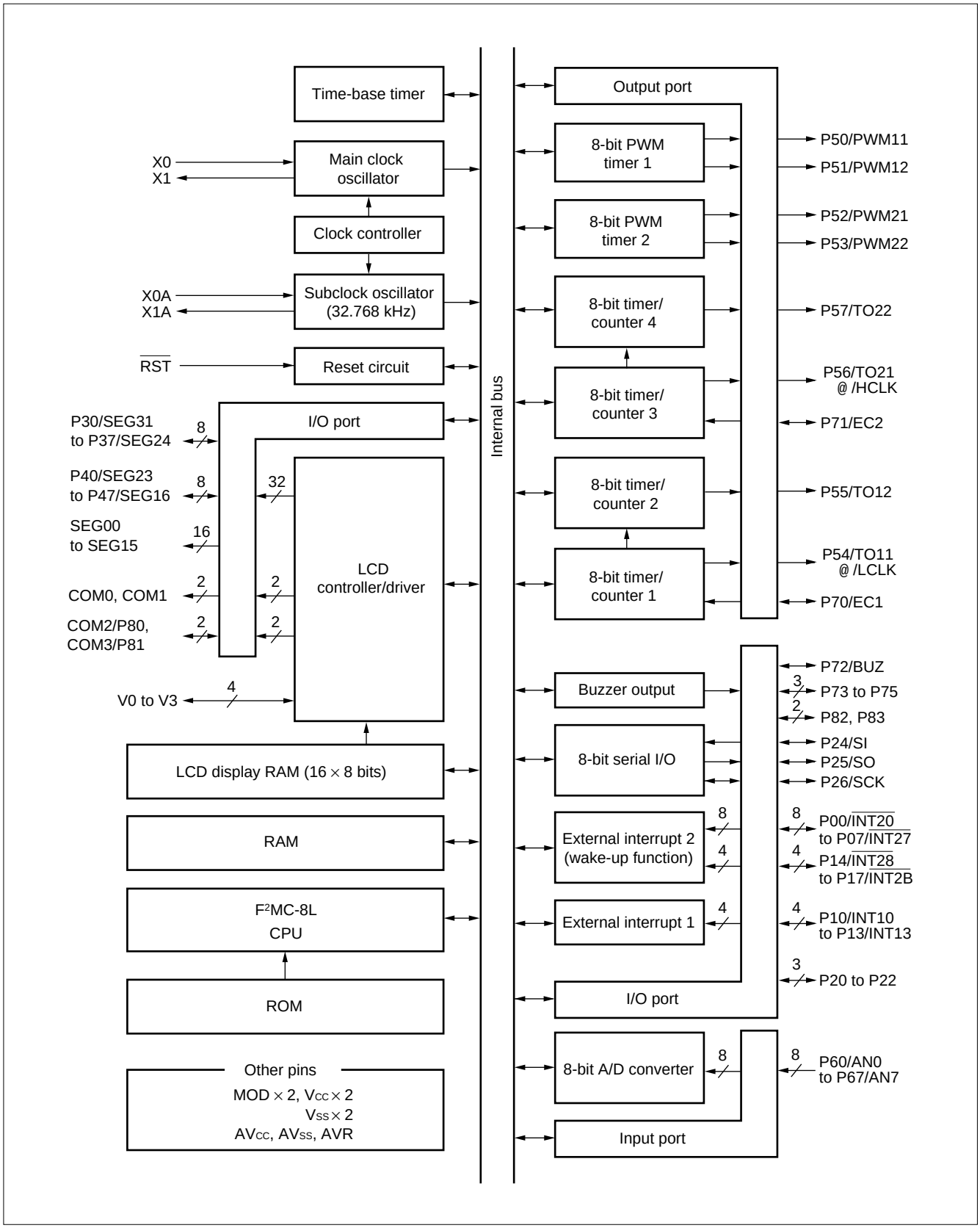
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0006_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

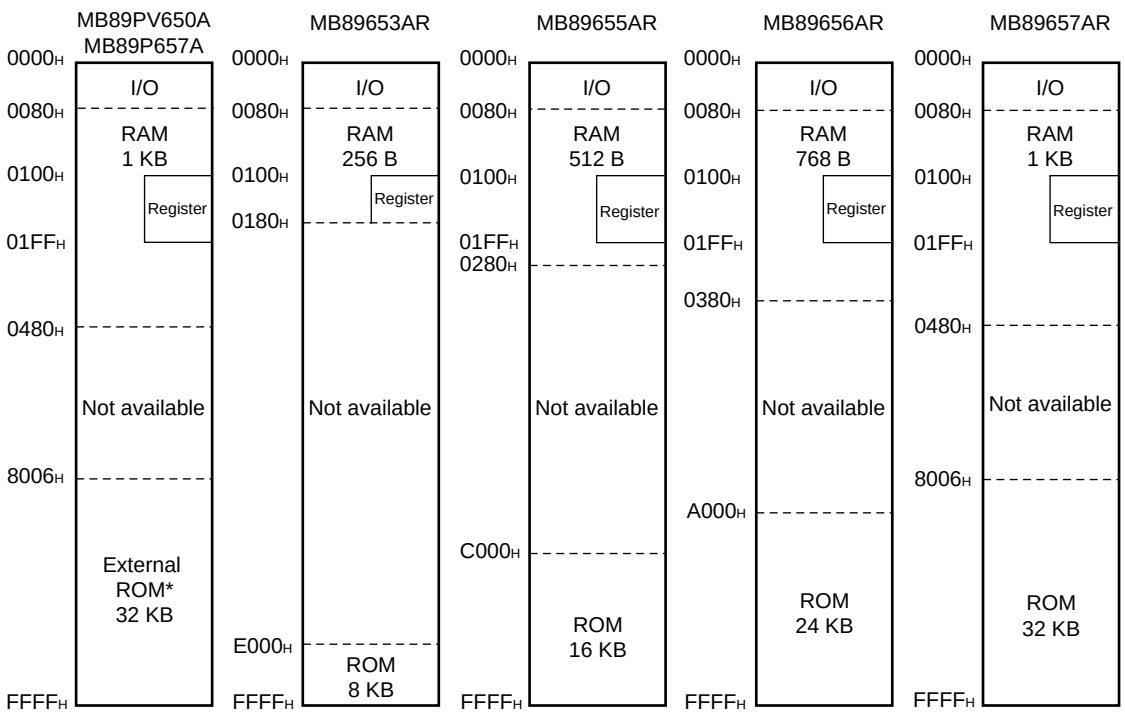


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89650AR series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89650AR series is structured as illustrated below.

Memory Space

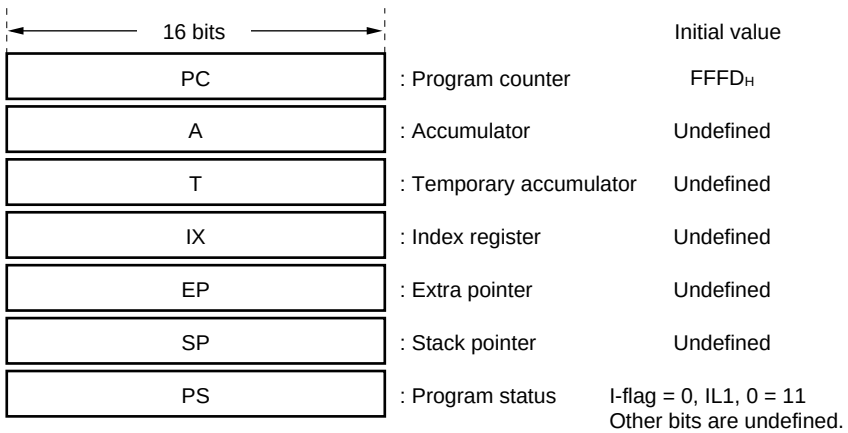


*: This is an internal PROM on the MB89P657A.
Since addresses 8000H to 8005H for the MB89P657A comprise an option area, do not use this area for the MB89PV650A.

2. Registers

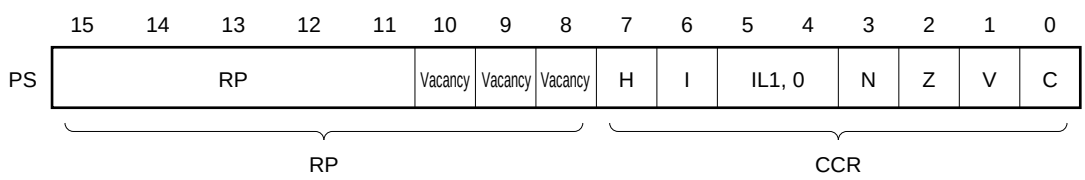
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



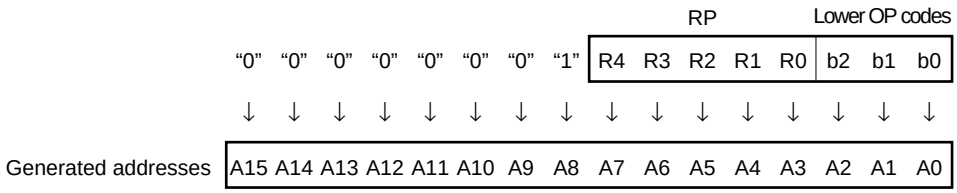
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

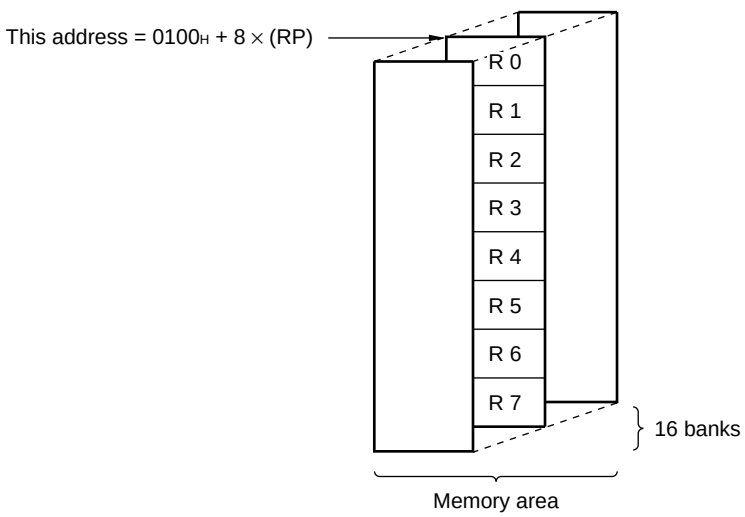
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89653AR (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size. Up to a total of 32 banks can be used on other than the MB89653AR.

Register Bank Configuration



MB89650AR Series

■ I/O MAP

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	DDR1	Port 1 data direction register
04_H	(R/W)	PDR2	Port 2 data register
05_H	(R/W)	DDR2	Port 2 data direction register
06_H			Vacancy
07_H	(R/W)	SCC	System clock control register
08_H	(R/W)	SMC	System mode control register
09_H	(R/W)	WDTC	Watchdog time control register
$0A_H$	(R/W)	TBTC	Time-base timer control register
$0B_H$	(R/W)	WCR	Watch prescaler control register
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$	(R/W)	DDR3	Port 3 data direction register
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$	(R/W)	DDR4	Port 4 data direction register
10_H	(R/W)	T4CR	Timer 4 control register
11_H	(R/W)	T3CR	Timer 3 control register
12_H	(R/W)	T4DR	Timer 4 data register
13_H	(R/W)	T3DR	Timer 3 data register
14_H			Vacancy
15_H			Vacancy
16_H	(R/W)	PDR5	Port 5 data register
17_H			Vacancy
18_H			Vacancy
19_H			Vacancy
$1A_H$	(W)	ICR6	Port 6 input control register
$1B_H$	(R)	PDR6	Port 6 data register
$1C_H$	(R/W)	PDR7	Port 7 data register
$1D_H$	(R/W)	CHG2	Port 2 switching register
$1E_H$	(R/W)	CNTR1	PWM 0/1 control register
$1F_H$	(W)	COMP1	PWM 0/1 compare register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20_H	(R/W)	CNTR2	PWM 2/3 control register
21_H	(W)	COMP2	PWM 2/3 compare register
22_H			Vacancy
23_H			Vacancy
24_H	(R/W)	T2CR	Timer 2 control register
25_H	(R/W)	T1CR	Timer 1 control register
26_H	(R/W)	T2DR	Timer 2 data register
27_H	(R/W)	T1DR	Timer 1 data register
28_H	(R/W)	SMR	Serial mode register
29_H	(R/W)	SDR	Serial data register
$2A_H$			Vacancy
$2B_H$			Vacancy
$2C_H$			Vacancy
$2D_H$	(R/W)	ADC1	A/D converter control register 1
$2E_H$	(R/W)	ADC2	A/D converter control register 2
$2F_H$	(R/W)	ADCD	A/D converter data register
30_H	(R/W)	EIE1	External interrupt 1 enable register
31_H	(R/W)	EIF1	External interrupt 1 flag register
32_H	(R/W)	EIE2	External interrupt 2 enable register
33_H	(R/W)	EIF2	External interrupt 2 flag register
34_H to $5F_H$			Vacancy
60_H to $6F_H$	(R/W)	VRAM	Display data RAM
70_H	(R/W)	LCR1	LCD controller/driver control register 1
71_H	(R/W)	LCR2	LCD controller/driver control register 2
72_H	(R/W)	PDR8	Port 8 data register
73_H	(W)	DDR8	Port 8 data direction register
74_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

Note: Do not use vacancies.

MB89650AR Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*1
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	
LCD power supply voltage	V0 to V3	V_{SS} – 0.3	V_{SS} + 7.0	V	V0 to V3 must not exceed V_{CC}.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P70 to P75*2
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P70 to P75
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P70 to P75*2
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P70 to P75
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AVR does not exceed AV_{CC} + 0.3 V and AV_{CC} does not exceed V_{CC}, such as when power is turned on.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89653AR/655AR/656AR/657AR
		2.7*	6.0*	V	Normal operation assurance range* MB89PV650A/P657A
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
LCD power supply voltage	V0 to V3	V_{SS}	V_{CC}	V	LCD power supply range (The optimum value is dependent on the LCD element in use.)
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

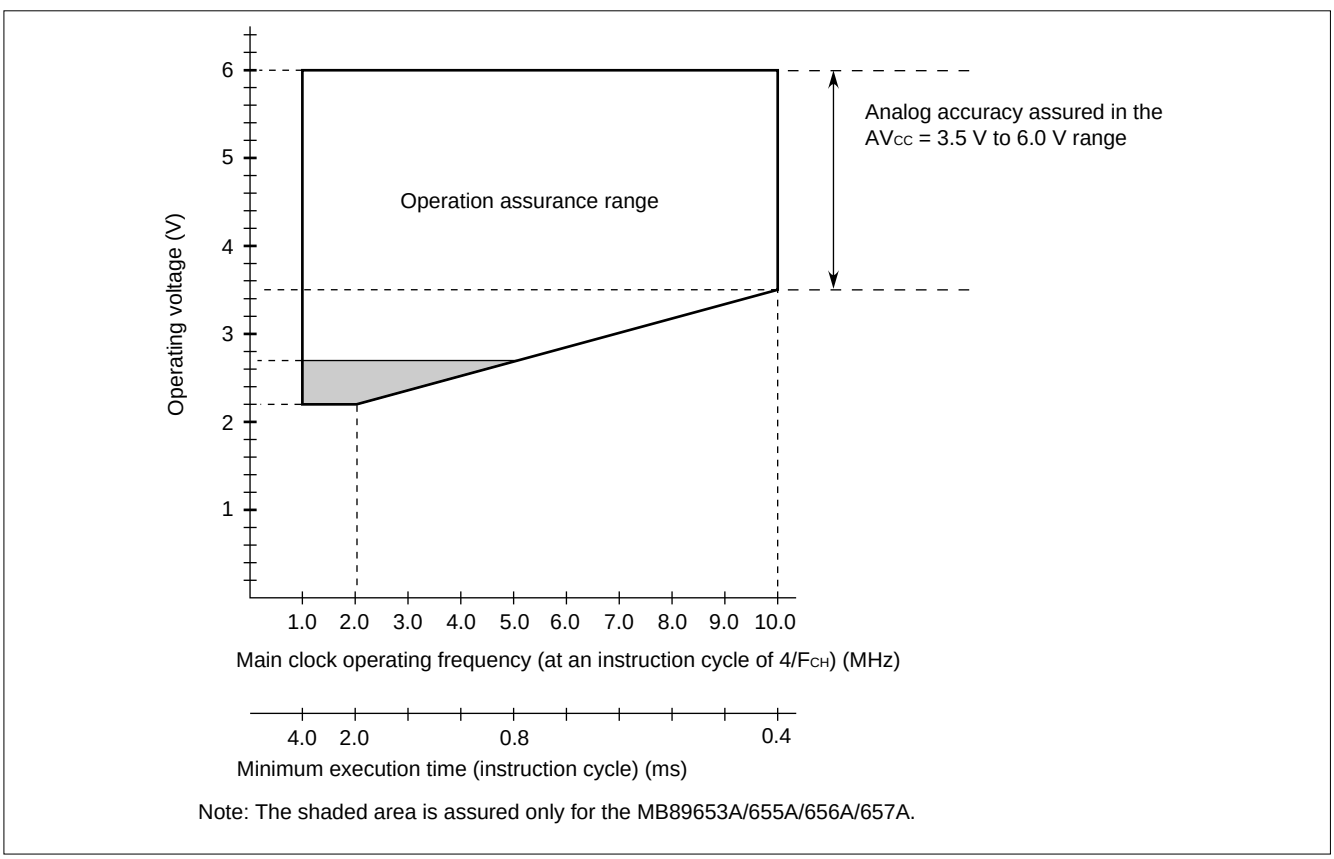


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_{CH}.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH1}	P20 to P26, P30 to P37, P40 to P47, P60 to P67, P80 to P83	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IH2}	P72 to P75	—	0.7 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
	V_{IHS}	P00 to P07, P10 to P17, $\overline{RST}$, MOD0, MOD1, P26 (at SC input)	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS2}	P70, P71	—	0.8 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
"L" level input voltage	V_{IL}	P20 to P26, P30 to P37, P40 to P47, P60 to P67, P72 to P75, P80 to P83	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{IS}	P00 to P07, P10 to P17, P26 (at SC input), P70, P71, $\overline{RST}$, MOD0, MOD1	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P24 to P26	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	N-ch open-drain
	V_{D2}	P70 to P75	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P80 to P83	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P70 to P75, P80 to P83	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P60 to P67, P70 to P75, P80 to P83, MOD0, MOD1, $\overline{RST}$	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P60 to P67, P70 to P75, P80 to P81	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89653AR/655AR/656AR/657AR/PV650A
				—	1.5	2.5	mA	MB89P657A
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89P657A/655AR/656AR/657AR/PV650A
				—	500	700	µA	MB89P657A
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	15	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	
	I_A	AV_{CC}	F_{CH} = 10 MHz, when A/D conversion is activated	—	1.5	3	mA	
	I_{AH}		F_{CH} = 10 MHz, T_A = +25°C, when A/D conversion is stopped	—	—	1	µA	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
LCD divided resistance	R_{LCD}	—	Between V_{CC} and V0 at V_{CC} = 5.0 V	300	500	750	kΩ	
COM0 to 3 output impedance	R_{VCOM}	COM0 to 3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
SEG0 to 31 output impedance	R_{VSEG}	SEG0 to 31		—	—	15	kΩ	
LCD controller/driver leakage current	I_{LCDL}	V0 to V3, COM0 to 3 SEG0 to SEG31	—	—	—	±1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The power supply current is measured at the external clock.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

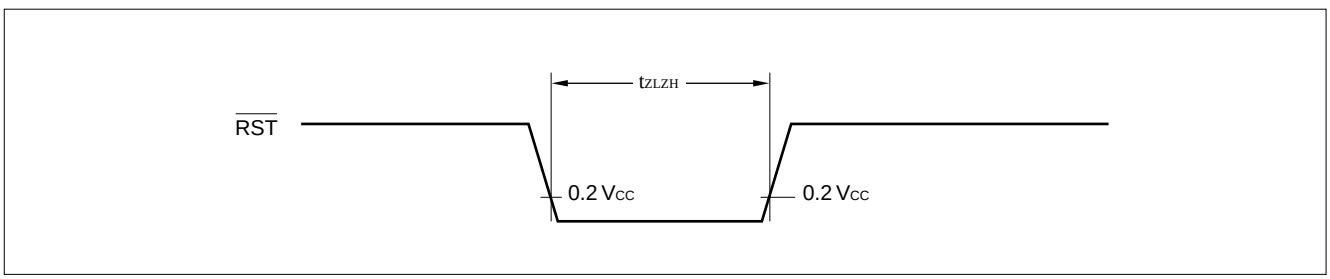
Note: For pins which serve as the LCD and ports (P30 to P37, P40 to P47, and P80 to P81), see the port parameter when these pins are used as ports and the LCD parameter when they are used as LCD pins.

4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

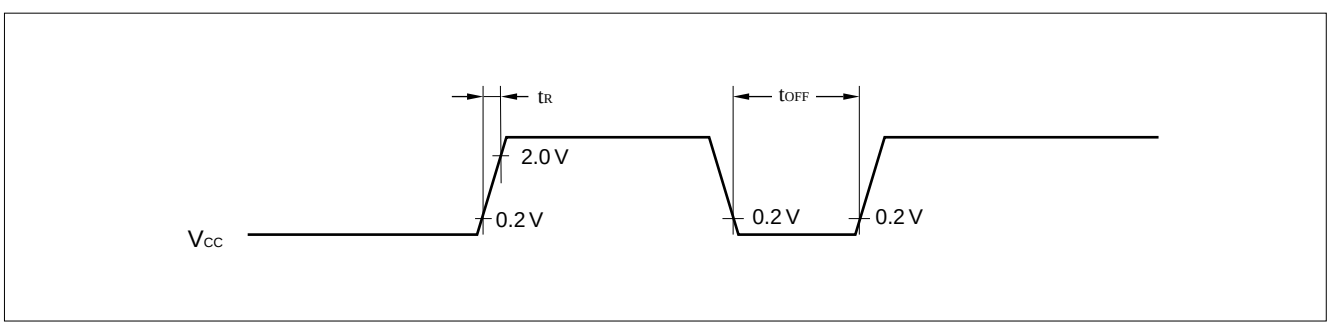


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

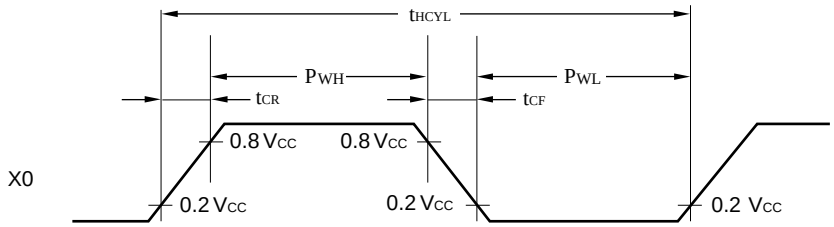


(3) Clock Timing

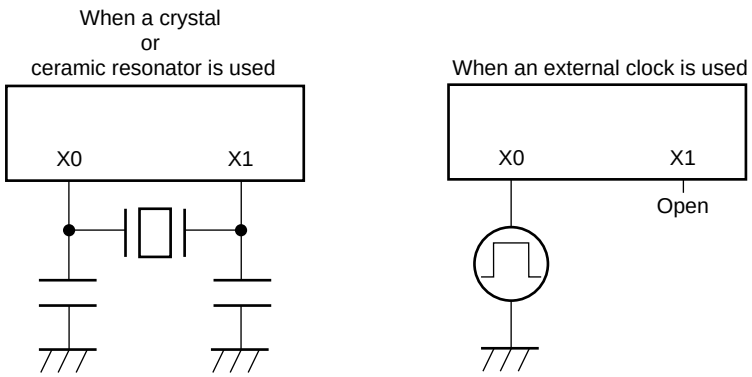
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

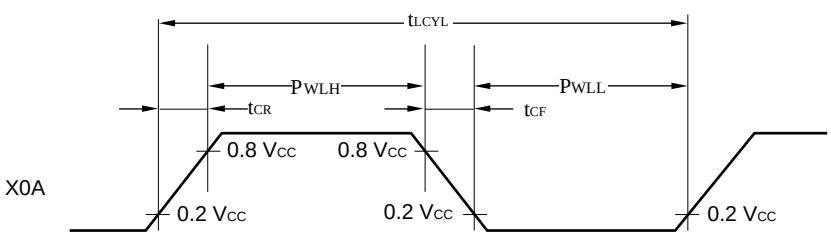
X0 and X1 Timing and Conditions



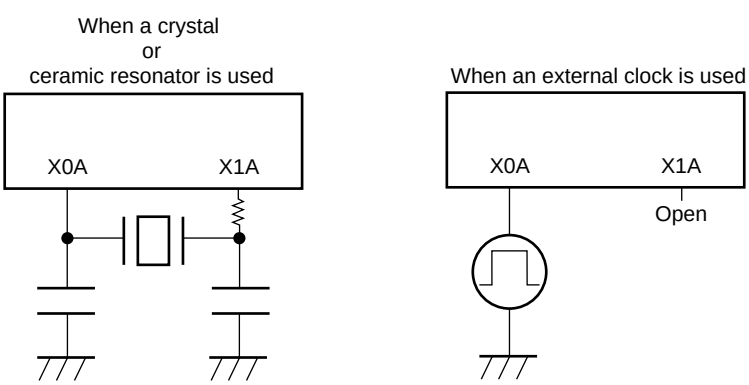
Main Clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 0.4 µs when operating at F_{CH} = 10 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

Note: When operating at 10 MHz, the cycle varies with the set execution time.

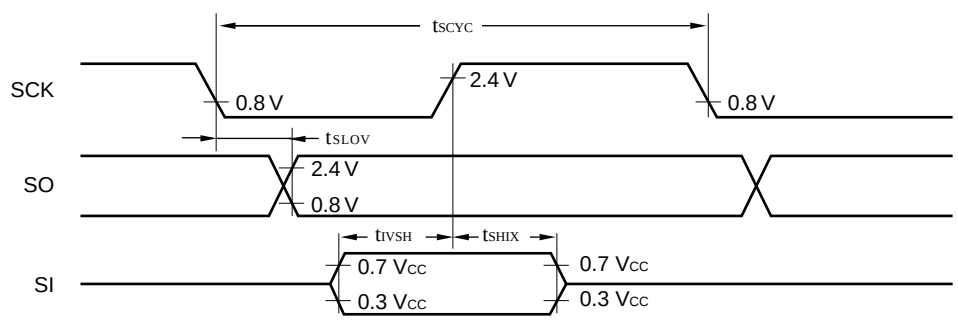
(5) Serial I/O Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

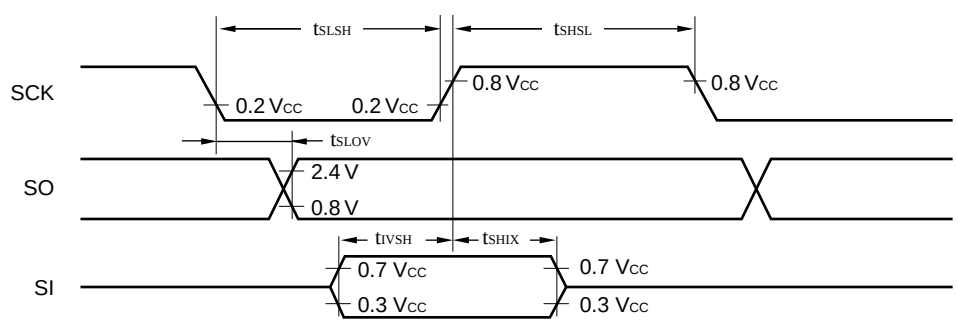
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

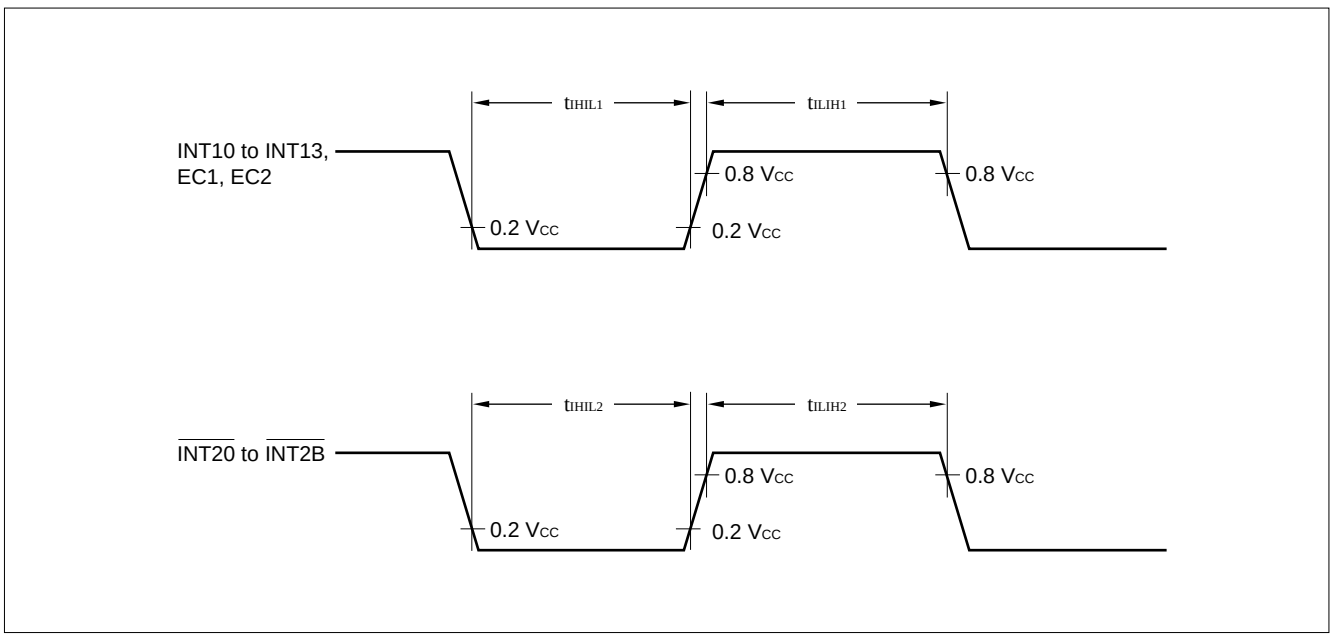


(6) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 to INT13, EC1, EC2	1 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		1 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	$\overline{INT20}$ to $\overline{INT2B}$	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

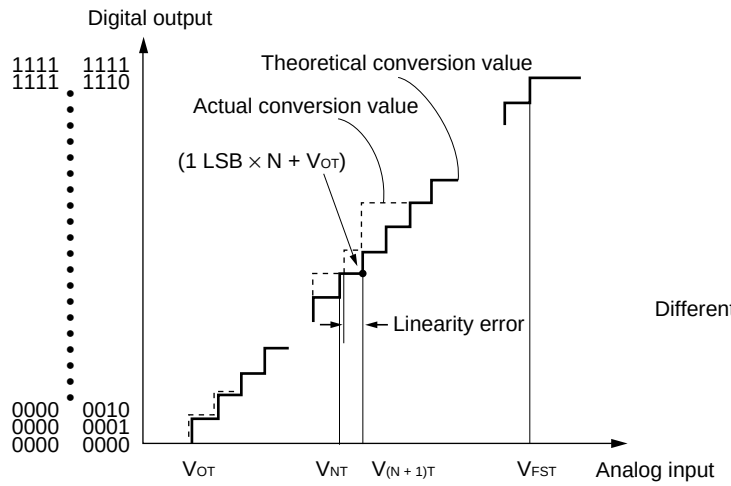
(AV_{CC} = V_{CC} = +3.5 V to +6.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVR = AV_{CC}	—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.0 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 3.0 LSB	AVR – 1.5 LSB	AVR	mV	
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time			—	—	44 t_{inst}*	—	µs	
Sense mode conversion time				—	12 t_{inst}*	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	—			0.0	—	AVR	V	
Reference voltage	—	AVR		0.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = 5.0V, when A/D conversion is activated	—	100	—	µA	
	I_{RH}		AVR = 5.0V, when A/D conversion is stopped	—	—	1	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

(1) A/D Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



$$1\ \text{LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 1\ \text{LSB})}{1\ \text{LSB}}$$

(2) Precautions

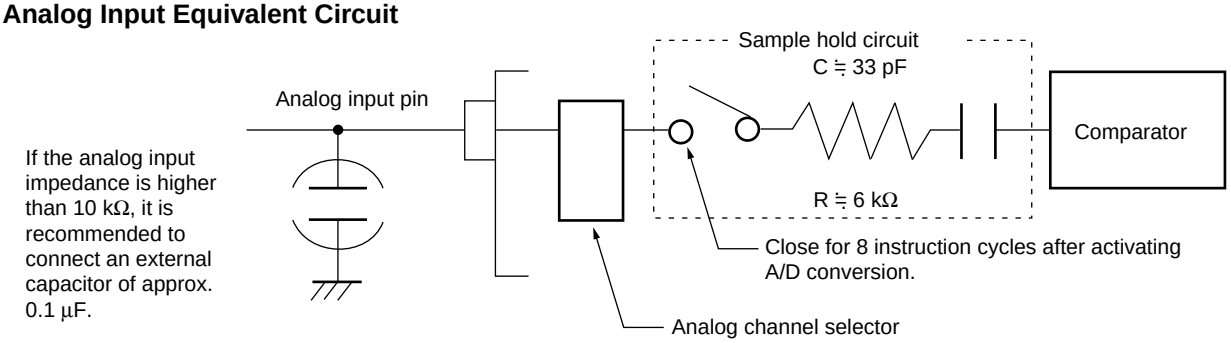
- **Input impedance of the analog input pins**

The A/D converter used for the MB89650AR series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

Analog Input Equivalent Circuit



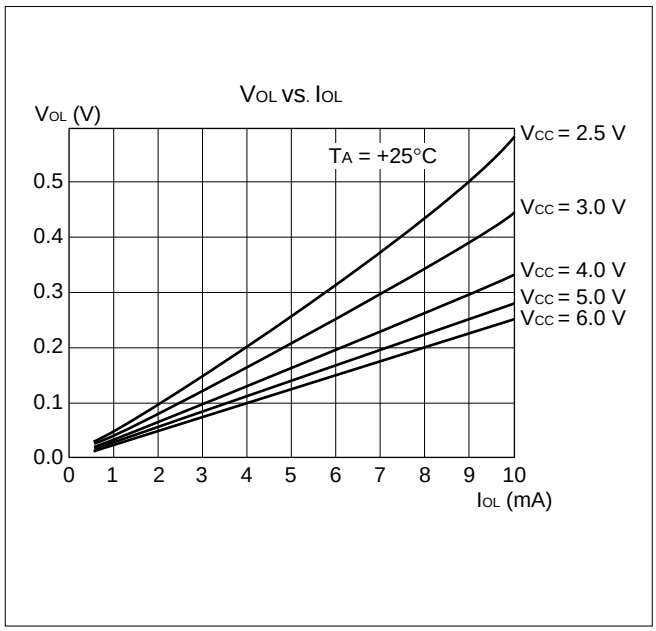
- **Error**

The smaller the | AVR – AVSS |, the greater the error would become relatively.

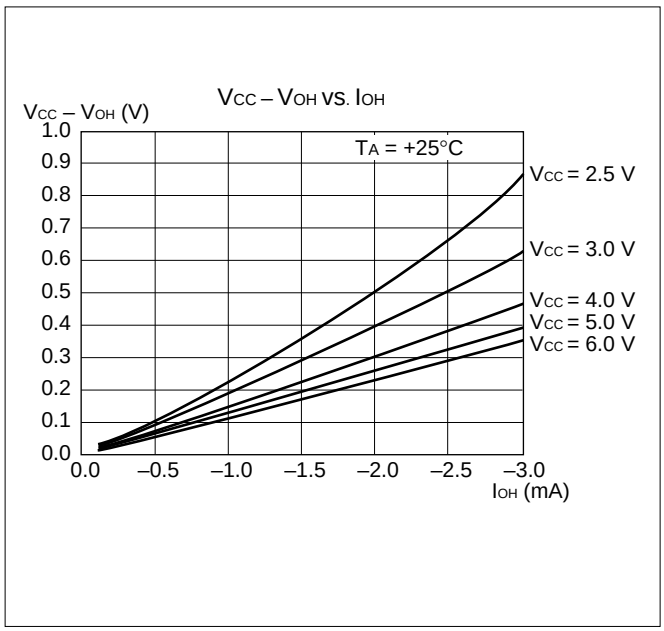
MB89650AR Series

■ EXAMPLE CHARACTERISTICS

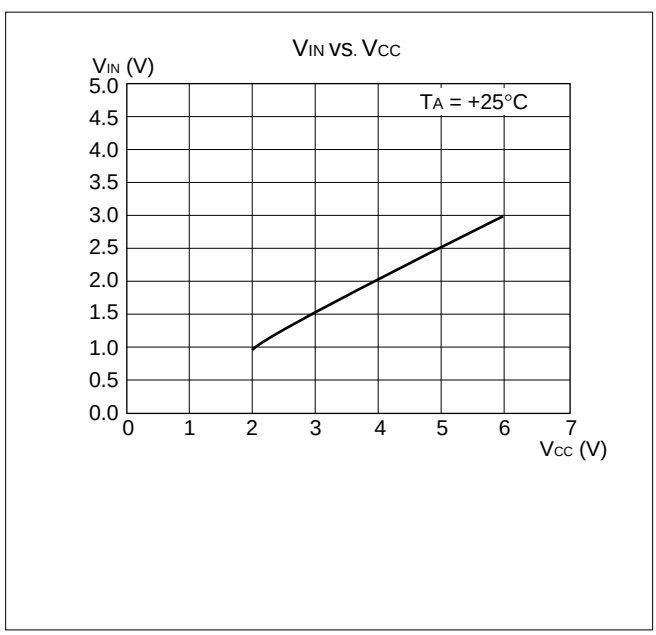
(1) “L” Level Output Voltage



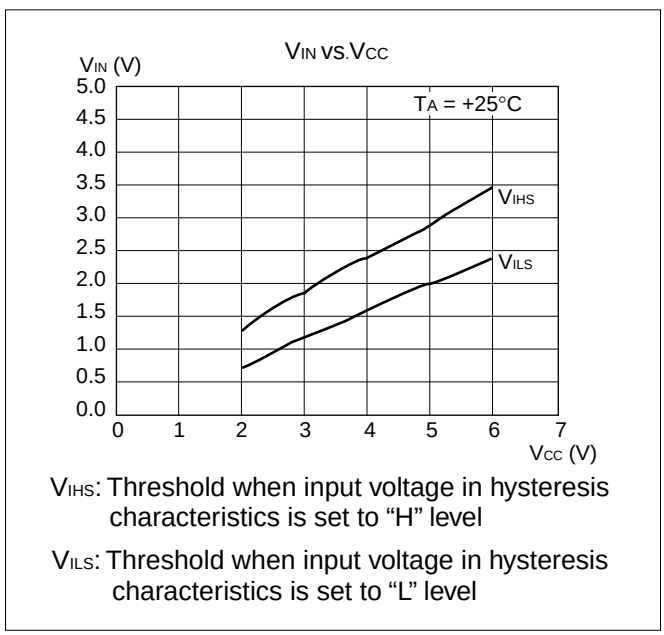
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

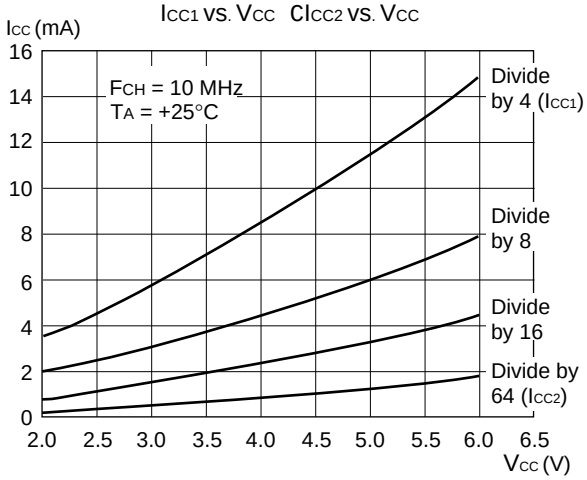


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

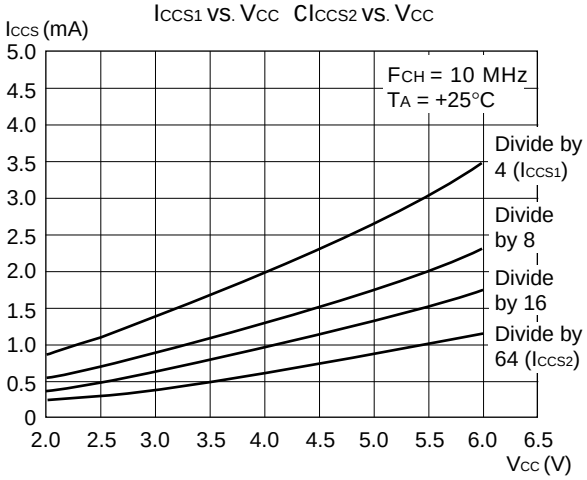
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)

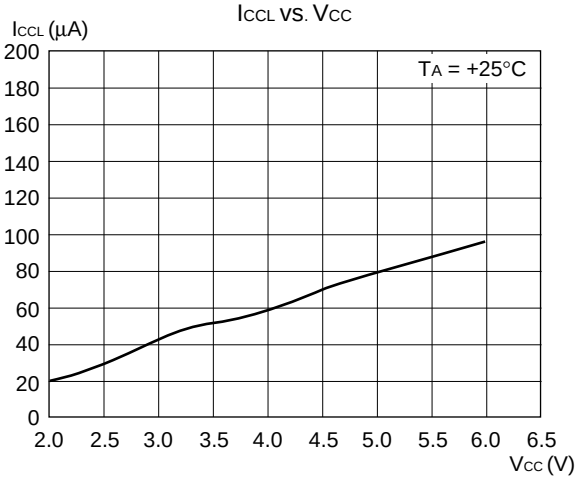
I_{CC1} vs. V_{CC} I_{CC2} vs. V_{CC}



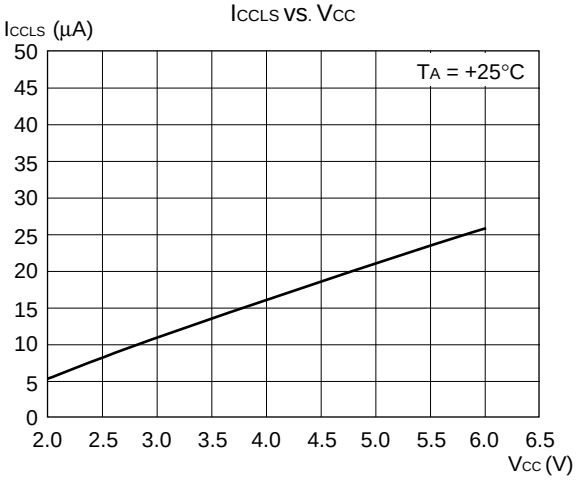
I_{CCS1} vs. V_{CC} I_{CCS2} vs. V_{CC}



I_{CCL} vs. V_{CC}



I_{CCLS} vs. V_{CC}



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MB89650AR Series

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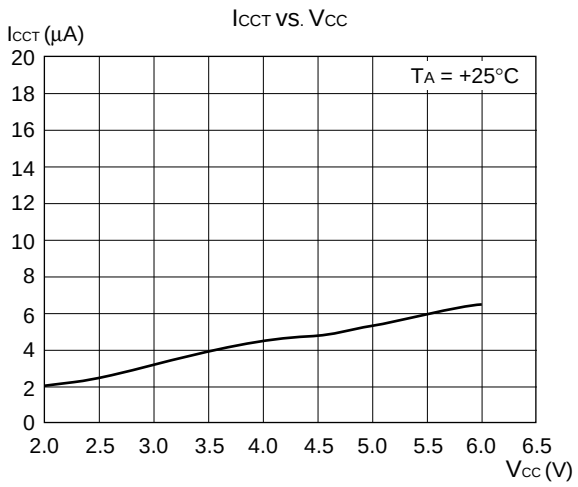
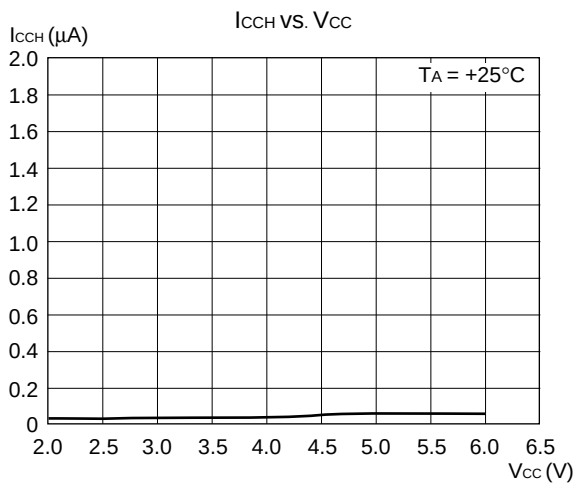
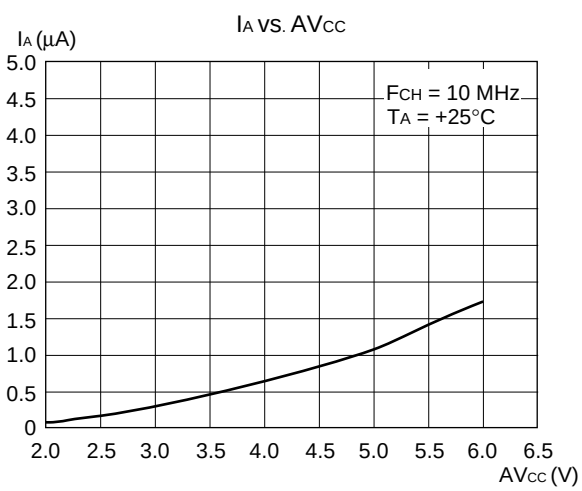
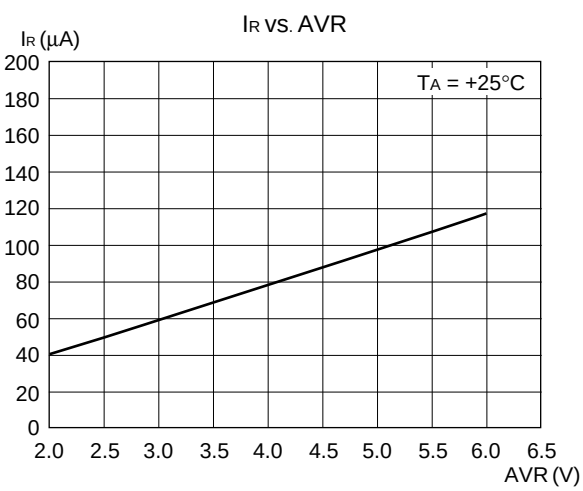
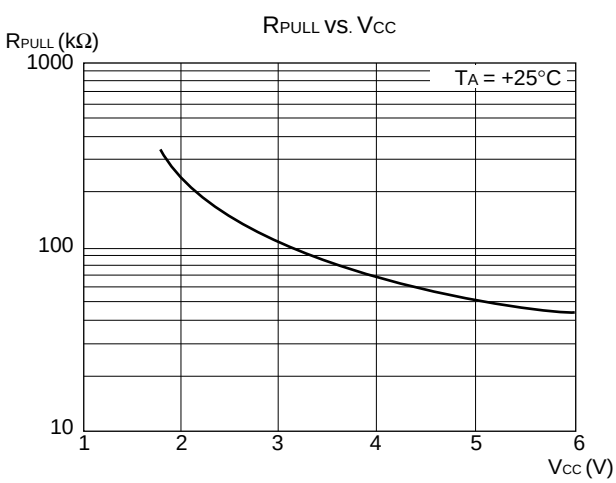








(6) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

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Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

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■ MASK OPTIONS

No.	Part number	MB89653AR MB89655AR MB89656AR MB89657AR	MB89P657A	MB89PV650A
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P20 to P22, P24 to P26, P30 to P37, P40 to P47, P60 to P67, P70 to P75, P80 to P81	Specify by pin	Can be set per pin. (Select in a group of four bits for P14 to P17, P40 to P43, and P40 to P47.) (P75 to P70 are available only for without a pull-up resistor.)	Fixed to without pull-up resistor
2	Power-on reset selection With power-on reset Without power-on reset	Selectable	With power-on reset	Fixed to with power-on reset
3	Selection of the oscillation stabilization time initial value Crystal oscillator: $2^{18}/F_{CH}$ (Approx. 26.2 ms*1) Ceramic oscillator: $2^{13}/F_{CH}$ (Approx. 26.2 ms*1)	Selectable	$2^{18}/F_{CH}$ (Approx. 26.2 ms*1)	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms*1)
4	Selection either single- or dual-clock system Single clock Dual clock	Selectable	Setting possible	Fixed to dual-clock system
5	Selection of a built-in booster*2 Without booster With booster (Segment output switching) 16 segments: Selection of P30 to P37 and P40 to P47 20 segments: Selection of P30 to P37 and P40 to P43 24 segments: Selection of P30 to P37 28 segments: Selection of P30 to P33 32 segments: No port selection	Selectable	Can be selected from the following six options: -101: Without booster -102: 16 segments -103: 20 segments -104: 24 segments -105: 28 segments -106: 32 segments	Fixed to without booster

*1: The value at F_{CH} = 10 MHz

*2: On microcontrollers with a built-in booster, only 1/3 bias can be used. The 1/2 duty cannot be used.

Note: Reset is input asynchronized with the internal clock whether with or without power-on reset.

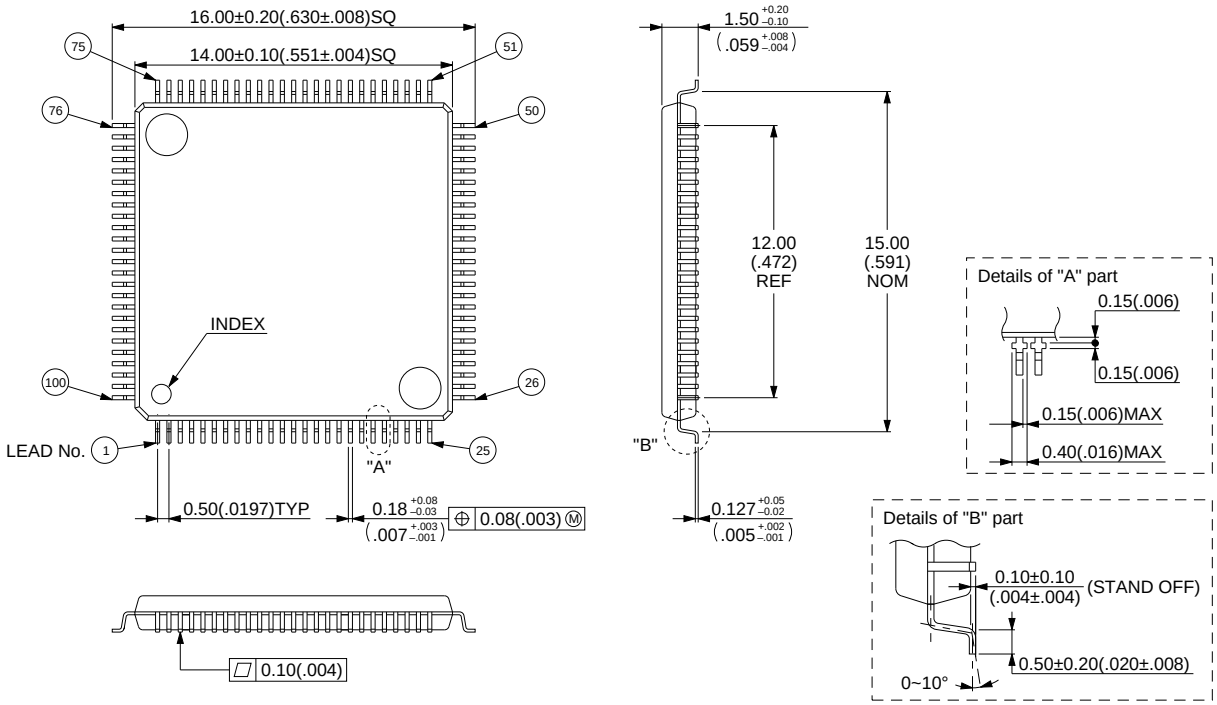
MB89650AR Series

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89653APFV MB89655APFV MB89656APFV MB89657APFV MB89P657APFV-101 MB89P657APFV-102 MB89P657APFV-103 MB89P657APFV-104 MB89P657APFV-105 MB89P657APFV-106	100-pin Plastic SQFP (FPT-100P-M05)	
MB89653APF MB89655APF MB89656APF MB89657APF MB89P657APF-101 MB89P657APF-102 MB89P657APF-103 MB89P657APF-104 MB89P657APF-105 MB89P657APF-106	100-pin Plastic QFP (FPT-100P-M06)	
MB89PV650ACF	100-pin Ceramic MQFP (MQP-100C-P02)	

■ PACKAGE DIMENSIONS

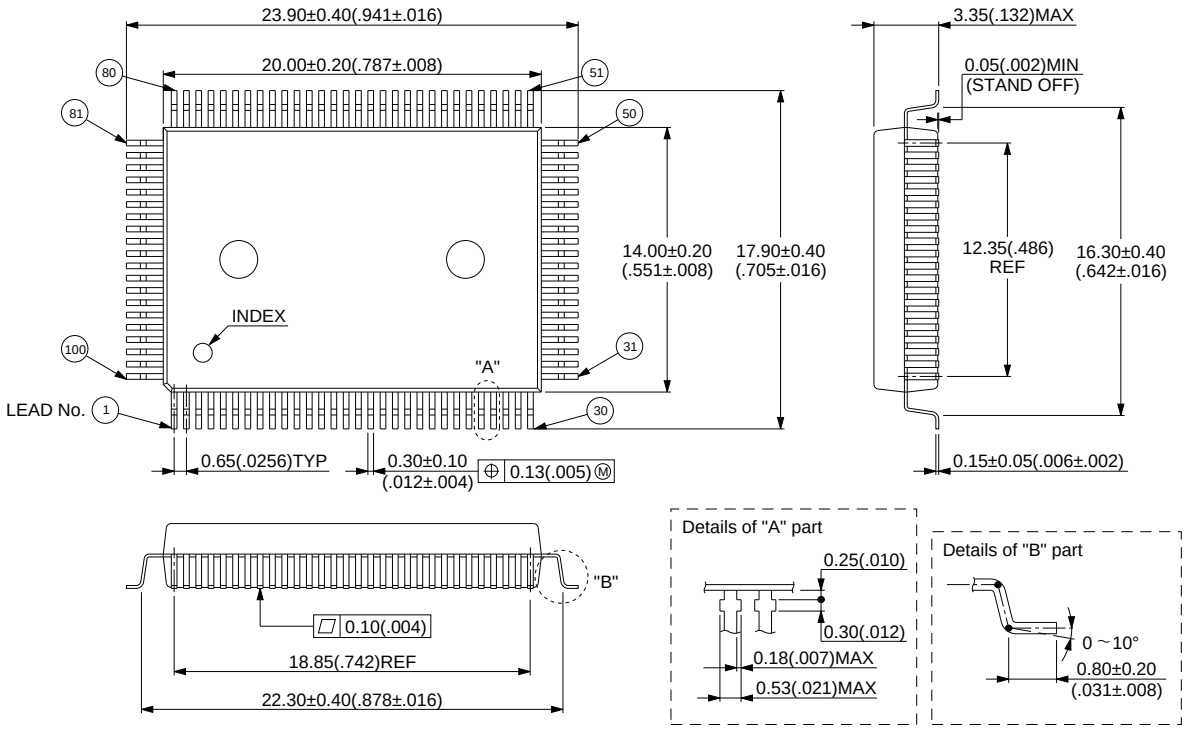
100-pin Plastic SQFP
(FPT-100P-M05)



Dimensions in mm (inches)

MB89650AR Series

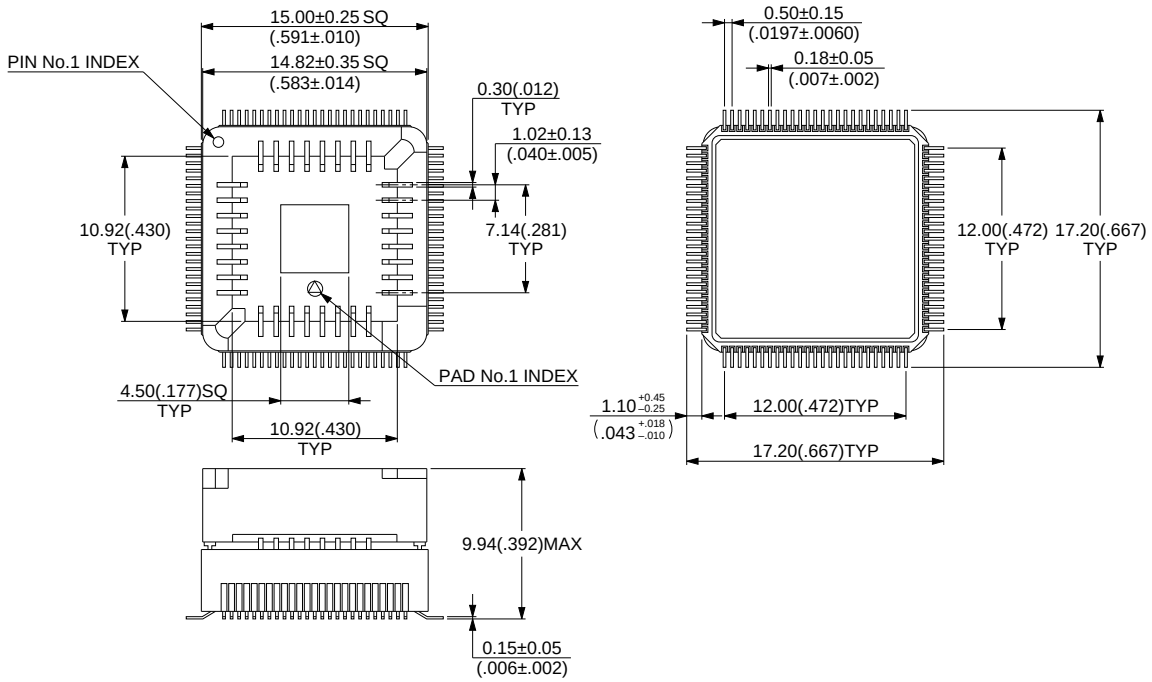
100-pin Plastic QFP
(FPT-100P-M06)



Dimensions in mm (inches)

MB89650AR Series

100-pin Ceramic MQFP
(MQP-100C-P02)



Dimensions in mm (inches)

MB89650AR Series

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