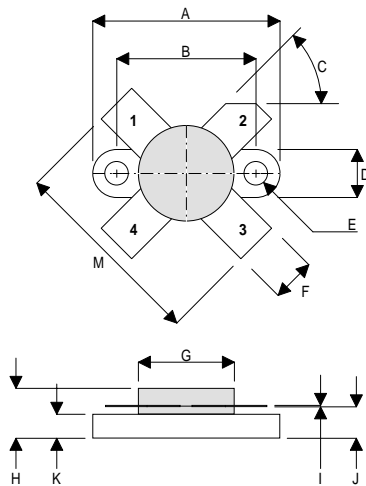


MECHANICAL DATA



DM

PIN 1 SOURCE                      PIN 2 DRAIN  
 PIN 3 SOURCE                      PIN 4 GATE

DIM	mm	Tol.	Inches	Tol.
A	24.76	0.13	0.975	0.005
B	18.42	0.13	0.725	0.005
C	45°	5°	45°	5°
D	6.35	0.13	0.25	0.005
E	3.17 Dia.	0.13	0.125 Dia.	0.005
F	5.71	0.13	0.225	0.005
G	12.7 Dia.	0.13	0.500 Dia.	0.005
H	6.60	REF	0.260	REF
I	0.13	0.02	0.005	0.001
J	4.32	0.13	0.170	0.005
K	3.17	0.13	0.125	0.005
M	26.16	0.25	1.03	0.010

**GOLD METALLISED  
 MULTI-PURPOSE SILICON  
 DMOS RF FET  
 80W – 28V – 175MHz  
 SINGLE ENDED**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW  $C_{rss}$
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 16 dB MINIMUM

APPLICATIONS

- HF/VHF COMMUNICATIONS  
 from 1 MHz to 175 MHz

ABSOLUTE MAXIMUM RATINGS ( $T_{case} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	146W
$BV_{DSS}$	Drain – Source Breakdown Voltage	70V
$BV_{GSS}$	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	20A
$T_{stg}$	Storage Temperature	$-65$ to $150^{\circ}C$
$T_j$	Maximum Operating Junction Temperature	$200^{\circ}C$

## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
B <sub>V</sub> DSS Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0      I <sub>D</sub> = 100mA	70			V
I <sub>D</sub> DSS Zero Gate Voltage Drain Current	V <sub>DS</sub> = 28V      V <sub>GS</sub> = 0			2	mA
I <sub>G</sub> DSS Gate Leakage Current	V <sub>GS</sub> = 20V      V <sub>DS</sub> = 0			1	μA
V <sub>GS(th)</sub> Gate Threshold Voltage *	I <sub>D</sub> = 10mA      V <sub>DS</sub> = V <sub>GS</sub>	1		7	V
g <sub>fs</sub> Forward Transconductance *	V <sub>DS</sub> = 10V      I <sub>D</sub> = 4A	3.2			S
G <sub>PS</sub> Common Source Power Gain	P <sub>O</sub> = 80W	16			dB
η Drain Efficiency	V <sub>DS</sub> = 28V      I <sub>DQ</sub> = 0.4A	50			%
VSWR Load Mismatch Tolerance	f = 175MHz	20:1			—
C <sub>i</sub> SS Input Capacitance	V <sub>DS</sub> = 0      V <sub>GS</sub> = -5V      f = 1MHz			240	pF
C <sub>o</sub> SS Output Capacitance	V <sub>DS</sub> = 28V      V <sub>GS</sub> = 0      f = 1MHz			100	pF
C <sub>r</sub> SS Reverse Transfer Capacitance	V <sub>DS</sub> = 28V      V <sub>GS</sub> = 0      f = 1MHz			10	pF

\* Pulse Test:    Pulse Duration = 300 μs , Duty Cycle ≤ 2%

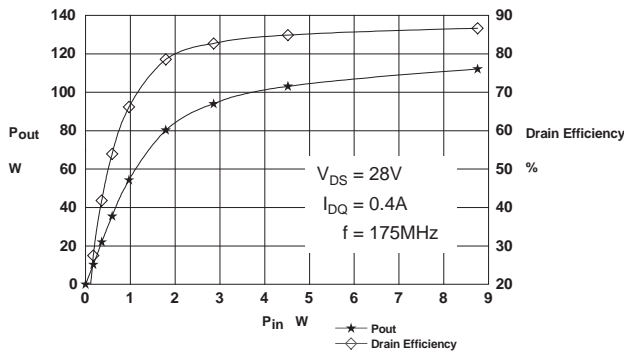
## HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

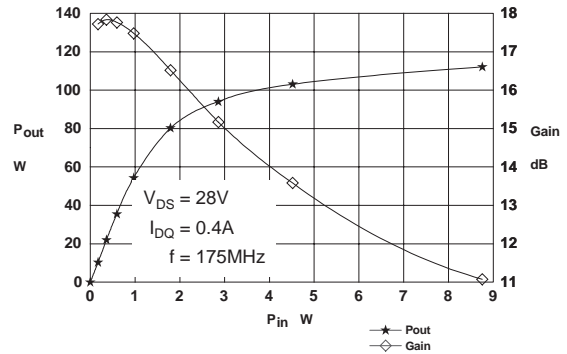
**THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.**

## THERMAL DATA

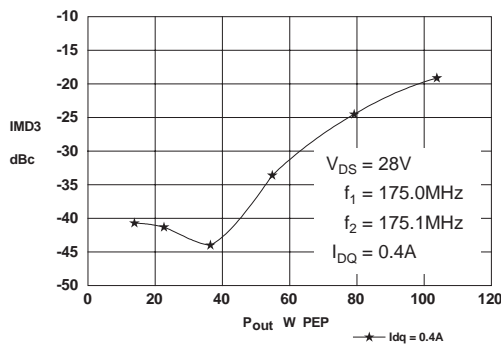
R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 1.2°C / W
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**Figure 1 – Power Output and Efficiency vs. Power Input.**



**Figure 2 – Power Output & Gain vs. Power Input.**



**Figure 3 – IMD vs. Output Power.**

## D1005UK OPTIMUM SOURCE AND LOAD IMPEDANCE

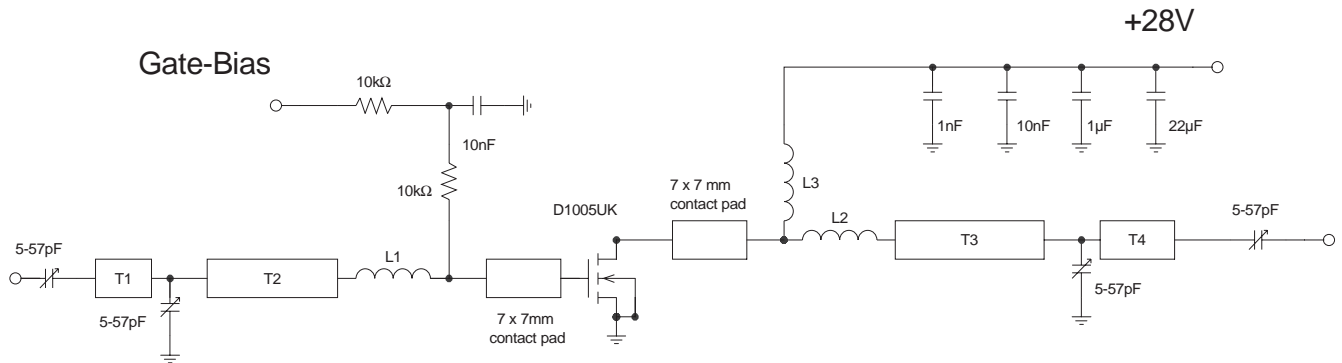
Frequency MHz	Z <sub>S</sub> Ω	Z <sub>L</sub> Ω
175MHz	3 + j1	3 - j2.5

### Typical S Parameters

! V<sub>DS</sub> = 28V, I<sub>DQ</sub> = 0.3A

# MHz S M A R 50

!Freq MHz	S11 mag ang	S21 mag ang	S12 mag ang	S22 mag ang
50	0.95 -58	4.29 94	0.006 34	0.66 -162
100	0.94 -79	3.32 81	0.006 57	0.75 -164
150	0.94 -104	2.26 65	0.01 98	0.84 -169
200	0.93 -124	1.59 53	0.019 107	0.88 -175
250	0.94 -140	1.2 41	0.031 103	0.92 -180
300	0.95 -152	0.94 34	0.042 102	0.93 176
350	0.96 -161	0.72 22	0.052 92	0.96 170
400	0.96 -169	0.59 19	0.064 91	0.98 164
450	0.97 -177	0.46 11	0.073 84	1.00 159
500	0.98 177	0.35 -2	0.091 82	1.00 154



## D1005UK 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/ glass,  $\epsilon_r = 2.5$   
All microstrip lines  $W = 4.4\text{mm}$

T1	8mm	L1	Hairpin loop 16swg 15.5mm dia
T2	22mm	L2	Hairpin loop 16swg 10mm dia
T3	18mm	L3	11 turns 18swg enamelled copper wire, 10mm i.d.
T4	4.5mm		