



Ultra37000 CPLD Family

5V, 3.3V, ISR™ High-Performance CPLDs

Features

- **In-System Reprogrammable™ (ISR™) CMOS CPLDs**
 - JTAG interface for reconfigurability
 - Design changes do not cause pinout changes
 - Design changes do not cause timing changes
- **High density**
 - 32 to 512 macrocells
 - 32 to 264 I/O pins
 - Five dedicated inputs including four clock pins
- **Simple timing model**
 - No fanout delays
 - No expander delays
 - No dedicated vs. I/O pin delays
 - No additional delay through PIM
 - No penalty for using full 16 product terms
 - No delay for steering or sharing product terms
- **3.3V and 5V versions**
- **PCI-compatible^[1]**
- **Programmable bus-hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
 - 0 to 16 product terms to any macrocell
 - Product term steering on an individual basis
 - Product term sharing among local macrocells
- **Flexible clocking**
 - Four synchronous clocks per device
 - Product term clocking
 - Clock polarity control per logic block
- **Consistent package/pinout offering across all densities**
 - Simplifies design migration
 - Same pinout for 3.3V and 5.0V devices
- **Packages**
 - 44 to 400 leads in PLCC, CLCC, PQFP, TQFP, CQFP, BGA, and Fine-Pitch BGA packages
 - Lead(Pb)-free packages available

Note:

1. Due to the 5V-tolerant nature of 3.3V device I/Os, the I/Os are not clamped to V_{CC} . PCI $V_{IH} = 2V$.

General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Ultra37000 family features user programmable bus-hold capabilities on all I/Os.

Ultra37000 5.0V Devices

The Ultra37000 devices operate with a 5V supply and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. These devices require 5V ISR programming.

Ultra37000V 3.3V Devices

Devices operating with a 3.3V supply require 3.3V on all V_{CCO} pins, reducing the device's power consumption. These devices support 3.3V JEDEC standard CMOS output levels, and are 5V-tolerant. These devices allow 3.3V ISR programming.

Selection Guide
5.0V Selection Guide
General Information

| Device | Macrocells | Dedicated Inputs | I/O Pins | Speed (t _{PD}) | Speed (f _{MAX}) |
|---------|------------|------------------|-------------|--------------------------|---------------------------|
| CY37032 | 32 | 5 | 32 | 6 | 200 |
| CY37064 | 64 | 5 | 32/64 | 6 | 200 |
| CY37128 | 128 | 5 | 64/128 | 6.5 | 167 |
| CY37192 | 192 | 5 | 120 | 7.5 | 154 |
| CY37256 | 256 | 5 | 128/160/192 | 7.5 | 154 |
| CY37384 | 384 | 5 | 160/192 | 10 | 118 |
| CY37512 | 512 | 5 | 160/192/264 | 10 | 118 |

Speed Bins

| Device | 200 | 167 | 154 | 143 | 125 | 100 | 83 | 66 |
|---------|-----|-----|-----|-----|-----|-----|----|----|
| CY37032 | X | | X | | X | | | |
| CY37064 | X | | X | | X | | | |
| CY37128 | | X | | | X | X | | |
| CY37192 | | | X | | X | | X | |
| CY37256 | | | X | | X | | X | |
| CY37384 | | | | | X | | X | |
| CY37512 | | | | | X | X | X | |

Device-Package Offering and I/O Count

| Device | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 160-Lead CQFP | 208-Lead PQFP | 208-Lead CQFP | 256-Lead BGA | 352-Lead BGA |
|---------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| CY37032 | 37 | 37 | | | | | | | | | | |
| CY37064 | 37 | 37 | 37 | 69 | | 69 | | | | | | |
| CY37128 | | | | 69 | 69 | 69 | 133 | | | | | |
| CY37192 | | | | | | | 125 | | | | | |
| CY37256 | | | | | | | 133 | 133 | 165 | | 197 | |
| CY37384 | | | | | | | | | 165 | | 197 | |
| CY37512 | | | | | | | | | 165 | 165 | 197 | 269 |

3.3V Selection Guide
General Information

| Device | Macrocells | Dedicated Inputs | I/O Pins | Speed (t _{PD}) | Speed (f _{MAX}) |
|----------|------------|------------------|-------------|--------------------------|---------------------------|
| CY37032V | 32 | 5 | 32 | 8.5 | 143 |
| CY37064V | 64 | 5 | 32/64 | 8.5 | 143 |
| CY37128V | 128 | 5 | 64/80/128 | 10 | 125 |
| CY37192V | 192 | 5 | 120 | 12 | 100 |
| CY37256V | 256 | 5 | 128/160/192 | 12 | 100 |
| CY37384V | 384 | 5 | 160/192 | 15 | 83 |
| CY37512V | 512 | 5 | 160/192/264 | 15 | 83 |



Speed Bins

| Device | 200 | 167 | 154 | 143 | 125 | 100 | 83 | 66 |
|----------|-----|-----|-----|-----|-----|-----|----|----|
| CY37032V | | | | X | | X | | |
| CY37064V | | | | X | | X | | |
| CY37128V | | | | | X | | X | |
| CY37192V | | | | | | X | | X |
| CY37256V | | | | | | X | | X |
| CY37384V | | | | | | | X | X |
| CY37512V | | | | | | | X | X |

Device-Package Offering and I/O Count

| Device | 44-Lead TQFP | 44-Lead CLCC | 48-Lead FBGA | 84-Lead CLCC | 100-Lead TQFP | 100-Lead FBGA | 160-Lead TQFP | 160-Lead CQFP | 208-Lead PQFP | 208-Lead CQFP | 256-Lead BGA | 256-Lead FBGA | 352-Lead BGA | 400-Lead FBGA |
|----------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|---------------|--------------|---------------|
| CY37032V | 37 | | 37 | | | | | | | | | | | |
| CY37064V | 37 | 37 | 37 | | 69 | 69 | | | | | | | | |
| CY37128V | | | | 69 | 69 | 85 | 133 | | | | | | | |
| CY37192V | | | | | | | 125 | | | | | | | |
| CY37256V | | | | | | | 133 | 133 | 165 | | 197 | 197 | | |
| CY37384V | | | | | | | | | 165 | | 197 | | | |
| CY37512V | | | | | | | | | 165 | 165 | 197 | | 269 | 269 |

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*[®] and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

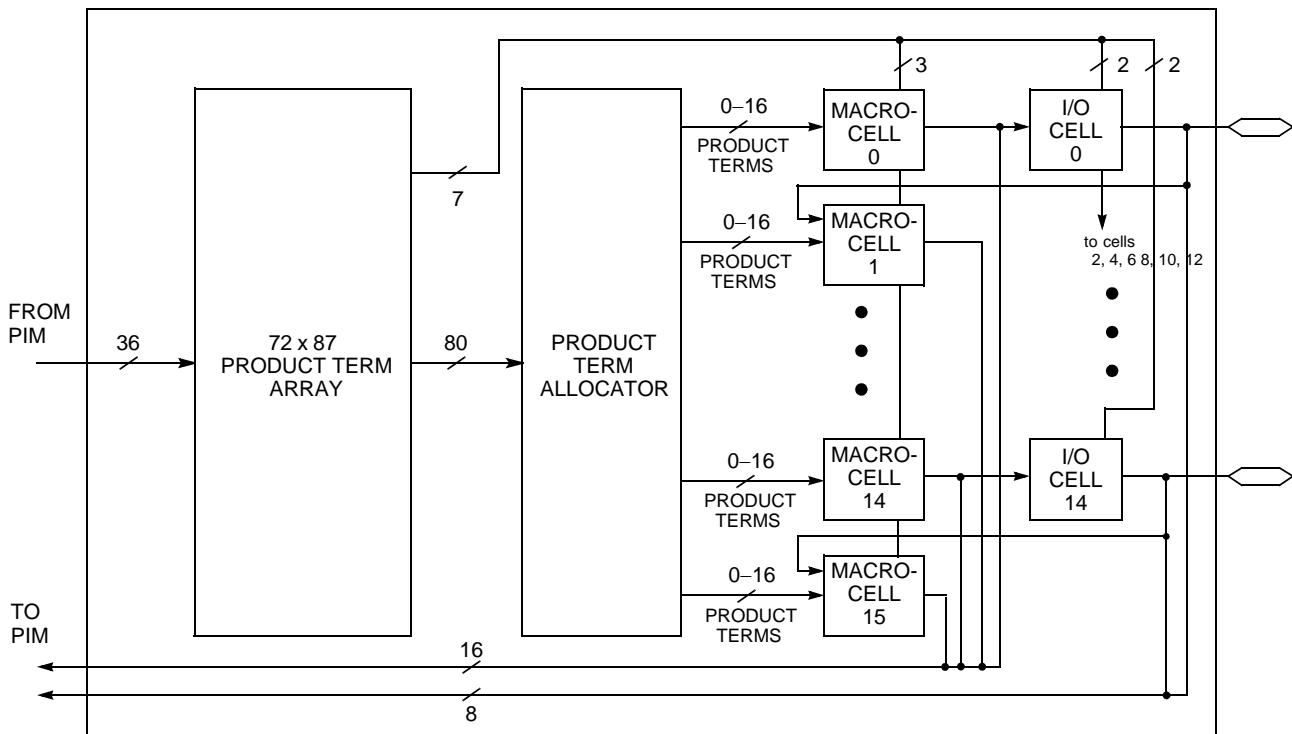


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block basis by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a

variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

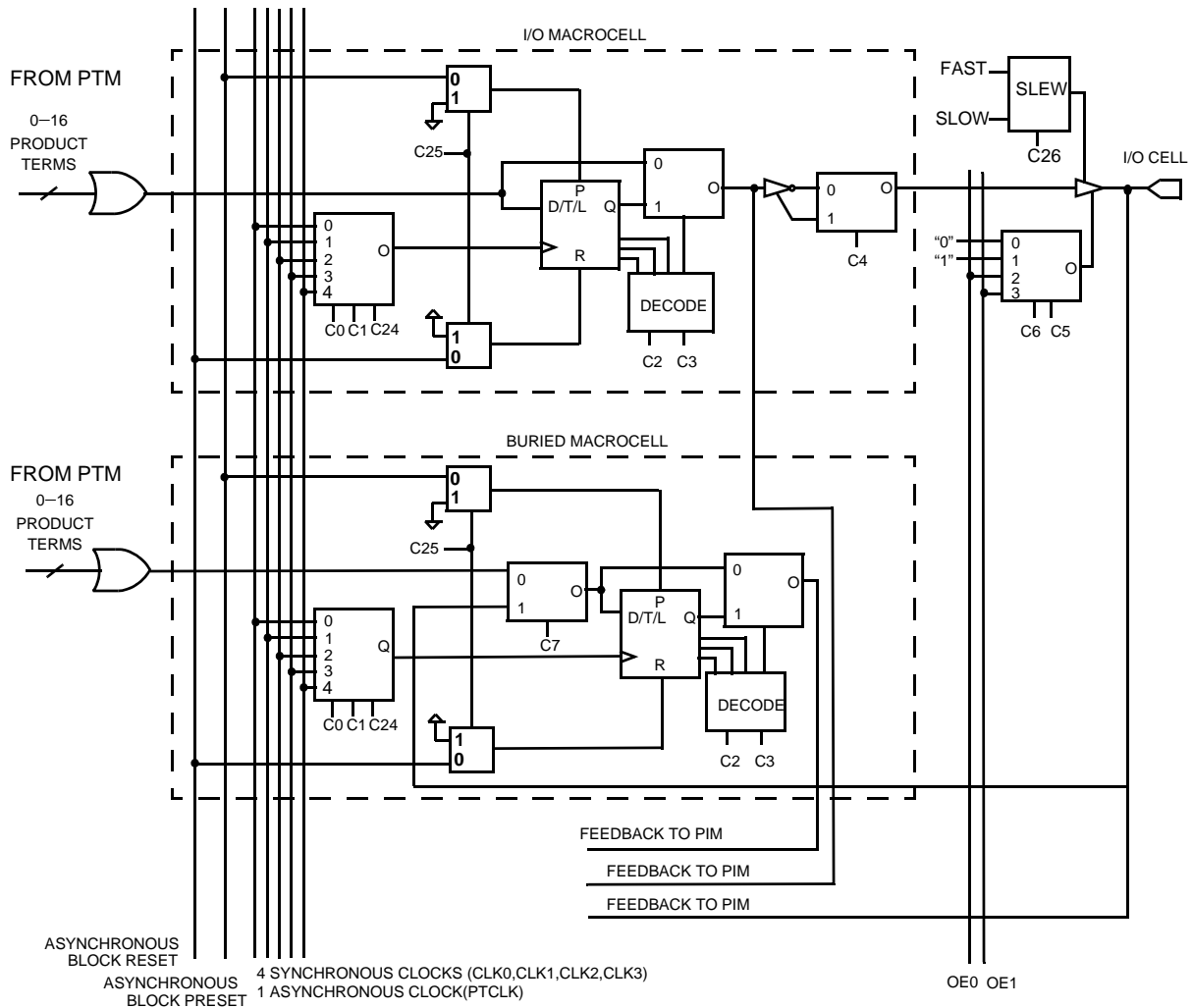


Figure 2. I/O and Buried Macrocells

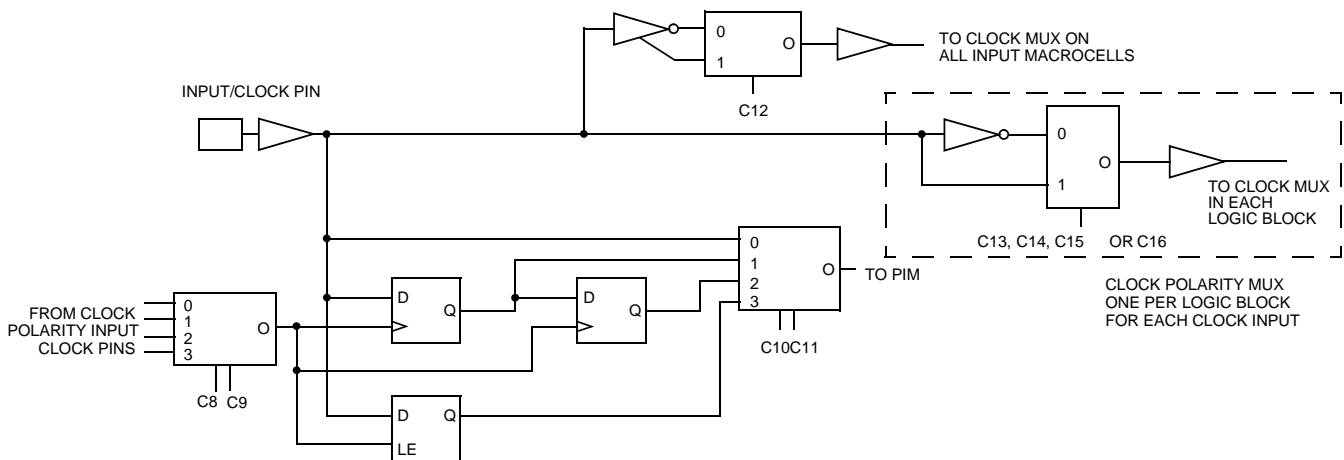


Figure 4. Input/Clock Macrocell

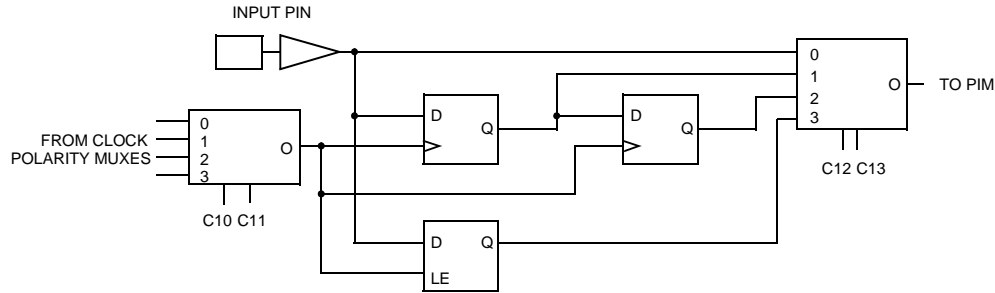


Figure 3. Input Macrocell

Clockin g

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

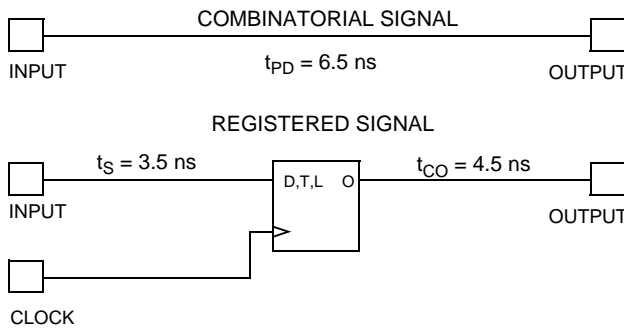


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in Figure 6.

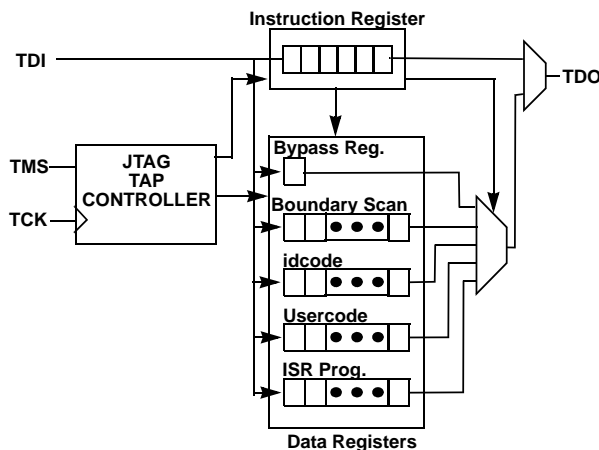


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing

resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp Professional* and *Warp Enterprise* data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.



Ultra37000 CPLD Family

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

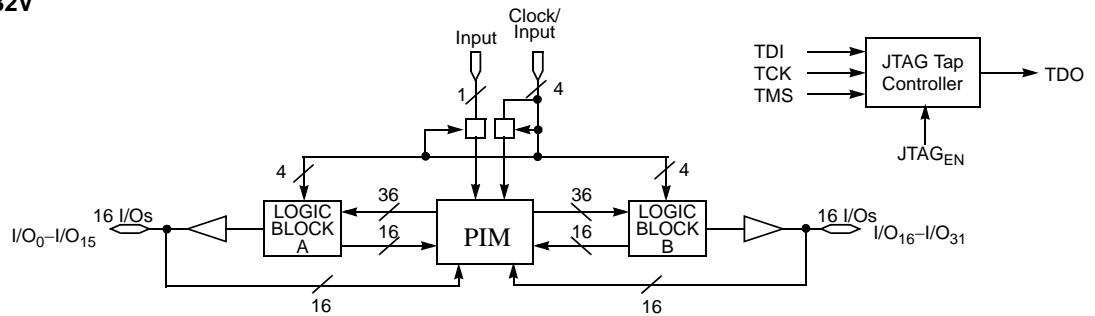
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

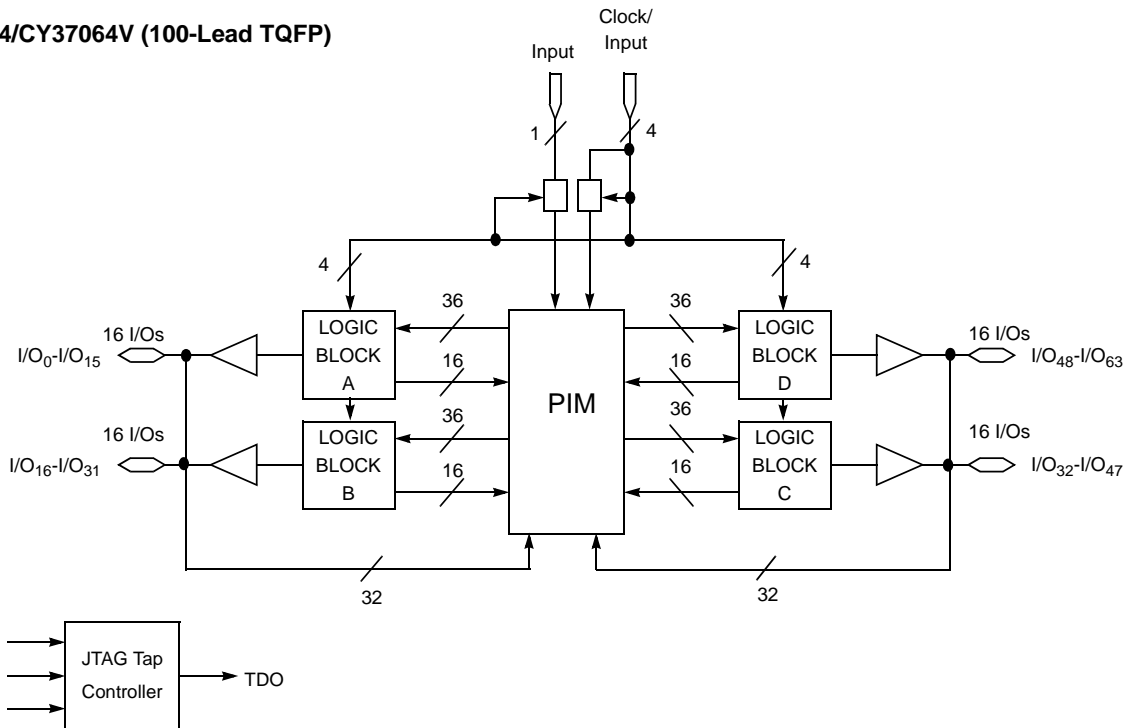
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

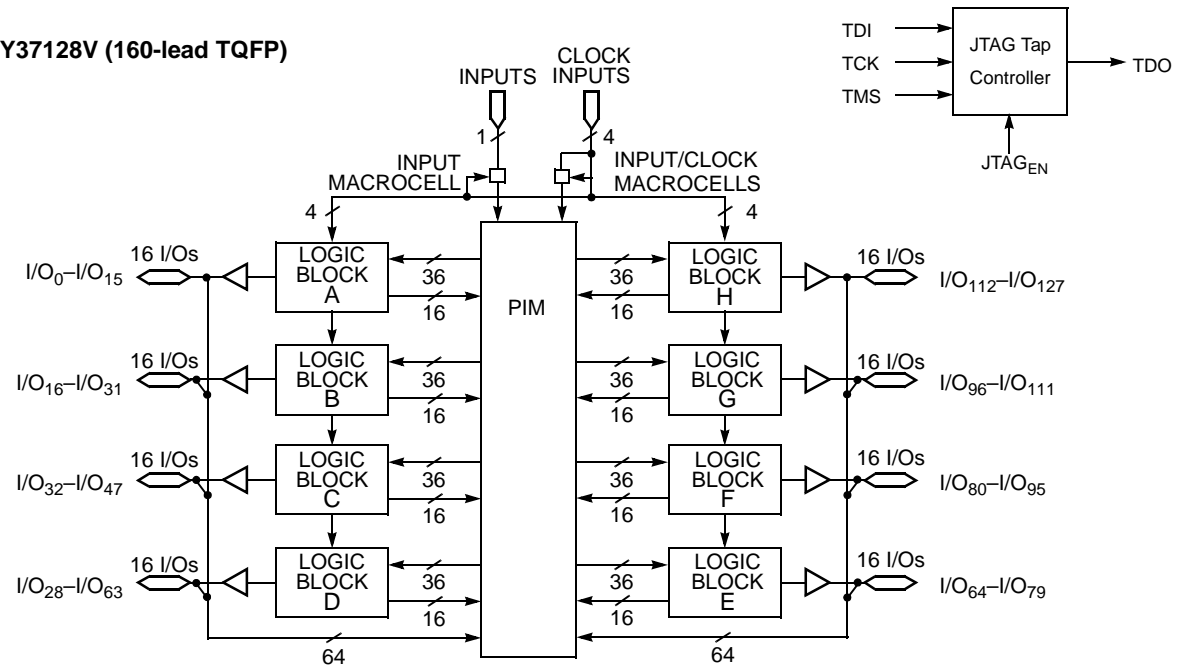
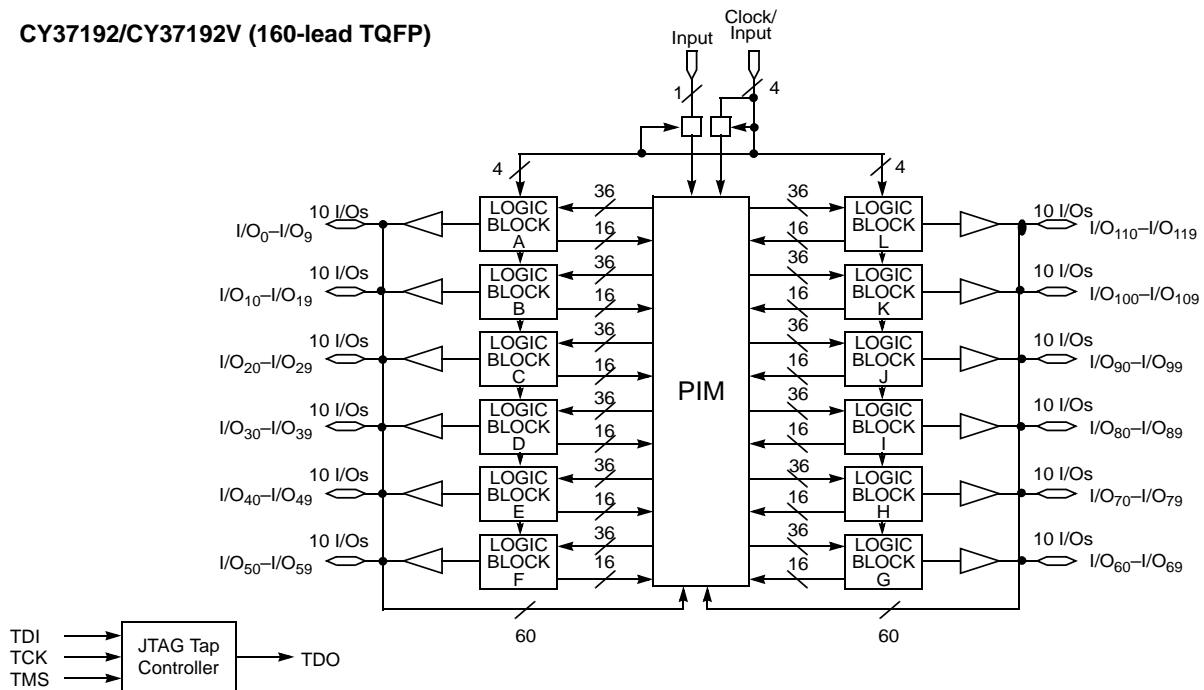
Logic Block Diagrams

CY37032/CY37032V



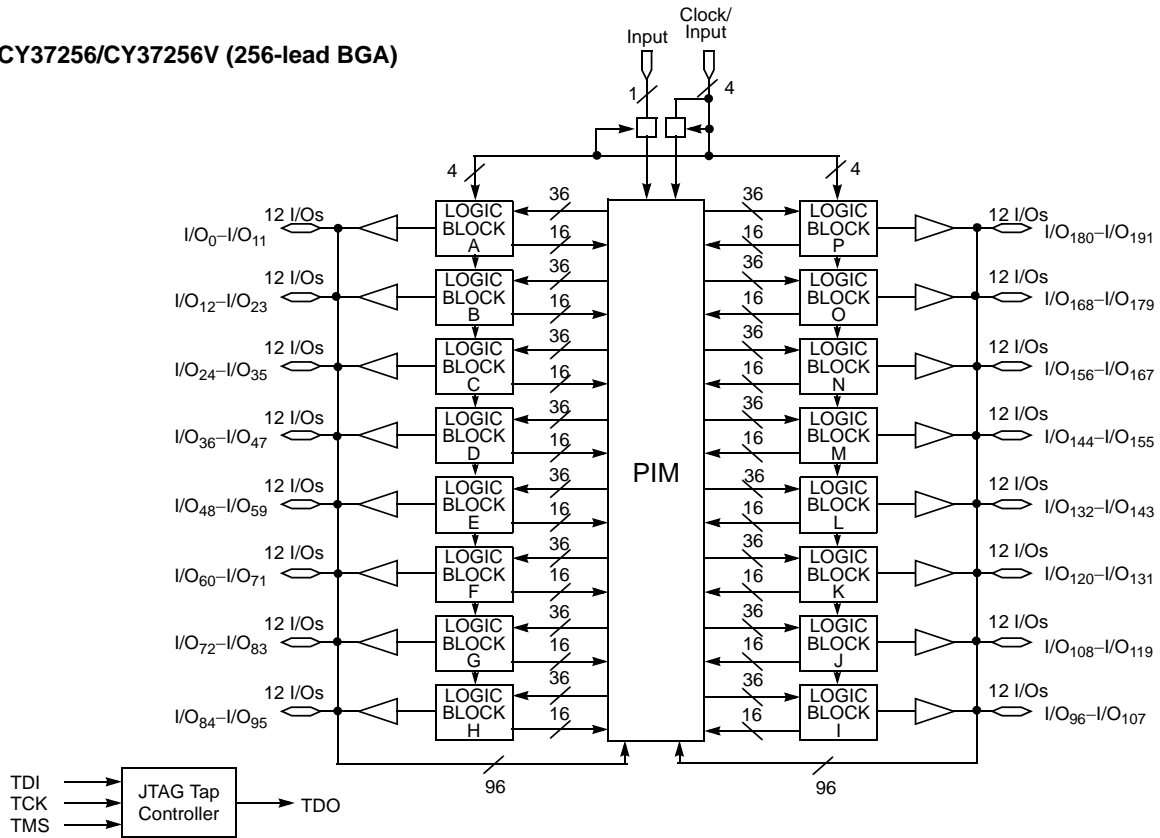
CY37064/CY37064V (100-Lead TQFP)



Logic Block Diagrams (continued)
CY37128/CY37128V (160-lead TQFP)

CY37192/CY37192V (160-lead TQFP)


Logic Block Diagrams (continued)

CY37256/CY37256V (256-lead BGA)



5.0V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State..... -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

DC Program Voltage..... 4.5 to 5.5V

Current into Outputs 16 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range^[2]

| Range | Ambient Temperature ^[2] | Junction Temperature | Output Condition | V _{CC} | V _{CCO} |
|-------------------------|------------------------------------|----------------------|------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 0°C to +90°C | 5V | 5V ± 0.25V | 5V ± 0.25V |
| | | | 3.3V | 5V ± 0.25V | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | -40°C to +105°C | 5V | 5V ± 0.5V | 5V ± 0.5V |
| | | | 3.3V | 5V ± 0.5V | 3.3V ± 0.3V |
| Military ^[3] | -55°C to +125°C | -55°C to +130°C | 5V | 5V ± 0.5V | 5V ± 0.5V |
| | | | 3.3V | 5V ± 0.5V | 3.3V ± 0.3V |

5.0V Device Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|--|--|------|--------------------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min. | I _{OH} = -3.2 mA (Com'I/Ind) ^[4] | 2.4 | | V |
| | | | I _{OH} = -2.0 mA (Mil) ^[4] | 2.4 | | V |
| V _{OHZ} | Output HIGH Voltage with Output Disabled ^[5] | V _{CC} = Max. | I _{OH} = 0 μA (Com'I) ^[6] | | 4.2 | V |
| | | | I _{OH} = 0 μA (Ind/Mil) ^[6] | | 4.5 | V |
| | | | I _{OH} = -100 μA (Com'I) ^[6] | | 3.6 | V |
| | | | I _{OH} = -150 μA (Ind/Mil) ^[6] | | 3.6 | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min. | I _{OL} = 16 mA (Com'I/Ind) ^[4] | | 0.5 | V |
| | | | I _{OL} = 12 mA (Mil) ^[4] | | 0.5 | V |
| V _{IH} | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs ^[7] | 2.0 | | V _{CCmax} | V |
| V _{IL} | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs ^[7] | -0.5 | | 0.8 | V |
| I _{IX} | Input Load Current | V _I = GND OR V _{CC} , Bus-Hold Disabled | -10 | | 10 | μA |
| I _{OZ} | Output Leakage Current | V _O = GND or V _{CC} , Output Disabled, Bus-Hold Disabled | -50 | | 50 | μA |
| I _{OS} | Output Short Circuit Current ^[8, 5] | V _{CC} = Max., V _{OUT} = 0.5V | -30 | | -160 | mA |
| I _{BHL} | Input Bus-Hold LOW Sustaining Current | V _{CC} = Min., V _{IL} = 0.8V | +75 | | | μA |
| I _{BHH} | Input Bus-Hold HIGH Sustaining Current | V _{CC} = Min., V _{IH} = 2.0V | -75 | | | μA |
| I _{BHLO} | Input Bus-Hold LOW Overdrive Current | V _{CC} = Max. | | | +500 | μA |
| I _{BHHO} | Input Bus-Hold HIGH Overdrive Current | V _{CC} = Max. | | | -500 | μA |

Notes:

- Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
- T_A is the "Instant On" case temperature.
- I_{OH} = -2 mA, I_{OL} = 2 mA for TDO.
- Tested initially and after any design or process changes that may affect these parameters.
- When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Inductance^[5]

| Parameter | Description | Test Conditions | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 208-Lead PQFP | Unit |
|-----------|------------------------|-------------------------------------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|------|
| L | Maximum Pin Inductance | V _{IN} = 5.0V at f = 1 MHz | 2 | 5 | 2 | 8 | 5 | 8 | 9 | 11 | nH |

Capacitance^[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|-----------------------------------|--|------|------|
| C _{I/O} | Input/Output Capacitance | V _{IN} = 5.0V at f = 1 MHz at T _A = 25°C | 10 | pF |
| C _{CLK} | Clock Signal Capacitance | V _{IN} = 5.0V at f = 1 MHz at T _A = 25°C | 12 | pF |
| C _{DP} | Dual-Function Pins ^[9] | V _{IN} = 5.0V at f = 1 MHz at T _A = 25°C | 16 | pF |

Endurance Characteristics^[5]

| Parameter | Description | Test Conditions | Min. | Typ. | Unit |
|-----------|------------------------------|--|-------|--------|--------|
| N | Minimum Reprogramming Cycles | Normal Programming Conditions ^[2] | 1,000 | 10,000 | Cycles |

3.3V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied | -55°C to +125°C |
| Supply Voltage to Ground Potential | -0.5V to +4.6V |

| | |
|---|--|
| DC Voltage Applied to Outputs in High-Z State | -0.5V to +7.0V |
| DC Input Voltage | -0.5V to +7.0V |
| DC Program Voltage | 3.0 to 3.6V |
| Current into Outputs | 8 mA |
| Static Discharge Voltage | > 2001V (per MIL-STD-883, Method 3015) |
| Latch-up Current | > 200 mA |

Operating Range^[2]

| Range | Ambient Temperature ^[2] | Junction Temperature | V _{CC} ^[10] |
|-------------------------|------------------------------------|----------------------|---------------------------------|
| Commercial | 0°C to +70°C | 0°C to +90°C | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | -40°C to +105°C | 3.3V ± 0.3V |
| Military ^[3] | -55°C to +125°C | -55°C to +130°C | 3.3V ± 0.3V |

3.3V Device Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-------------------|--|---|------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min. I _{OH} = -4 mA (Com'I) ^[4] I _{OH} = -3 mA (Mil) ^[4] | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min. I _{OL} = 8 mA (Com'I) ^[4] I _{OL} = 6 mA (Mil) ^[4] | | 0.5 | V |
| V _{IH} | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs ^[7] | 2.0 | 5.5 | V |
| V _{IL} | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs ^[7] | -0.5 | 0.8 | V |
| I _{IX} | Input Load Current | V _I = GND OR V _{CC} , Bus-Hold Disabled | -10 | 10 | μA |
| I _{OZ} | Output Leakage Current | V _O = GND or V _{CC} , Output Disabled, Bus-Hold Disabled | -50 | 50 | μA |
| I _{OS} | Output Short Circuit Current ^[8, 5] | V _{CC} = Max., V _{OUT} = 0.5V | -30 | -160 | mA |
| I _{BHL} | Input Bus-Hold LOW Sustaining Current | V _{CC} = Min., V _{IL} = 0.8V | +75 | | μA |
| I _{BHH} | Input Bus-Hold HIGH Sustaining Current | V _{CC} = Min., V _{IH} = 2.0V | -75 | | μA |
| I _{BHLO} | Input Bus-Hold LOW Overdrive Current | V _{CC} = Max. | | +500 | μA |

Notes:

9. Dual pins are I/O with JTAG pins.

10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V ± 0.16V.

3.3V Device Electrical Characteristics Over the Operating Range (continued)

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-------------------|---------------------------------------|------------------------|------|------|---------------|
| $I_{BH\text{HO}}$ | Input Bus-Hold HIGH Overdrive Current | $V_{CC} = \text{Max.}$ | | -500 | μA |

Inductance^[5]

| Parameter | Description | Test Conditions | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 208-Lead PQFP | Unit |
|-----------|------------------------|---|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|------|
| L | Maximum Pin Inductance | $V_{IN} = 3.3\text{V}$ at $f = 1\text{ MHz}$ | 2 | 5 | 2 | 8 | 5 | 8 | 9 | 11 | nH |

Capacitance^[5]

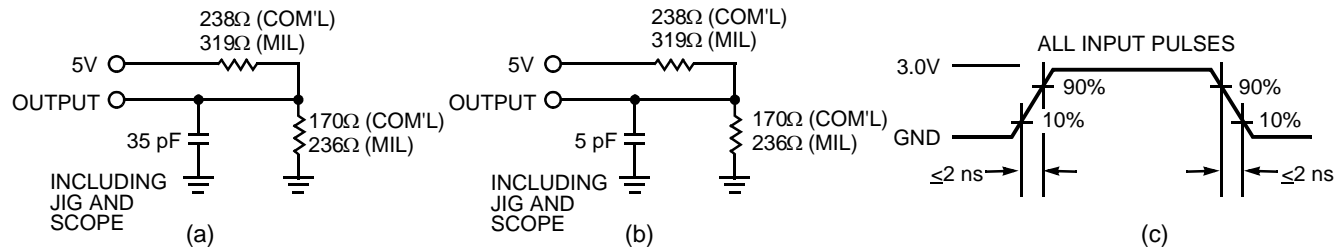
| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|-------------------------------------|--|------|------|
| $C_{I/O}$ | Input/Output Capacitance | $V_{IN} = 3.3\text{V}$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ\text{C}$ | 8 | pF |
| C_{CLK} | Clock Signal Capacitance | $V_{IN} = 3.3\text{V}$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ\text{C}$ | 12 | pF |
| C_{DP} | Dual Functional Pins ^[9] | $V_{IN} = 3.3\text{V}$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ\text{C}$ | 16 | pF |

Endurance Characteristics^[5]

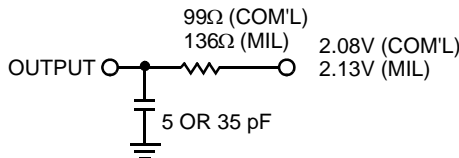
| Parameter | Description | Test Conditions | Min. | Typ. | Unit |
|-----------|------------------------------|--|-------|--------|--------|
| N | Minimum Reprogramming Cycles | Normal Programming Conditions ^[2] | 1,000 | 10,000 | Cycles |

AC Characteristics

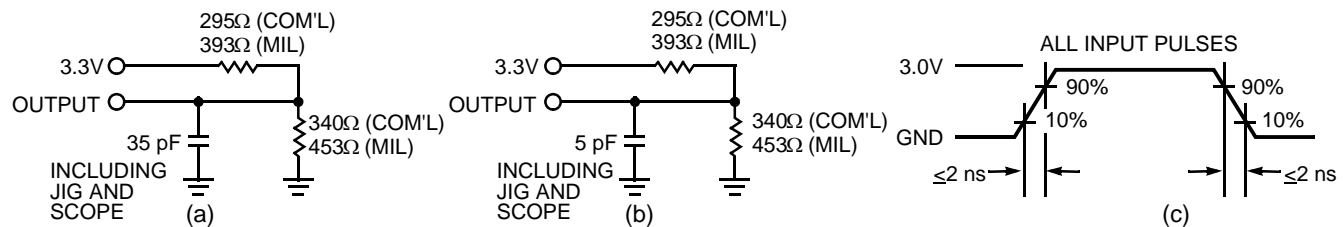
5.0V AC Test Loads and Waveforms



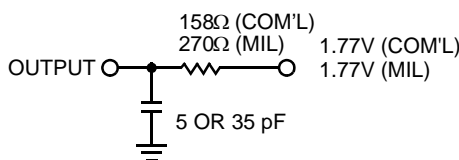
Equivalent to: THÉVENIN EQUIVALENT

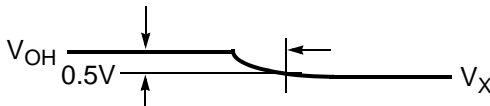
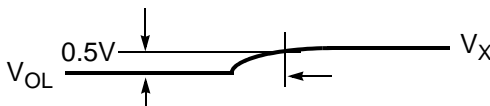
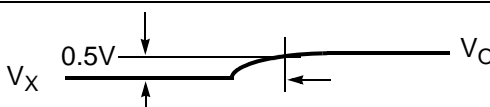
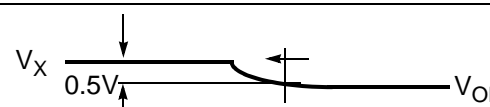


3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



| Parameter ^[11] | V _X | Output Waveform—Measurement Level |
|---------------------------|------------------|--|
| t _{ER(-)} | 1.5V |  |
| t _{ER(+)} | 2.6V |  |
| t _{EA(+)} | 1.5V |  |
| t _{EA(-)} | V _{the} |  |

(d) Test Waveforms
Switching Characteristics Over the Operating Range ^[12]

| Parameter | Description | Unit |
|---|--|------|
| Combinatorial Mode Parameters | | |
| t _{PD} ^[13, 14, 15] | Input to Combinatorial Output | ns |
| t _{PDL} ^[13, 14, 15] | Input to Output Through Transparent Input or Output Latch | ns |
| t _{PDLL} ^[13, 14, 15] | Input to Output Through Transparent Input and Output Latches | ns |
| t _{EA} ^[13, 14, 15] | Input to Output Enable | ns |
| t _{ER} ^[11, 13] | Input to Output Disable | ns |
| Input Register Parameters | | |
| t _{WL} | Clock or Latch Enable Input LOW Time ^[8] | ns |
| t _{WH} | Clock or Latch Enable Input HIGH Time ^[8] | ns |
| t _{IS} | Input Register or Latch Set-up Time | ns |
| t _{IH} | Input Register or Latch Hold Time | ns |
| t _{ICO} ^[13, 14, 15] | Input Register Clock or Latch Enable to Combinatorial Output | ns |
| t _{COL} ^[13, 14, 15] | Input Register Clock or Latch Enable to Output Through Transparent Output Latch | ns |
| Synchronous Clocking Parameters | | |
| t _{CO} ^[14, 15] | Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output | ns |
| t _S ^[13] | Set-Up Time from Input to Sync. Clk (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable | ns |
| t _H | Register or Latch Data Hold Time | ns |
| t _{CO2} ^[13, 14, 15] | Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Combinatorial Output Delay (Through Logic Array) | ns |
| t _{SCS} ^[13] | Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable (Through Logic Array) | ns |
| t _{SL} ^[13] | Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable | ns |
| t _{HL} | Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable | ns |

Notes:

11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CC0} = 3.3V, add t_{3,3IO} to this spec.

Switching Characteristics Over the Operating Range (continued)^[12]

| Parameter | Description | Unit |
|---|---|------|
| Product Term Clocking Parameters | | |
| $t_{COPT}^{[13, 14, 15]}$ | Product Term Clock or Latch Enable (PTCLK) to Output | ns |
| t_{SPT} | Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK) | ns |
| t_{HPT} | Register or Latch Data Hold Time | ns |
| $t_{ISPT}^{[13]}$ | Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK) | ns |
| t_{IHPT} | Buried Register Used as an Input Register or Latch Data Hold Time | ns |
| $t_{CO2PT}^{[13, 14, 15]}$ | Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array) | ns |
| Pipelined Mode Parameters | | |
| $t_{ICS}^{[13]}$ | Input Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) | ns |
| Operating Frequency Parameters | | |
| f_{MAX1} | Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[5] | MHz |
| f_{MAX2} | Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[5] | MHz |
| f_{MAX3} | Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$) ^[5] | MHz |
| f_{MAX4} | Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_S)$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$) ^[5] | MHz |
| Reset/Preset Parameters | | |
| t_{RW} | Asynchronous Reset Width ^[5] | ns |
| $t_{RR}^{[13]}$ | Asynchronous Reset Recovery Time ^[5] | ns |
| $t_{RO}^{[13, 14, 15]}$ | Asynchronous Reset to Output | ns |
| t_{PW} | Asynchronous Preset Width ^[5] | ns |
| $t_{PR}^{[13]}$ | Asynchronous Preset Recovery Time ^[5] | ns |
| $t_{PO}^{[13, 14, 15]}$ | Asynchronous Preset to Output | ns |
| User Option Parameters | | |
| t_{LP} | Low Power Adder | ns |
| t_{SLEW} | Slow Output Slew Rate Adder | ns |
| $t_{3.3IO}$ | 3.3V I/O Mode Timing Adder ^[5] | ns |
| JTAG Timing Parameters | | |
| $t_{S JTAG}$ | Set-up Time from TDI and TMS to TCK ^[5] | ns |
| $t_{H JTAG}$ | Hold Time on TDI and TMS ^[5] | ns |
| $t_{CO JTAG}$ | Falling Edge of TCK to TDO ^[5] | ns |
| f_{JTAG} | Maximum JTAG Tap Controller Frequency ^[5] | ns |

Switching Characteristics Over the Operating Range ^[12]

| Parameter | 200 MHz | | 167 MHz | | 154 MHz | | 143 MHz | | 125 MHz | | 100 MHz | | 83 MHz | | 66 MHz | | Unit |
|---|---------|------|---------|------|---------|------|---------|------|---------------------|---------------------|---------------------|---------------------|---------------------|-------------------|--------|------|------|
| | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Combinatorial Mode Parameters | | | | | | | | | | | | | | | | | |
| $t_{PD}^{[13, 14, 15]}$ | | 6 | | 6.5 | | 7.5 | | 8.5 | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{PDL}^{[13, 14, 15]}$ | | 11 | | 12.5 | | 14.5 | | 16 | | 16.5 | | 17 | | 19 | | 22 | ns |
| $t_{PDLL}^{[13, 14, 15]}$ | | 12 | | 13.5 | | 15.5 | | 17 | | 17.5 | | 18 | | 20 | | 24 | ns |
| $t_{EA}^{[13, 14, 15]}$ | | 8 | | 8.5 | | 11 | | 13 | | 14 | | 16 | | 19 | | 24 | ns |
| $t_{ER}^{[11, 13]}$ | | 8 | | 8.5 | | 11 | | 13 | | 14 | | 16 | | 19 | | 24 | ns |
| Input Register Parameters | | | | | | | | | | | | | | | | | |
| t_{WL} | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 3 | | 3 | | 4 | | 5 | | ns |
| t_{WH} | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 3 | | 3 | | 4 | | 5 | | ns |
| t_{IS} | 2 | | 2 | | 2 | | 2 | | 2 | | 2.5 | | 3 | | 4 | | ns |
| t_{IH} | 2 | | 2 | | 2 | | 2 | | 2 | | 2.5 | | 3 | | 4 | | ns |
| $t_{ICO}^{[13, 14, 15]}$ | | 11 | | 11 | | 11 | | 12.5 | | 12.5 | | 16 | | 19 | | 24 | ns |
| $t_{ICOL}^{[13, 14, 15]}$ | | 12 | | 12 | | 12 | | 14 | | 16 | | 18 | | 21 | | 26 | ns |
| Synchronous Clocking Parameters | | | | | | | | | | | | | | | | | |
| $t_{CO}^{[14, 15]}$ | | 4 | | 4 | | 4.5 | | 6 | | 6.5 ^[16] | | 6.5 ^[17] | | 8 ^[18] | | 10 | ns |
| $t_S^{[13]}$ | 4 | | 4 | | 5 | | 5 | | 5.5 ^[16] | | 6 ^[17] | | 8 ^[18] | | 10 | | ns |
| t_H | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{CO2}^{[13, 14, 15]}$ | | 9.5 | | 10 | | 11 | | 12 | | 14 | | 16 | | 19 | | 24 | ns |
| $t_{SCS}^{[13]}$ | 5 | | 6 | | 6.5 | | 7 | | 8 ^[16] | | 10 | | 12 | | 15 | | ns |
| $t_{SL}^{[13]}$ | 7.5 | | 7.5 | | 8.5 | | 9 | | 10 | | 12 | | 15 | | 15 | | ns |
| t_{HL} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Product Term Clocking Parameters | | | | | | | | | | | | | | | | | |
| $t_{COPT}^{[13, 14, 15]}$ | | 7 | | 10 | | 10 | | 13 | | 13 | | 13 | | 15 | | 20 | ns |
| t_{SPT} | 2.5 | | 2.5 | | 2.5 | | 3 | | 5 | | 5.5 | | 6 | | 7 | | ns |
| t_{HPT} | 2.5 | | 2.5 | | 2.5 | | 3 | | 5 | | 5.5 | | 6 | | 7 | | ns |
| $t_{ISPT}^{[13]}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{IHPT} | 6 | | 6.5 | | 6.5 | | 7.5 | | 9 | | 11 | | 14 | | 19 | | ns |
| $t_{CO2PT}^{[13, 14, 15]}$ | | 12 | | 14 | | 15 | | 19 | | 19 | | 21 | | 24 | | 30 | ns |
| Pipelined Mode Parameters | | | | | | | | | | | | | | | | | |
| $t_{ICS}^{[13]}$ | 5 | | 6 | | 6 | | 7 | | 8 ^[16] | | 10 | | 12 | | 15 | | ns |
| Operating Frequency Parameters | | | | | | | | | | | | | | | | | |
| f_{MAX1} | 200 | | 167 | | 154 | | 143 | | 125 ^[16] | | 100 | | 83 | | 66 | | MHz |
| f_{MAX2} | 200 | | 200 | | 200 | | 167 | | 154 | | 153 ^[17] | | 125 ^[18] | | 100 | | MHz |
| f_{MAX3} | 125 | | 125 | | 105 | | 91 | | 83 | | 80 ^[17] | | 62.5 | | 50 | | MHz |
| f_{MAX4} | 167 | | 167 | | 154 | | 125 | | 118 | | 100 | | 83 | | 66 | | MHz |
| Reset/Preset Parameters | | | | | | | | | | | | | | | | | |
| t_{RW} | 8 | | 8 | | 8 | | 8 | | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{RR}^{[13]}$ | 10 | | 10 | | 10 | | 10 | | 12 | | 14 | | 17 | | 22 | | ns |

Notes:

16. The following values correspond to the CY37512 and CY37384 devices: $t_{CO} = 5$ ns, $t_S = 6.5$ ns, $t_{SCS} = 8.5$ ns, $t_{ICS} = 8.5$ ns, $f_{MAX1} = 118$ MHz.

17. The following values correspond to the CY37192V and CY37256V devices: $t_{CO} = 6$ ns, $t_S = 7$ ns, $f_{MAX2} = 143$ MHz, $f_{MAX3} = 77$ MHz, and $f_{MAX4} = 100$ MHz; and for the CY37512 devices: $t_S = 7$ ns.

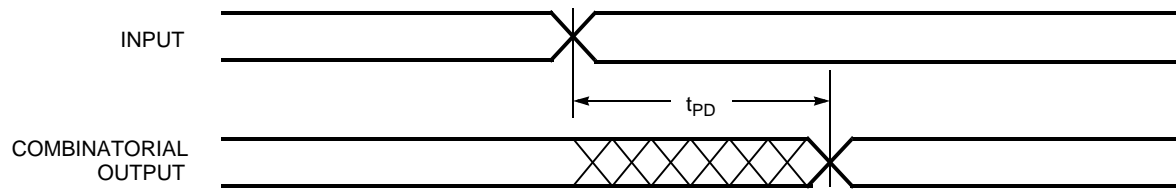
18. The following values correspond to the CY37512V and CY37384V devices: $t_{CO} = 6.5$ ns, $t_S = 9.5$ ns, and $f_{MAX2} = 105$ MHz.

Switching Characteristics Over the Operating Range (continued)^[12]

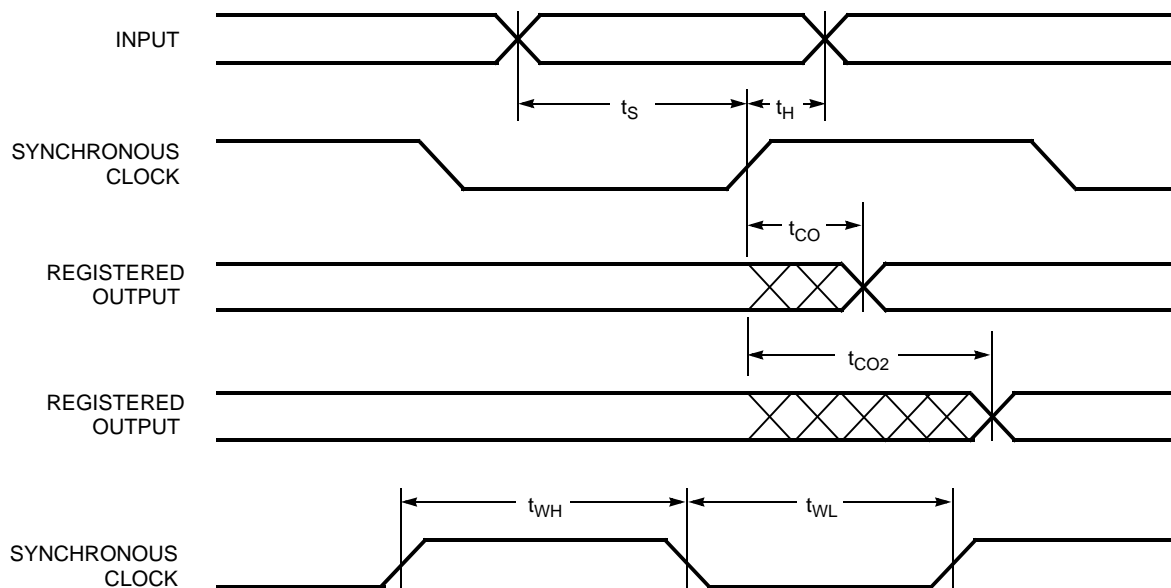
| Parameter | 200 MHz | | 167 MHz | | 154 MHz | | 143 MHz | | 125 MHz | | 100 MHz | | 83 MHz | | 66 MHz | | Unit |
|----------------------------------|---------|------|---------|------|---------|------|---------|------|---------|------|---------|------|--------|------|--------|------|------|
| | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{RO} ^[13, 14, 15] | | 12 | | 13 | | 13 | | 14 | | 15 | | 18 | | 21 | | 26 | ns |
| t_{PW} | 8 | | 8 | | 8 | | 8 | | 10 | | 12 | | 15 | | 20 | | ns |
| t_{PR} ^[13] | 10 | | 10 | | 10 | | 10 | | 12 | | 14 | | 17 | | 22 | | ns |
| t_{PO} ^[13, 14, 15] | | 12 | | 13 | | 13 | | 14 | | 15 | | 18 | | 21 | | 26 | ns |
| User Option Parameters | | | | | | | | | | | | | | | | | |
| t_{LP} | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 2.5 | ns |
| t_{SLEW} | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | ns |
| $t_{3.3IO}$ ^[19] | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| JTAG Timing Parameters | | | | | | | | | | | | | | | | | |
| $t_{S\ JTAG}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{H\ JTAG}$ | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| $t_{CO\ JTAG}$ | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | ns |
| f_{JTAG} | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | MHz |

Switching Waveforms

Combinatorial Output

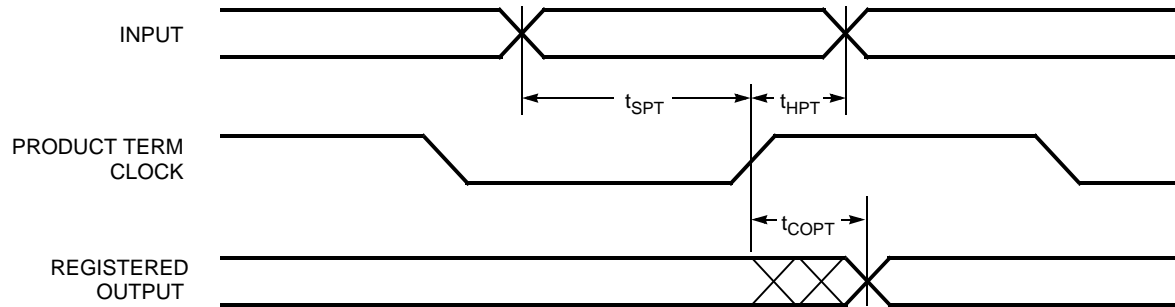
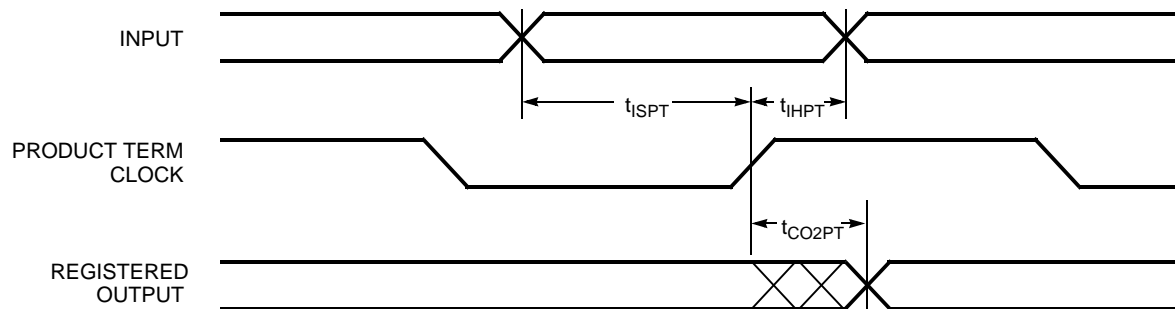
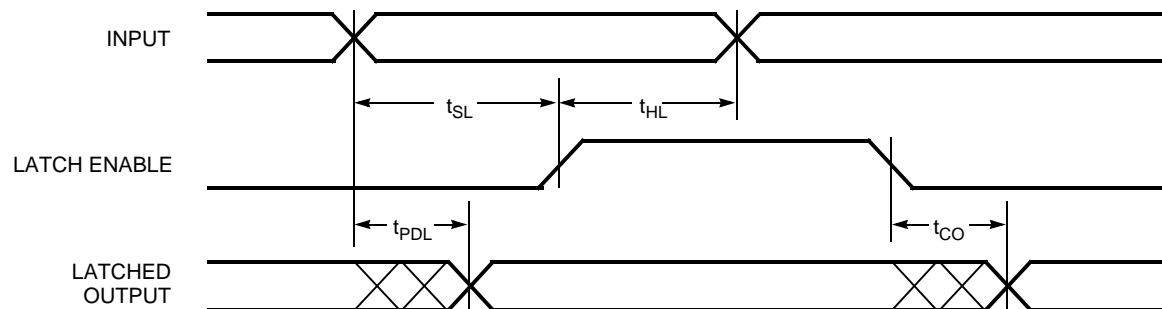


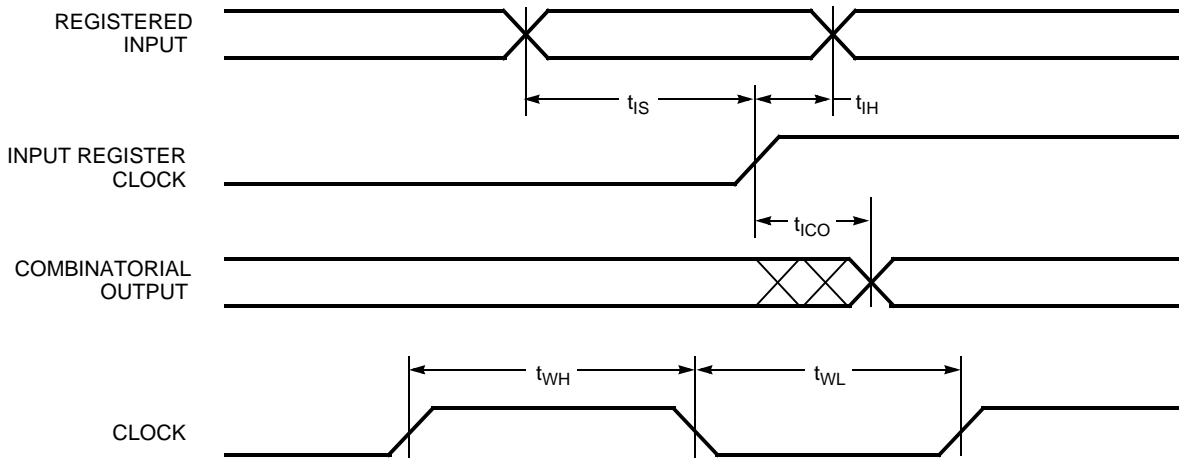
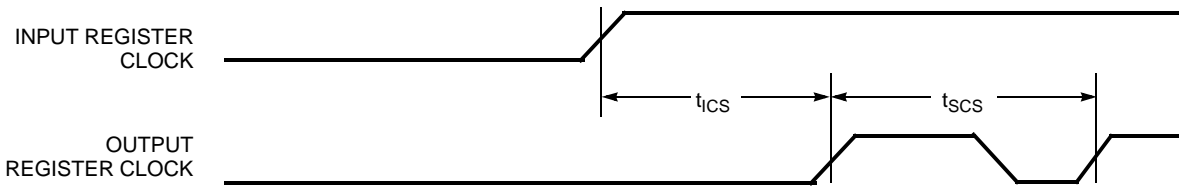
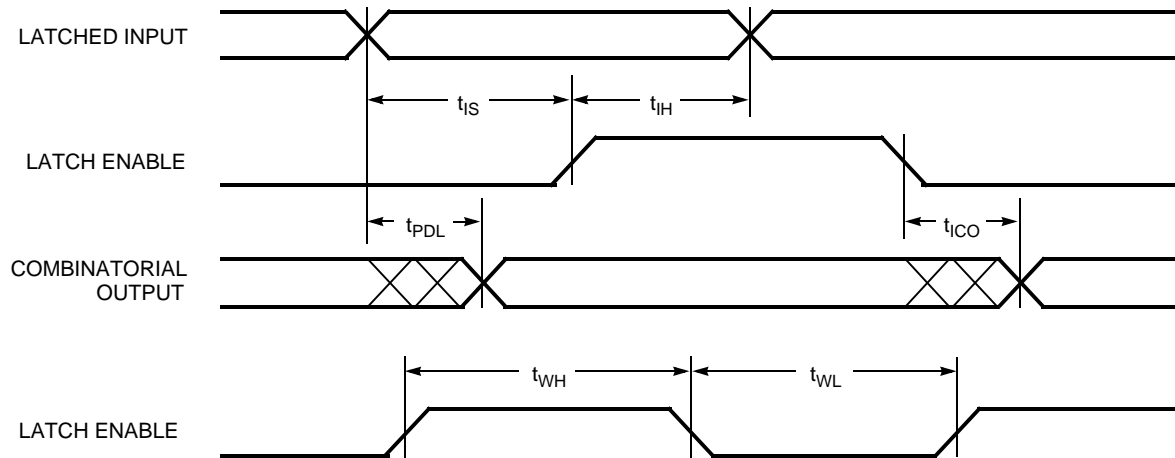
Registered Output with Synchronous Clocking

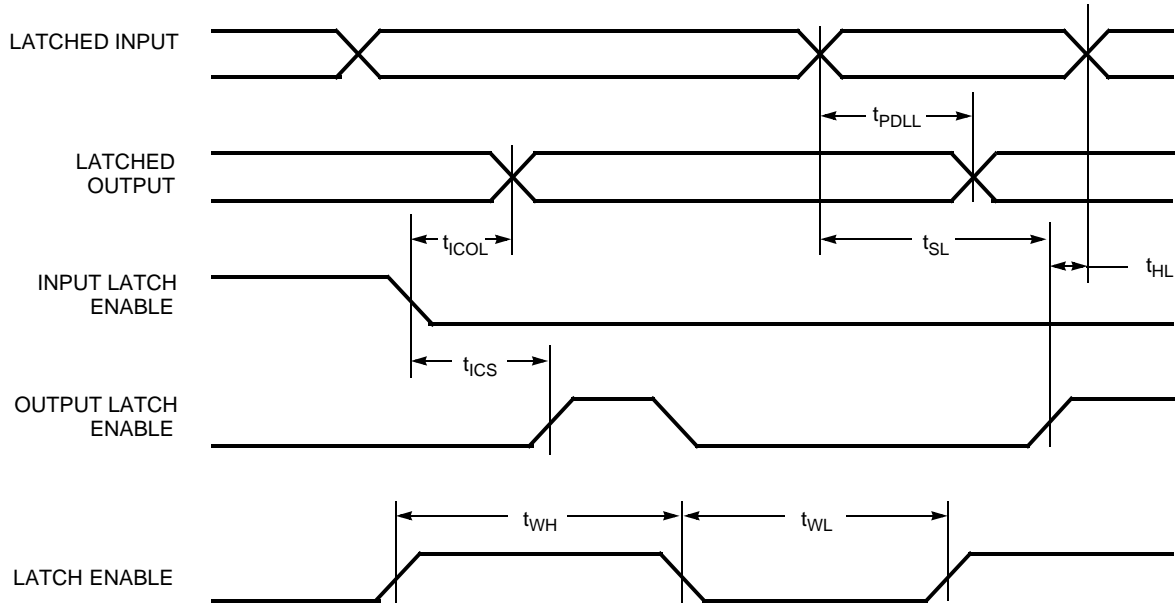
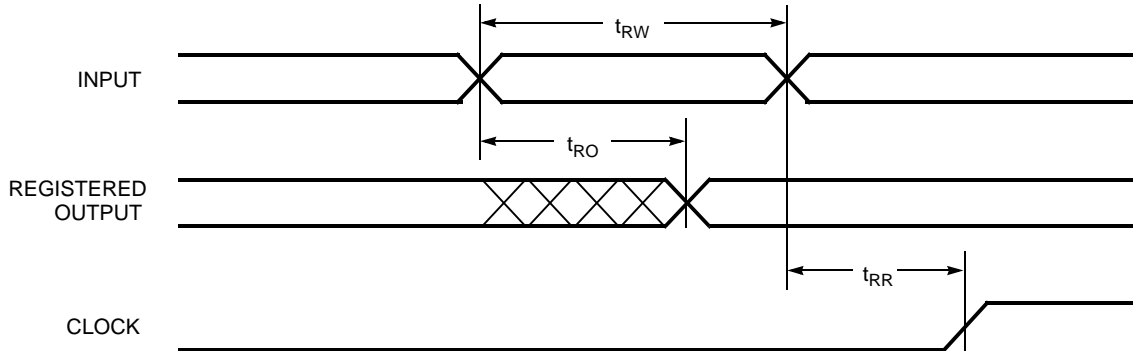
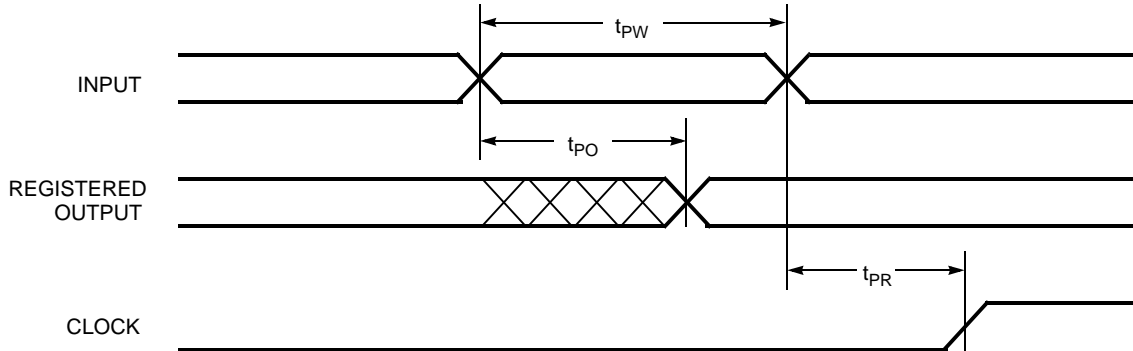


Note:

19. Only applicable to the 5V devices.

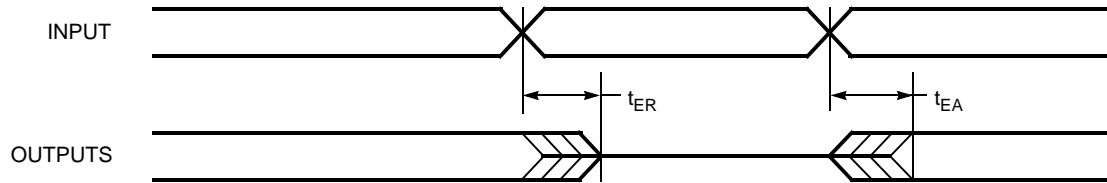
Switching Waveforms (continued)
**Registered Output with Product Term Clocking
Input Going Through the Array**

**Registered Output with Product Term Clocking
Input Coming From Adjacent Buried Register**

Latched Output


Switching Waveforms (continued)
Registered Input

Clock to Clock

Latched Input


Switching Waveforms (continued)
Latched Input and Output

Asynchronous Reset

Asynchronous Preset


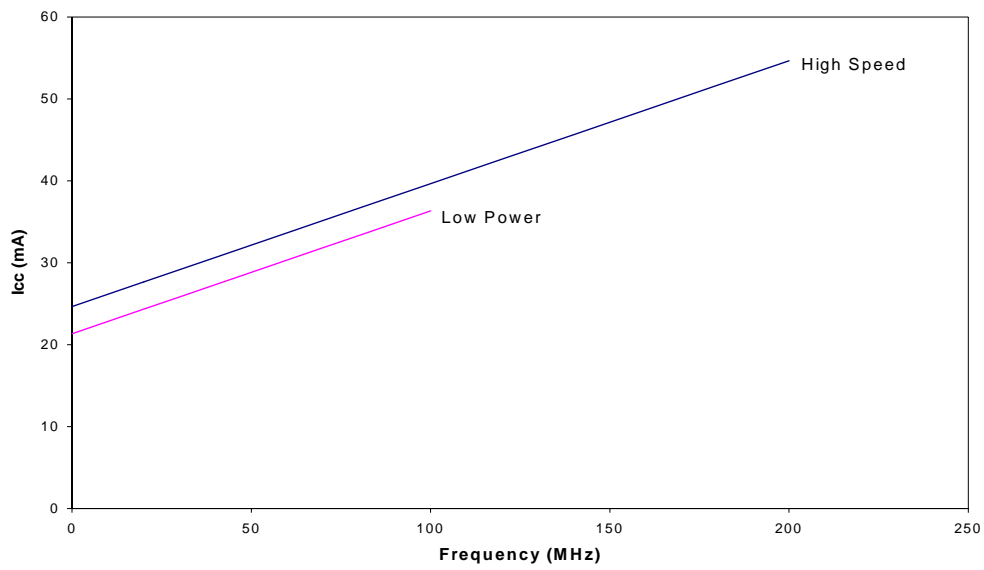
Switching Waveforms (continued)

Output Enable/Disable



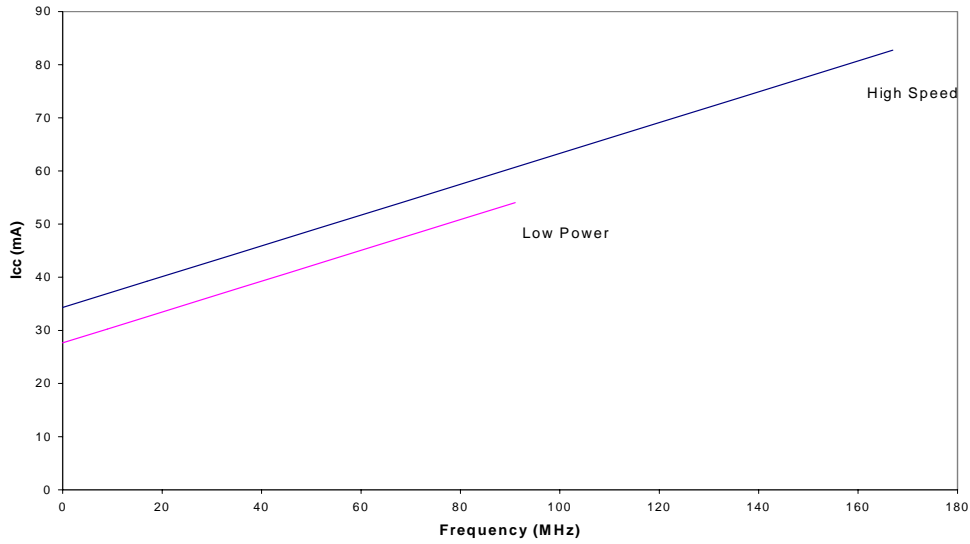
Power Consumption

Typical 5.0V Power Consumption
CY37032



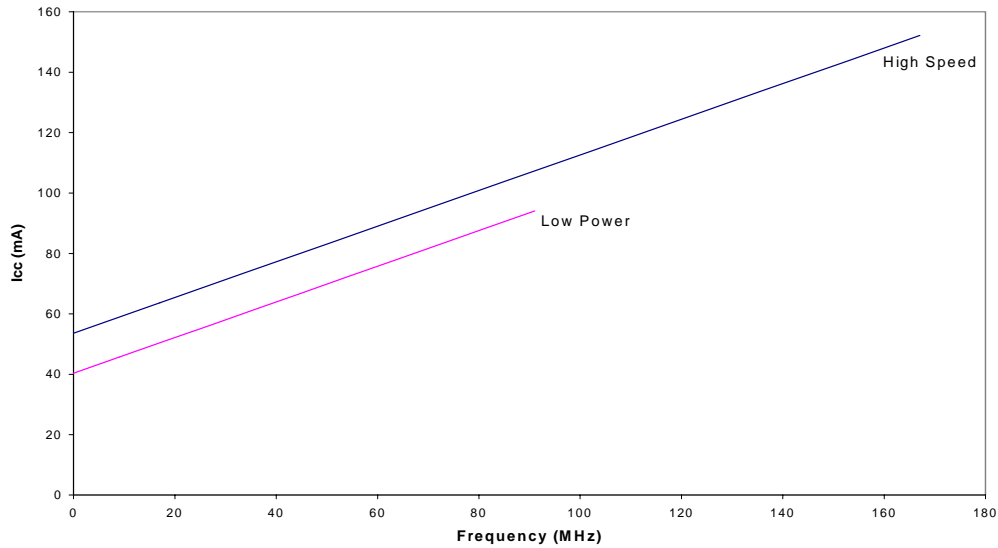
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 5.0V Power Consumption (continued)
CY37064



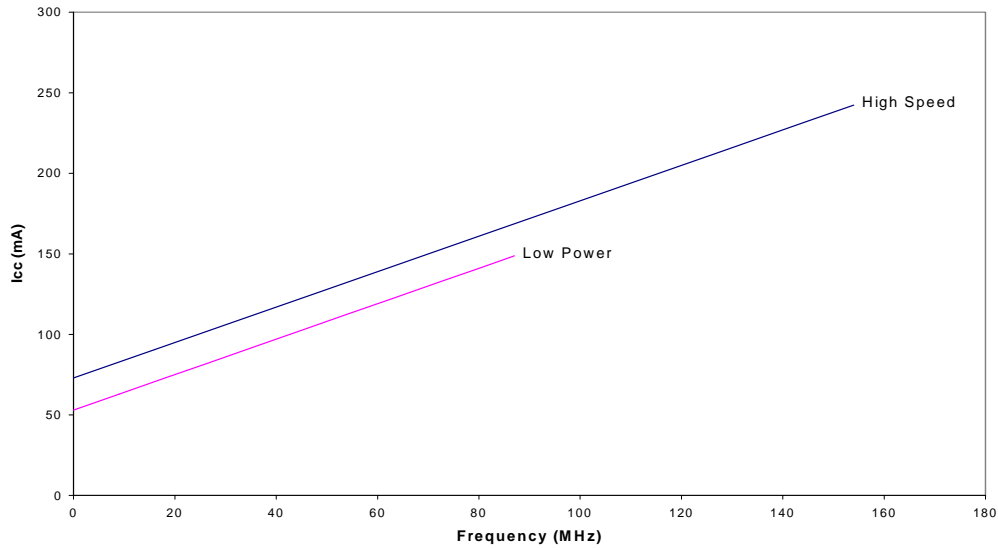
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

CY37128



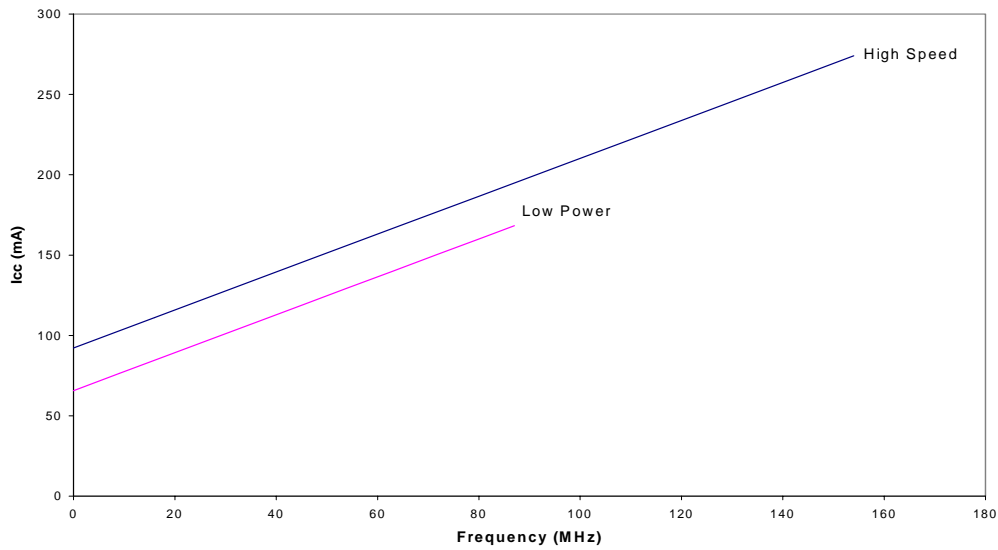
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 5.0V Power Consumption (continued)
CY37192



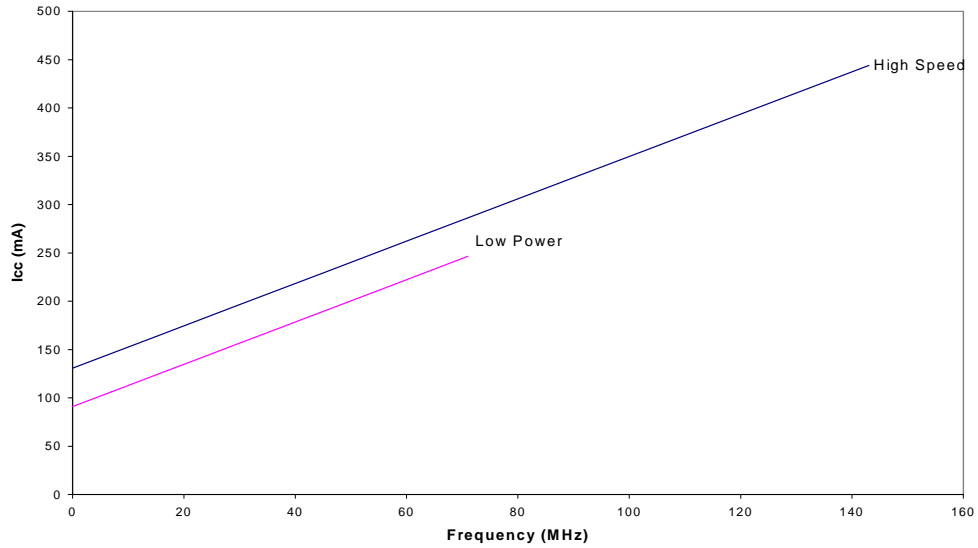
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

CY37256



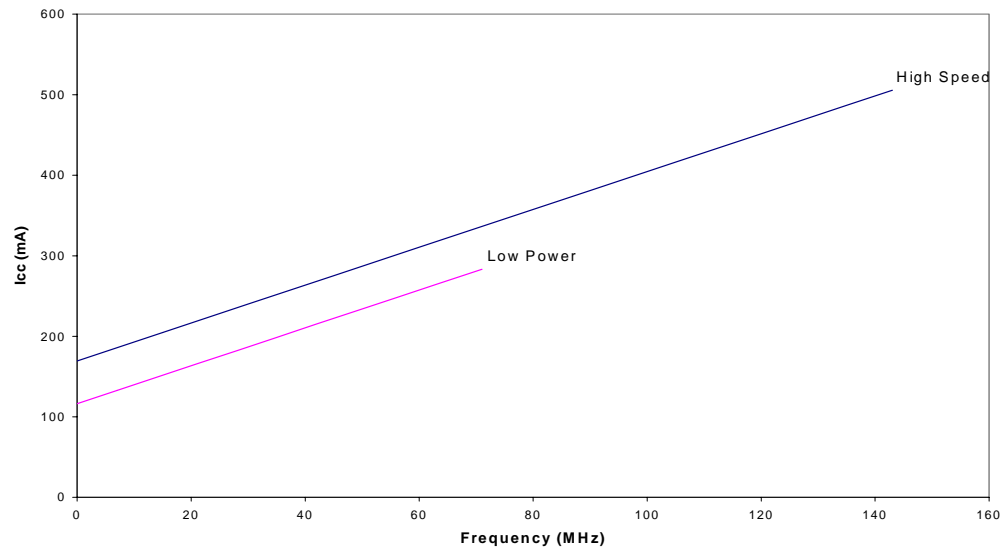
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 5.0V Power Consumption (continued)
CY37384



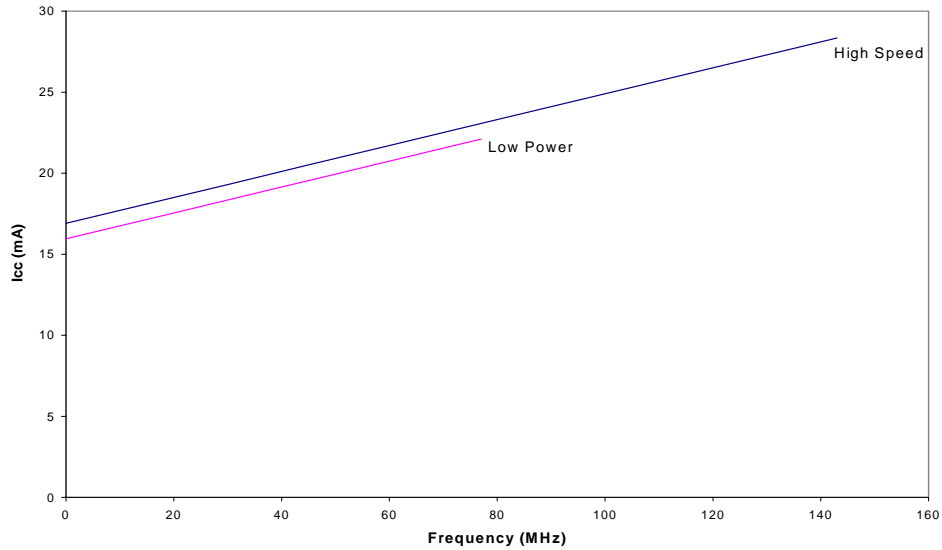
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

CY37512



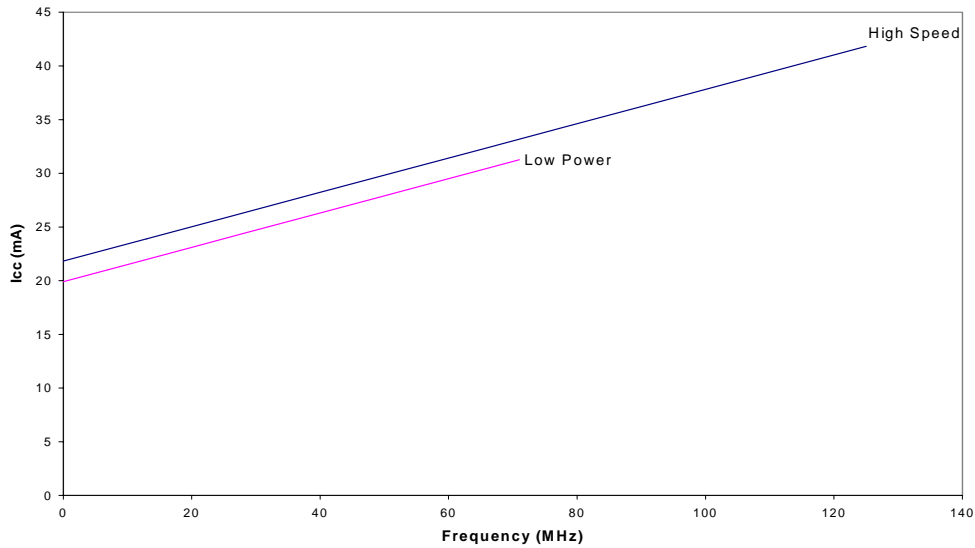
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

**Typical 3.3V Power Consumption
CY37032V**



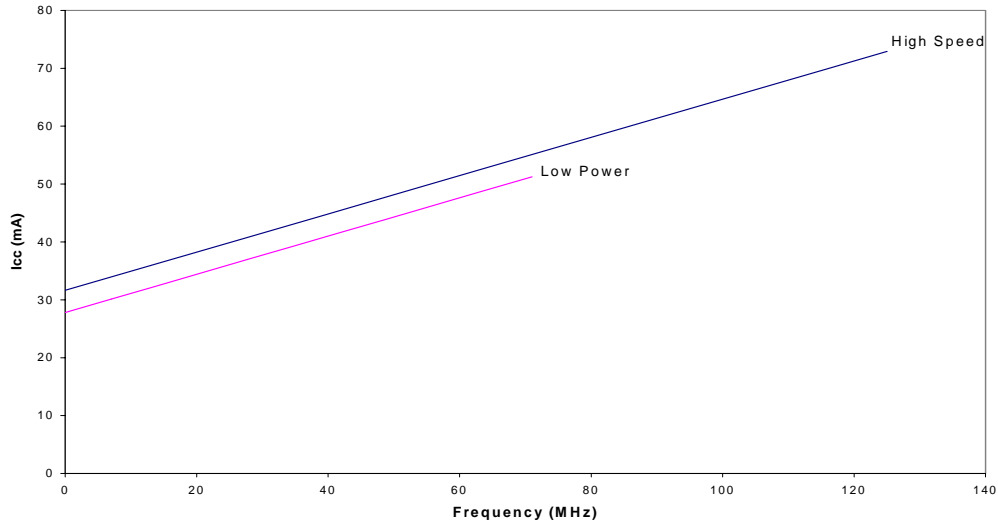
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37064V



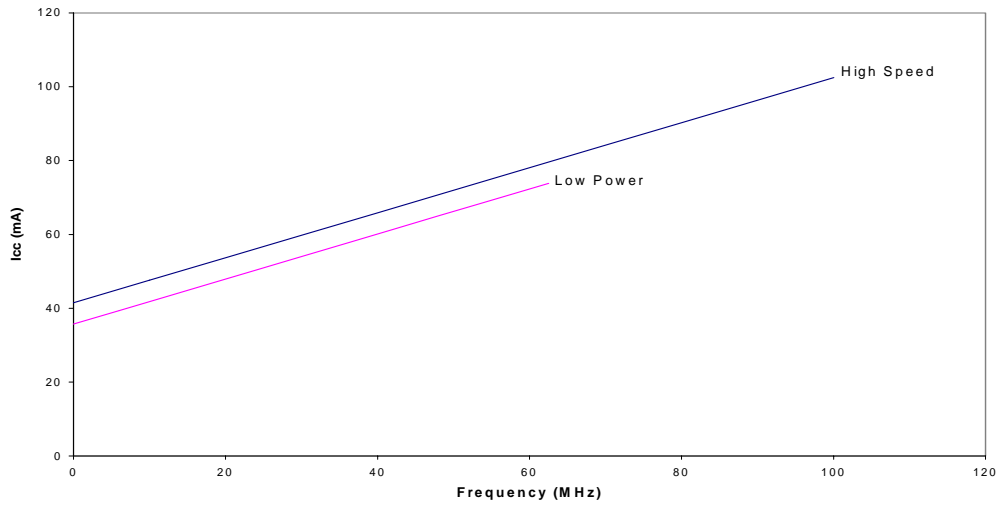
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Typical 3.3V Power Consumption (continued)
CY37128V



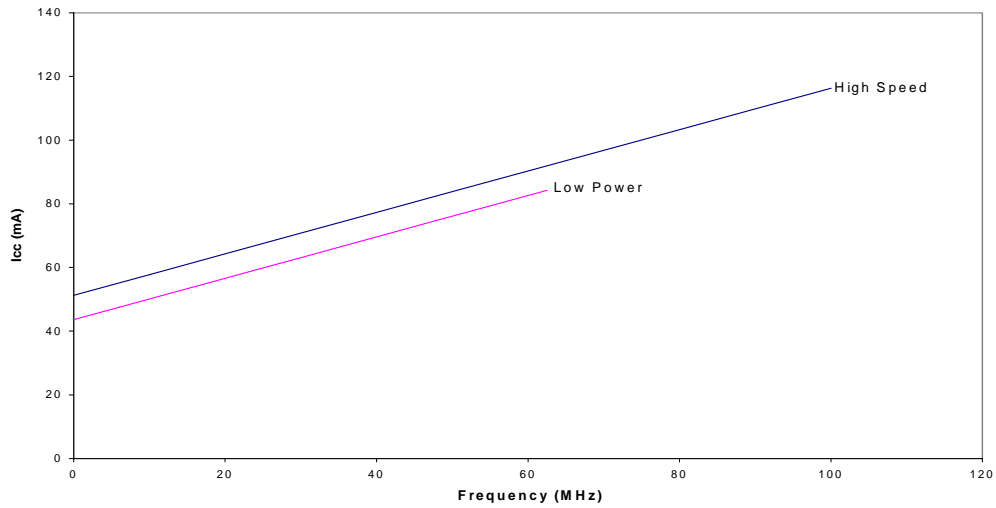
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

CY37192V



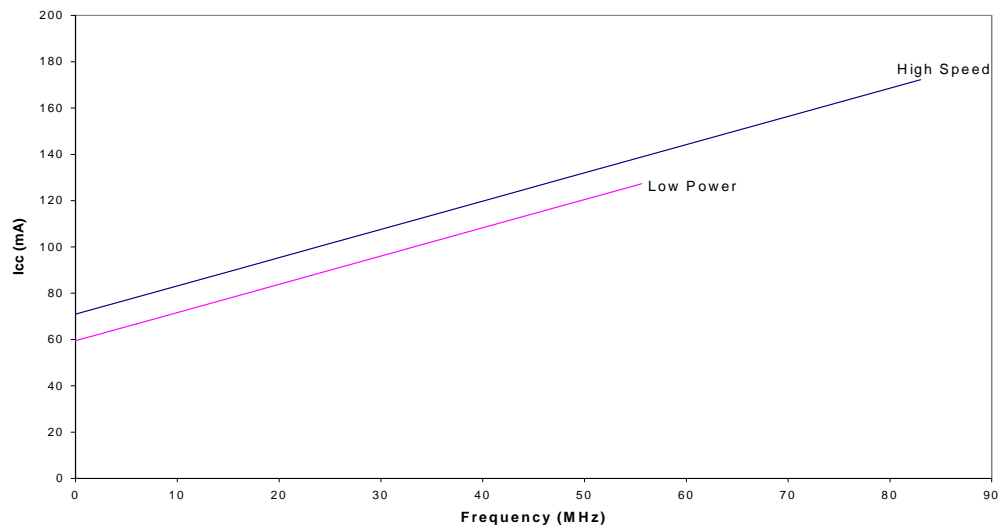
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

Typical 3.3V Power Consumption (continued)
CY37256V

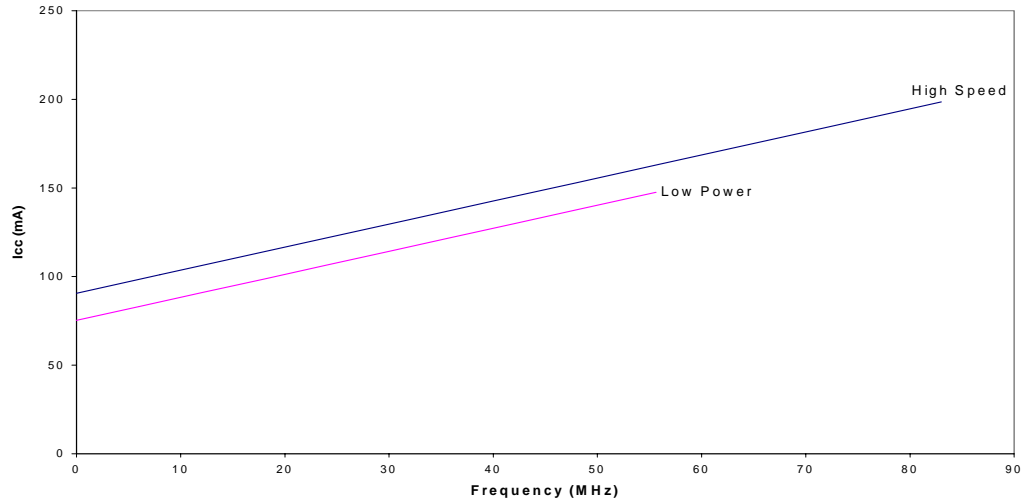


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

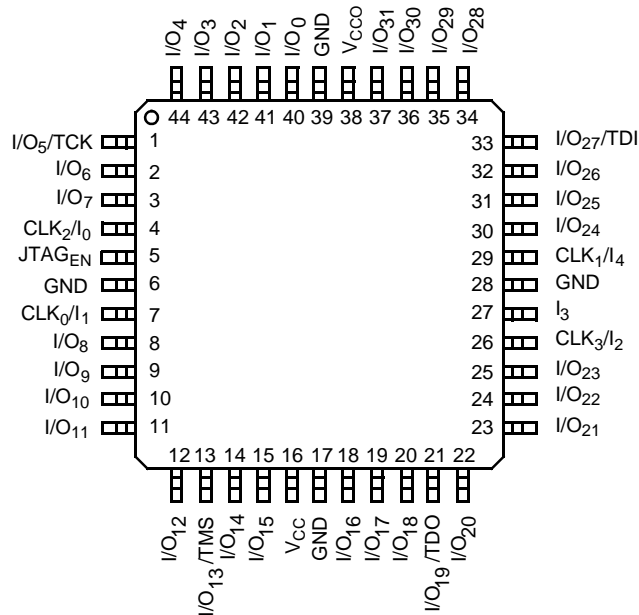
CY37384V

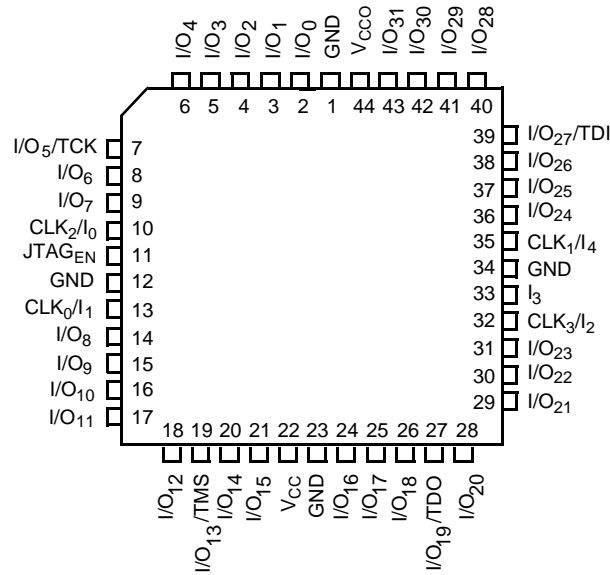


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

Typical 3.3V Power Consumption (continued)
CY37512V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

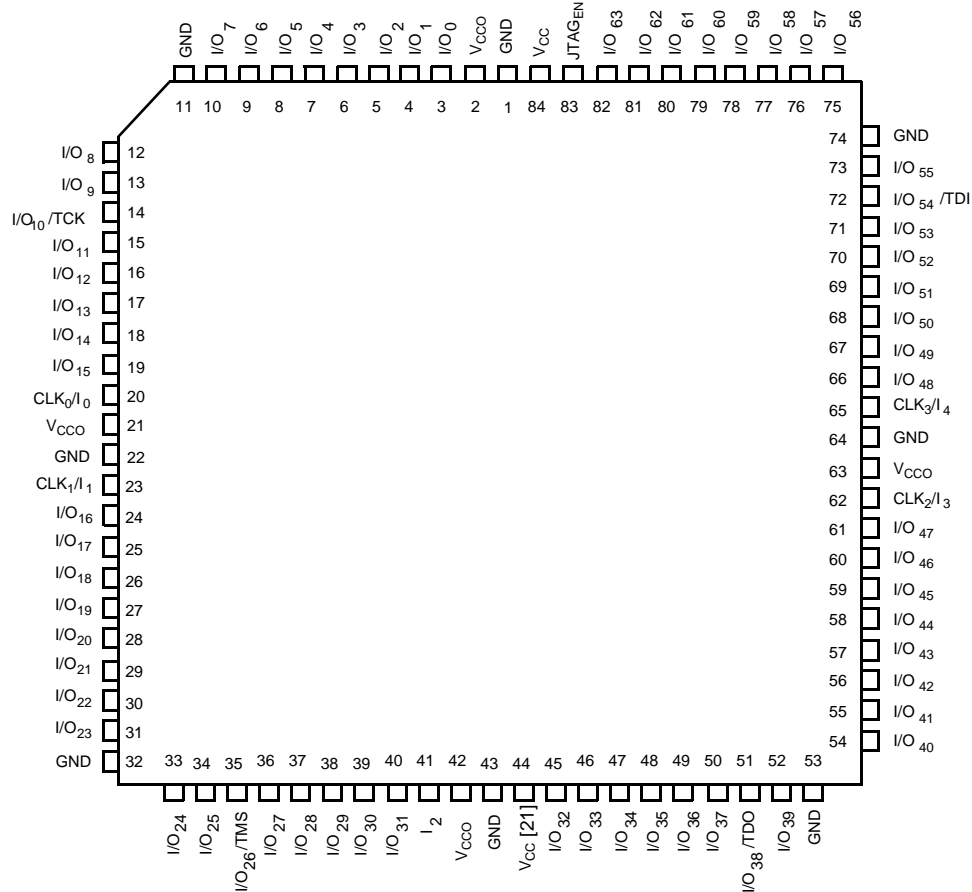
Pin Configurations^[20]
44-pin TQFP (A44)
Top View


Pin Configurations^[20] (continued)
44-pin PLCC (J67) / CLCC (Y67)
Top View

48-ball Fine-Pitch BGA (BA50)
Top View

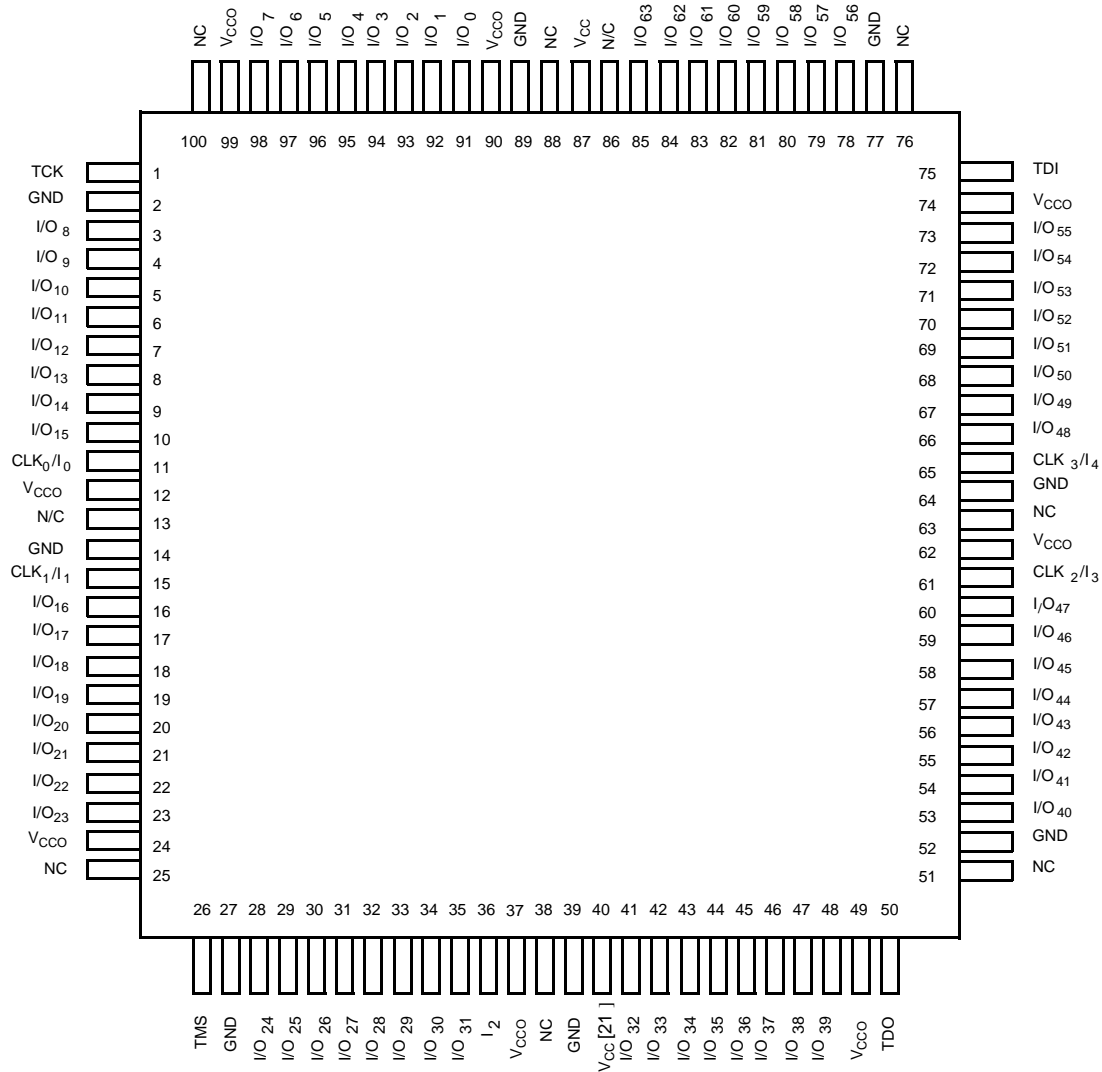
| | | | | | | | | |
|---|----------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|----------------------------------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| A | I/O ₅ TCK | V _{CC} | I/O ₃ | I/O ₁ | I/O ₃₁ | I/O ₃₀ | V _{CC} | I/O ₂₇ TDI |
| B | V _{CC} | I/O ₄ | I/O ₂ | I/O ₀ | I/O ₂₉ | I/O ₂₈ | I/O ₂₆ | CLK ₁ /I ₄ |
| C | CLK ₂ /I ₀ | I/O ₇ | I/O ₆ | GND | GND | I/O ₂₅ | I/O ₂₄ | I ₃ |
| D | JTAG _{EN} | I/O ₈ | I/O ₉ | GND | GND | I/O ₂₂ | I/O ₂₃ | CLK ₃ /I ₂ |
| E | CLK ₀ /I ₁ | I/O ₁₂ | I/O ₁₁ | I/O ₁₀ | I/O ₁₆ | I/O ₂₀ | I/O ₂₁ | V _{CC} |
| F | I/O ₁₃ TMS | V _{CC} | I/O ₁₄ | I/O ₁₅ | I/O ₁₇ | I/O ₁₈ | V _{CC} | I/O ₁₉ TDO |

Note:

 20. For 3.3V versions (Ultra37000V), V_{CCO} = V_{CC}.


Pin Configurations^[20] (continued)
**84-lead PLCC (J83) / CLCC (Y84)
Top View**

Note:

21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.


Pin Configurations^[20] (continued)
100-lead TQFP (A100)
Top View


Pin Configurations^[20] (continued)
100-ball Fine-Pitch BGA (BB100) for CY37064V
Top View

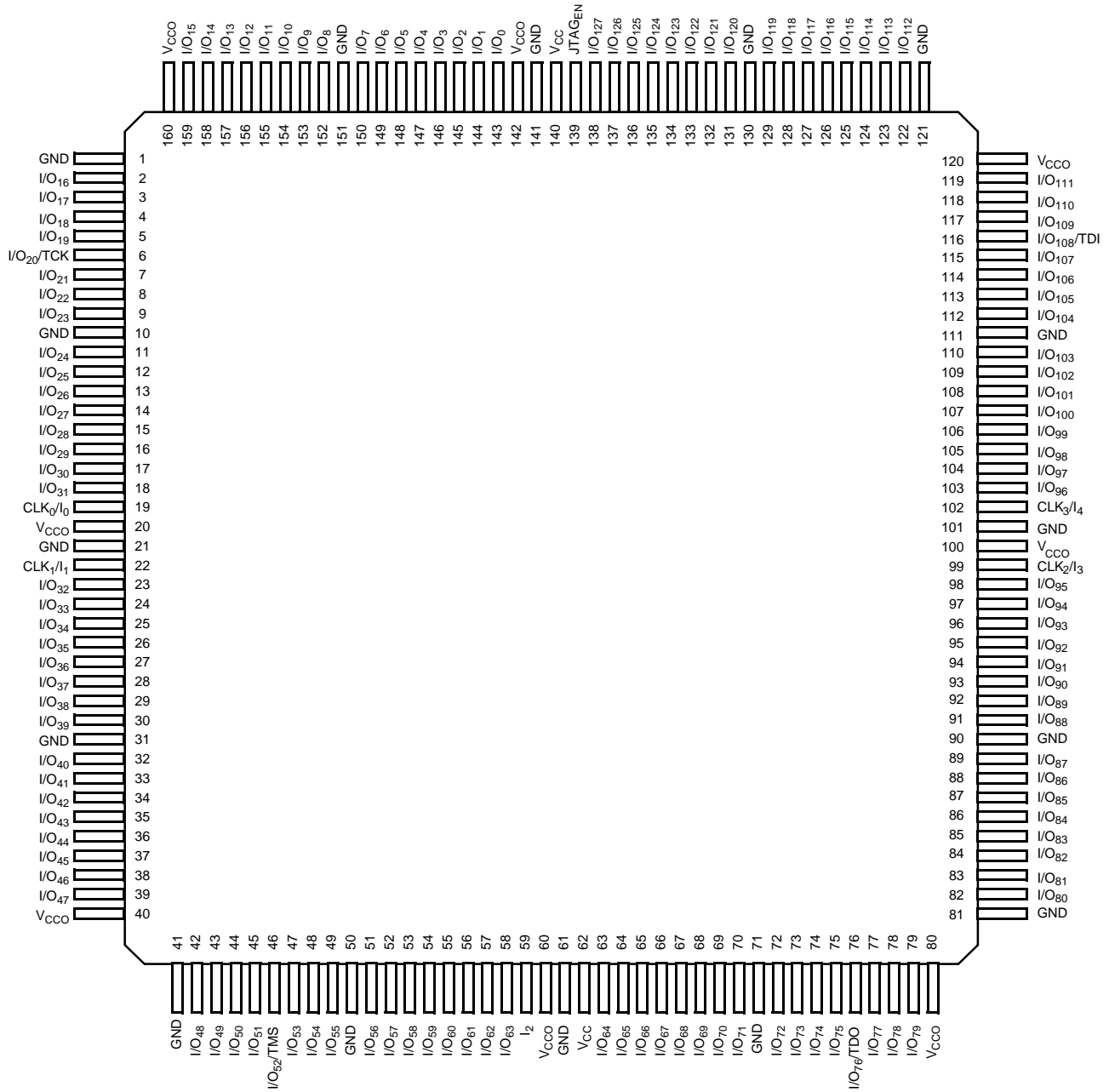
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|-------------------|--------------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------------------------|-------------------|
| A | NC | NC | I/O ₇ | I/O ₅ | I/O ₂ | I/O ₆₂ | I/O ₆₀ | I/O ₅₈ | I/O ₅₇ | I/O ₅₆ |
| B | I/O ₉ | I/O ₈ | I/O ₆ | I/O ₄ | I/O ₁ | I/O ₆₃ | V _{CC} | I/O ₅₉ | I/O ₅₅ | NC |
| C | I/O ₁₀ | TCK | V _{CC} | I/O ₃ | NC | NC | I/O ₆₁ | V _{CC} | TDI | I/O ₅₄ |
| D | I/O ₁₁ | NC | I/O ₁₂ | I/O ₁₃ | I/O ₀ | NC | I/O ₅₁ | I/O ₅₂ | CLK ₃ / I ₄ | I/O ₅₃ |
| E | I/O ₁₄ | CLK ₀ / I ₀ | I/O ₁₅ | NC | GND | GND | I/O ₄₈ | I/O ₄₉ | CLK ₂ / I ₃ | I/O ₅₀ |
| F | I/O ₁₇ | NC | NC | I/O ₁₆ | GND | GND | NC | NC | I ₂ | I/O ₄₇ |
| G | I/O ₂₂ | CLK ₁ / I ₁ | I/O ₂₁ | I/O ₁₉ | I/O ₁₈ | I/O ₄₆ | I/O ₄₅ | I/O ₄₄ | NC | I/O ₄₃ |
| H | I/O ₂₃ | TMS | V _{CC} | I/O ₂₀ | NC | I/O ₃₂ | I/O ₄₂ | V _{CC} | TDO | I/O ₄₁ |
| J | NC | I/O ₂₆ | I/O ₂₈ | NC | I/O ₃₁ | I/O ₃₃ | I/O ₃₅ | I/O ₃₇ | I/O ₃₉ | I/O ₄₀ |
| K | I/O ₂₄ | I/O ₂₅ | I/O ₂₇ | I/O ₂₉ | I/O ₃₀ | I/O ₃₄ | I/O ₃₆ | I/O ₃₈ | NC | NC |

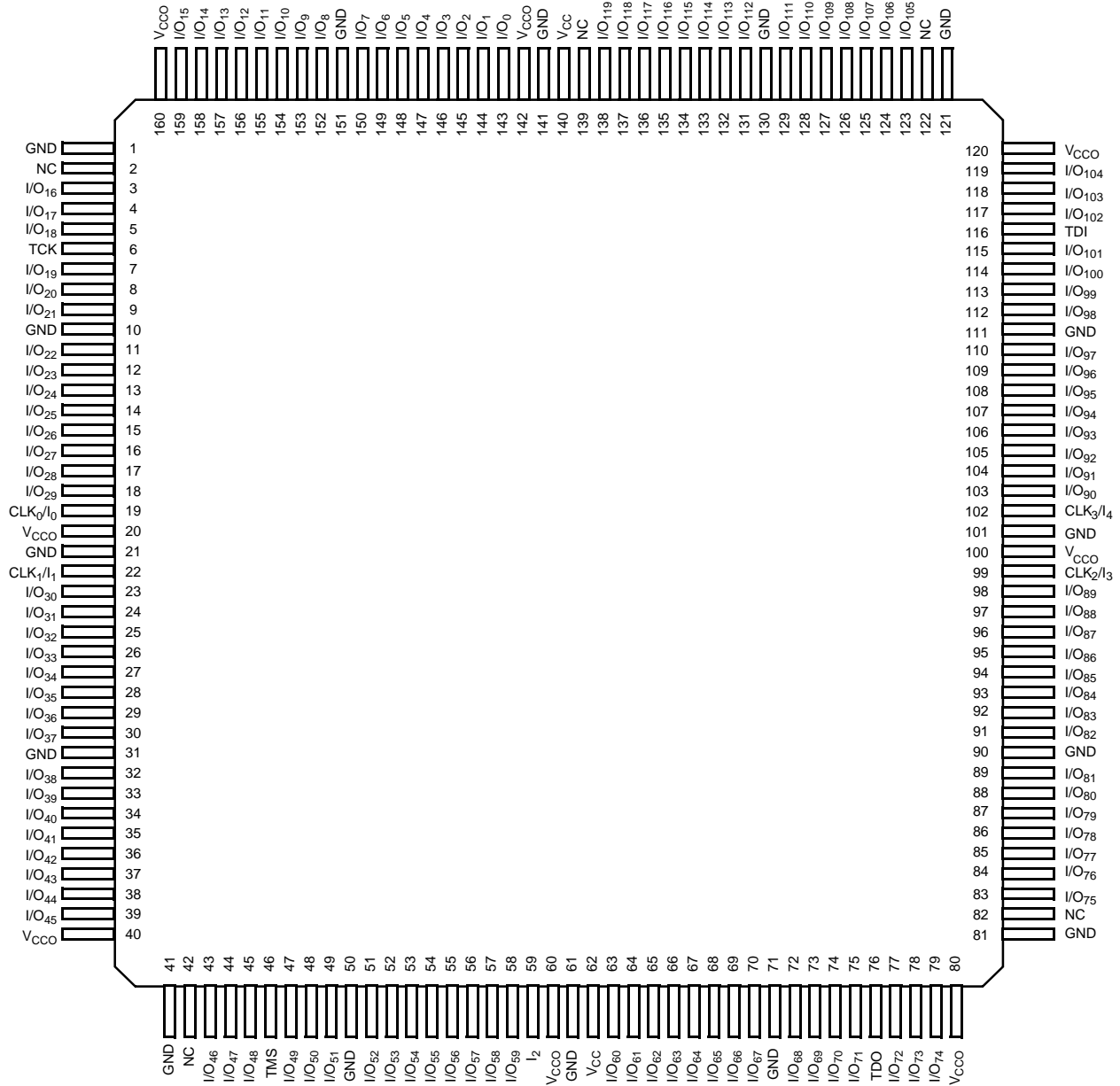
100-ball Fine-Pitch BGA (BB100) for CY37128V
Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|-------------------|--------------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------------------------|-------------------|
| A | NC | I/O ₉ | I/O ₈ | I/O ₆ | I/O ₃ | I/O ₇₆ | I/O ₇₄ | I/O ₇₂ | I/O ₇₁ | I/O ₇₀ |
| B | I/O ₁₁ | I/O ₁₀ | I/O ₇ | I/O ₅ | I/O ₂ | I/O ₇₇ | V _{CC} | I/O ₇₃ | I/O ₆₈ | I/O ₆₉ |
| C | I/O ₁₂ | I/O ₁₃ TCK | V _{CC} | I/O ₄ | I/O ₁ | I/O ₇₈ | I/O ₇₅ | V _{CC} | I/O ₆₇ TDI | I/O ₆₆ |
| D | I/O ₁₄ | NC | I/O ₁₅ | I/O ₁₆ | I/O ₀ | I/O ₇₉ | I/O ₆₃ | I/O ₆₄ | CLK ₃ / I ₄ | I/O ₆₅ |
| E | I/O ₁₇ | CLK ₀ / I ₀ | I/O ₁₈ | I/O ₁₉ | GND | GND | I/O ₆₀ | I/O ₆₁ | CLK ₂ / I ₃ | I/O ₆₂ |
| F | I/O ₂₂ | JTAG EN | I/O ₂₁ | I/O ₂₀ | GND | GND | I/O ₅₉ | I/O ₅₈ | I ₂ | I/O ₅₇ |
| G | I/O ₂₇ | CLK ₁ / I ₁ | I/O ₂₆ | I/O ₂₄ | I/O ₂₃ | I/O ₅₆ | I/O ₅₅ | I/O ₅₄ | NC | I/O ₅₃ |
| H | I/O ₂₈ | I/O ₃₃ TMS | V _{CC} | I/O ₂₅ | I/O ₃₉ | I/O ₄₀ | I/O ₅₂ | V _{CC} | I/O ₄₇ TDO | I/O ₅₁ |
| J | I/O ₂₉ | I/O ₃₂ | I/O ₃₅ | V _{CC} | I/O ₃₈ | I/O ₄₁ | I/O ₄₃ | I/O ₄₅ | I/O ₄₈ | I/O ₅₀ |
| K | I/O ₃₀ | I/O ₃₁ | I/O ₃₄ | I/O ₃₆ | I/O ₃₇ | I/O ₄₂ | I/O ₄₄ | I/O ₄₆ | I/O ₄₉ | NC |

Pin Configurations^[20] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View

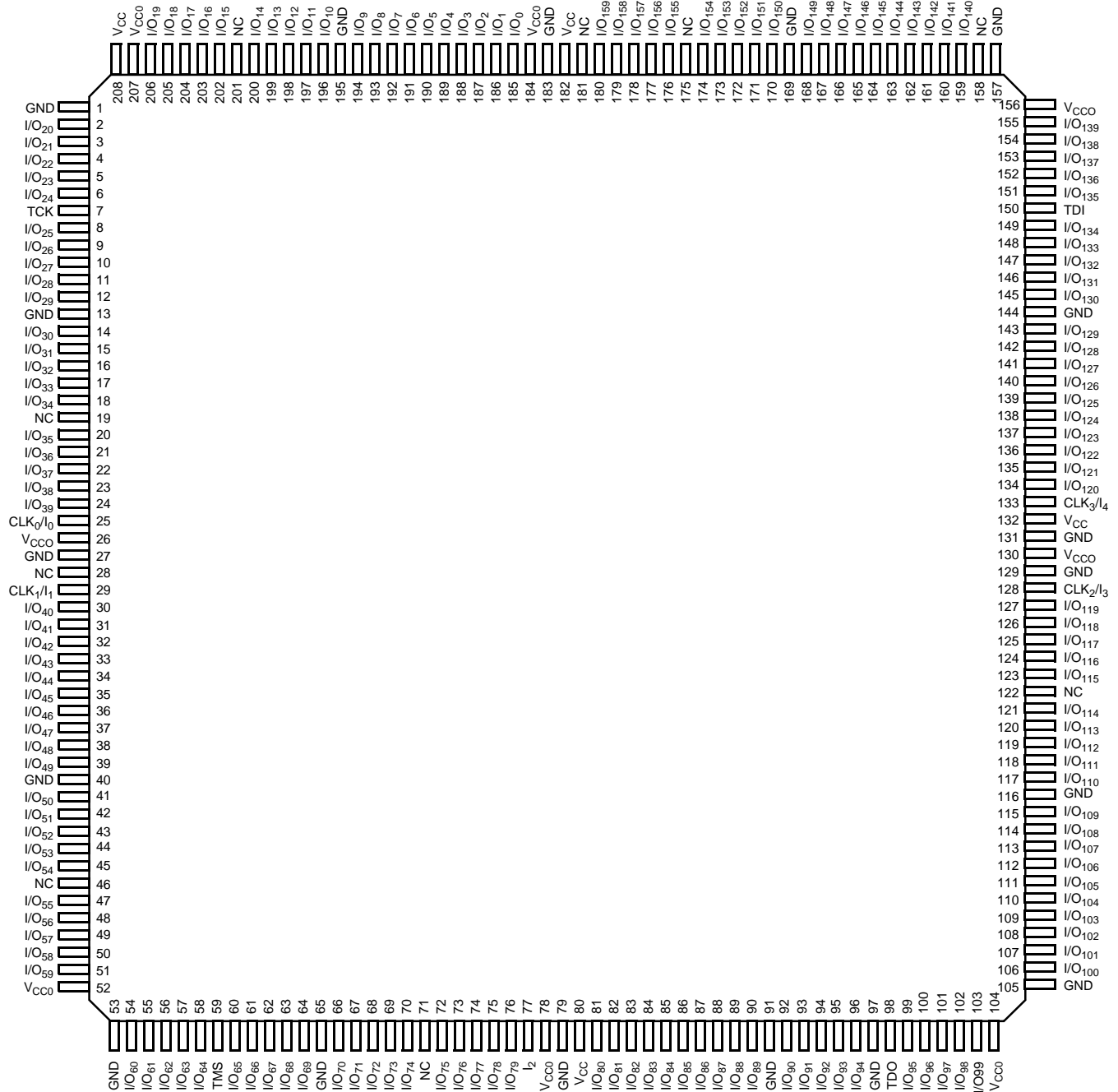


Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) for CY37192(V)
Top View**




Pin Configurations^[20] (continued)

208-Lead PQFP (N208) / CQFP (U208) Top View





Pin Configurations^[20] (continued)

256-Ball PBGA (BG256)
Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | |
|---|-------------------|----------------------------------|----------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|----------------------------------|--------------------|--------------------|---|
| A | GND | I/O ₂₁ | NC | I/O ₁₆ | I/O ₁₂ | I/O ₉ | I/O ₇ | I/O ₄ | I/O ₀ | I/O ₁₉₀ | I/O ₁₈₉ | I/O ₁₈₆ | I/O ₁₈₂ | NC | I/O ₁₇₈ | I/O ₁₇₅ | NC | NC | I/O ₁₆₉ | I/O ₁₆₈ | A |
| B | I/O ₂₃ | I/O ₂₀ | I/O ₁₉ | I/O ₁₈ | I/O ₁₅ | I/O ₁₁ | I/O ₈ | I/O ₅ | I/O ₁ | I/O ₁₉₁ | I/O ₁₈₇ | I/O ₁₈₅ | I/O ₁₈₁ | NC | NC | I/O ₁₇₄ | I/O ₁₇₁ | I/O ₁₇₀ | NC | I/O ₁₆₆ | B |
| C | NC | NC | I/O ₂₂ | NC | I/O ₁₇ | I/O ₁₄ | I/O ₁₀ | I/O ₆ | I/O ₂ | NC | I/O ₁₈₈ | I/O ₁₈₄ | I/O ₁₈₀ | I/O ₁₇₉ | I/O ₁₇₆ | I/O ₁₇₃ | I/O ₁₇₂ | I/O ₁₆₇ | I/O ₁₆₅ | I/O ₁₆₂ | C |
| D | I/O ₂₄ | NC | NC | GND | NC | V _{CCO} | I/O ₁₃ | GND | I/O ₃ | NC | V _{CC} | I/O ₁₈₃ | GND | I/O ₁₇₇ | V _{CCO} | NC | GND | I/O ₁₆₄ | TDI | I/O ₁₆₀ | D |
| E | I/O ₂₇ | I/O ₂₆ | I/O ₂₅ | NC | | | | | | | | | | | | | I/O ₁₆₃ | I/O ₁₆₁ | I/O ₁₅₉ | I/O ₁₅₆ | E |
| F | I/O ₃₀ | TCK | I/O ₂₈ | V _{CCO} | | | | | | | | | | | | | V _{CCO} | I/O ₁₅₈ | NC | I/O ₁₅₄ | F |
| G | I/O ₃₃ | I/O ₃₂ | I/O ₃₁ | I/O ₂₉ | | | | | | | | | | | | | I/O ₁₅₇ | I/O ₁₅₅ | I/O ₁₅₃ | I/O ₁₅₂ | G |
| H | I/O ₃₅ | NC | I/O ₃₄ | GND | | | | | | | | | | | | | GND | I/O ₁₅₁ | I/O ₁₅₀ | I/O ₁₄₉ | H |
| J | I/O ₃₉ | I/O ₃₈ | I/O ₃₇ | I/O ₃₆ | | | | | | | | | | | | | I/O ₁₄₈ | I/O ₁₄₇ | I/O ₁₄₆ | I/O ₁₄₅ | J |
| K | I/O ₄₂ | I/O ₄₀ | I/O ₄₁ | V _{CC} | | | | | | | | | | | | | I/O ₁₄₄ | CLK ₃ /I ₄ | NC | NC | K |
| L | I/O ₄₃ | I/O ₄₄ | I/O ₄₅ | I/O ₄₆ | | | | | | | | | | | | | V _{CC} | CLK ₂ /I ₃ | I/O ₁₄₃ | NC | L |
| M | I/O ₄₇ | CLK ₀ /I ₀ | CLK ₁ /I ₁ | I/O ₄₈ | | | | | | | | | | | | | I/O ₁₃₉ | I/O ₁₄₀ | I/O ₁₄₁ | I/O ₁₄₂ | M |
| N | I/O ₄₉ | I/O ₅₀ | I/O ₅₁ | GND | | | | | | | | | | | | | GND | I/O ₁₃₆ | I/O ₁₃₇ | I/O ₁₃₈ | N |
| P | I/O ₅₂ | I/O ₅₃ | I/O ₅₅ | I/O ₅₈ | | | | | | | | | | | | | I/O ₁₃₁ | I/O ₁₃₃ | I/O ₁₃₄ | I/O ₁₃₅ | P |
| R | I/O ₅₄ | I/O ₅₆ | I/O ₅₉ | V _{CCO} | | | | | | | | | | | | | V _{CCO} | I/O ₁₃₀ | NC | I/O ₁₃₂ | R |
| T | I/O ₅₇ | I/O ₆₀ | I/O ₆₂ | I/O ₆₅ | | | | | | | | | | | | | I/O ₁₂₄ | I/O ₁₂₇ | I/O ₁₂₈ | I/O ₁₂₉ | T |
| U | I/O ₆₁ | I/O ₆₃ | I/O ₆₆ | GND | I/O ₇₆ | V _{CCO} | I/O ₈₂ | GND | I/O ₉₁ | V _{CC} | I/O ₉₈ | I/O ₁₀₂ | GND | I/O ₁₁₂ | V _{CCO} | NC | GND | I/O ₁₂₃ | I/O ₁₂₂ | I/O ₁₂₆ | U |
| V | I/O ₆₄ | I/O ₆₇ | I/O ₆₉ | I/O ₇₅ | I/O ₇₈ | I/O ₈₁ | I/O ₈₅ | I/O ₈₈ | I/O ₉₂ | I ₂ | I/O ₉₇ | I/O ₁₀₁ | I/O ₁₀₅ | I/O ₁₀₉ | I/O ₁₁₃ | TD0 | I/O ₁₁₄ | I/O ₁₁₇ | I/O ₁₂₁ | I/O ₁₂₅ | V |
| W | I/O ₆₈ | I/O ₇₀ | I/O ₇₂ | I/O ₇₄ | I/O ₇₉ | I/O ₈₃ | I/O ₈₆ | I/O ₈₉ | I/O ₉₃ | I/O ₉₅ | I/O ₉₆ | I/O ₁₀₀ | I/O ₁₀₄ | I/O ₁₀₇ | I/O ₁₁₀ | NC | NC | I/O ₁₁₅ | I/O ₁₁₈ | I/O ₁₂₀ | W |
| Y | I/O ₇₁ | I/O ₇₃ | I/O ₇₇ | TMS | I/O ₈₀ | I/O ₈₄ | I/O ₈₇ | I/O ₉₀ | I/O ₉₄ | NC | NC | I/O ₉₉ | I/O ₁₀₃ | I/O ₁₀₆ | I/O ₁₀₈ | I/O ₁₁₁ | NC | NC | I/O ₁₁₆ | I/O ₁₁₉ | Y |



Pin Configurations^[20] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|-------------------|-------------------|-------------------|-------------------|-------------------------------------|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|-------------------------------------|--------------------|--------------------|--------------------|--------------------|
| A | GND | GND | I/O ₂₆ | I/O ₂₄ | I/O ₂₀ | V _{CC} | I/O ₁₁ | GND | GND | I/O ₁₈₆ | V _{CC} | I/O ₁₇₇ | I/O ₁₇₂ | I/O ₁₆₇ | GND | GND |
| B | GND | I/O ₂₇ | I/O ₂₅ | I/O ₂₃ | I/O ₁₉ | I/O ₁₅ | I/O ₁₀ | GND | GND | I/O ₁₈₅ | I/O ₁₈₁ | I/O ₁₇₆ | I/O ₁₇₁ | I/O ₁₆₆ | I/O ₁₆₅ | GND |
| C | I/O ₂₉ | I/O ₂₈ | NC | I/O ₂₂ | I/O ₁₈ | I/O ₁₄ | I/O ₉ | I/O ₄ | I/O ₁₉₁ | I/O ₁₈₄ | I/O ₁₈₀ | I/O ₁₇₅ | I/O ₁₇₀ | NC | I/O ₁₆₃ | I/O ₁₆₄ |
| D | I/O ₃₂ | I/O ₃₁ | I/O ₃₀ | NC | I/O ₁₇ | I/O ₁₃ | I/O ₈ | I/O ₃ | I/O ₁₉₀ | I/O ₁₈₃ | I/O ₁₇₉ | I/O ₁₇₄ | I/O ₁₆₉ | I/O ₁₆₀ | I/O ₁₆₁ | I/O ₁₆₂ |
| E | I/O ₃₅ | I/O ₃₄ | I/O ₃₃ | I/O ₂₁ | I/O ₁₆ | I/O ₁₂ | I/O ₇ | I/O ₂ | I/O ₁₈₉ | V _{CC} | I/O ₁₇₈ | I/O ₁₇₃ | I/O ₁₆₈ | I/O ₁₅₇ | I/O ₁₅₈ | I/O ₁₅₉ |
| F | V _{CC} | I/O ₃₈ | I/O ₃₇ | I/O ₃₆ | TCK | V _{CC} | I/O ₆ | I/O ₁ | I/O ₁₈₈ | I/O ₁₈₂ | V _{CC} | TDI | I/O ₁₅₄ | I/O ₁₅₅ | I/O ₁₅₆ | V _{CC} |
| G | I/O ₄₃ | I/O ₄₂ | I/O ₄₁ | I/O ₄₀ | V _{CC} | I/O ₃₉ | I/O ₅ | I/O ₀ | I/O ₁₈₇ | I/O ₁₄₈ | I/O ₁₄₉ | CLK ₃ /I ₄ | I/O ₁₅₀ | I/O ₁₅₁ | I/O ₁₅₂ | I/O ₁₅₃ |
| H | GND | GND | I/O ₄₇ | I/O ₄₆ | CLK ₀ /I ₀ | I/O ₄₅ | I/O ₄₄ | GND | GND | I/O ₁₄₄ | I/O ₁₄₅ | CLK ₂ /I ₃ | I/O ₁₄₆ | I/O ₁₄₇ | GND | GND |
| J | GND | GND | I/O ₅₁ | I/O ₅₀ | NC | I/O ₄₉ | I/O ₄₈ | GND | GND | I/O ₁₄₀ | I/O ₁₄₁ | I ₂ | I/O ₁₄₂ | I/O ₁₄₃ | GND | GND |
| K | I/O ₅₇ | I/O ₅₆ | I/O ₅₅ | I/O ₅₄ | CLK ₁ /I ₁ | I/O ₅₃ | I/O ₅₂ | I/O ₉₁ | I/O ₉₆ | I/O ₁₀₁ | I/O ₁₃₅ | V _{CC} | I/O ₁₃₆ | I/O ₁₃₇ | I/O ₁₃₈ | I/O ₁₃₉ |
| L | V _{CC} | I/O ₆₀ | I/O ₅₉ | I/O ₅₈ | TMS | V _{CC} | I/O ₈₆ | I/O ₉₂ | I/O ₉₇ | I/O ₁₀₂ | V _{CC} | TDO | I/O ₁₃₂ | I/O ₁₃₃ | I/O ₁₃₄ | V _{CC} |
| M | I/O ₆₃ | I/O ₆₂ | I/O ₆₁ | I/O ₇₂ | I/O ₇₇ | I/O ₈₂ | V _{CC} | I/O ₉₃ | I/O ₉₈ | I/O ₁₀₃ | I/O ₁₀₈ | I/O ₁₁₂ | I/O ₁₁₇ | I/O ₁₂₉ | I/O ₁₃₀ | I/O ₁₃₁ |
| N | I/O ₆₆ | I/O ₆₅ | I/O ₆₄ | I/O ₇₃ | I/O ₇₈ | I/O ₈₃ | I/O ₈₇ | I/O ₉₄ | I/O ₉₉ | I/O ₁₀₄ | I/O ₁₀₉ | I/O ₁₁₃ | NC | I/O ₁₂₆ | I/O ₁₂₇ | I/O ₁₂₈ |
| P | I/O ₆₈ | I/O ₆₇ | NC | I/O ₇₄ | I/O ₇₉ | I/O ₈₄ | I/O ₈₈ | I/O ₉₅ | I/O ₁₀₀ | I/O ₁₀₅ | I/O ₁₁₀ | I/O ₁₁₄ | I/O ₁₁₈ | NC | I/O ₁₂₄ | I/O ₁₂₅ |
| R | GND | I/O ₆₉ | I/O ₇₀ | I/O ₇₅ | I/O ₈₀ | I/O ₈₅ | I/O ₈₉ | GND | GND | I/O ₁₀₆ | I/O ₁₁₁ | I/O ₁₁₅ | I/O ₁₁₉ | I/O ₁₂₁ | I/O ₁₂₃ | GND |
| T | GND | GND | I/O ₇₁ | I/O ₇₆ | I/O ₈₁ | V _{CC} | I/O ₉₀ | GND | GND | I/O ₁₀₇ | V _{CC} | I/O ₁₁₆ | I/O ₁₂₀ | I/O ₁₂₂ | GND | GND |



Ultra37000 CPLD Family

Pin Configurations^[20] (continued)

352-Lead BGA (BG352)

Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|----|--------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| A | GND | GND | I/O ₁₉ | I/O ₁₅ | I/O ₁₃ | I/O ₃₄ | I/O ₃₁ | I/O ₂₈ | I/O ₂₅ | I/O ₁₀ | I/O ₇ | I/O ₄ | I/O ₁ | I/O ₂₆₃ | I/O ₂₆₀ | I/O ₂₅₇ | I/O ₂₅₄ | I/O ₂₃₉ | I/O ₂₃₇ | I/O ₂₃₂ | I/O ₂₂₉ | I/O ₂₅₀ | I/O ₂₄₈ | I/O ₂₄₄ | GND | GND |
| B | GND | NC | I/O ₁₈ | I/O ₁₇ | I/O ₁₄ | I/O ₃₅ | I/O ₃₂ | I/O ₂₉ | I/O ₂₆ | I/O ₁₁ | I/O ₈ | I/O ₅ | I/O ₂ | V _{CC} | I/O ₂₆₁ | I/O ₂₅₈ | I/O ₂₅₅ | I/O ₂₅₂ | I/O ₂₃₄ | I/O ₂₃₁ | I/O ₂₂₈ | I/O ₂₄₉ | I/O ₂₄₆ | I/O ₂₄₅ | I/O ₂₄₀ | GND |
| C | I/O ₂₃ | I/O ₃₈ | I/O ₃₇ | I/O ₁₆ | I/O ₁₂ | I/O ₃₃ | I/O ₃₀ | I/O ₂₇ | I/O ₂₄ | I/O ₉ | I/O ₆ | I/O ₃ | I/O ₀ | I/O ₂₆₂ | I/O ₂₅₉ | I/O ₂₅₆ | I/O ₂₅₃ | I/O ₂₃₈ | I/O ₂₃₅ | I/O ₂₃₃ | I/O ₂₃₀ | I/O ₂₅₁ | I/O ₂₄₇ | I/O ₂₂₅ | I/O ₂₂₄ | I/O ₂₂₇ |
| D | I/O ₃₉ | I/O ₄₀ | I/O ₃₆ | NC | NC | I/O ₂₁ | I/O ₂₀ | V _{CCO} | V _{CCO} | NC | GND | GND | V _{CCO} | V _{CCO} | GND | GND | NC | V _{CCO} | V _{CCO} | I/O ₂₃₆ | I/O ₂₄₃ | NC | NC | I/O ₂₂₆ | I/O ₂₂₂ | I/O ₂₂₃ |
| E | I/O ₄₂ | TCK | I/O ₄₁ | NC | | | | | | | | | | | | | | | | | | | NC | TDI | I/O ₂₂₁ | I/O ₂₂₀ |
| F | I/O ₄₅ | I/O ₄₄ | I/O ₄₃ | I/O ₂₂ | | | | | | | | | | | | | | | | | | | I/O ₂₄₂ | I/O ₂₁₉ | I/O ₂₁₈ | I/O ₂₁₇ |
| G | I/O ₄₈ | I/O ₄₇ | I/O ₄₆ | I/O ₆₃ | | | | | | | | | | | | | | | | | | | I/O ₂₄₁ | I/O ₂₁₆ | I/O ₂₁₅ | I/O ₂₁₄ |
| H | I/O ₄₉ | I/O ₅₀ | I/O ₅₁ | V _{CCO} | | | | | | | | | | | | | | | | | | | V _{CCO} | I/O ₂₁₁ | I/O ₂₁₂ | I/O ₂₁₃ |
| J | I/O ₅₂ | I/O ₅₃ | I/O ₅₄ | V _{CCO} | | | | | | | | | | | | | | | | | | | V _{CCO} | I/O ₂₀₈ | I/O ₂₀₉ | I/O ₂₁₀ |
| K | I/O ₅₅ | I/O ₅₆ | I/O ₅₇ | NC | | | | | | | | | | | | | | | | | | | NC | I/O ₂₀₅ | I/O ₂₀₆ | I/O ₂₀₇ |
| L | I0 | I/O ₅₉ | I/O ₅₈ | GND | GND | | | | | | GND | | | | | | GND | | | | | | GND | I/O ₂₀₄ | I4 | I/O ₁₉₇ |
| M | I/O ₆₁ | I/O ₆₀ | I1 | GND | GND | | | | | | GND | | | | | | GND | | | | | | GND | I3 | I/O ₂₀₃ | I/O ₂₀₂ |
| N | I/O ₆₄ | V _{CC} | I/O ₆₂ | V _{CCO} | GND | | | | | | GND | | | | | | GND | | | | | | V _{CCO} | I/O ₂₀₁ | I/O ₂₀₀ | I/O ₁₉₉ |
| P | I/O ₆₅ | I/O ₆₆ | I/O ₆₇ | V _{CCO} | GND | | | | | | GND | | | | | | GND | | | | | | V _{CCO} | I/O ₁₉₆ | V _{CC} | I/O ₁₉₈ |
| R | I/O ₆₈ | I/O ₆₉ | I/O ₇₀ | GND | GND | | | | | | GND | | | | | | GND | | | | | | GND | I/O ₁₉₃ | I/O ₁₉₄ | I/O ₁₉₅ |
| T | I/O ₇₁ | I/O ₈₄ | I/O ₈₅ | GND | GND | | | | | | GND | | | | | | GND | | | | | | GND | I/O ₁₇₈ | I/O ₁₇₉ | I/O ₁₉₂ |
| U | I/O ₈₈ | I/O ₈₇ | I/O ₈₆ | NC | | | | | | | | | | | | | | | | | | | NC | I/O ₁₇₇ | I/O ₁₇₆ | I/O ₁₇₅ |
| V | I/O ₉₁ | I/O ₉₀ | I/O ₈₉ | V _{CCO} | | | | | | | | | | | | | | | | | | | V _{CCO} | I/O ₁₇₄ | I/O ₁₇₃ | I/O ₁₇₂ |
| W | I/O ₉₄ | I/O ₉₃ | I/O ₉₂ | V _{CCO} | | | | | | | | | | | | | | | | | | | V _{CCO} | I/O ₁₇₁ | I/O ₁₇₀ | I/O ₁₆₉ |
| Y | I/O ₉₅ | I/O ₇₂ | I/O ₇₃ | I/O ₁₁₀ | | | | | | | | | | | | | | | | | | | I/O ₁₅₃ | I/O ₁₉₀ | I/O ₁₉₁ | I/O ₁₆₈ |
| AA | I/O ₇₄ | I/O ₇₅ | I/O ₇₆ | I/O ₁₁₁ | | | | | | | | | | | | | | | | | | | I/O ₁₅₂ | I/O ₁₈₇ | I/O ₁₈₈ | I/O ₁₈₉ |
| AB | I/O ₇₇ | I/O ₇₈ | I/O ₇₉ | N/C | | | | | | | | | | | | | | | | | | | NC | I/O ₁₈₄ | I/O ₁₈₅ | I/O ₁₈₆ |
| AC | I/O ₈₁ | I/O ₈₀ | I/O ₁₀₈ | N/C | NC | I/O ₁₁₂ | I/O ₁₁₃ | V _{CCO} | V _{CCO} | NC | GND | GND | V _{CCO} | V _{CCO} | GND | GND | NC | V _{CCO} | V _{CCO} | I/O ₁₅₀ | I/O ₁₅₁ | NC | NC | I/O ₁₅₅ | I/O ₁₈₃ | I/O ₁₈₂ |
| AD | I/O ₁₀₉ | I/O ₈₂ | I/O ₈₃ | I/O ₁₁₇ | I/O ₉₇ | I/O ₁₀₀ | I/O ₁₀₂ | I/O ₁₀₅ | I/O ₁₂₀ | I/O ₁₂₃ | I/O ₁₂₆ | I/O ₁₂₉ | I2 | I/O ₁₃₃ | I/O ₁₃₆ | I/O ₁₃₉ | I/O ₁₄₂ | I/O ₁₅₇ | I/O ₁₅₉ | I/O ₁₆₁ | I/O ₁₆₃ | I/O ₁₆₆ | I/O ₁₄₆ | I/O ₁₈₀ | I/O ₁₈₁ | I/O ₁₅₄ |
| AE | GND | NC | I/O ₁₁₅ | I/O ₁₁₆ | I/O ₁₁₉ | I/O ₉₈ | I/O ₁₀₁ | I/O ₁₀₃ | I/O ₁₀₆ | I/O ₁₂₁ | I/O ₁₂₄ | I/O ₁₂₇ | V _{CC} | I/O ₁₃₀ | I/O ₁₃₄ | I/O ₁₃₇ | I/O ₁₄₀ | I/O ₁₄₃ | I/O ₁₆₀ | I/O ₁₆₂ | I/O ₁₆₅ | I/O ₁₄₄ | I/O ₁₄₇ | I/O ₁₄₈ | NC | GND |
| AF | GND | GND | I/O ₁₁₄ | I/O ₁₁₈ | I/O ₉₆ | I/O ₉₉ | TMS | I/O ₁₀₄ | I/O ₁₀₇ | I/O ₁₂₂ | I/O ₁₂₅ | I/O ₁₂₈ | I/O ₁₃₁ | I/O ₁₃₂ | I/O ₁₃₅ | I/O ₁₃₈ | I/O ₁₄₁ | I/O ₁₅₆ | I/O ₁₅₈ | TDO | I/O ₁₆₄ | I/O ₁₆₇ | I/O ₁₄₅ | I/O ₁₄₉ | GND | GND |

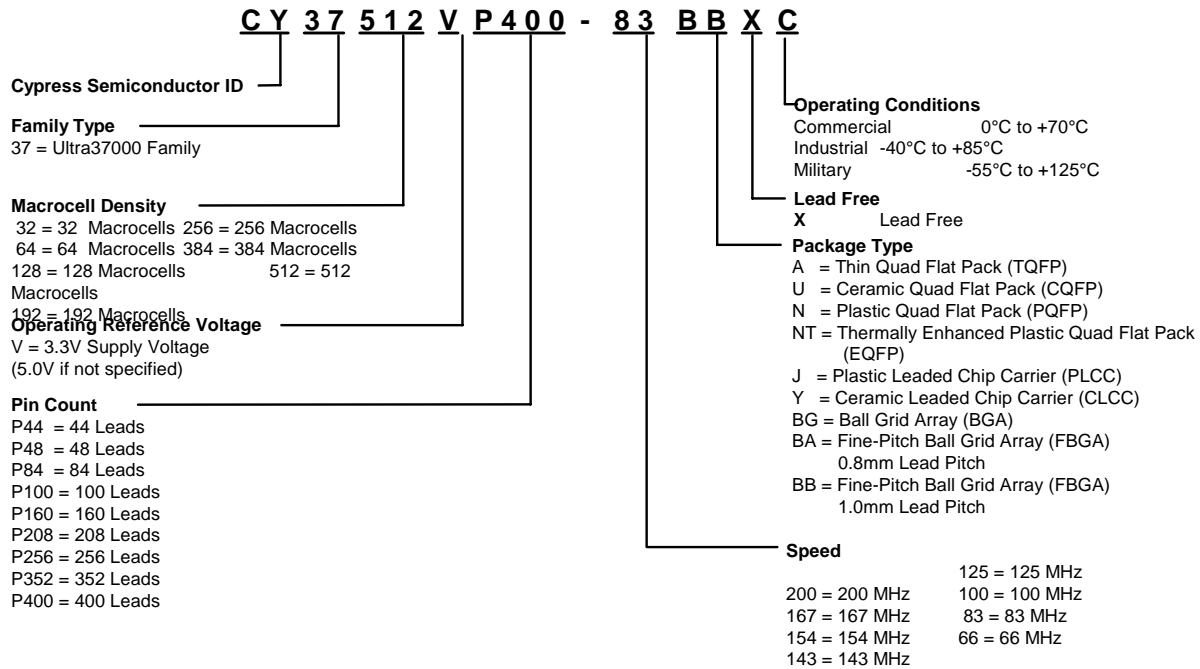


Pin Configurations^[20] (continued)

400-Ball Fine-Pitch BGA (BB400)
Top View

| | | | | | | | | | | | | | | | | | | | | |
|---|-------------------|-------------------|--------------------|--------------------|--------------------|--------------------|-------------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------------------------------------|------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| A | GND | GND | NC | I/O ₁₇ | I/O ₁₆ | I/O ₁₄ | I/O ₂₉ | V _{CC} | I/O ₁₁ | GND | GND | I/O ₂₅₇ | V _{CC} | I/O ₂₃₉ | I/O ₂₃₃ | I/O ₂₃₂ | I/O ₂₃₀ | NC | GND | GND |
| B | GND | GND | GND | NC | I/O ₁₅ | I/O ₁₃ | I/O ₂₈ | V _{CC} | I/O ₁₀ | GND | GND | I/O ₂₅₆ | V _{CC} | I/O ₂₃₈ | I/O ₂₃₁ | I/O ₂₂₉ | NC | GND | GND | GND |
| C | NC | GND | GND | GND | I/O ₂₀ | I/O ₁₂ | I/O ₂₇ | V _{CC} | I/O ₉ | GND | GND | I/O ₂₅₅ | V _{CC} | I/O ₂₃₇ | I/O ₂₂₈ | I/O ₂₄₅ | GND | GND | GND | NC |
| D | I/O ₄₄ | NC | GND | I/O ₂₁ | I/O ₁₉ | I/O ₁₈ | I/O ₂₆ | I/O ₂₅ | I/O ₈ | GND | GND | I/O ₂₅₄ | I/O ₂₃₅ | I/O ₂₃₆ | I/O ₂₅₁ | I/O ₂₄₄ | I/O ₂₄₃ | GND | NC | I/O ₂₂₇ |
| E | I/O ₄₆ | I/O ₄₃ | I/O ₂₃ | I/O ₂₂ | NC | I/O ₃₅ | I/O ₃₄ | I/O ₂₄ | I/O ₇ | I/O ₄ | I/O ₂₆₃ | I/O ₂₅₃ | I/O ₂₃₄ | I/O ₂₅₀ | I/O ₂₄₈ | NC | I/O ₂₄₁ | I/O ₂₄₂ | I/O ₂₂₅ | I/O ₂₂₆ |
| F | I/O ₄₇ | I/O ₄₅ | I/O ₄₂ | I/O ₄₁ | I/O ₄₀ | NC | I/O ₃₃ | I/O ₃₂ | I/O ₆ | I/O ₃ | I/O ₂₆₂ | I/O ₂₅₂ | I/O ₂₄₉ | I/O ₂₄₇ | I/O ₂₂₀ | I/O ₂₂₁ | I/O ₂₄₀ | I/O ₂₂₂ | I/O ₂₂₃ | I/O ₂₂₄ |
| G | I/O ₅₃ | I/O ₅₂ | I/O ₅₁ | I/O ₅₀ | I/O ₃₉ | I/O ₃₈ | I/O ₃₇ | I/O ₃₁ | I/O ₅ | I/O ₂ | I/O ₂₆₁ | V _{CC} | I/O ₂₄₆ | I/O ₂₁₇ | I/O ₂₁₈ | I/O ₂₁₉ | I/O ₂₁₂ | I/O ₂₁₃ | I/O ₂₁₄ | I/O ₂₁₅ |
| H | V _{CC} | V _{CC} | V _{CC} | I/O ₄₉ | I/O ₄₈ | I/O ₃₆ | TCK | V _{CC} | I/O ₃₀ | I/O ₁ | I/O ₂₅₉ | I/O ₂₆₀ | V _{CC} | TDI | I/O ₂₁₆ | I/O ₂₁₀ | I/O ₂₁₁ | V _{CC} | V _{CC} | V _{CC} |
| J | I/O ₅₉ | I/O ₅₈ | I/O ₅₇ | I/O ₅₆ | I/O ₅₅ | I/O ₅₄ | V _{CC} | I/O ₆₂ | I/O ₆₀ | I/O ₀ | I/O ₂₅₈ | I/O ₂₀₂ | I/O ₂₀₃ | CLK ₃ /I ₄ | I/O ₂₀₄ | I/O ₂₀₅ | I/O ₂₀₆ | I/O ₂₀₇ | I/O ₂₀₈ | I/O ₂₀₉ |
| K | GND | GND | GND | GND | I/O ₆₅ | I/O ₆₄ | CLK ₀ /I ₀ | I/O ₆₃ | I/O ₆₁ | GND | GND | I/O ₁₉₈ | I/O ₁₉₉ | CLK ₂ /I ₃ | I/O ₂₀₀ | I/O ₂₀₁ | GND | GND | GND | GND |
| L | GND | GND | GND | GND | I/O ₆₉ | I/O ₆₈ | NC | I/O ₆₇ | I/O ₆₆ | GND | GND | I/O ₁₉₃ | I/O ₁₉₅ | I ₂ | I/O ₁₉₆ | I/O ₁₉₇ | GND | GND | GND | GND |
| M | I/O ₈₉ | I/O ₈₈ | I/O ₈₇ | I/O ₈₆ | I/O ₈₅ | I/O ₈₄ | CLK ₁ /I ₁ | I/O ₇₁ | I/O ₇₀ | I/O ₁₂₆ | I/O ₁₃₂ | I/O ₁₉₂ | I/O ₁₉₄ | V _{CC} | I/O ₁₇₄ | I/O ₁₇₅ | I/O ₁₇₆ | I/O ₁₇₇ | I/O ₁₇₈ | I/O ₁₇₉ |
| N | V _{CC} | V _{CC} | V _{CC} | I/O ₉₁ | I/O ₉₀ | I/O ₇₂ | TMS | V _{CC} | I/O ₁₂₈ | I/O ₁₂₇ | I/O ₁₃₃ | I/O ₁₆₂ | V _{CC} | TDO | I/O ₁₈₀ | I/O ₁₆₈ | I/O ₁₆₉ | V _{CC} | V _{CC} | V _{CC} |
| P | I/O ₉₅ | I/O ₉₄ | I/O ₉₃ | I/O ₉₂ | I/O ₇₅ | I/O ₇₄ | I/O ₇₃ | I/O ₁₁₄ | V _{CC} | I/O ₁₂₉ | I/O ₁₃₄ | I/O ₁₃₇ | I/O ₁₆₃ | I/O ₁₈₁ | I/O ₁₈₂ | I/O ₁₈₃ | I/O ₁₇₀ | I/O ₁₇₁ | I/O ₁₇₂ | I/O ₁₇₃ |
| R | I/O ₉₀ | I/O ₇₉ | I/O ₇₈ | I/O ₁₀₈ | I/O ₇₇ | I/O ₇₆ | I/O ₁₁₅ | I/O ₁₁₇ | I/O ₁₂₀ | I/O ₁₃₀ | I/O ₁₃₅ | I/O ₁₃₈ | I/O ₁₆₄ | I/O ₁₆₅ | NC | I/O ₁₈₄ | I/O ₁₈₅ | I/O ₁₈₆ | I/O ₁₈₉ | I/O ₁₉₁ |
| T | I/O ₈₂ | I/O ₈₁ | I/O ₁₁₀ | I/O ₁₀₉ | NC | I/O ₁₁₆ | I/O ₁₁₈ | I/O ₁₀₂ | I/O ₁₂₁ | I/O ₁₃₁ | I/O ₁₃₆ | I/O ₁₃₉ | I/O ₁₅₆ | I/O ₁₆₆ | I/O ₁₆₇ | NC | I/O ₁₅₄ | I/O ₁₅₅ | I/O ₁₈₇ | I/O ₁₉₀ |
| U | I/O ₈₃ | NC | GND | I/O ₁₁₁ | I/O ₁₁₂ | I/O ₁₁₉ | I/O ₁₀₄ | I/O ₁₀₃ | I/O ₁₂₂ | GND | GND | I/O ₁₄₀ | I/O ₁₅₇ | I/O ₁₅₈ | I/O ₁₅₀ | I/O ₁₅₁ | I/O ₁₅₃ | GND | NC | I/O ₁₈₈ |
| V | NC | GND | GND | GND | I/O ₁₁₃ | I/O ₉₆ | I/O ₁₀₅ | V _{CC} | I/O ₁₂₃ | GND | GND | I/O ₁₄₁ | V _{CC} | I/O ₁₅₉ | I/O ₁₄ 4 | I/O ₁₅₂ | GND | GND | GND | NC |
| W | GND | GND | GND | NC | I/O ₉₇ | I/O ₉₉ | I/O ₁₀₆ | V _{CC} | I/O ₁₂₄ | GND | GND | I/O ₁₄₂ | V _{CC} | I/O ₁₆₀ | I/O ₁₄₅ | I/O ₁₄₇ | NC | GND | GND | GND |
| Y | GND | GND | NC | I/O ₉₈ | I/O ₁₀₀ | I/O ₁₀₁ | I/O ₁₀₇ | V _{CC} | I/O ₁₂₅ | GND | GND | I/O ₁₄₃ | V _{CC} | I/O ₁₆₁ | I/O ₁₄₆ | I/O ₁₄₈ | I/O ₁₄₉ | NC | GND | GND |

Ordering Information



5.0V Ordering Information

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | |
|-------------|-------------|-------------------|-------------------|---|---|------------|
| 32 | 200 | CY37032P44-200AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial | |
| | | CY37032P44-200AXC | A44 | 44-Lead Lead Free Thin Quad Flat Pack | | |
| | | CY37032P44-200JC | J67 | 44-Lead Plastic Leaded Chip Carrier | | |
| | | CY37032P44-200JXC | J67 | 44-Lead Lead Free Plastic Leaded Chip Carrier | | |
| 154 | 154 | CY37032P44-154AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial | |
| | | CY37032P44-154JC | J67 | 44-Lead Plastic Leaded Chip Carrier | | |
| | 125 | 125 | CY37032P44-154AI | A44 | 44-Lead Thin Quad Flat Pack | Industrial |
| | | | CY37032P44-154AXI | A44 | 44-Lead Lead Free Thin Quad Flat Pack | |
| | | | CY37032P44-154JI | J67 | 44-Lead Plastic Leaded Chip Carrier | |
| | | | CY37032P44-154JXI | J67 | 44-Lead Lead Free Plastic Leaded Chip Carrier | |
| 125 | 125 | CY37032P44-125AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial | |
| | | CY37032P44-125AXC | A44 | 44-Lead Lead Free Thin Quad Flat Pack | | |
| | | CY37032P44-125JC | J67 | 44-Lead Plastic Leaded Chip Carrier | | |
| | | CY37032P44-125JXC | J67 | 44-Lead Lead Free Plastic Leaded Chip Carrier | | |
| | 125 | 125 | CY37032P44-125AI | A44 | 44-Lead Thin Quad Flat Pack | Industrial |
| | | | CY37032P44-125JI | J67 | 44-Lead Plastic Leaded Chip Carrier | |


5.0V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | |
|--------------------|-----------------|--|---------------------------------------|---|---|------------|
| 64 | 200 | CY37064P44-200AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial | |
| | | CY37064P44-200AXC | A44 | 44-Lead Lead Free Thin Quad Flat Pack | | |
| | | CY37064P44-200JC | J67 | 44-Lead Plastic Ledged Chip Carrier | | |
| | | CY37064P44-200JXC | J67 | 44-Lead Lead Free Plastic Ledged Chip Carrier | | |
| | | CY37064P84-200JC | J83 | 84-Lead Plastic Ledged Chip Carrier | | |
| | | CY37064P100-200AC | A100 | 100-Lead Thin Quad Flat Pack | | |
| | | CY37064P100-200AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | |
| 64 | 154 | CY37064P44-154AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial | |
| | | CY37064P44-154JC | J67 | 44-Lead Plastic Ledged Chip Carrier | | |
| | | CY37064P84-154JC | J83 | 84-Lead Plastic Ledged Chip Carrier | | |
| | | CY37064P100-154AC | A100 | 100-Lead Thin Quad Flat Pack | Industrial | |
| | | CY37064P44-154AI | A44 | 44-Lead Thin Quad Flat Pack | | |
| | | CY37064P44-154AXI | A44 | 44-Lead Lead Free Thin Quad Flat Pack | | |
| | | CY37064P44-154JI | J67 | 44-Lead Plastic Ledged Chip Carrier | | |
| | | CY37064P44-154JXI | J67 | 44-Lead Lead Free Plastic Ledged Chip Carrier | | |
| | | CY37064P84-154JI | J83 | 84-Lead Plastic Ledged Chip Carrier | | |
| | | CY37064P100-154AI | A100 | 100-Lead Thin Quad Flat Pack | | |
| | 5962-9951902QYA | Y67 | 44-Lead Ceramic Leadless Chip Carrier | Military | | |
| | 125 | 125 | CY37064P44-125AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial |
| | | | CY37064P44-125AXC | A44 | 44-Lead Lead Free Thin Quad Flat Pack | |
| | | | CY37064P44-125JC | J67 | 44-Lead Plastic Ledged Chip Carrier | |
| | | | CY37064P44-125JXC | J67 | 44-Lead Lead Free Plastic Ledged Chip Carrier | Industrial |
| | | | CY37064P84-125JC | J83 | 84-Lead Plastic Ledged Chip Carrier | |
| | | | CY37064P100-125AC | A100 | 100-Lead Thin Quad Flat Pack | |
| CY37064P100-125AXC | | | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | |
| CY37064P44-125AI | | | A44 | 44-Lead Thin Quad Flat Pack | | |
| CY37064P44-125AXI | | | A44 | 44-Lead Lead Free Thin Quad Flat Pack | | |
| CY37064P44-125JI | | | J67 | 44-Lead Plastic Ledged Chip Carrier | | |
| CY37064P84-125JI | J83 | 84-Lead Plastic Ledged Chip Carrier | | | | |
| CY37064P100-125AI | A100 | 100-Lead Thin Quad Flat Pack | Military | | | |
| CY37064P100-125AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | | | |
| | | 5962-9951901QYA | Y67 | 44-Lead Ceramic Leadless Chip Carrier | | |

5.0V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | | |
|-------------|-------------|--------------------|--------------------|---|---|---|------------|
| 128 | 167 | CY37128P84-167JC | J83 | 84-Lead Plastic Leaded Chip Carrier | Commercial | | |
| | | CY37128P84-167JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | | | |
| | | CY37128P100-167AC | A100 | 100-Lead Thin Quad Flat Pack | | | |
| | | CY37128P100-167AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | | |
| | | CY37128P160-167AC | A160 | 160-Lead Thin Quad Flat Pack | | | |
| | | CY37128P160-167AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | |
| | 125 | 125 | CY37128P84-125JC | J83 | 84-Lead Plastic Leaded Chip Carrier | Commercial | |
| | | | CY37128P84-125JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | | |
| | | | CY37128P100-125AC | A100 | 100-Lead Thin Quad Flat Pack | | |
| | | | CY37128P100-125AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | |
| | | | CY37128P160-125AC | A160 | 160-Lead Thin Quad Flat Pack | | |
| | | | CY37128P160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | |
| | | 125 | 125 | CY37128P84-125JI | J83 | 84-Lead Plastic Leaded Chip Carrier | Industrial |
| | | | | CY37128P84-125JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | | | | CY37128P100-125AI | A100 | 100-Lead Thin Quad Flat Pack | |
| | | | | CY37128P100-125AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | | | CY37128P160-125AI | A160 | 160-Lead Thin Quad Flat Pack | |
| | | | | CY37128P160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | 100 | 100 | 5962-9952102QYA | Y84 | 84-Lead Ceramic Leaded Chip Carrier | Military | |
| | | | CY37128P84-100JC | J83 | 84-Lead Plastic Leaded Chip Carrier | | |
| | | | CY37128P84-100JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | | |
| | | | CY37128P100-100AC | A100 | 100-Lead Thin Quad Flat Pack | | |
| | | | CY37128P100-100AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | |
| | | | CY37128P160-100AC | A160 | 160-Lead Thin Quad Flat Pack | | |
| 100 | | 100 | CY37128P160-100AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | Industrial | |
| | | | CY37128P84-100JI | J83 | 84-Lead Plastic Leaded Chip Carrier | | |
| | | | CY37128P100-100AI | A100 | 100-Lead Thin Quad Flat Pack | | |
| | | | CY37128P100-100AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | |
| | | | CY37128P160-100AI | A160 | 160-Lead Thin Quad Flat Pack | | |
| | | | 5962-9952101QYA | Y84 | 84-Lead Ceramic Leaded Chip Carrier | | Military |
| 192 | 154 | CY37192P160-154AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial | | |
| | | CY37192P160-154AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | |
| | 125 | 125 | CY37192P160-125AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial | |
| | | | CY37192P160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | |
| | | | CY37192P160-125AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial | |
| | | | CY37192P160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | |
| | 83 | 83 | CY37192P160-83AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial | |
| | | | CY37192P160-83AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | |
| | | | CY37192P160-83AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial | |
| | | | CY37192P160-83AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | |


5.0V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------------|-----------------|---------------------------------|---------------------------------|--|-----------------|
| 256 | 154 | CY37256P160-154AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37256P160-154AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37256P208-154NC | N208 | 208-Lead Plastic Quad Flat Pack | |
| | | CY37256P256-154BGC | BG256 | 256-Ball Ball Grid Array | |
| | 125 | CY37256P160-125AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37256P160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37256P208-125NC | N208 | 208-Lead Plastic Quad Flat Pack | |
| | | CY37256P256-125BGC | BG256 | 256-Ball Ball Grid Array | |
| | | CY37256P160-125AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial |
| | | CY37256P160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37256P208-125NI | N208 | 208-Lead Plastic Quad Flat Pack | |
| | | CY37256P256-125BGI | BG256 | 256-Ball Ball Grid Array | |
| | 5962-9952302QZC | U162 | 160-Lead Ceramic Quad Flat Pack | Military | |
| | 83 | CY37256P160-83AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37256P160-83AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37256P208-83NC | N208 | 208-Lead Plastic Quad Flat Pack | |
| | | CY37256P256-83BGC | BG256 | 256-Ball Ball Grid Array | |
| | | CY37256P160-83AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial |
| | | CY37256P160-83AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37256P208-83NI | N208 | 208-Lead Plastic Quad Flat Pack | |
| CY37256P256-83BGI | | BG256 | 256-Ball Ball Grid Array | | |
| 5962-9952301QZC | U162 | 160-Lead Ceramic Quad Flat Pack | Military | | |
| 384 | 125 | CY37384P208-125NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial |
| | | CY37384P256-125BGC | BG256 | 256-Ball Ball Grid Array | |
| | 83 | CY37384P208-83NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial |
| | | CY37384P256-83BGC | BG256 | 256-Ball Ball Grid Array | |
| | | CY37384P208-83NI | N208 | 208-Lead Plastic Quad Flat Pack | Industrial |
| | | CY37384P256-83BGI | BG256 | 256-Ball Ball Grid Array | |

5.0V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | |
|-------------------|-------------|--------------------|--------------------|---------------------------------|---------------------------------|---------------------------------|
| 512 | 125 | CY37512P208-125NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial | |
| | | CY37512P256-125BGC | BG256 | 256-Ball Ball Grid Array | | |
| | | CY37512P352-125BGC | BG352 | 352-Ball Ball Grid Array | | |
| | 100 | 100 | CY37512P208-100NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial |
| | | | CY37512P256-100BGC | BG256 | 256-Ball Ball Grid Array | |
| | | | CY37512P352-100BGC | BG352 | 352-Ball Ball Grid Array | |
| | | Industrial | | CY37512P208-100NI | N208 | 208-Lead Plastic Quad Flat Pack |
| | | | | CY37512P256-100BGI | BG256 | 256-Ball Ball Grid Array |
| | | | | CY37512P352-100BGI | BG352 | 352-Ball Ball Grid Array |
| | | | | 5962-9952502QZC | U208 | 208-Lead Ceramic Quad Flat Pack |
| | 83 | 83 | CY37512P208-83NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial |
| | | | CY37512P256-83BGC | BG256 | 256-Ball Ball Grid Array | |
| | | | CY37512P352-83BGC | BG352 | 352-Ball Ball Grid Array | |
| | | Industrial | | CY37512P208-83NI | N208 | 208-Lead Plastic Quad Flat Pack |
| | | | | CY37512P256-83BGI | BG256 | 256-Ball Ball Grid Array |
| CY37512P352-83BGI | | | | BG352 | 352-Ball Ball Grid Array | |
| 5962-9952501QZC | | | | U208 | 208-Lead Ceramic Quad Flat Pack | Military |

3.3V Ordering Information

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | |
|-------------|-------------|--------------------|--------------------|---------------------------------------|---------------------------------------|---|
| 32 | 143 | CY37032VP44-143AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial | |
| | | CY37032VP44-143AXC | A44 | 44-Lead Lead Free Thin Quad Flat Pack | | |
| | | CY37032VP48-143BAC | BA50 | 48-Ball Fine Pitch Ball Grid Array | | |
| | 100 | 100 | CY37032VP44-100AC | A44 | 44-Lead Thin Quad Flat Pack | Commercial |
| | | | CY37032VP44-100AXC | A44 | 44-Lead Lead Free Thin Quad Flat Pack | |
| | | | CY37032VP48-100BAC | BA50 | 48-Ball Fine Pitch Ball Grid Array | |
| | | Industrial | | CY37032VP44-100AI | A44 | 44-Lead Thin Quad Flat Pack |
| | | | | CY37032VP44-100AXI | A44 | 44-Lead Lead Free Thin Quad Flat Pack |
| | | | | CY37032VP48-100BAI | BA50 | 48-Ball Fine Pitch Ball Grid Array |
| | | | | CY37032VP44-100JI | J67 | 44-Lead Plastic Leaded Chip Carrier |
| | | | | CY37032VP44-100JXI | J67 | 44-Lead Lead Free Plastic Leaded Chip Carrier |

3.3V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | | | |
|---------------------|--------------------|---------------------|---------------------|--|--|--|--|------------------------------|
| 64 | 143 | CY37064VP44-143AC | A44 | 44-Lead Thin Quad Flatpack | Commercial | | | |
| | | CY37064VP44-143AXC | A44 | 44-Lead Lead Free Thin Quad Flatpack | | | | |
| | | CY37064VP48-143BAC | BA50 | 48-Ball Fine-Pitch Ball Grid Array | | | | |
| | | CY37064VP100-143AC | A100 | 100-Lead Thin Quad Flatpack | | | | |
| | | CY37064VP100-143AXC | A100 | 100-Lead Lead Free Thin Quad Flatpack | | | | |
| | | CY37064VP100-143BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | | | | |
| | 100 | 100 | CY37064VP44-100AC | A44 | 44-Lead Thin Quad Flatpack | Commercial | | |
| | | | CY37064VP44-100AXC | A44 | 44-Lead Lead Free Thin Quad Flatpack | | | |
| | | | CY37064VP48-100BAC | BA50 | 48-Ball Fine-Pitch Ball Grid Array | | | |
| | | | CY37064VP100-100AC | A100 | 100-Lead Thin Quad Flatpack | | | |
| | | | CY37064VP100-100AXC | A100 | 100-Lead Lead Free Thin Quad Flatpack | | | |
| | | | CY37064VP100-100BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | | | |
| | | Industrial | 100AI | CY37064VP44-100AI | A44 | 44-Lead Thin Quad Flatpack | Industrial | |
| | | | | CY37064VP44-100AXI | A44 | 44-Lead Lead Free Thin Quad Flatpack | | |
| | | | 100BAI | CY37064VP48-100BAI | BA50 | 48-Ball Fine-Pitch Ball Grid Array | | |
| | | | | CY37064VP100-100BBI | BB100 | 100-Ball Fine-Pitch Ball Grid Array | | |
| | | | 100AI | CY37064VP100-100AI | A100 | 100-Lead Thin Quad Flatpack | | |
| | | | | CY37064VP100-100AXI | A100 | 100-Lead Lead Free Thin Quad Flatpack | | |
| | | | | 5962-9952001QYA | Y67 | 44-Lead Ceramic Leaded Chip Carrier | | Military |
| 128 | 125 | CY37128VP100-125AC | A100 | 100-Lead Thin Quad Flat Pack | Commercial | | | |
| | | CY37128VP100-125AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | | | | |
| | | CY37128VP100-125BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | | | | |
| | | CY37128VP160-125AC | A160 | 160-Lead Thin Quad Flat Pack | | | | |
| | | CY37128VP160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | | |
| | | CY37128VP160-125AI | A160 | 160-Lead Thin Quad Flat Pack | | | | |
| | | Industrial | 125AXI | CY37128VP160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | Industrial | |
| | | | | 83 | CY37128VP100-83AC | A100 | | 100-Lead Thin Quad Flat Pack |
| | | CY37128VP100-83AXC | A100 | | 100-Lead Lead Free Thin Quad Flat Pack | | | |
| | | CY37128VP100-83BBC | BB100 | | 100-Ball Fine-Pitch Ball Grid Array | | | |
| | | CY37128VP160-83AC | A160 | | 160-Lead Thin Quad Flat Pack | | | |
| | | Industrial | 83AXC | | CY37128VP160-83AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | Industrial |
| | 83AI | | | | CY37128VP100-83AI | A100 | 100-Lead Thin Quad Flat Pack | |
| | | | | | CY37128VP100-83AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | Military | 83BBI | CY37128VP100-83BBI | BB100 | 100-Ball Fine-Pitch Ball Grid Array | Military | | |
| | | | 83AI | CY37128VP160-83AI | A160 | | 160-Lead Thin Quad Flat Pack | |
| | | CY37128VP160-83AXI | | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | |
| | | 5962-9952201QYA | | Y84 | 84-Lead Ceramic Leaded Chip Carrier | | | |
| | | 192 | 100 | CY37192VP160-100AC | A160 | | 160-Lead Thin Quad Flat Pack | Commercial |
| CY37192VP160-100AXC | | | | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | |
| 66 | | | CY37192VP160-66AC | A160 | 160-Lead Thin Quad Flat Pack | | Commercial | |
| | CY37192VP160-66AXC | | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | | |
| | CY37192VP160-66AI | | A160 | 160-Lead Thin Quad Flat Pack | Industrial | | | |

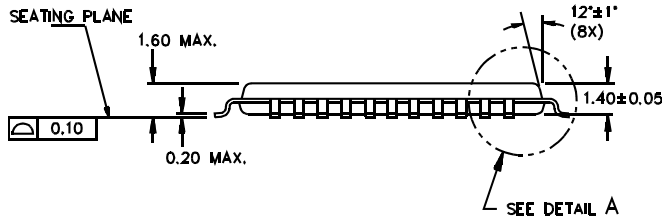
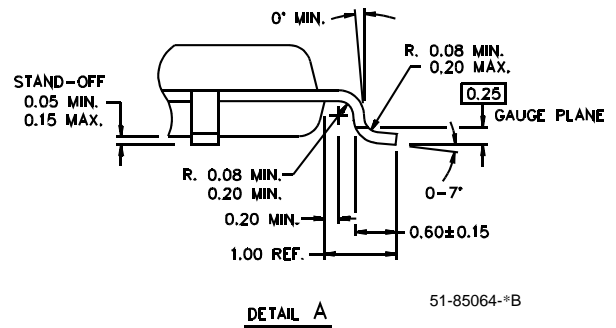
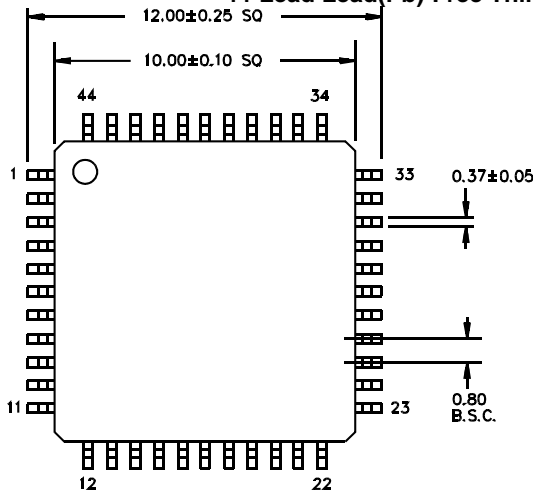
3.3V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range | | | |
|--------------------|---------------------|---------------------|--|--|--|-------------------------------------|------------|-------------------------------------|
| 256 | 100 | CY37256VP160-100AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial | | | |
| | | CY37256VP160-100AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | | |
| | | CY37256VP208-100NC | N208 | 208-Lead Plastic Quad Flat Pack | | | | |
| | | CY37256VP256-100BGC | BG256 | 256-Ball Ball Grid Array | | | | |
| | | CY37256VP256-100BBC | BB256 | 256-Ball Fine-Pitch Ball Grid Array | | | | |
| | | CY37256VP160-100AI | A160 | 160-Lead Thin Quad Flat Pack | | Industrial | | |
| | CY37256VP160-100AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | | | |
| | 66 | 66 | CY37256VP160-66AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial | | |
| | | | CY37256VP160-66AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | | | |
| | | | CY37256VP208-66NC | N208 | 208-Lead Plastic Quad Flat Pack | | | |
| | | | CY37256VP256-66BGC | BG256 | 256-Ball Ball Grid Array | | | |
| | | 66 | 66 | CY37256VP256-66BBC | BB256 | 256-Ball Fine-Pitch Ball Grid Array | Industrial | |
| | | | | CY37256VP160-66AI | A160 | 160-Lead Thin Quad Flat Pack | | |
| | | | CY37256VP256-66BGI | BG256 | 256-Ball Ball Grid Array | | | |
| CY37256VP256-66BBI | | | BB256 | 256-Ball Fine-Pitch Ball Grid Array | | | | |
| | | 5962-9952401QZC | U162 | 160-Lead Ceramic Quad Flat Pack | Military | | | |
| 384 | 83 | CY37384VP208-83NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial | | | |
| | | CY37384VP256-83BGC | BG256 | 256-Ball Ball Grid Array | | | | |
| | 66 | 66 | CY37384VP208-66NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial | | |
| | | | CY37384VP256-66BGC | BG256 | 256-Ball Ball Grid Array | | | |
| | | 66 | 66 | CY37384VP208-66NI | N208 | 208-Lead Plastic Quad Flat Pack | Industrial | |
| | | | | CY37384VP256-66BGI | BG256 | 256-Ball Ball Grid Array | | |
| 512 | 83 | CY37512VP208-83NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial | | | |
| | | CY37512VP256-83BGC | BG256 | 256-Ball Ball Grid Array | | | | |
| | | CY37512VP352-83BGC | BG352 | 352-Ball Ball Grid Array | | | | |
| | | CY37512VP400-83BBC | BB400 | 400-Ball Fine-Pitch Ball Grid Array | | | | |
| | 66 | 66 | CY37512VP208-66NC | N208 | 208-Lead Plastic Quad Flat Pack | Commercial | | |
| | | | CY37512VP256-66BGC | BG256 | 256-Ball Ball Grid Array | | | |
| | | | CY37512VP352-66BGC | BG352 | 352-Ball Ball Grid Array | | | |
| | | | CY37512VP400-66BBC | BB400 | 400-Ball Fine-Pitch Ball Grid Array | | | |
| | | 66 | 66 | CY37512VP208-66NI | N208 | 208-Lead Plastic Quad Flat Pack | Industrial | |
| | | | | CY37512VP256-66BGI | BG256 | 256-Ball Ball Grid Array | | |
| | | | 66 | 66 | CY37512VP352-66BGI | BG352 | | 352-Ball Ball Grid Array |
| | | | | | CY37512VP400-66BBI | BB400 | | 400-Ball Fine-Pitch Ball Grid Array |
| | | | 5962-9952601QZC | U208 | 208-Lead Ceramic Quad Flat Pack | Military | | |

Package Diagrams

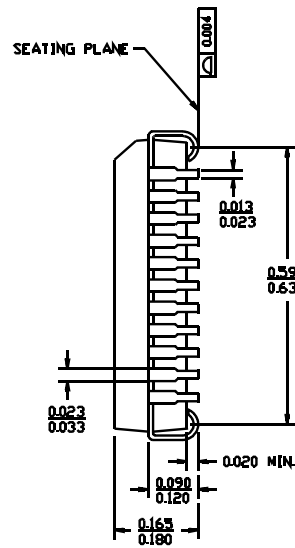
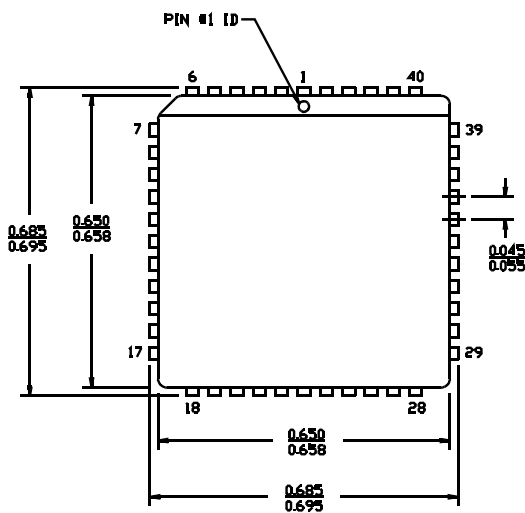
44-Lead Lead(Pb)-Free Thin Plastic Quad Flat Pack A44

DIMENSIONS ARE IN MILLIMETERS



44-Lead Lead(Pb)-Free Plastic Leaded Chip Carrier J67

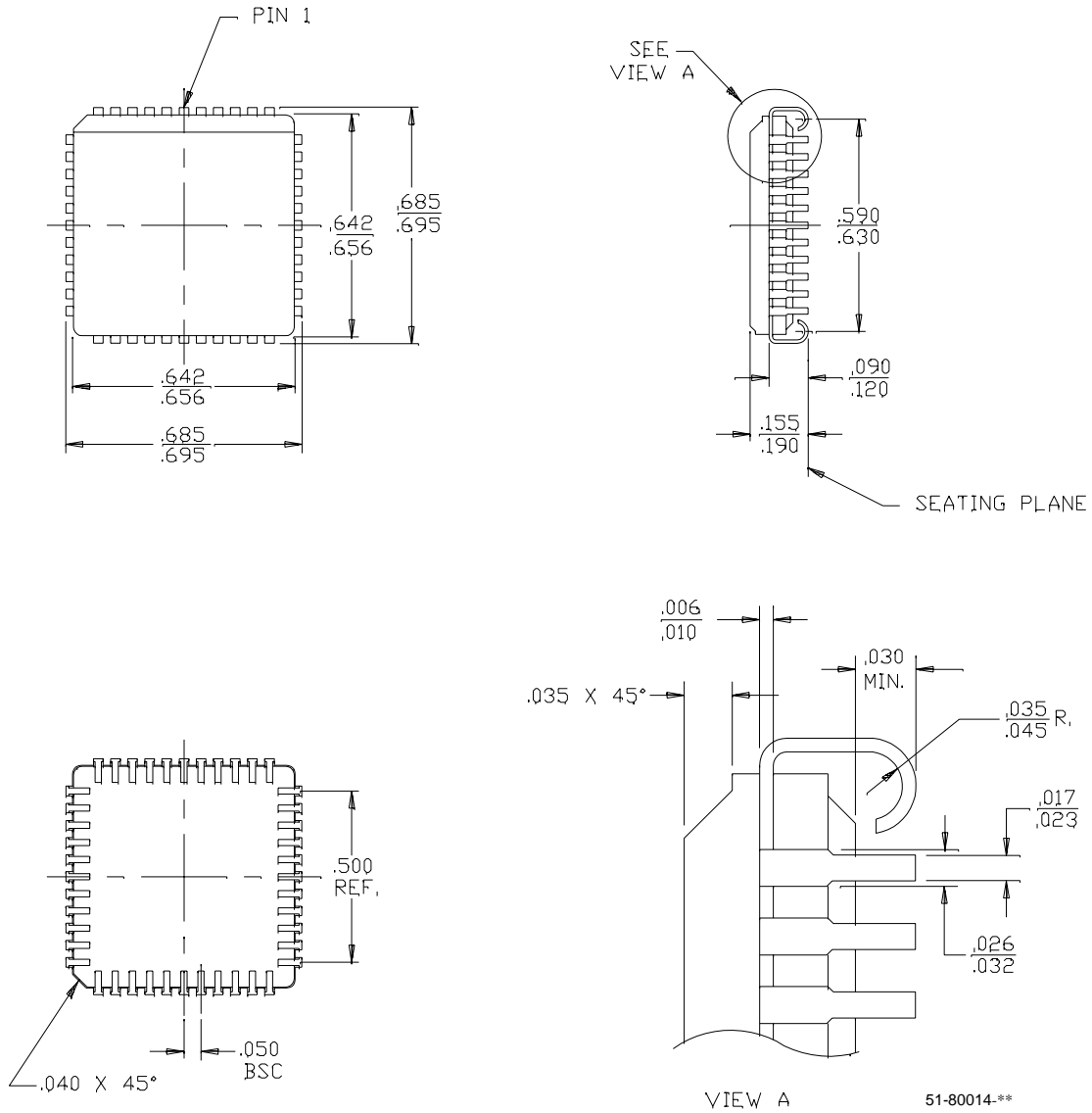
DIMENSIONS IN INCHES MIN. MAX.



51-85003-*A

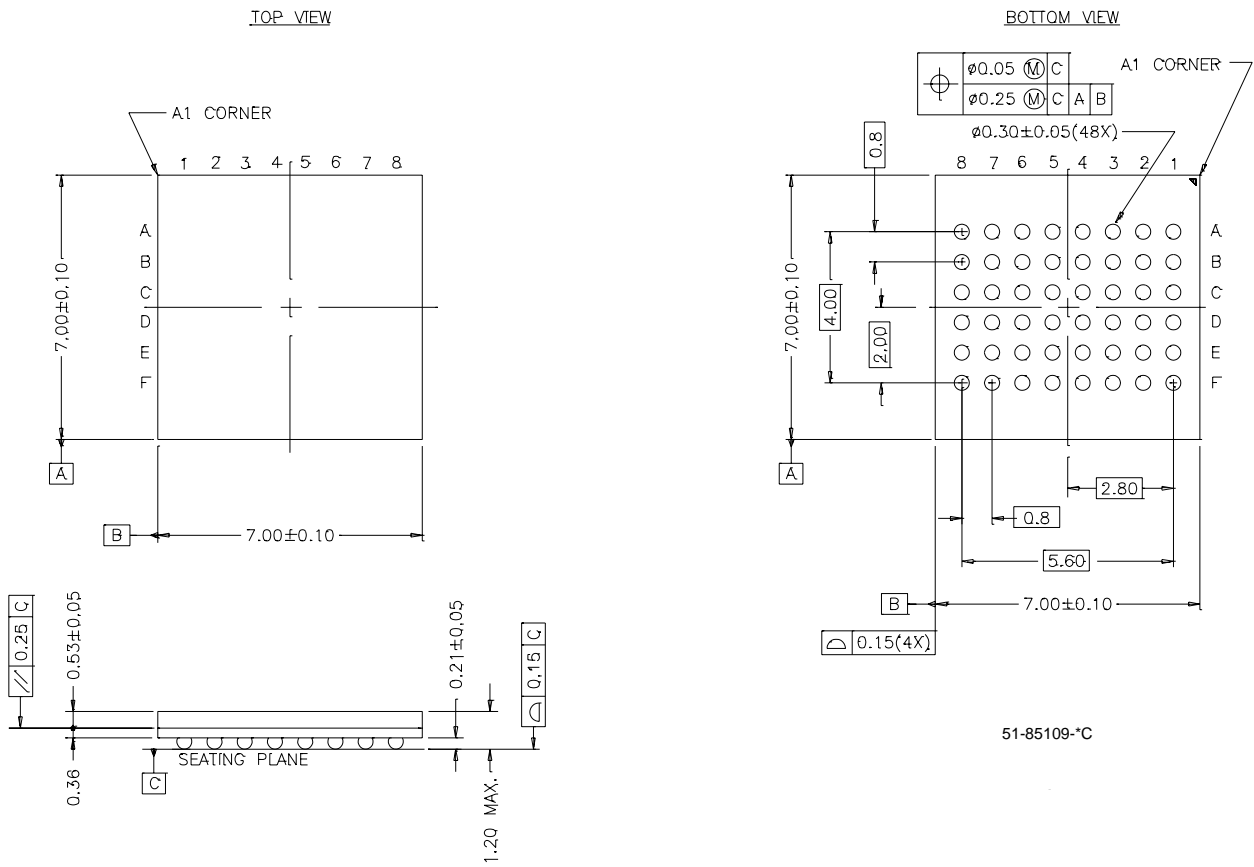
Package Diagrams (continued)

44-Lead Ceramic Leaded Chip Carrier Y67



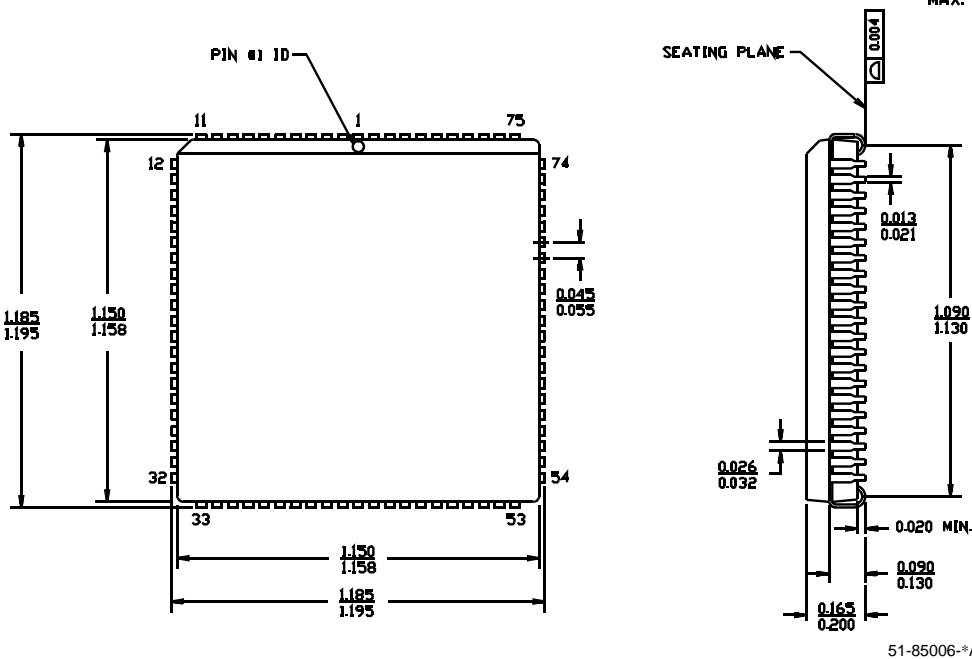
Package Diagrams (continued)

48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D



84-Lead Lead(Pb)-Free Plastic Leaded Chip Carrier J83

DIMENSIONS IN INCHES MIN. MAX.

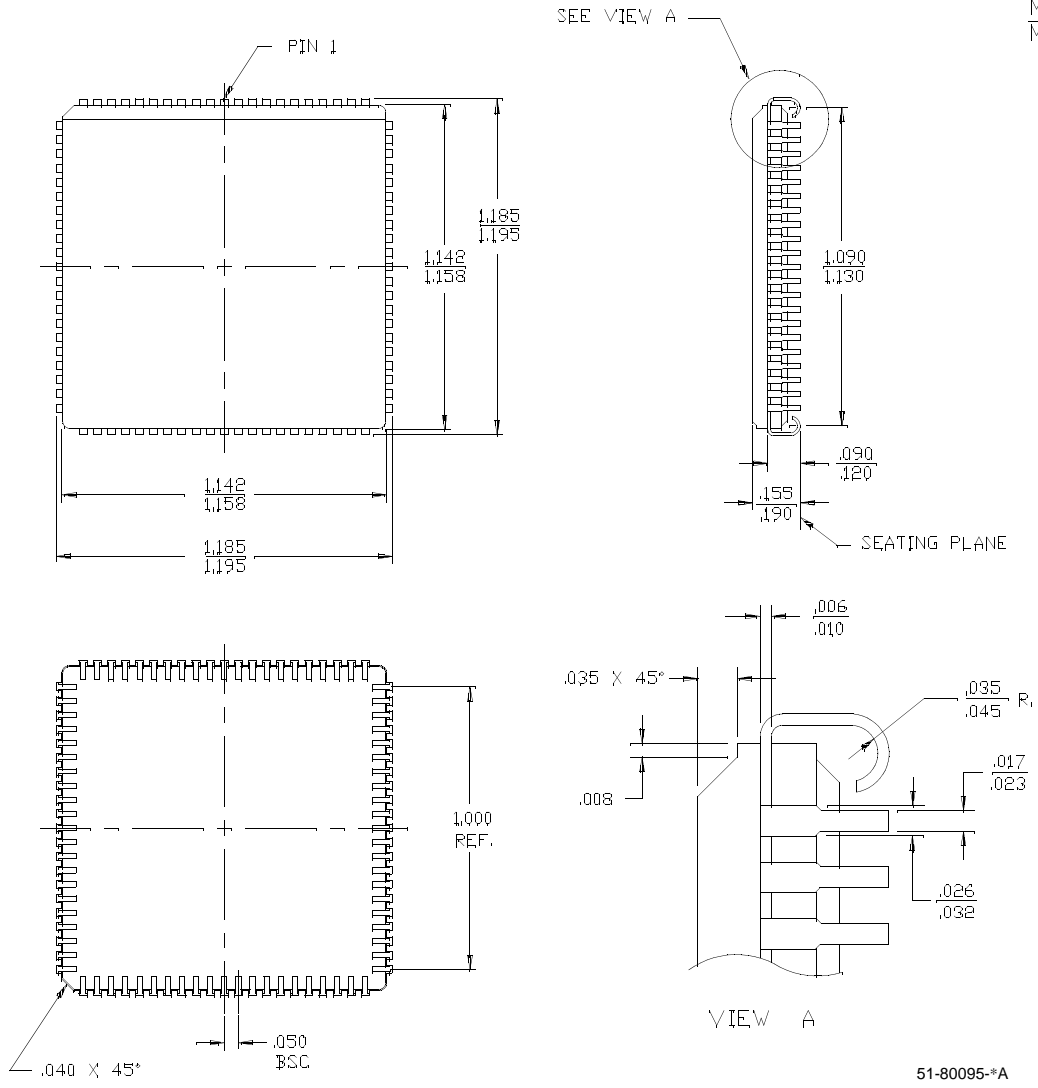


Package Diagrams (continued)

84-Lead Ceramic Leaded Chip Carrier Y84

DIMENSIONS IN INCHES

MIN.
MAX.

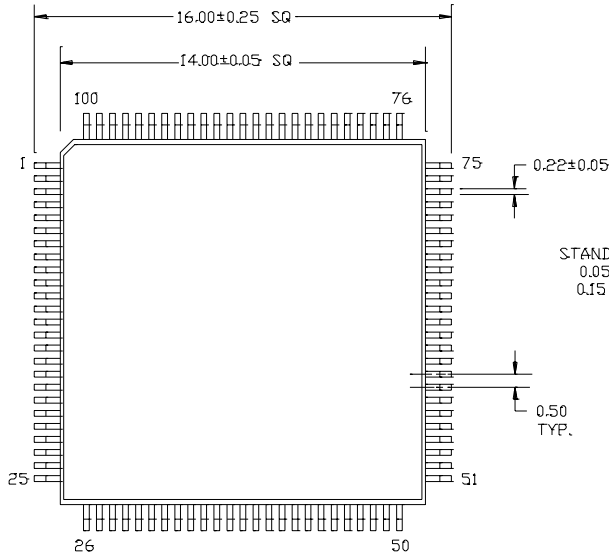


51-80095-*A

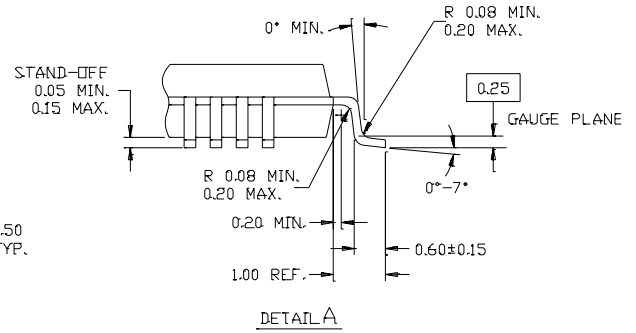


Package Diagrams (continued)

100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100



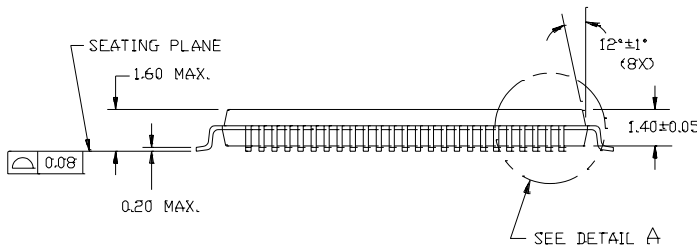
DIMENSIONS ARE IN MILLIMETERS.



NOTE: PKG. CAN HAVE



51-85048-*B

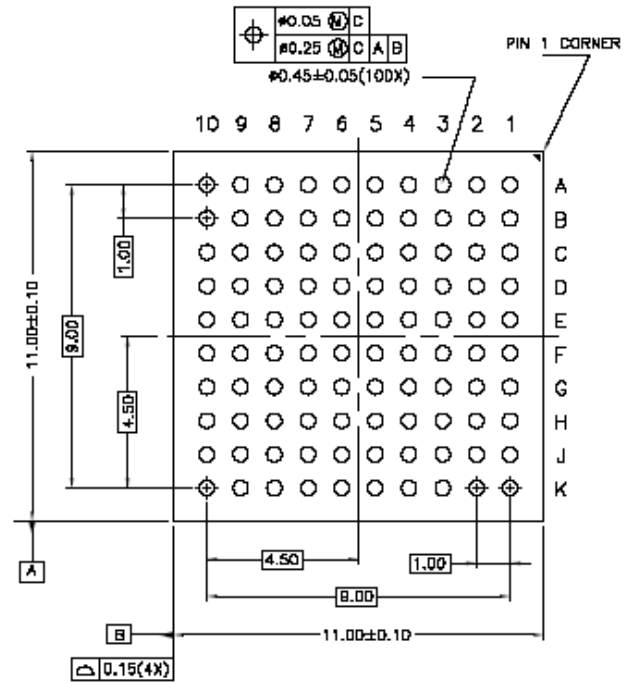
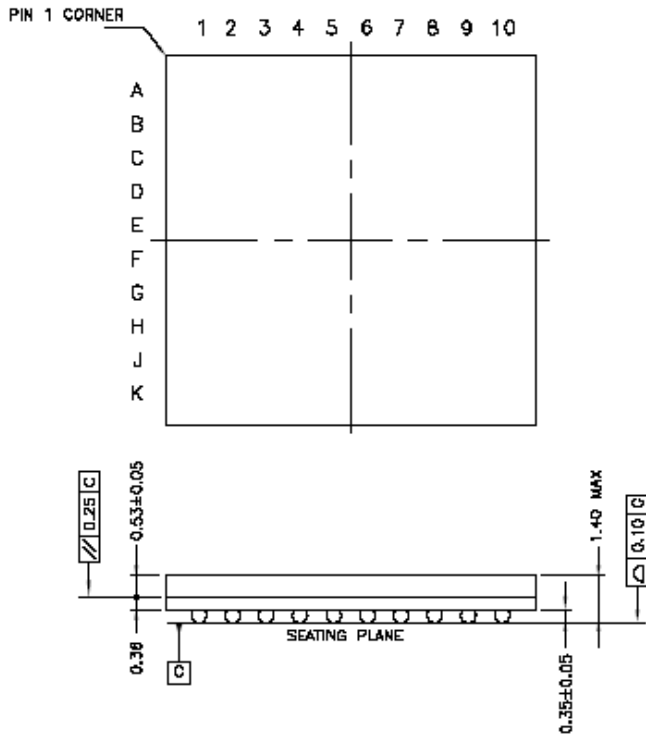


Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100

TOP VIEW

BOTTOM VIEW

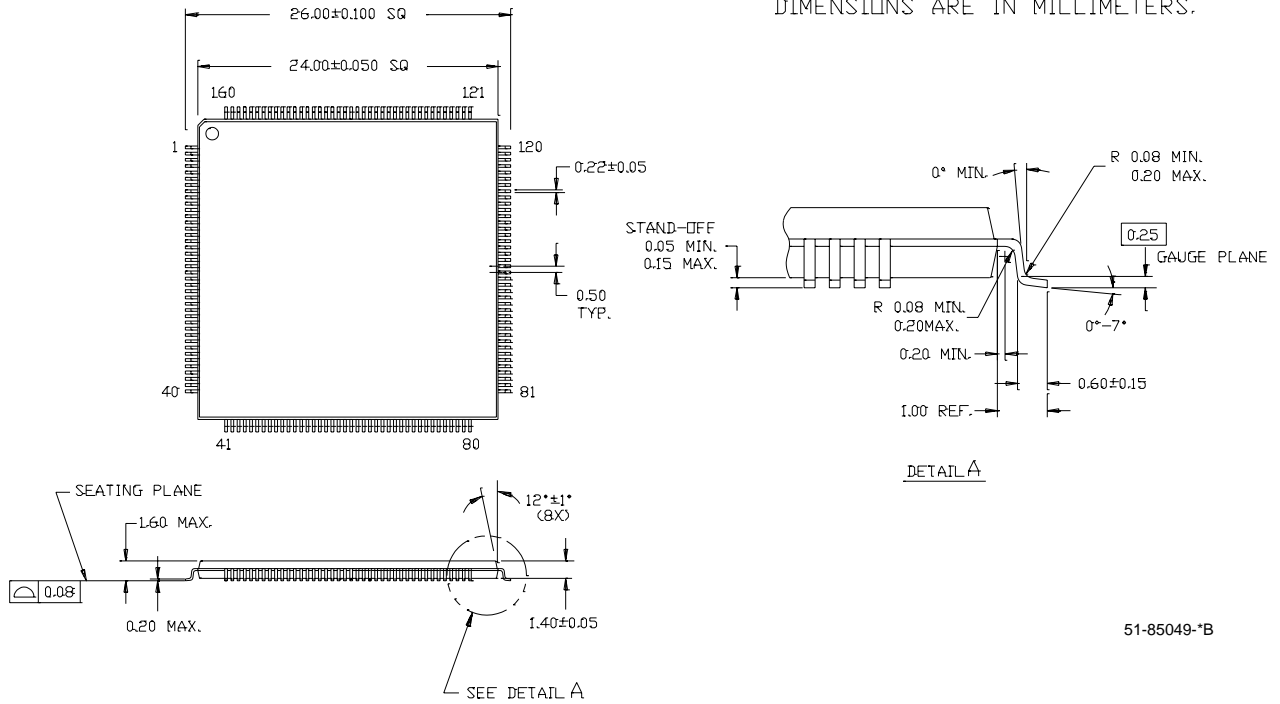


51-85107-B

Package Diagrams (continued)

160-Lead Lead(Pb)-Free Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160

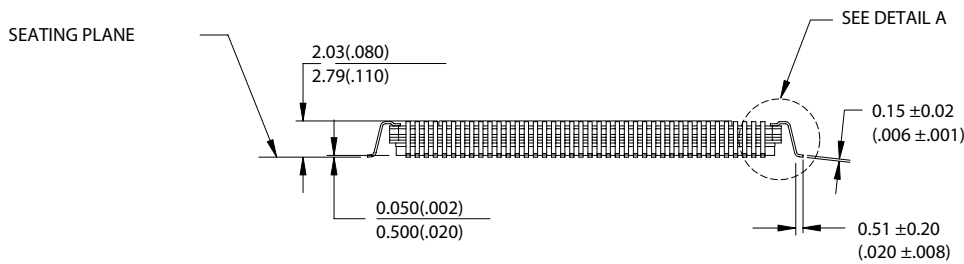
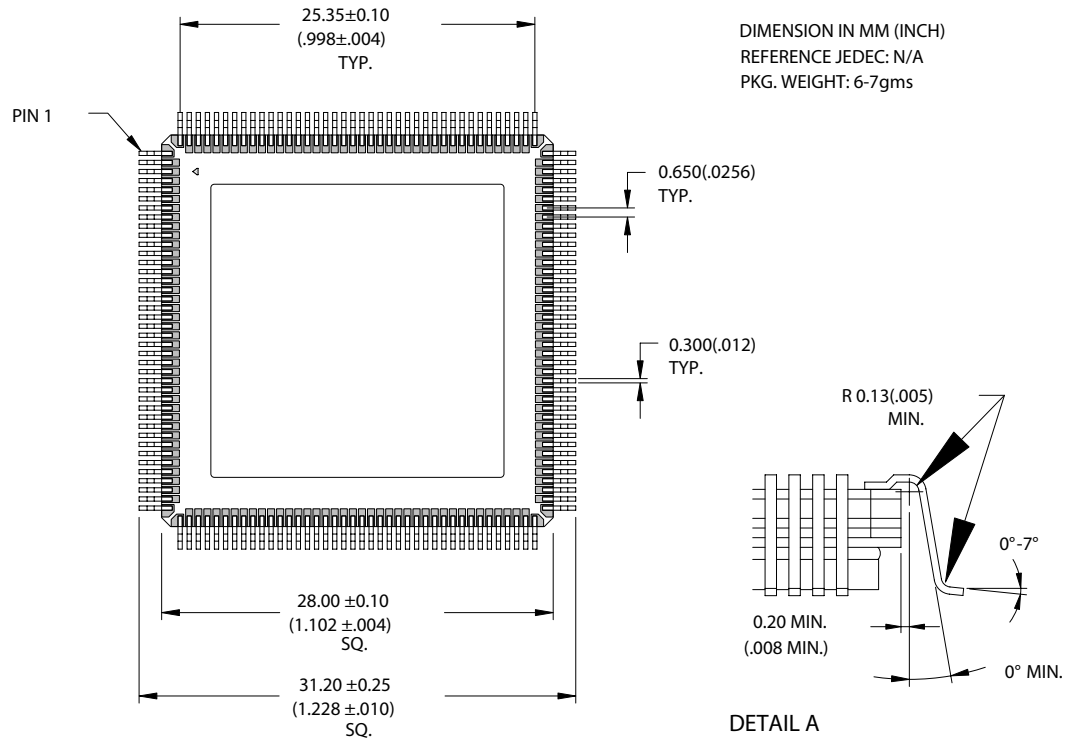
DIMENSIONS ARE IN MILLIMETERS.



51-85049-B

Package Diagrams (continued)

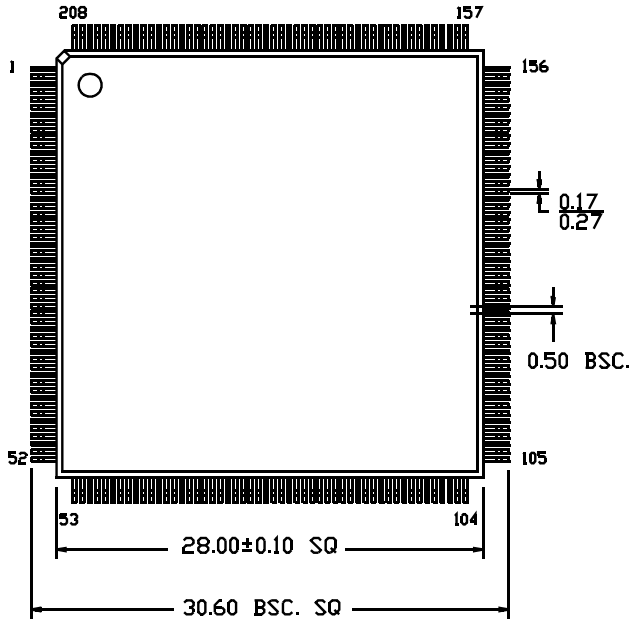
160-Lead Ceramic Quad Flatpack (Cavity Up) U162



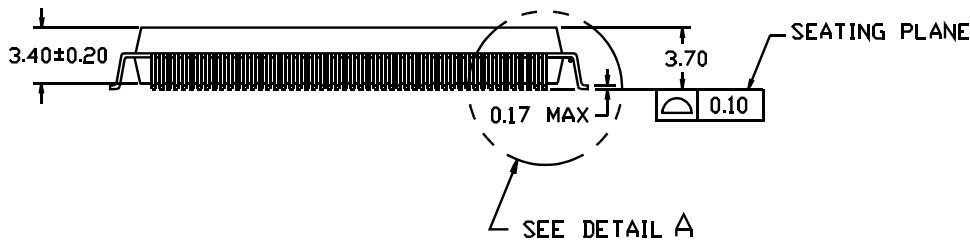
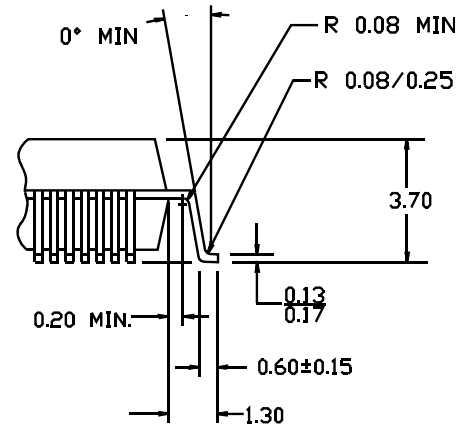
51-80106-*A

Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



DIMENSIONS ARE IN MILLIMETERS

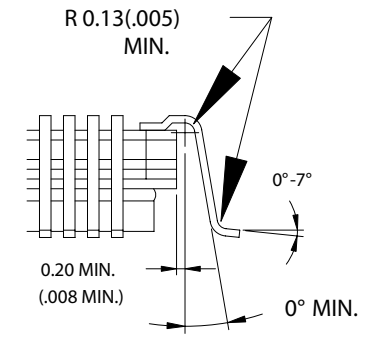
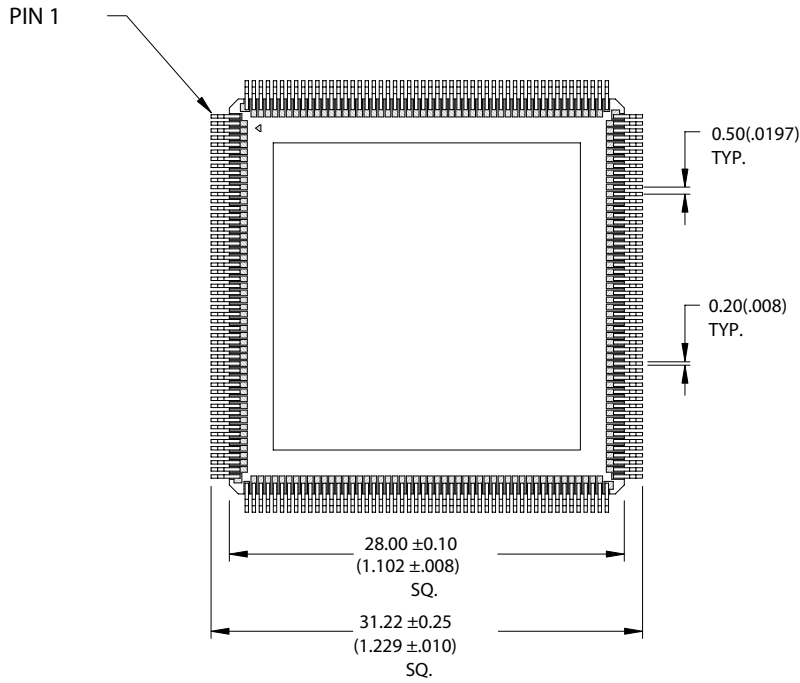


51-85069-*B

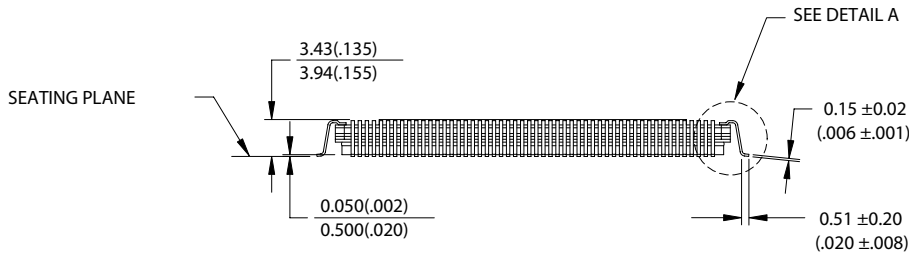
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208

DIMENSIONS IN MM (INCH)
 REFERENCE JEDEC: N/A
 PKG. WEIGHT: 6-7gms



DETAIL A

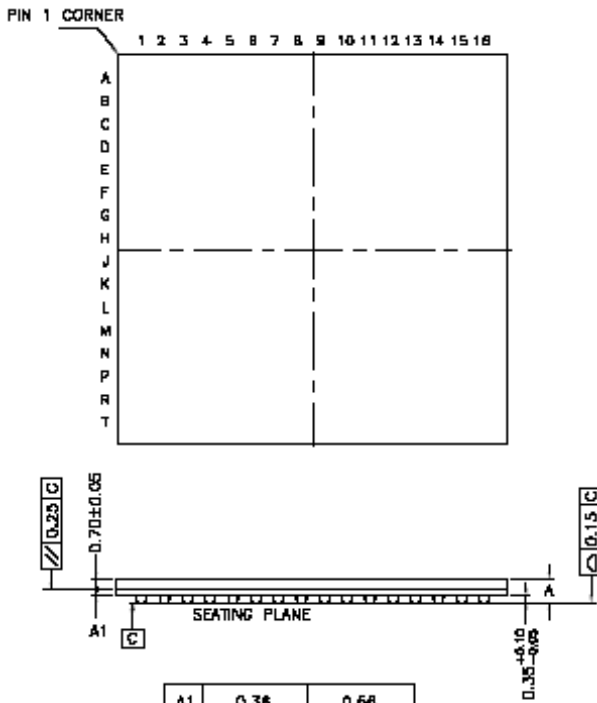


51-80105-*B

Package Diagrams (continued)

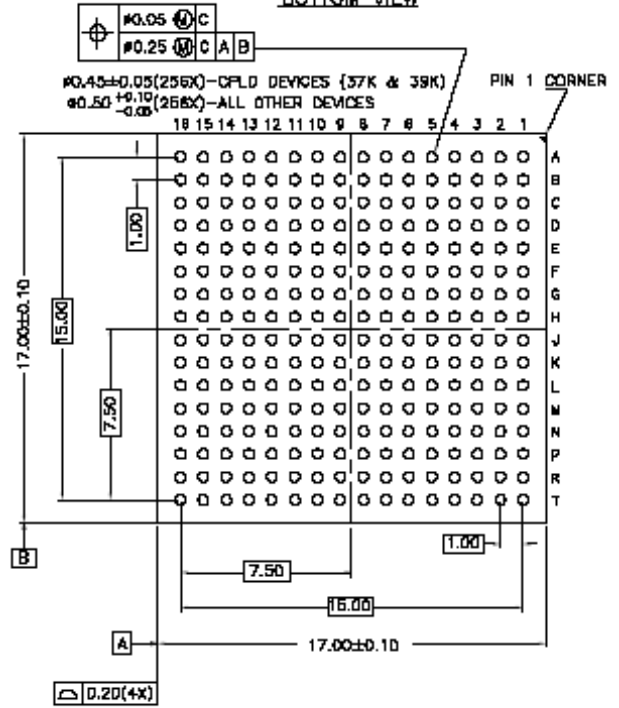
256-Ball FBGA (17 x 17 mm) BB256

TOP VIEW



| | | |
|----|-----------|-----------|
| A1 | 0.35 | 0.56 |
| A | 1.40 MAX. | 1.70 MAX. |

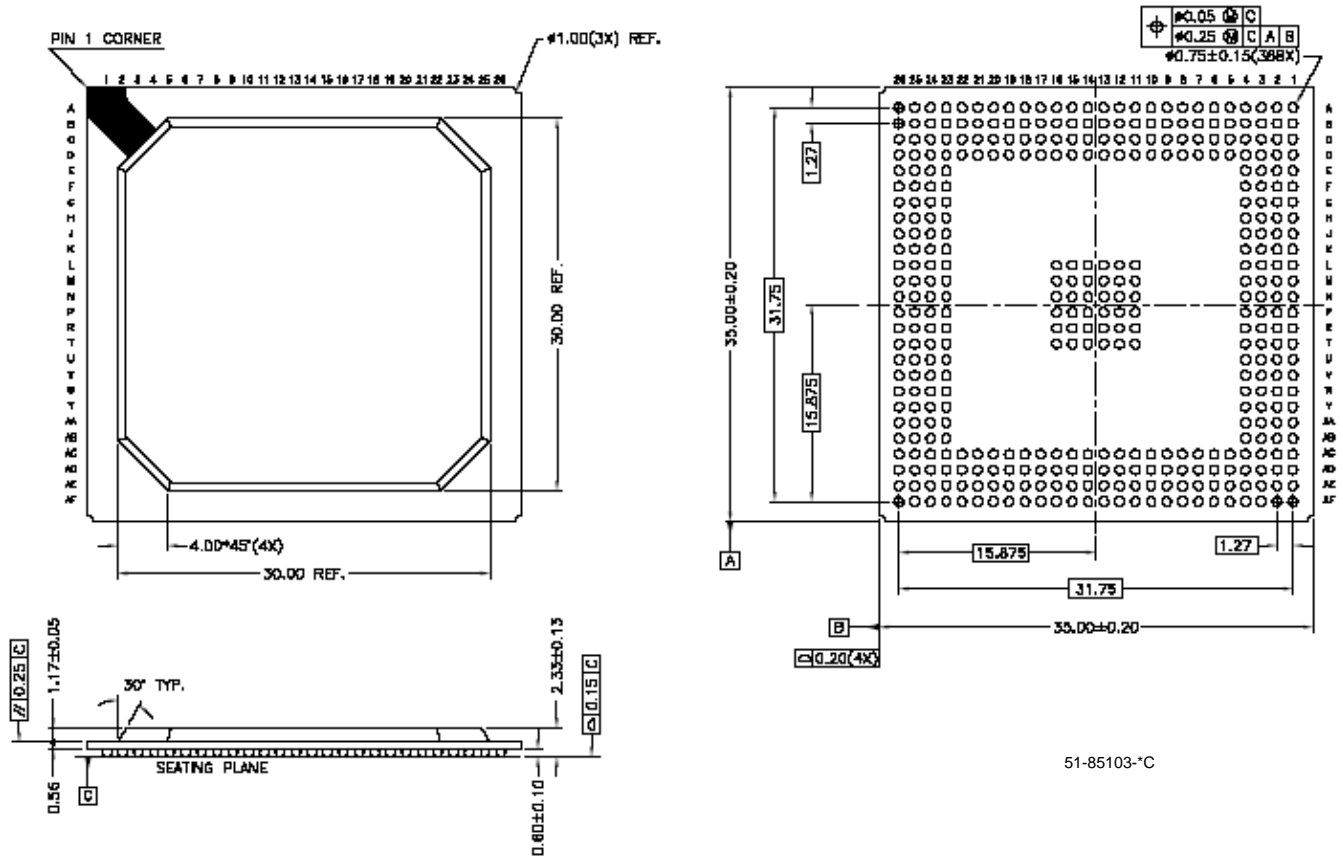
BOTTOM VIEW



51-85108-*F

Package Diagrams (continued)

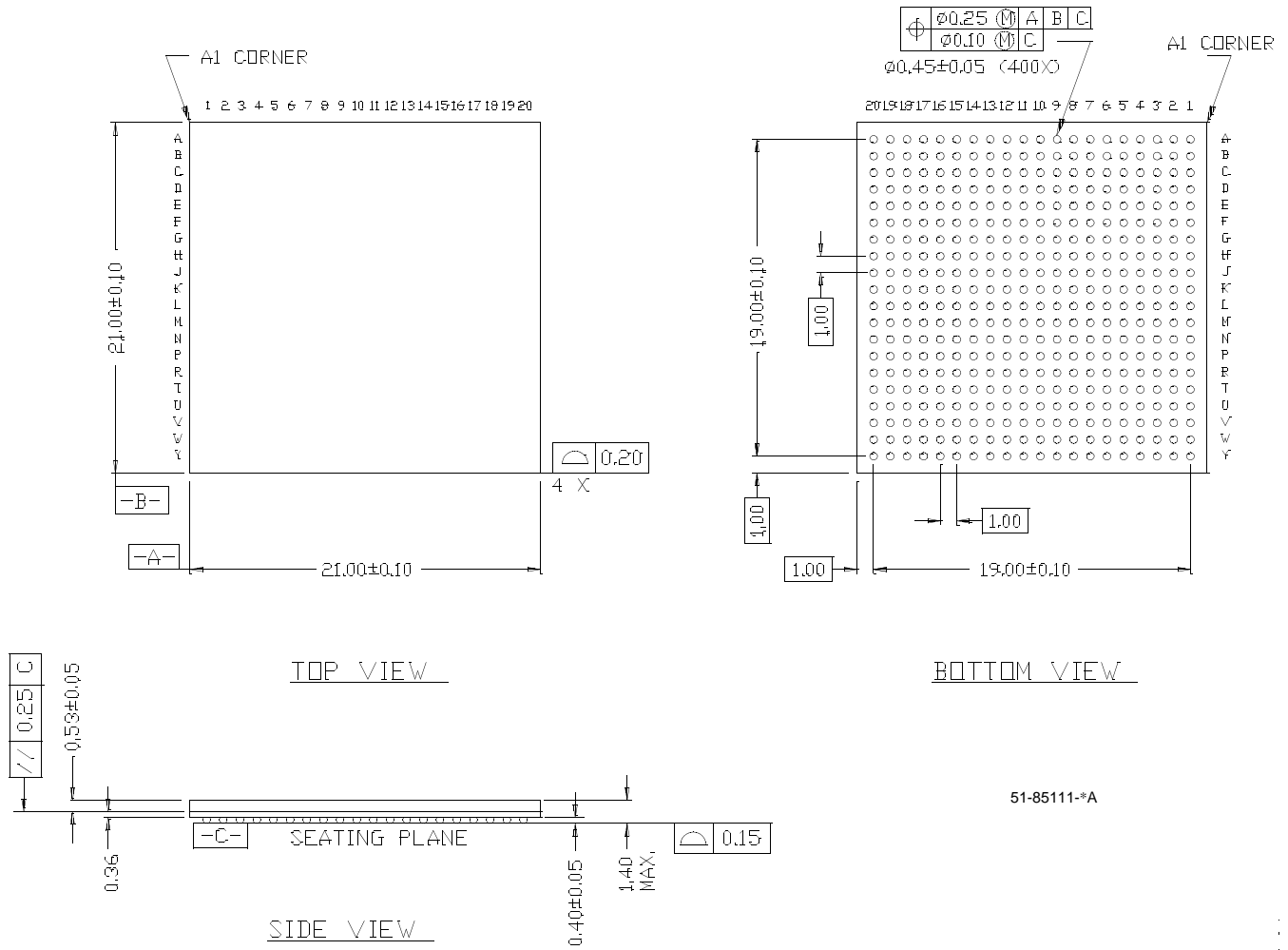
388-Ball PBGA (35 x 35 x 2.33 mm) BG388



51-85103-1C

Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



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Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

| Range | Ambient Temperature ^[2] | Junction Temperature | V _{CC} |
|------------|------------------------------------|----------------------|-----------------|
| Commercial | 0°C to +70°C | 0°C to +90°C | 3.3V ± 0.16V |



Document History Page

| Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs | | | | |
|--|---------|------------|-----------------|---|
| Document Number: 38-03007 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106272 | 04/18/01 | SZV | Change from Spec number: 38-00475 to 38-03007 |
| *A | 124942 | 03/21/03 | OOR | Updated 3.3V V _{CC} requirements for -144 speeds Added an Addendum |
| *B | 126262 | 05/09/03 | TEH | Changed pinout for CY37128V BB100 package |
| *C | 128125 | 07/16/03 | HOM | Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI |
| *D | 282709 | See ECN | YDT | Changed package diagrams and labels for consistency Added Lead(Pb)-free logo on first page, as well as a note in Features Added Lead(Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC |