QUAD D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- **Four edge-triggered D flip-flops**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs.

The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}	propagation delay $\overline{CP}$ to Q_n, $\overline{Q}_n$ $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 5 V	17 15	16 19	ns ns
t_{PLH}	propagation delay $\overline{CP}$ to Q_n, $\overline{Q}_n$ $\overline{MR}$ to $\overline{Q}_n$		17 15	16 16	ns ns
f_{max}	maximum clock frequency		83	54	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 7, 10, 15	Q_0 to Q_3	flip-flop outputs
3, 6, 11, 14	$\overline{Q}_0$ to $\overline{Q}_3$	complementary flip-flop outputs
4, 5, 12, 13	D_0 to D_3	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

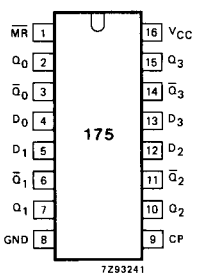

Fig. 1 Pin configuration.

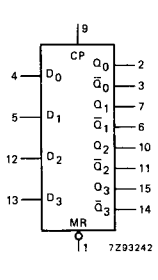

Fig. 2 Logic symbol.

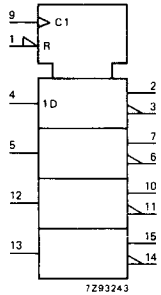

Fig. 3 IEC logic symbol.

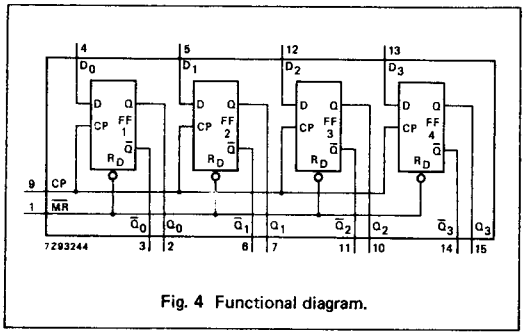

Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care

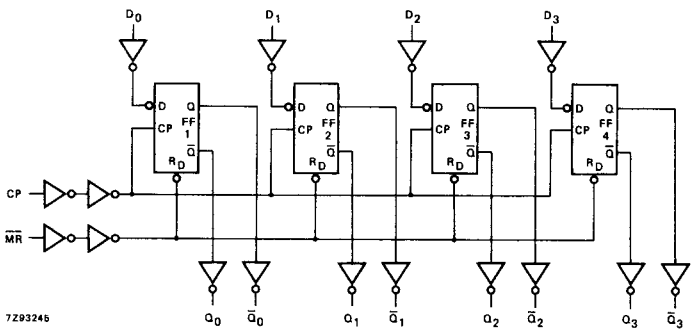

Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5	−33 −12 −10		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t_{su}	set-up time D_n to CP	80 16 14	3 1 1		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_h	hold time CP to D_n	25 5 4	2 0 0		30 6 5		40 8 7		ns	2.0 4.5 6.0	Fig. 7
f_{max}	maximum clock pulse frequency	6.0 30 35	25 75 89		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	1.00
CP	0.60
D_n	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n, $\overline{Q}_n$		19	33		41		50	ns	4.5	Fig. 6
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		22	38		48		57	ns	4.5	Fig. 8
t_{PLH}	propagation delay $\overline{MR}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	20	12		25		30		ns	4.5	Fig. 6
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t_{rem}	removal time $\overline{MR}$ to CP	5	−10		5		5		ns	4.5	Fig. 8
t_{su}	set-up time D_n to CP	16	5		20		24		ns	4.5	Fig. 7
t_h	hold time CP to D_n	5	0		5		5		ns	4.5	Fig. 7
f_{max}	maximum clock pulse frequency	25	49		20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

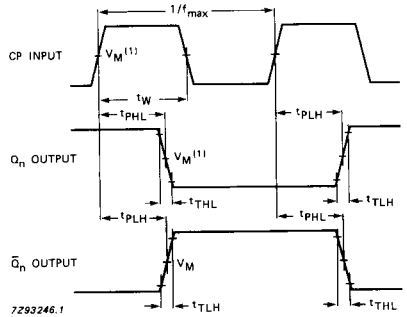

Fig. 6 Waveforms showing the clock (CP) to outputs (Q_n, $\overline{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

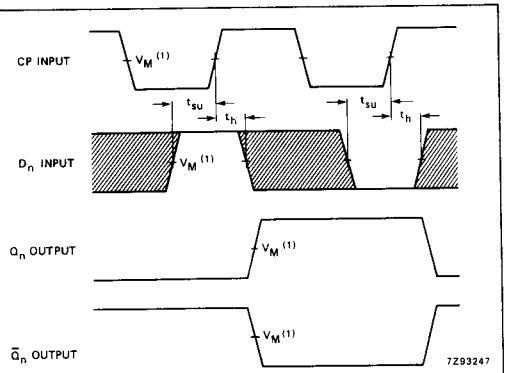

Fig. 7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

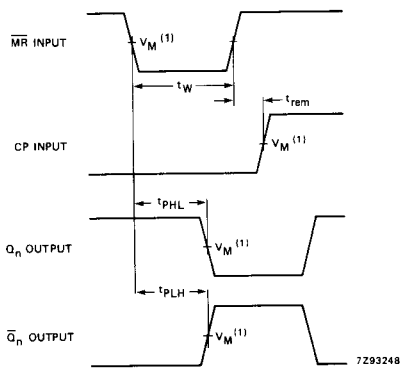

Fig. 8 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to outputs (Q_n, $\overline{Q}_n$) propagation delays and the master reset to clock (CP) removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.