Z86227

40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER (4LDTC™)

FEATURES

8-Bit CMOS Microcontroller for Consumer Television, Cable and Satellite Receiver Applications.

- 40-Pin DIP Package
- Lowest Cost DTC Family Member
- Low Power Consumption
- Fast Instruction Pointer - 1.5 µs @ 4 MHz
- Two Standby Modes - STOP and HALT
- Low Voltage Detection/Voltage Sensitive Reset
- 24 Input/Output Lines
- Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports
- Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports
- All Digital CMOS Levels Schmitt-Triggered
- 6 Kbytes of ROM
- 236 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive
- Permanently Enabled Watch-Dog/Power-On Reset Timer

On-Screen Display Controller

- 3K x 6-Bit Character Generator ROM
- 120 x 7-Bit Video RAM
- Mask Programmable 96-Character Set Displayed in an 6-Row x 20-Column Format, 12 x 15 Pixel Character Cell, Capable of Supporting English, Korean, Chinese and Japanese High Resolution Characters.
- Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character Size.
- Programmable Display Position and Character Size Control
- One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control.
- Three Pulse Width Modulator (8-Bit Resolution) for Picture Control
- Three Pulse Width Modulators (6-Bit Resolution) for Audio Control

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GENERAL DESCRIPTION

The Z86227 40-pin Low-Cost Digital Television Controller (4LDTC™) introduces a new level of sophistication to single-chip architecture. The Z86227 is a member of the Z8® single-chip microcontroller family with 6 Kbytes of ROM and 236 bytes of RAM. The device is offered in a 40-pin package and is CMOS compatible. The 4LDTC offers mask programmed ROM which enables the Z8® microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program) and combines together with the Z86C27 (DTC) and Z86127 (LDTC) to provide support for high end, mid range and low end TV applications.

GENERAL DESCRIPTION (Continued)

Zilog's 4LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86227 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On Screen Display (OSD) logic circuits and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support 6 rows x 20 columns of characters. The character color is specified by row. One of the six rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5 x 7 dot pattern) or high resolution (11 x 15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports used to vary picture levels.

For 4LDTC applications demanding powerful I/O capabilities, the Z86227 fulfills this with 24 I/O pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general-purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the 4LDTC offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

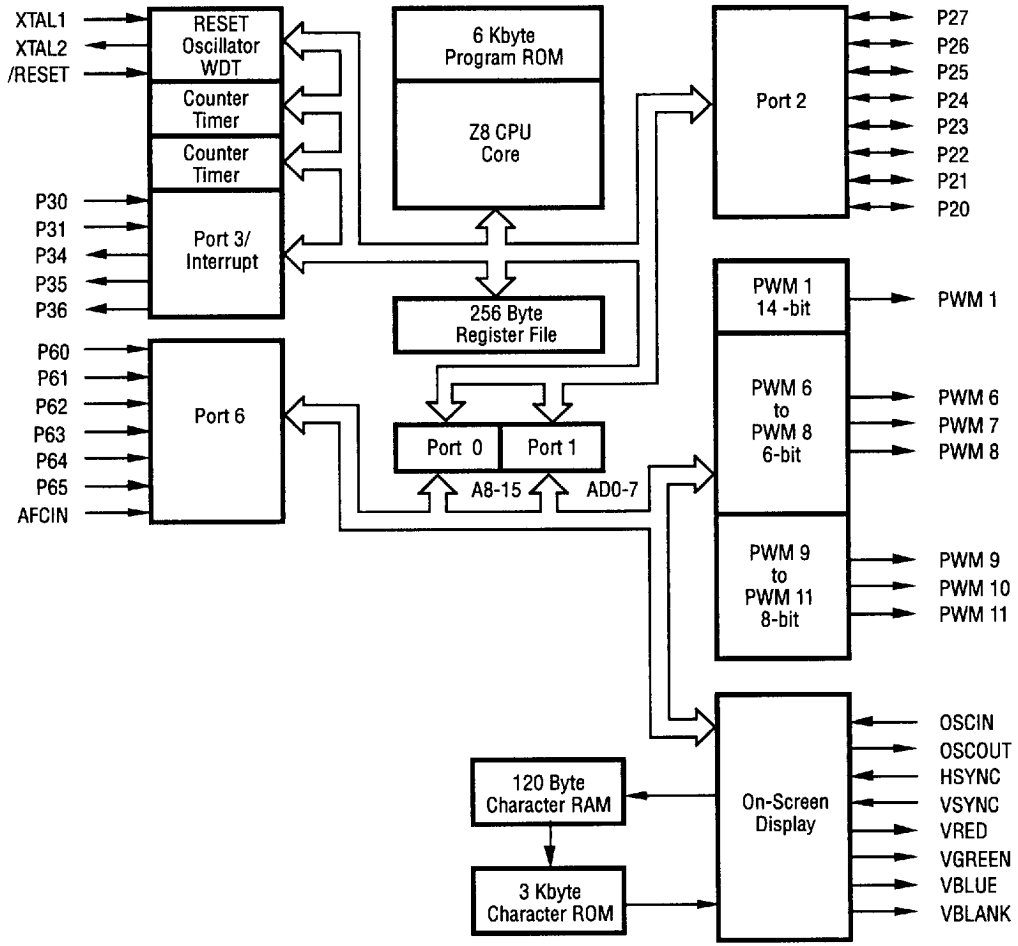

Figure 1. Functional Block Diagram

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PIN CONFIGURATION

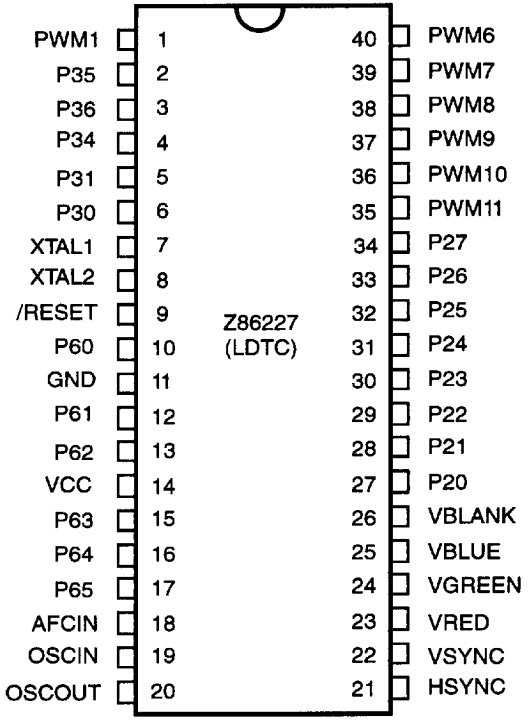


Figure 2. 40-Pin Mask-ROM Plastic DIP

PIN IDENTIFICATION

40-Pin	Name	Function	Direction
1	PWM1	Pulse Width Modulator 1	Output
2, 3	P35-36	Port 3, Pins 5, 6	Output
4	P34	Port 3, Pin 4	Output
5	P31	Port 3, Pin 1	Input
6	P30	Port 3, Pin 0	Input
7	XTAL1	Crystal Oscillator	Input
8	XTAL2	Crystal Oscillator	Output
9	/RESET	System Reset	Input
10	P60	Port 6, Pin 0	Input
11	GND	Ground	Input
12	P61	Port 6, Pin 1	Input
13	P62	Port 6, Pin 2	Input
14	V_{CC}	Power Supply	Input
15, 16, 17	P63-65	Port 6, Pins 3, 4, 5	Input
18	AFC_{IN}	AFC Voltage Level	Input
19	OSC_{IN}	Video Dot Clock Osc	Input
20	OSC_{OUT}	Video Dot Clock Osc	Output
21	H_{SYNC}	Horizontal Sync	Input
22	V_{SYNC}	Vertical Sync	Input
23	Vred	Video Red	Output
24	Vgreen	Video Green	Output
25	Vblue	Video Blue	Output
26	Vblank	Video Blank	Output
27-34	P20-27	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
35	PWM11	Pulse Width Modulator 11	Output
36	PWM10	Pulse Width Modulator 10	Output
37	PWM9	Pulse Width Modulator 9	Output
38	PWM8	Pulse Width Modulator 8	Output
39	PWM7	Pulse Width Modulator 7	Output
40	PWM6	Pulse Width Modulator 6	Output

PIN DESCRIPTION

XTAL1, XTAL2. (time-based input, output, respectively). These pins connect to the internal parallel-resonant clock crystal (4 MHz max) oscillator circuit with two capacitors to GND. XTAL1 is also used as an external clock input.

SCLK *System Clock.* SCLK is the internal system clock. It can be used to clock external glue logic.

H_{SYNC} (input, Schmitt triggered, CMOS level). Horizontal Sync is an input pin that accepts an externally generated Horizontal Sync signal of either negative or positive polarity.

V_{SYNC} (input ,Schmitt-triggered, CMOS level). Vertical Sync is an input pin that accepts an externally generated Vertical Sync signal of either negative or positive polarity.

OSC_{IN}, OSC_{OUT} (Video Oscillator input, output, respectively). Oscillator input and output pins for on-screen display circuits. These pins connect to an inductor and two capacitors to generate the character dot clock (typically around 6 MHz). The dot clock frequency determines the character pixel width and phase synchronized to H_{SYNC}.

Vblank *Video Blank* (output). CMOS output, programmable polarity. Used as a superimpose control port to display characters from video RAM. The signal controls Y signal output of the CRT and turns off the incoming video display while the characters in video RAM are superimposed on the screen. The red, green, and blue outputs drive the three electron guns on the CRT directly, while the blank output turns off the Y signal.

Vblue *Video Blue* (output). CMOS Output of the Blue video signal (B-Y) and is programmable for either polarity.

Vgreen *Video Green* (output). CMOS Output of the Green video signal (G-Y) and is programmable for either polarity.

Vred *Video Red* (output). CMOS Output of the Red video signal (R-Y) and is programmable for either polarity.

Port 2 (P27-P20). Port 2 is an 8-bit port, CMOS compatible, bit programmable for either input or output. Input buffers are Schmitt triggered. Bits programmed as outputs may be globally programmed as either push pull or open-drain (Figure 3).

Port 3 (P30, P31, P34-P36). Port 3, P30 input, is read directly. If appropriately enabled, a negative edge event is latched in IRQ3 to initiate an IRQ3 vectored interrupt. An application could place the device in STOP mode when P30 goes Low (in the IRQ3 interrupt routine). P30 initiates a STOP mode recovery when it subsequently goes to a High. Port 3, P31 are read directly. If appropriately enabled, a negative edge event is latched in IRQ2 to initiate an IRQ2 vectored interrupt. P31 High is signified as the T_{IN} signal to Timer1. Port 3, P34 and P35 are general-purpose output lines. Port 3, P36 can be used as a general-purpose output or as an output for T_{OUT} (from Timer1 or Timer2) or SCLK (Figure 4).

Port 6 (P65-P60). Port 6 is a 6-bit, Schmitt triggered CMOS compatible, input port. The outputs of the AFC comparators internally feed into the Port 6, bit 6 and bit 7 inputs (Figure 5).

AFC_{IN} (Comparator input port, memory mapped). The input signal is supplied to two comparators with VTH1=2/5 V_{CC} and VTH2=3/5 V_{CC} typical threshold voltage. The comparator outputs are internally connected to Port 6, bit 6 and bit 7. AFC_{IN} is typically used to detect AFC voltage level to accommodate digital automatic fine tuning functions (Figure 6).

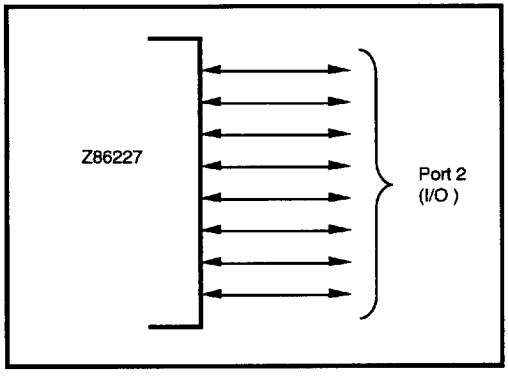
Pulse Width Modulator 1 (PWM). PWM1 is typically used as the D/A converter for Voltage Synthesis Tuning systems. It is a push-pull output with 14-bit resolution.

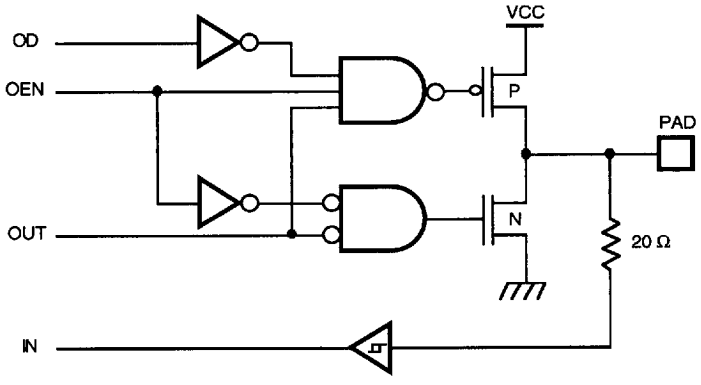
Pulse Width Modulator 6-8 (PWM). PWM8-PWM6 are Pulse Width Modulators with 6-bit resolution.

Pulse Width Modulator 9, 10, 11 (PWM). Pulse Width Modulator circuits with 8-bit resolution. These PWMs are 12 volt, open-drain outputs.

Pulse Width Modulator 1, 6, 7, 8 (PWM). Can be programmed as general-purpose outputs. PWM 1 is 5 V_{OH} push-pull, and PWMs 6, 7, 8 are 12 volt open-drain outputs.

/RESET *System Reset.* Code is executed from memory address 000CH after the /RESET pin is set to a high level. The reset function is also carried out by detecting a V_{CC} transition state (automatic Power-On Reset) so that the external reset pin can be permanently tied to V_{CC}. A low level on /RESET forces a restart of the device.

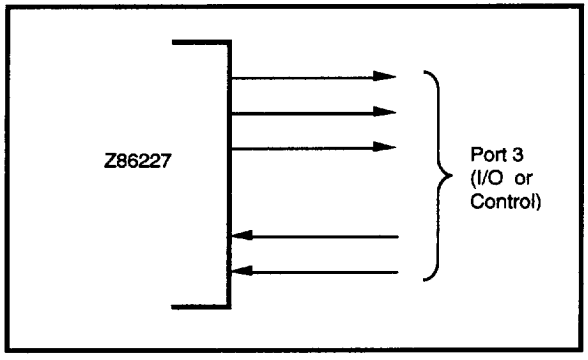


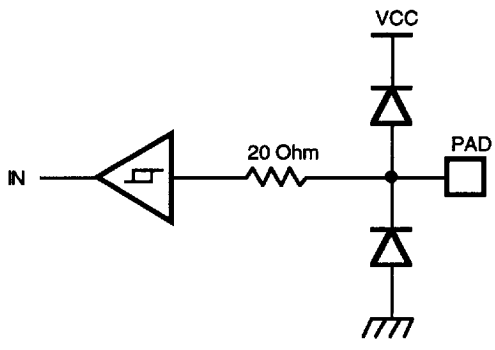


Note: Input/Output, Tri-State, Open Drain, Pad Type 5

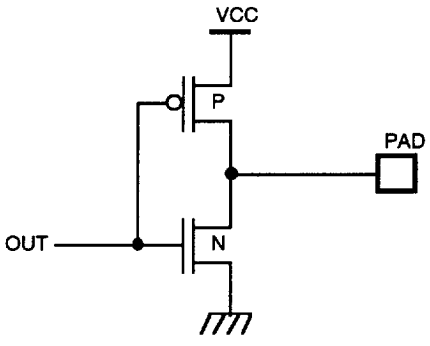
Figure 3. Port 2 Configuration

PIN DESCRIPTION (Continued)



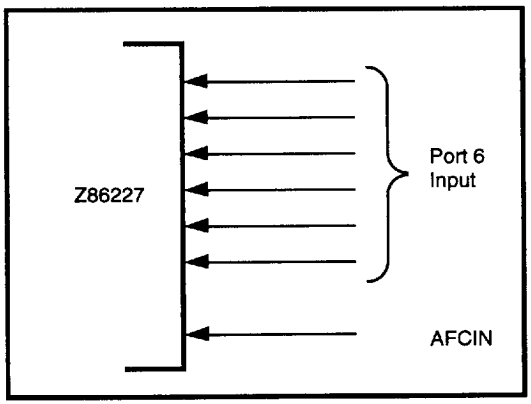


Note: Input Only, Schmitt-triggered, Pad Type 2



Note: Output Only, Pad Type 3

Figure 4. Port 3 Configuration



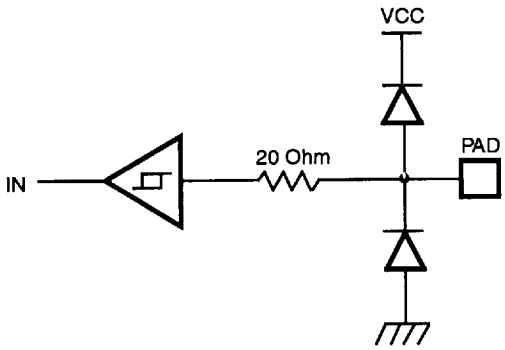


Figure 5. Port 6 Configuration

PIN DESCRIPTION (Continued)

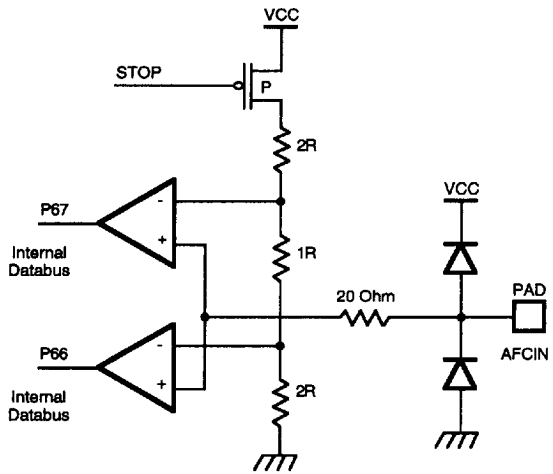


Figure 6. AFC_{IN} Comparator Circuits

FUNCTIONAL DESCRIPTION

The Z8 4LDTC incorporates special functions to enhance the Z8's versatility in consumer, industrial and television control applications.

Pulse Width Modulator (PWM). The 4LDTC has seven PWM channels (Figure 7). There are three types of PWM circuits: PWM1 (one channel of 14-bit resolution) typically used for Voltage Synthesis Tuning, PWM8-PWM6 (three channels of 6-bit resolution) typically used for audio level control, and PWM9, 10, 11 (three channels of 8-bit resolution) typically used for picture level control. The PWM control registers are mapped into external memory and are accessed through LDE and LDEI instructions.

PWM1. It is a push-pull output.

PWMs 6 through 11. They have their maximum values (on times) when all 1s are loaded in their PWM Value registers (and minimum value for all 0s). PWM1 has a maximum value for all 0s and minimum value for all 1s.

On-Screen Display (OSD). The OSD has a capability of displaying 6 rows x 20 columns of 96 kinds of characters for high resolution (11 x 15 dots) patterns (Figures 8 and 9).

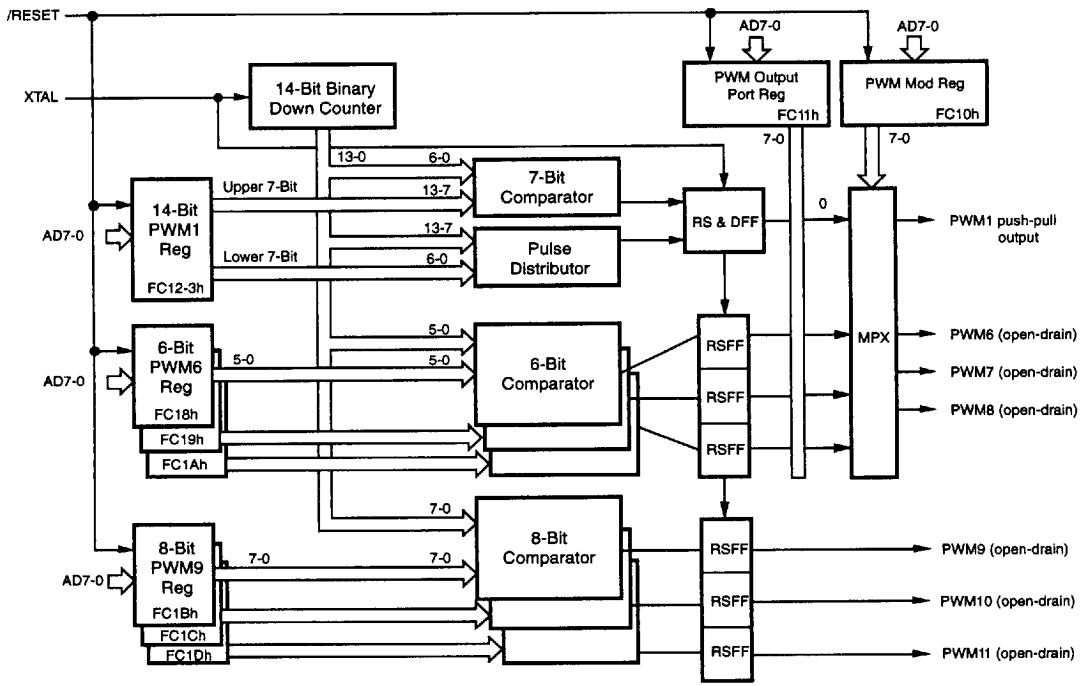


Figure 7. Pulse Width Modulator Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

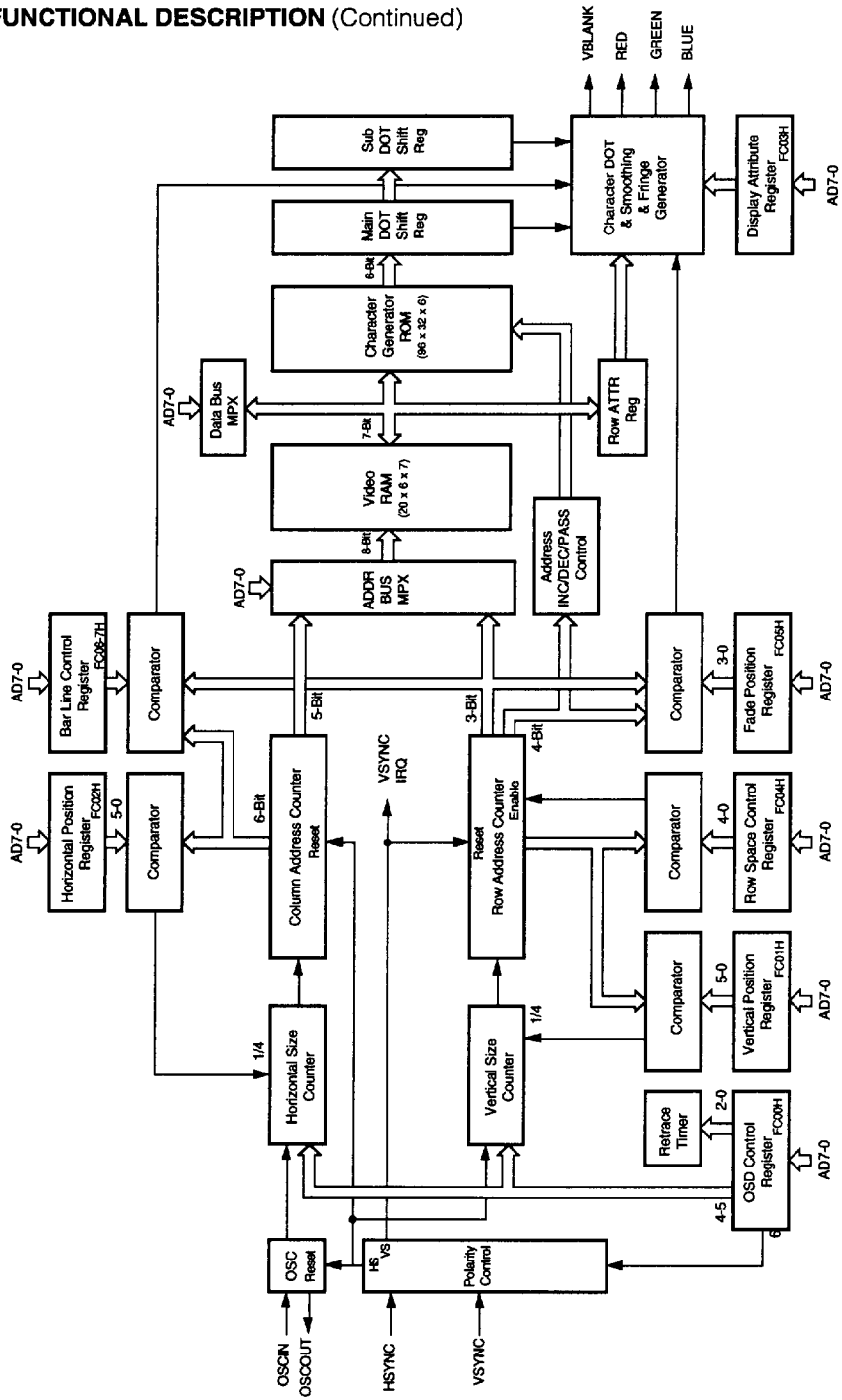


Figure 8. On-Screen Display Block Diagram

The OSD features are as follows:

- **Character Color:** Seven kinds of color are specified on a row basis.
- **Character Pixel Size:** Four character pixel sizes are selected for a high resolution (1HL, 2HL, 3HL, and 4HL) Horizontal Line (HL).
- **Polarity Selections:** Can select active low or high for horizontal/vertical sync input and RGB outputs.
- **Display Position:** Can display 64 vertical positions by 4HL units and 64 horizontal positions by a 4-dot clock.
- **Inter Row Spacing:** Inter row vertical line spacing is set from 2HL to 17HL.
- **Fade In/Out Control:** Fade position can be determined in vertical direction.
- **Bar Line Type Display:** One of the rows is selected to display an analog bar line every half column by setting second color with proper character set.
- **Fringe Function:** Fringe off/on and the color selected.
- **Background Color:** Eight kinds of color including black background color.
- **ON/OFF Control:** Character display, backgrounds are turned on and off.
- **Number of Display Characters:** 6 rows x 20 columns.
- **Character Set:** 96 (11 x 15 dots).

Character Generator ROM. The character generator ROM is organized as 3 Kbytes of six bits. The ROM defines either 11 x 15 dot (high resolution)

Video RAM. The Video RAM is organized as 8-row arrays (21 x 7 bits each, Figure 9). The first location of each row array contains the attribute for that row. Row attributes include programmable character color, row background color and control for background off/on. The next 20 bytes contain row character data. Each character byte contains the ASCII code in order to select one of the 96 displayable characters. LDE or LDEI instructions are required to access the Video RAM (Figure 10).

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FUNCTIONAL DESCRIPTION (Continued)

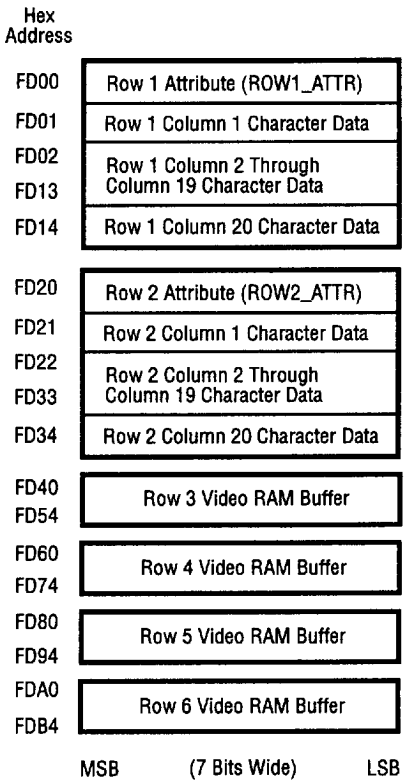

Figure 9. Video RAM Configuration

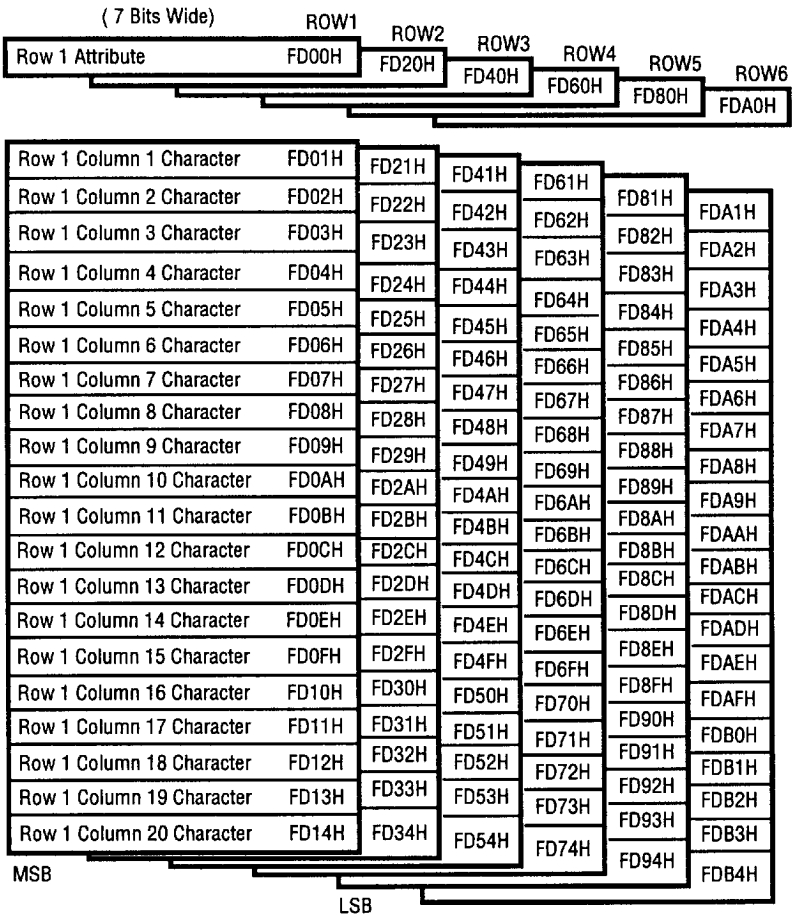

Figure 10. Video RAM Map (Write/Read Registers)

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FUNCTIONAL DESCRIPTION (Continued)

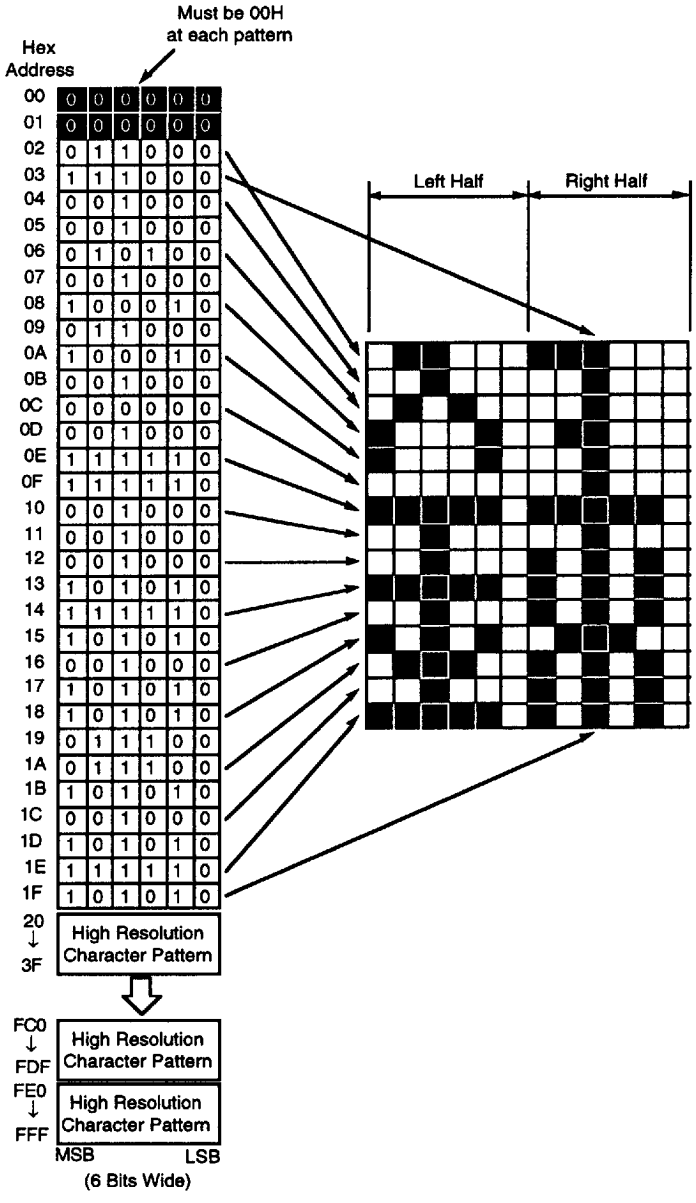

Figure 11. High Resolution Character ROM Configuration

Program Memory. The program ROM size is 6 Kbytes (Figure 12). The IRQ vector table is located in the lower address space. The vector address is fetched after the corresponding interrupt and program control is passed to the specified vector address. IRQ1 vector is fixed to V_{SYNC} interrupt request and occurs at the leading edge of the filtered V_{SYNC} input. Program memory start at address 000CH after reset.

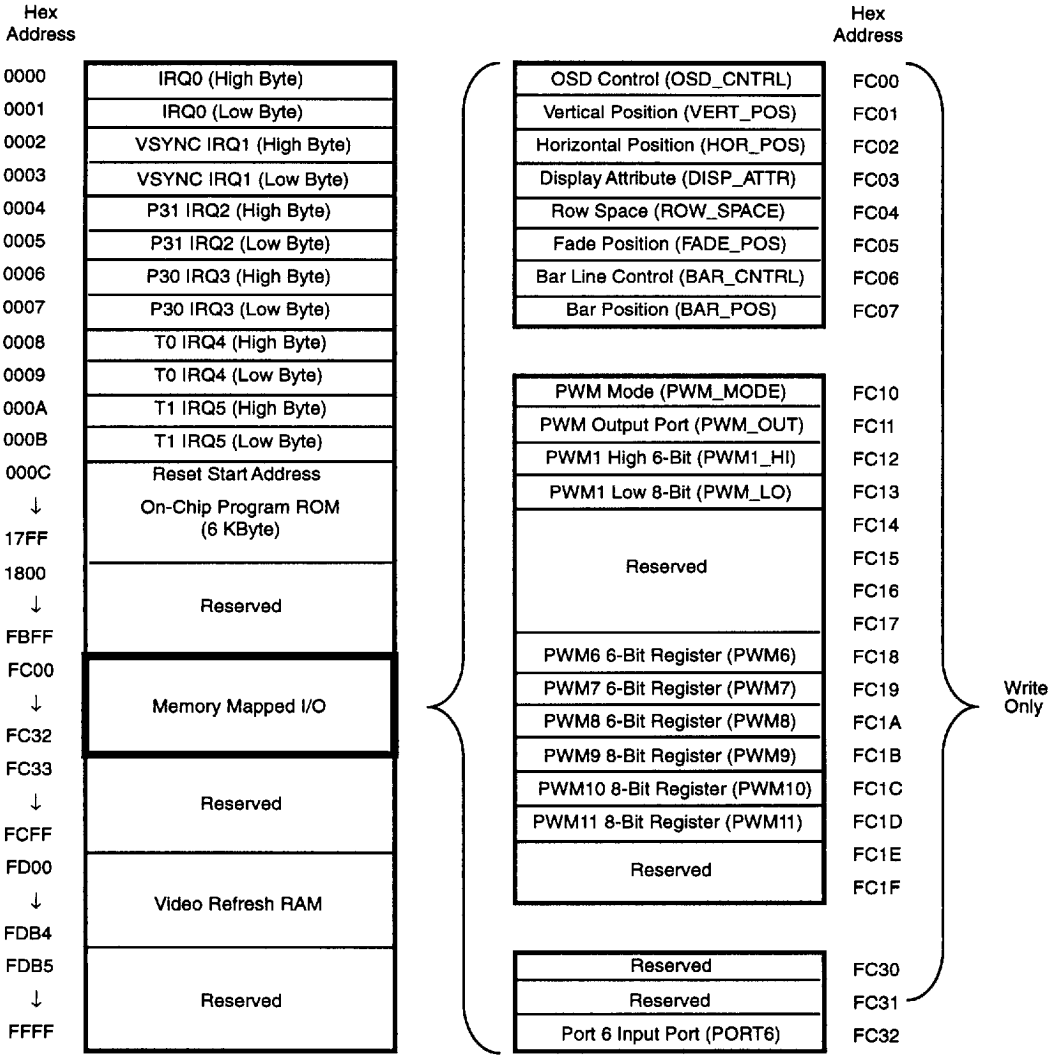

Figure 12. Program Memory

FUNCTIONAL DESCRIPTION (Continued)

Memory Mapped Register. All control registers and I/O ports (except Port 2 and Port 3) are assigned to program memory space. Address space FC00H contains OSD control registers, PWM output registers and Port 6 I/O registers. Two bits of the decoded AFC_{IN} port are assigned to Port 6 input port. LDE and LDEI instructions are required to transfer data between the Register File and the Memory Mapped Registers.

Register File. A total of 253 byte registers are implemented in the Z8 core. Address 00H, 01H and FOH are reserved. The register file consists of two I/O Port registers, 236 general-purpose registers and 15 control and status registers (Figure 13). The instructions can access registers directly or indirectly with an 8-bit address field. This also allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into sixteen working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group (Figure 14).

Note: Register Bank E0-EF is only accessed through a working register and indirect addressing modes.

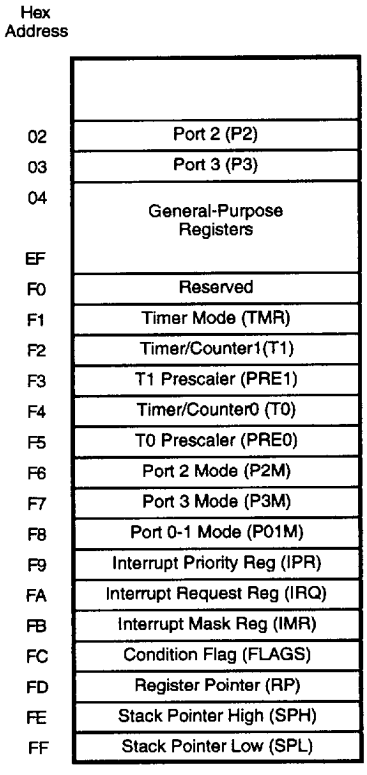

Figure 13. Register File Configuration

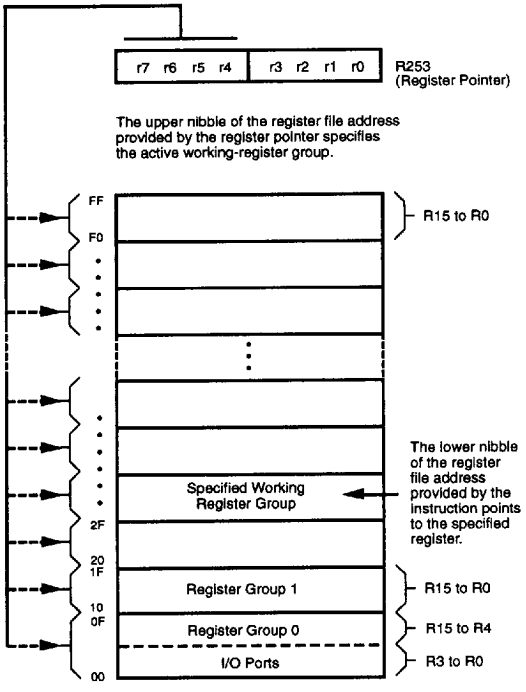

Figure 14. Register Pointer

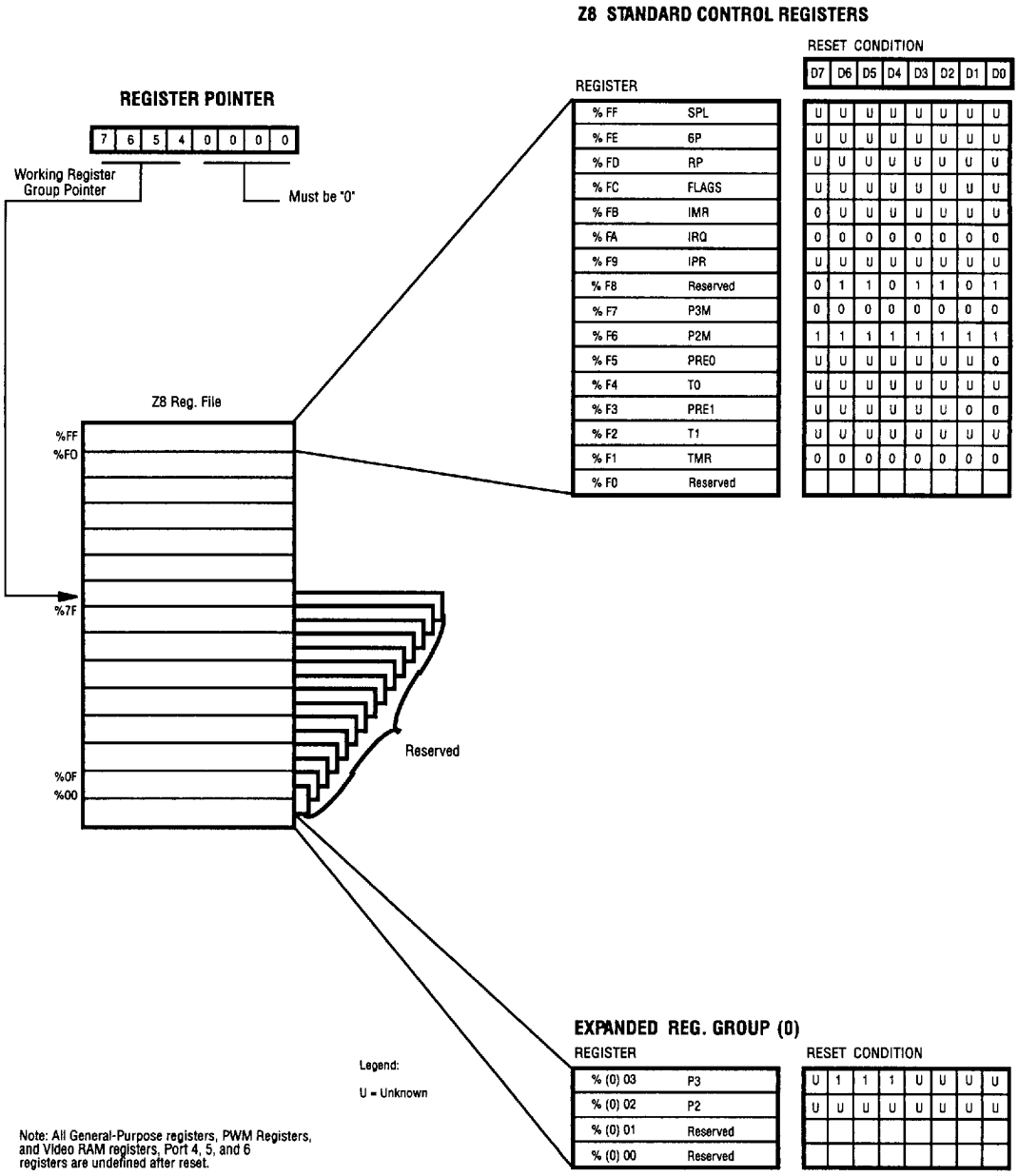

Figure 15. Z86227 Register File Reset Condition

FUNCTIONAL DESCRIPTION (Continued)

Stack. Either the internal register file or the external data memory is used for the stack. An 8-bit Stack Pointer is used for the internal stack that resides within the 236 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (PRE0 and PRE1). The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 16).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user definable and is the internal microprocessor clock (XTAL clock/4), or an external signal input through Port 3, P31. The counter/timers are programmably cascaded by connecting the T0 output to the input of T1.

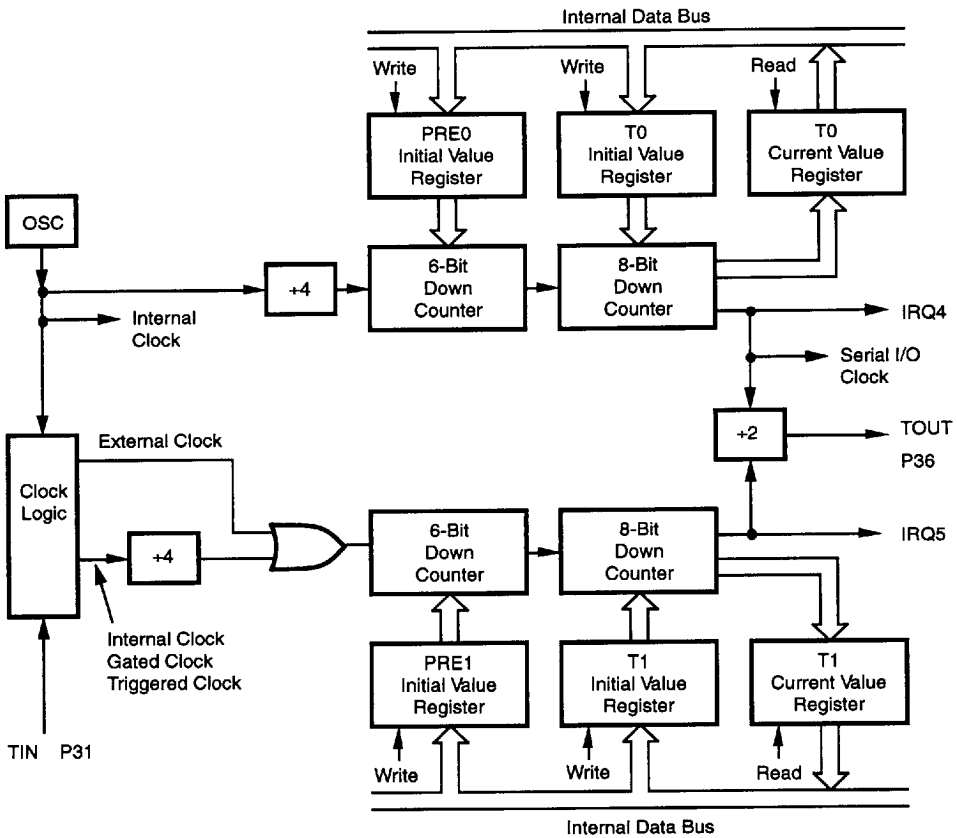

Figure 16. Counter/Timer Block Diagram

Interrupts. The 4LDTC has six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 17). The six sources are divided as follows: two sources are claimed by Port 3 (P30, P31), one by V_{SYNC}, two by the counter/timers, and one is software triggered only.

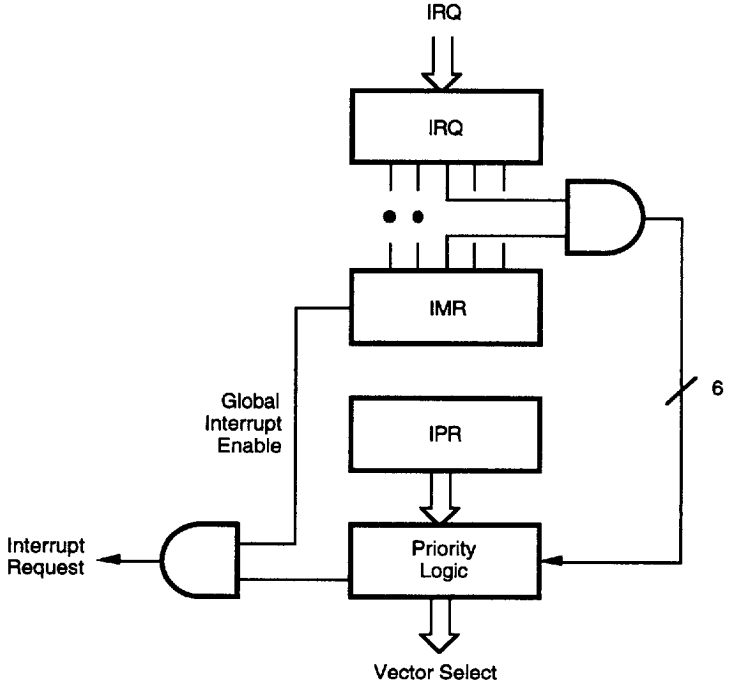

Figure 17. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

HALT Mode. The Z86227 is driven by two internal clocks, TCLK and SCLK. They both oscillate at the crystal frequency. TCLK provides the clock signal for the counter-timers and the interrupt block. SCLK provides the clock signal for all other CPU blocks. HALT mode turns off the internal CPU clock (SCLK), but not the XTAL oscillation. The counter/timers and external interrupts remain active. The device may be recovered by interrupts, either externally or internally generated. An interrupt request may be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. The STOP instruction stops crystal oscillation, thereby stopping both SCLK and TCLK. The device ceases to operate. The STOP mode can be released by two methods. The first method is to reset the device. A high input condition on Port 3 P30 is the second method. After releasing the STOP mode by using either one of the two methods, program execution begins at location 000CH. To complete an instruction prior to entering the standby modes, a NOP instruction has to be placed before the HALT or STOP instructions. This is required because of instruction pipelining, i.e.:

```
FF NOP    ; clear the pipeline
6F STOP   ; enter STOP mode
          or
FF NOP    ; clear the pipeline
7F HALT   ; enter HALT mode
```

Note:
In STOP mode, XTAL2 pin has an internal pull-up on it and OSC_{OUT} has an internal pull-down.

Clock. The Z86227 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal is an AT cut, parallel resonant, 4 MHz max with a series resistance (RS) less than or equal to 100 Ohms.

The crystal source is connected across XTAL1 and XTAL2 using the crystal manufacturer's recommended capacitors (10 pF < CL < 300 pF, where C1=C2=CL) from each pin to device ground (Figure 17).

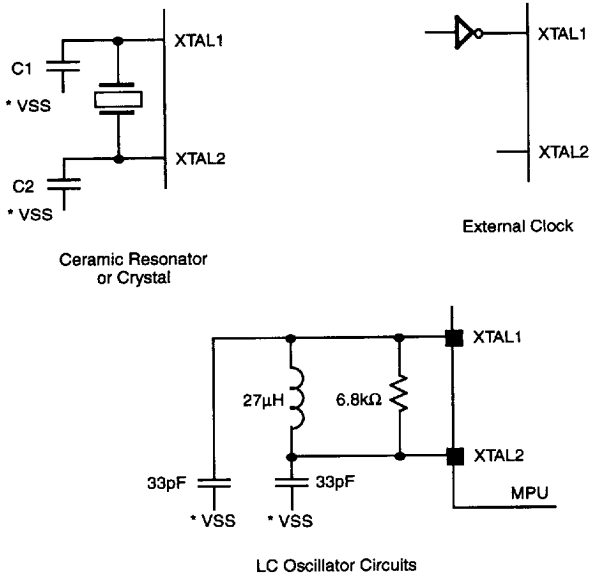

Figure 18. Oscillator Configuration

Watch-Dog Timer (WDT). The Z86227 is equipped with a permanently enabled Watch-Dog Timer which must be refreshed every 12 ms. Failure to refresh the timer results in a reset of the device. The WDT is permanently enabled and is initially reset upon POR. Every subsequent WDT instruction resets the timer. The Watch-Dog Timer may or may not be enabled during the HALT mode. The instruction WDT 4F (HEX) enables the timer during HALT. If the WDH instruction is used, and if the HALT mode is not released and the Watch-Dog Timer is not retriggered (by the WDT instruction) within 12 ms, a device reset occurs. The WDT instruction affects the Z (Zero) S (Sign), and V (Overflow) flags. WDT does not run during STOP mode.

V_{cc} Voltage Sensitive Reset (VSR). Reset is globally driven if V_{cc} is below the specified voltage (Figure 18).

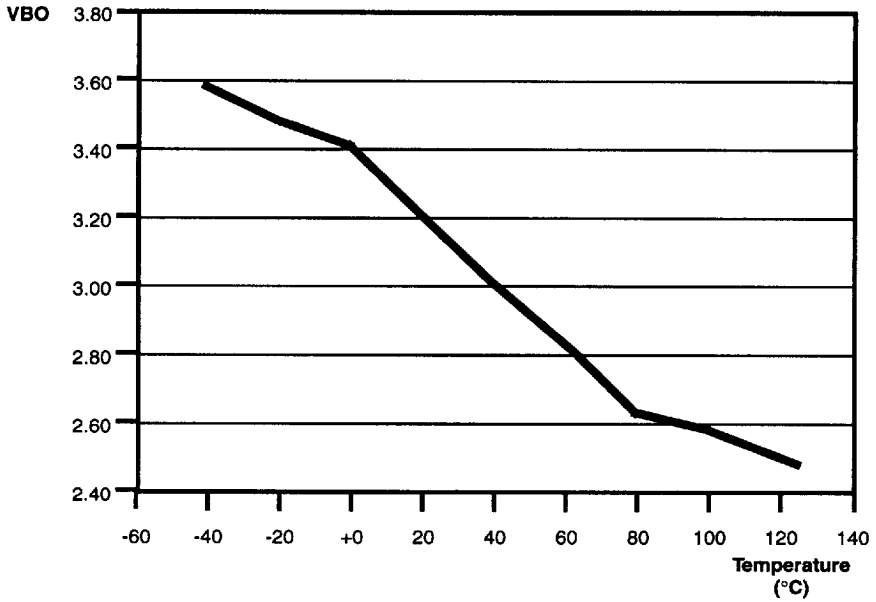

Figure 19. Voltage Sensitive Reset vs Temperature

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Units	Notes
V_{CC}	Power Supply Voltage*	–0.3	+7	V	
V_I	Input Voltage	–0.3	V_{CC} +0.3	V	
V_I	Input Voltage	–0.3	V_{CC} +0.3	V	[1]
V_O	Output Voltage	–0.3	13.2	V	[2, 3]
I_{OH}	Output Current High		–10	mA	1 pin
I_{OH}	Output Current High		–100	mA	All total
I_{OL}	Output Current Low		20	mA	1 pin
I_{OL}	Output Current Low		200	mA	All total
T_A	Operating Temperature	†			
T_{STG}	Storage Temperature	–65	+150	C	

Notes:
[1] Port 2 open-drain
[2] PWM open-drain outputs
[3] Absolute maximum operating voltage 13.2V.
Absolute maximum momentary (non-operating) voltage is 16.0V.
* Voltage on all pins with respect to GND.
† See Ordering Information

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 20).

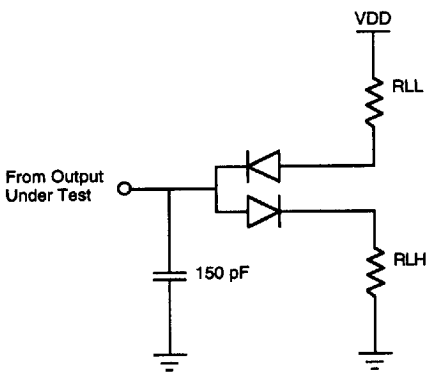

Figure 20. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; Freq =1.0 MHz; unmeasured pins to GND.

Parameter	Max	Units
Input capacitance	10	pF
Output capacitance	20	pF
I/O capacitance	25	pF
AFC_{IN} input capacitance	10	pF

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +4.5V to +5.5V; F_{OSC} = 4 MHz

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	1.48	V	
V_{ILC}	Input XTAL/Osc In Low		0.07 V_{CC}	0.98	V	External Clock Generator Driven
V_{IH}	Input Voltage High	0.7 V_{CC}	V_{CC}	3.0	V	
V_{IHC}	Input XTAL/Osc In High	0.8 V_{CC}	V_{CC}	3.2	V	External Clock Generator Driven
V_{HY}	Schmitt Hysteresis	0.1 V_{CC}		0.8	V	
V_{PU}	Maximum Pull-Up Voltage		13.2		V	[1, 2]
V_{OL}	Output Voltage Low		0.4	0.16	V	I_{OL}=1.00 mA
			0.4	0.19	V	I_{OL}=0.75 mA [1]
V_{00-01}	AFC Level 01 In		0.45 V_{CC}	1.9	V	
V_{01-11}	AFC Level 11 In	0.5 V_{CC}	0.75 V_{CC}	3.12	V	
V_{OH}	Output Voltage High	V_{CC}–0.4		4.75	V	I_{OH}=–0.75 mA
I_{IR}	Reset Input Current		–80	–46	µA	V_{RL}=0V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	0V, V_{CC}
I_{OL}	Tri-State Leakage	–3.0	3.0	0.02	µA	0V, V_{CC}
I_{CC}	Supply Current		20	13.2	mA	All inputs at rail & outputs floating
I_{CC1}			6	3.2	mA	All inputs at rail & outputs floating
I_{CC2}			10	2.0	µA	All inputs at rail & outputs floating

Note:
[1] PWM open-drain
[2] Recommended operating voltage 12V with maximum positive tolerance 10%, i.e., 13.2V.

5

AC CHARACTERISTICS
Timing Diagrams

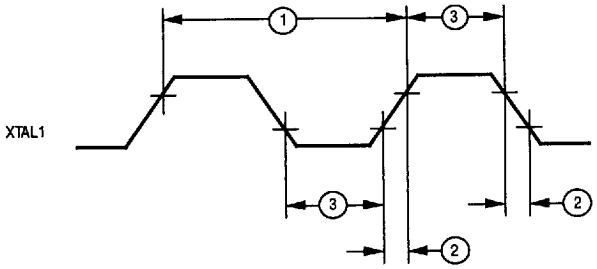

Figure 21. External Clock

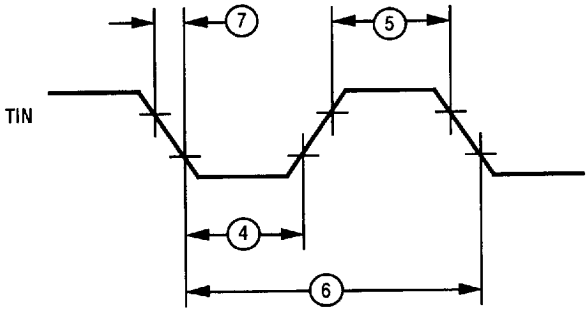

Figure 22. Counter Timer

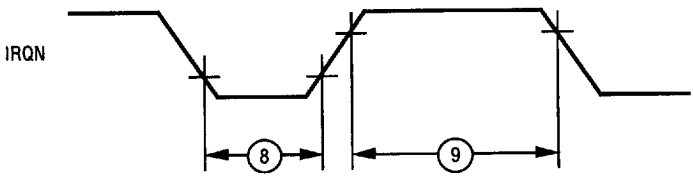

Figure 23. Interrupt Request

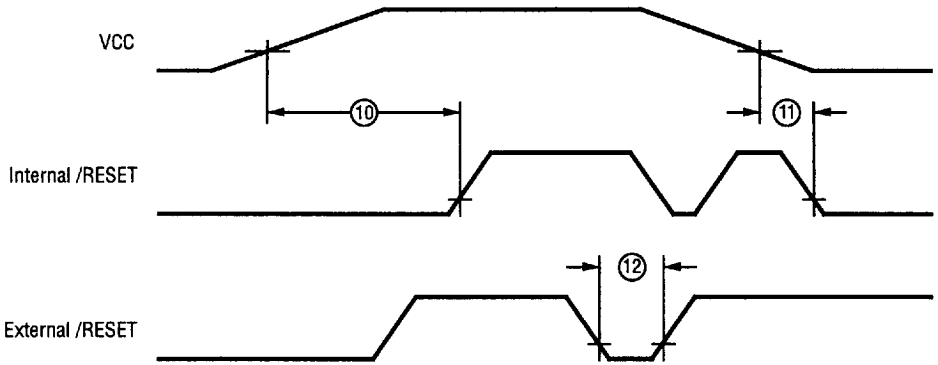

Figure 24. Power-On Reset

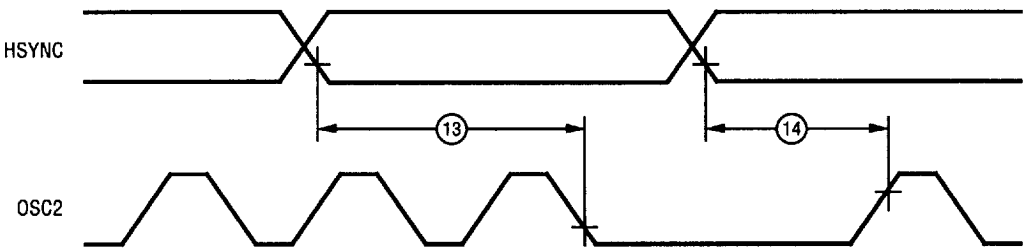

Figure 25. On-Screen Display

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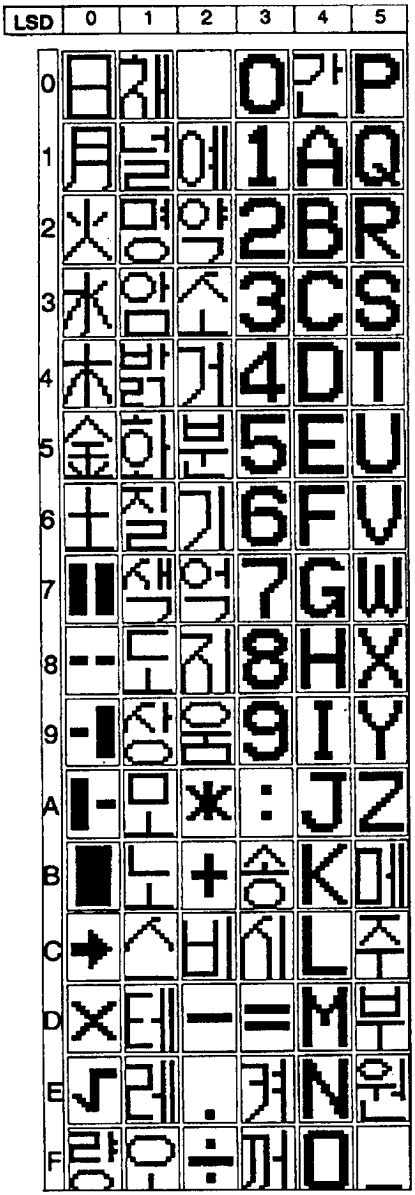
AC CHARACTERISTICS

T_A = 0° C to +70° C; V_{CC} = +4.5V to +5.5V; F_{OSC} = 4 MHz

No	Symbol	Parameter	Min	Max	Unit
1	TpC	Input Clock Period	250	1000	ns
2	TrC,TfC	Clock Input Rise and Fall		15	ns
3	TwC	Input Clock Width	125		ns
4	TwTinL	Timer Input Low Width	70		ns
5	TwTinH	Timer Input High Width	3TpC		
6	TpTin	Timer Input Period	8TpC		
7	TrTin,TfTin	Timer Input Rise and Fall		100	ns
8a	TwIL	Int Req Input Low	70		ns
8b	TwIL		3TpC		
9	TwIH	Int Request Input High	3TpC		
10	TdPOR	Power On Reset Delay	25	100	ms
11	TdLVIRES	Low Voltage Detect to Internal RESET Condition	200		ns
12	TwRES	Reset Minimum Width	5TpC		
13	TdHsOl	H_{SYNC} Start to V_{OSC} Stop	2TpV	3TpV	
14	TdHsOh	H_{SYNC} End to V_{OSC} Start		1TpV	
15	TdWDT	WDT Refresh Time		12	ms

Note:
Refer to DC Characteristics for details on switching levels.

STANDARD CHARACTER SETS



SUMMARY

Input/Output Circuits

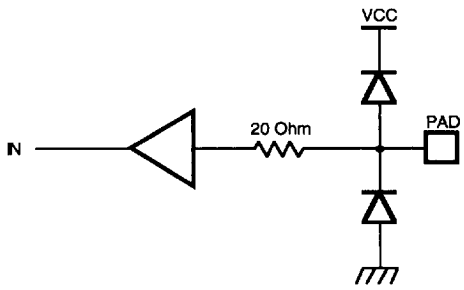


Figure 26. Input Only
(Pad Type 1)

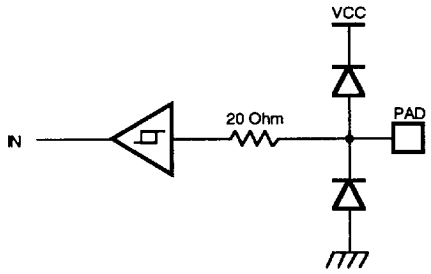


Figure 27. Input Only, Schmitt-Triggered
(Pad Type 2)

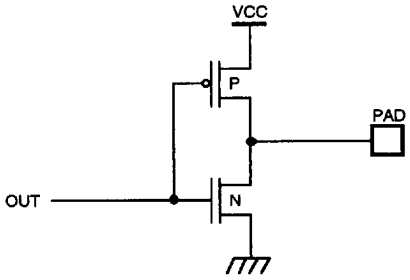


Figure 28. Output Only
(Pad Type 3)

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SUMMARY
Input/Output Circuits (Continued)

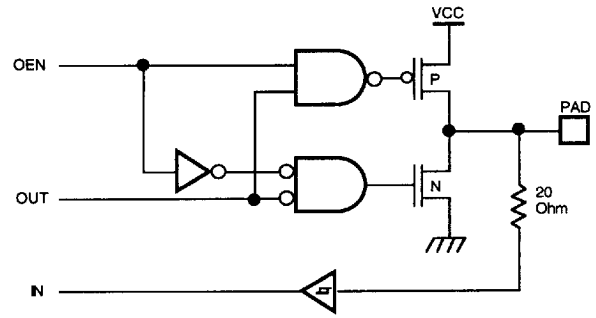

Figure 29 Input/Output Tri-State
(Pad Type 4)

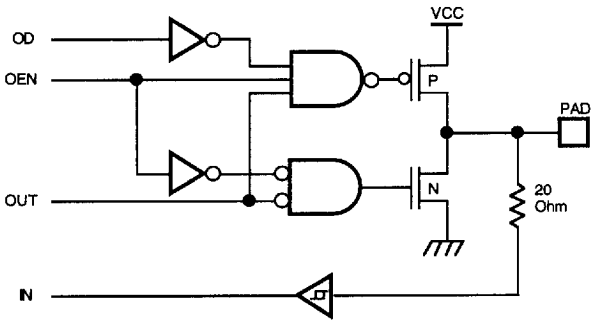

Figure 30. Input/Output, Tri-State, Open-Drain
(Pad Type 5)

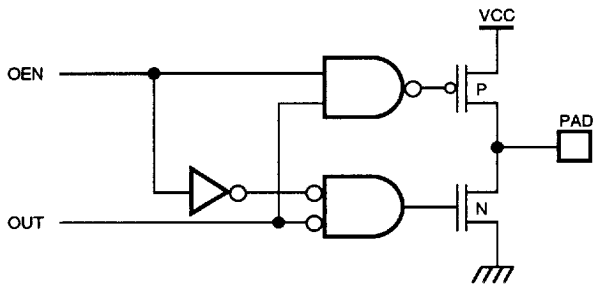

Figure 31. Output Only, Tri-State
(Pad Type 6)

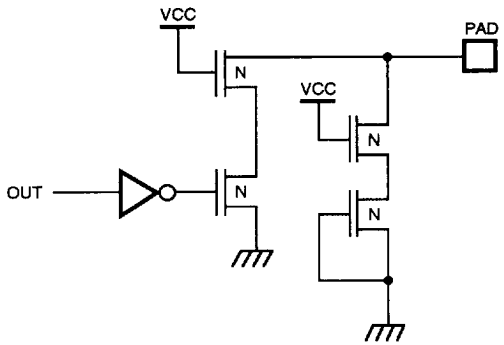

Figure 32. Output Only, 12-Volt Open-Drain
(Pad Type 7)

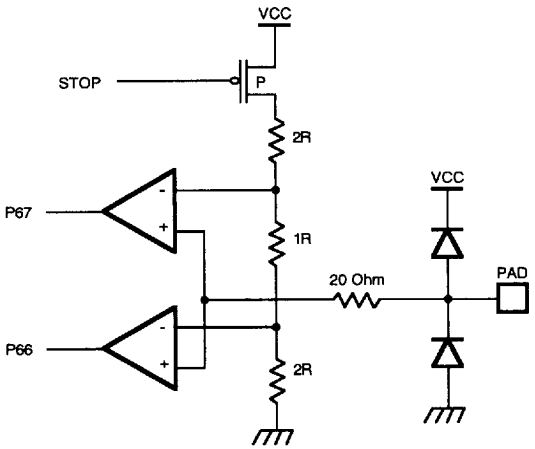

Figure 34. AFC Input Circuit
(Pad Type 9)

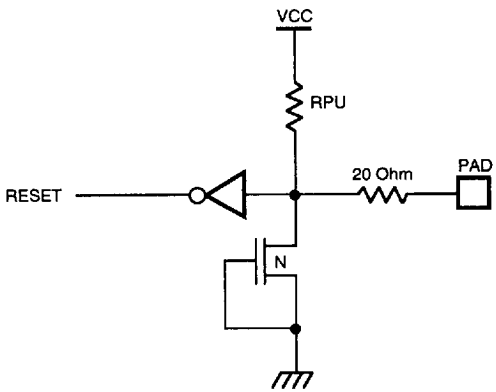

Figure 33. Reset Input Circuit
(Pad Type 8)

Mapping of Symbolic Pad Types to Pin Functions

Pin Name	Pad Type
XTAL1, OSC_{IN}	1
XTAL2, OSC_{OUT}	*
/RESET	8
P20-P27	5
P30-P31	2
P34-P36	3
P60-P65	2
AFC_{IN}	9
H_{SYNC}, V_{SYNC}	2
VRED, VBLUE, VGREEN,	3
VBLANK	3
PWM1	3
PWM [6 -11]	7

Note:
*High gain start, low gain run amplifier circuit.

DTC CONTROL REGISTER DIAGRAMS
Port Registers

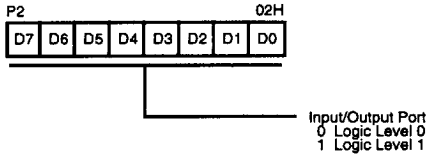

Figure 35. Port 2 Register
(Read/Write)

Figure 36. Port 2 Mode Register
(Write Only)

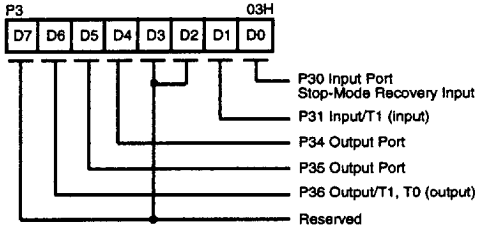

Figure 37. Port 3 Register
(P30, P31 Read Only)
(P34, P35, P36 Write Only)

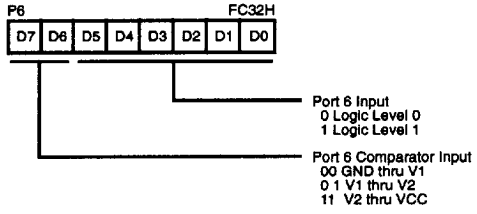

Figure 38. Port 6 Register
(Read Only)

DTC CONTROL REGISTER DIAGRAMS
PWM Registers

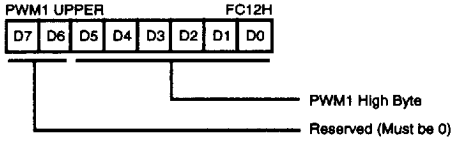

Figure 39. PWM 1 High Value
(Write Only)

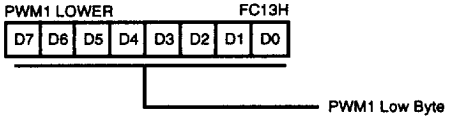

Figure 40. PWM 1 Low Value
(Write Only)

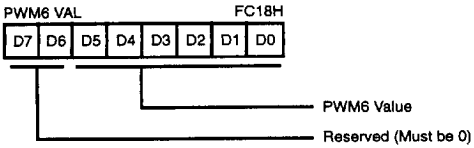

Figure 41. PWM 6 Value
(Write Only)

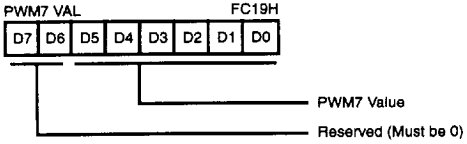

Figure 42. PWM 7 Value
(Write Only)

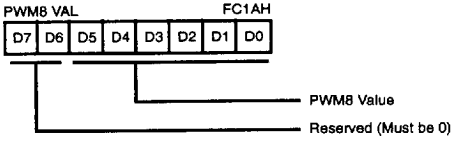

Figure 43. PWM 8 Value
(Write Only)

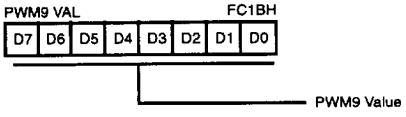

Figure 44. PWM 9 Value
(Write Only)

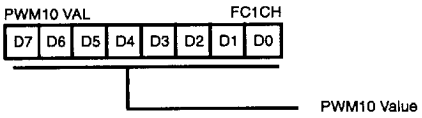

Figure 45. PWM 10 Value
(Write Only)

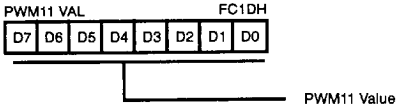

Figure 46. PWM 11 Value
(Write Only)

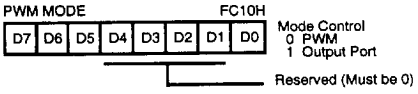

Figure 47. PWM Mode Register
(Write Only)

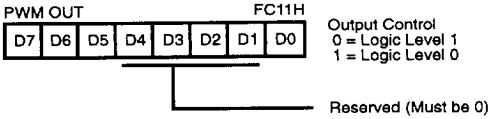

Figure 48. PWM Port Output Register
(Write Only)

5

DTC CONTROL REGISTER DIAGRAMS

Z8 Microcontroller Control Register Diagrams (Continued)

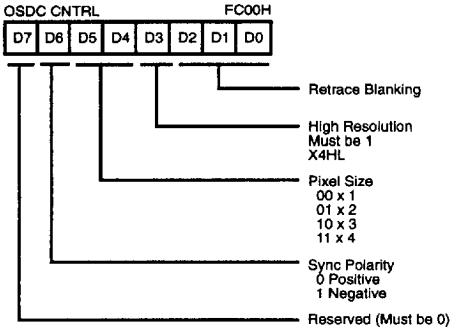

Figure 49. OSD Control Register
(Write Only)

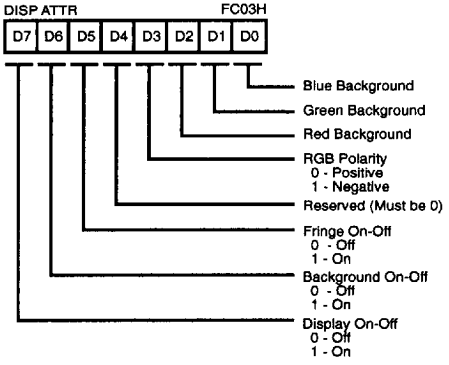

Figure 52. OSD Display Attribute Register
(Write Only)

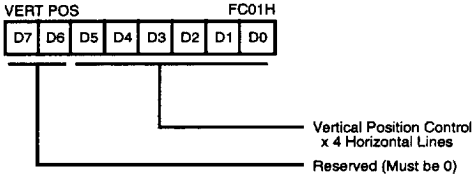

Figure 50. OSD Vertical Position Register
(Write Only)

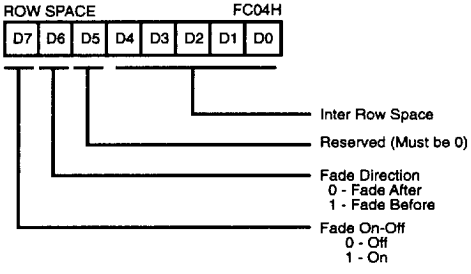

Figure 53. OSD Row Space Register
(Write Only)

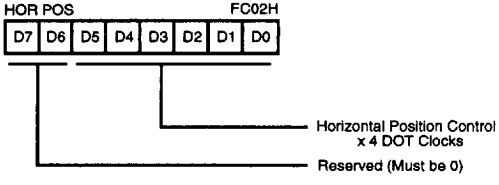

Figure 51. OSD Horizontal Position Register
(Write Only)

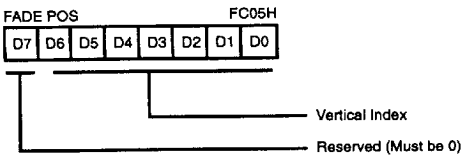

Figure 54. OSD Fade Position Register
(Write Only)

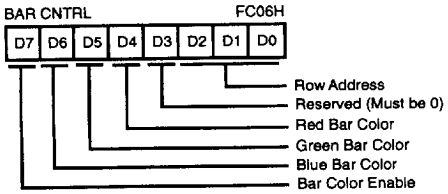

Figure 55. OSD Bar Control Register
(Write Only)

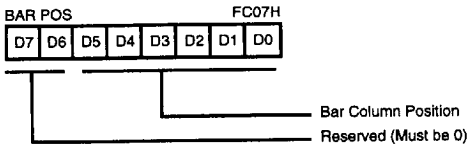

Figure 56. OSD Bar Position Register
(Write Only)

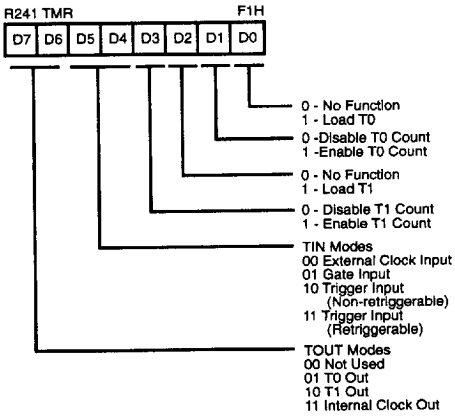

Figure 57. Timer Mode Register
(F1H; Read/Write)

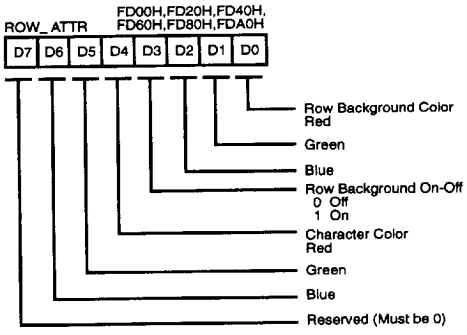

Figure 58. ROW_ATTR Register
(Write Only)

DTC CONTROL REGISTER DIAGRAMS

Z8 Microcontroller Control Register Diagrams (Continued)

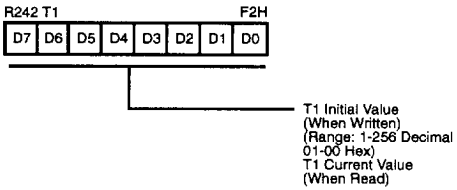

Figure 59. Counter Timer 1 Register
(F1H; Read/Write)

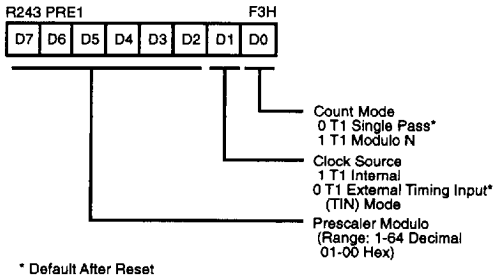

Figure 60. Prescaler 1 Register
(F3H; Write Only)

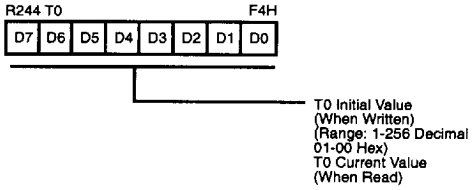

Figure 61. Counter/Timer 0 Register
(F4H; Read/Write)

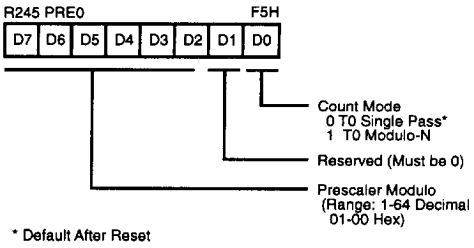

Figure 62. Prescaler 0 Register
(F5H; Write Only)

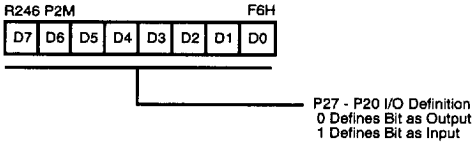

Figure 63. Port 2 Mode Register
(F6H; Write Only)

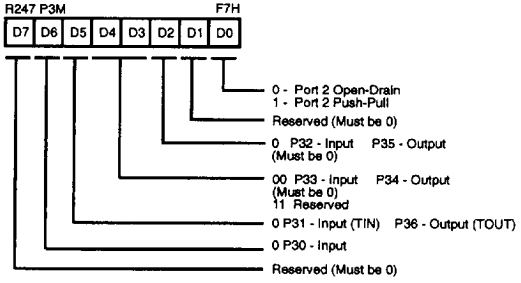

Figure 64. Port 3 Mode Register
(F7H; Write Only)

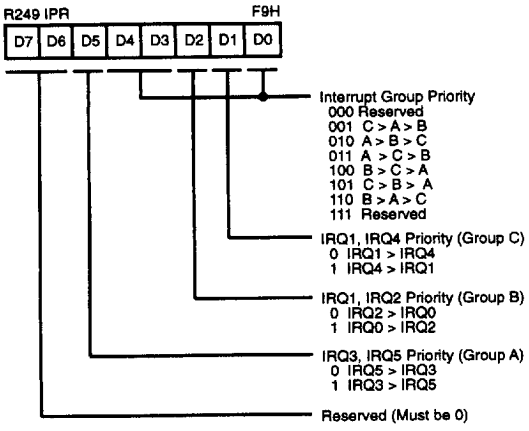

Figure 65. Interrupt Priority Register
(F9H; Write Only)

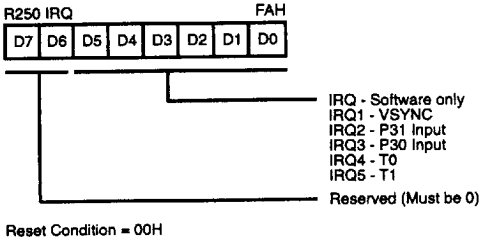

Figure 66. Interrupt Request Register
(FAH; Read/Write)

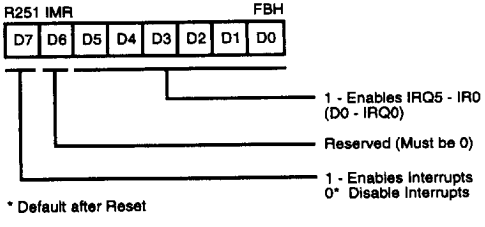

Figure 67. Interrupt Mask Register
(FBH; Read/Write)

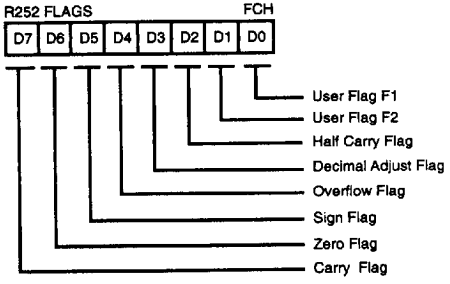

Figure 68. Flag Register
(FCH; Read/Write)

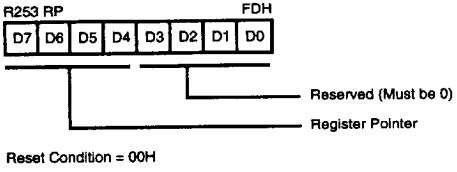

Figure 69. Register Pointer
(FDH; Read/Write)

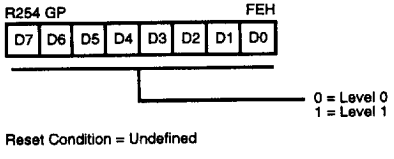

Figure 70. General-Purpose
(FEH; Read/Write)

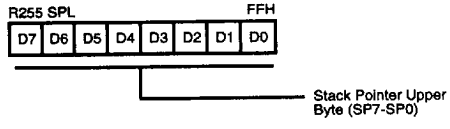

Figure 71. Stack Pointer
(FFH; Read/Write)

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INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

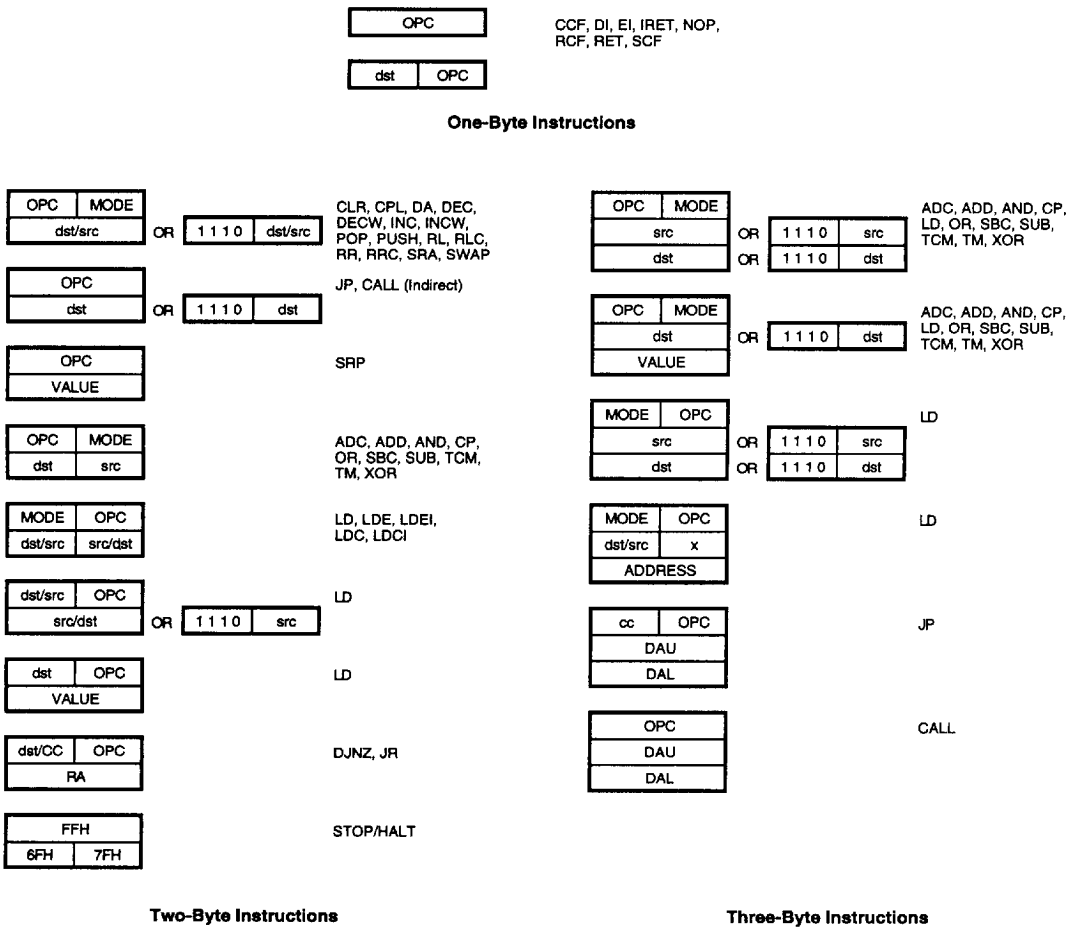
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	T	Always True (Never False)	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	–	*	*	0	–	–
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	–	–	–	–	–	–
CCF C←NOT C			EF	*	–	–	–	–	–
CLR dst dst←0	R IR		B0 B1	–	–	–	–	–	–
COM dst dst←NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src dst – src	†		A[ ]	*	*	*	*	–	–
DA dst dst←DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst dst←dst – 1	R IR		00 01	–	*	*	*	–	–
DECW dst dst←dst – 1	RR IR		80 81	–	*	*	*	–	–
DI IMR(7)←0			8F	–	–	–	–	–	–
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	–	–	–	–	–	–
EI IMR(7)←1			9F	–	–	–	–	–	–
HALT			7F	–	–	–	–	–	–

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	–	*	*	*	–	–
INCW dst dst←dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	–	–	–	–	–	–
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	–	–	–	–	–	–
LDC dst, src	r	Irr	C2	–	–	–	–	–	–
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	–	–	–	–	–	–

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INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	–	–	–	–	–	–
OR dst, src dst←dst OR src	†		4[ ]	–	*	*	0	–	–
POP dst dst←@SP; SP←SP + 1	R IR		50 51	–	–	–	–	–	–
PUSH src SP←SP – 1; @SP←src		R IR	70 71	–	–	–	–	–	–
RCF C←0			CF	0	–	–	–	–	–
RET PC←@SP; SP←SP + 2			AF	–	–	–	–	–	–
RL dst	R IR		90 91	*	*	*	*	–	–
RLC dst	R IR		10 11	*	*	*	*	–	–
RR dst	R IR		E0 E1	*	*	*	*	–	–
RRC dst	R IR		C0 C1	*	*	*	*	–	–
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	–	–	–	–	–
SRA dst	R IR		D0 D1	*	*	*	0	–	–
SRP src RP←src		Im	31	–	–	–	–	–	–

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	–	–	–	–	–	–
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	–	–
TCM dst, src (NOT dst) AND src	†		6[ ]	–	*	*	0	–	–
TM dst, src dst AND src	†		7[ ]	–	*	*	0	–	–
WDH			4F	–	X	X	X	–	–
WDT			5F	–	X	X	X	–	–
XOR dst, src dst←dst XOR src	†		B[ ]	–	*	*	0	–	–

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

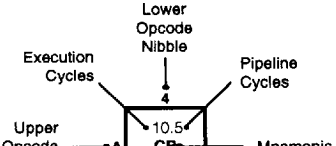
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								6.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2				3		1	



Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

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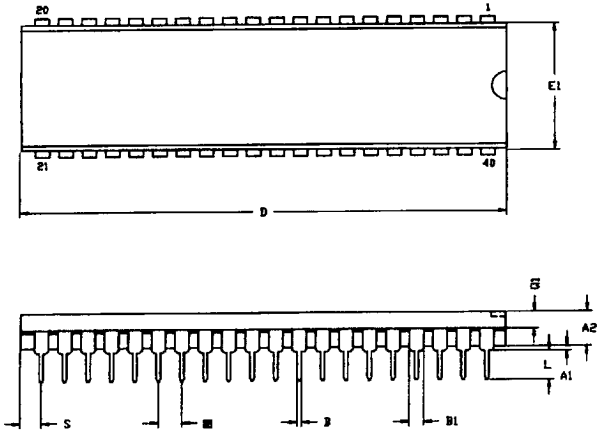
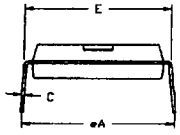
PACKAGE INFORMATION





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram

ORDERING INFORMATION

Z86227

4 MHz
40–Pin DIP
Z8622704PSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

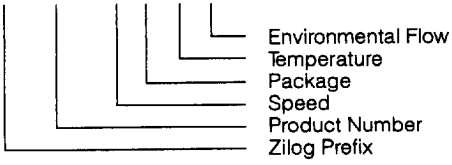
Package
P = Plastic DIP

Temperature
S = 0°C to +70°C

Speed
04 = 4 MHz

Environmental
C= Plastic Standard

Example:
Z 86227 04 P S C is an 86227, 4 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Note:
Four additional letter/numbers will be appended to the end of the part number to identify the individual customer's ROM code.

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