Bluetooth Single-Chip Transceiver IC

Description

The T2901 is a bipolar intergrated circuit manufactured using TEMIC Semiconductors' advanced UHF process. This IC includes a transceiver for the 2.45 GHz ISM band especially for Bluetooth applications.

Features

- Complete Bluetooth transceiver with fully integrated synthesizer and VCO
- TX with advanced closed-loop modulation
- TX PA with +3 dBm output power at 2.5 GHz and ramp-signal generator for optional front end
- Image rejection mixer
- Auxiliary voltage regulator on chip
- Supply-voltage range 2.7 V to 3.3 V (6 V with additional external PNP transistor)
- Few low-cost external components / No mechanical tuning required
- HP-VQFP-N48 package

Block Diagram

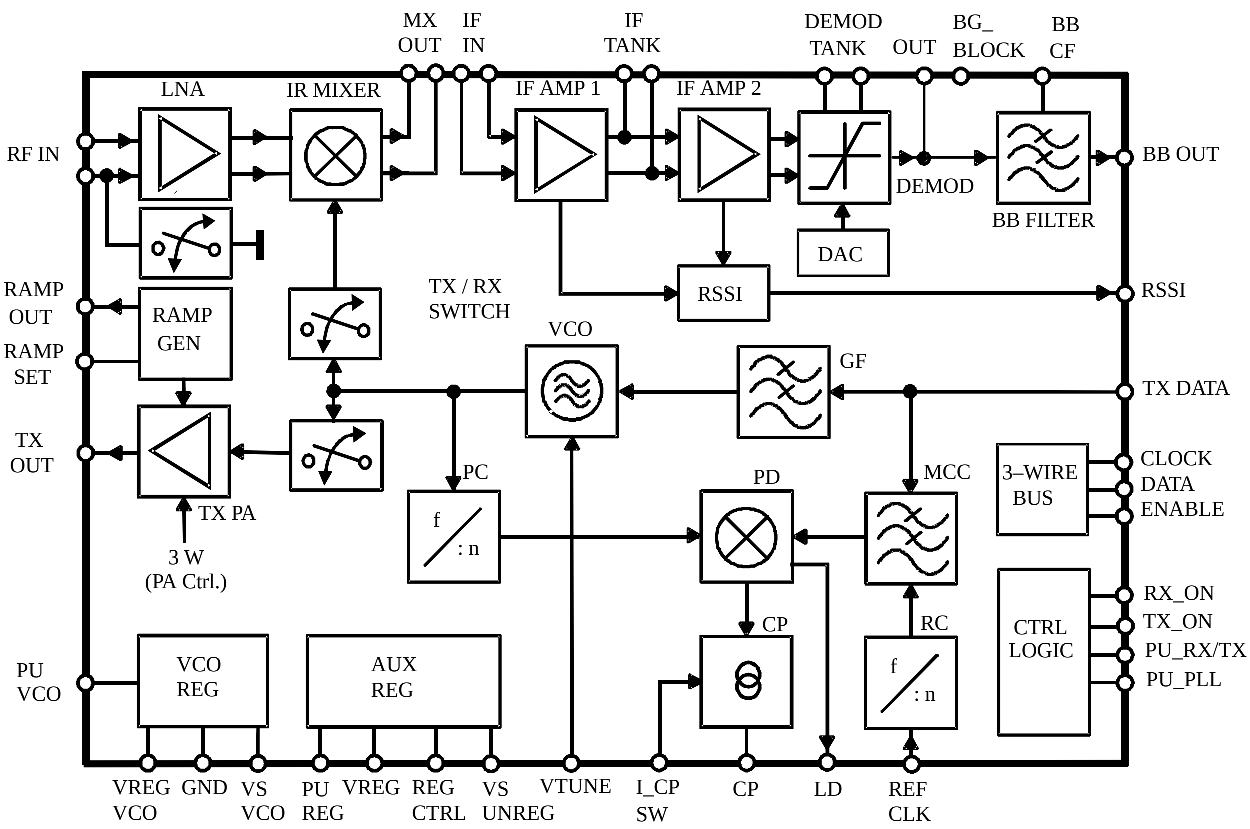


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
T2901– PLT	HP-VQFP-N48	Tray
T2901– PLQ	HP-VQFP-N48	Taped and reeled

Functional Blocks

Name	Description
AUX REG	Auxiliary voltage regulator
BBF	Baseband filter
CP	Charge pump
DAC	D/A converter for demodulator tuning
GF	Gaussian filter for transmit data
IF AMP1	1st intermediate frequency amplifier
IF AMP2	2nd intermediate frequency amplifier
IR MIXER	Image rejection mixer
LNA	Low noise amplifier

Name	Description
MCC	Modulation-compensation circuit
PC	Programmable counter
PD	Phase detector
RAMP GEN	Ramp-signal generator
RC	Reference counter
RSSI	Received signal-strength indicator
TX PA	Transmit power amplifier
VCO	Voltage-controlled oscillator
VCO REG	Voltage regulator for VCO

Pin Description

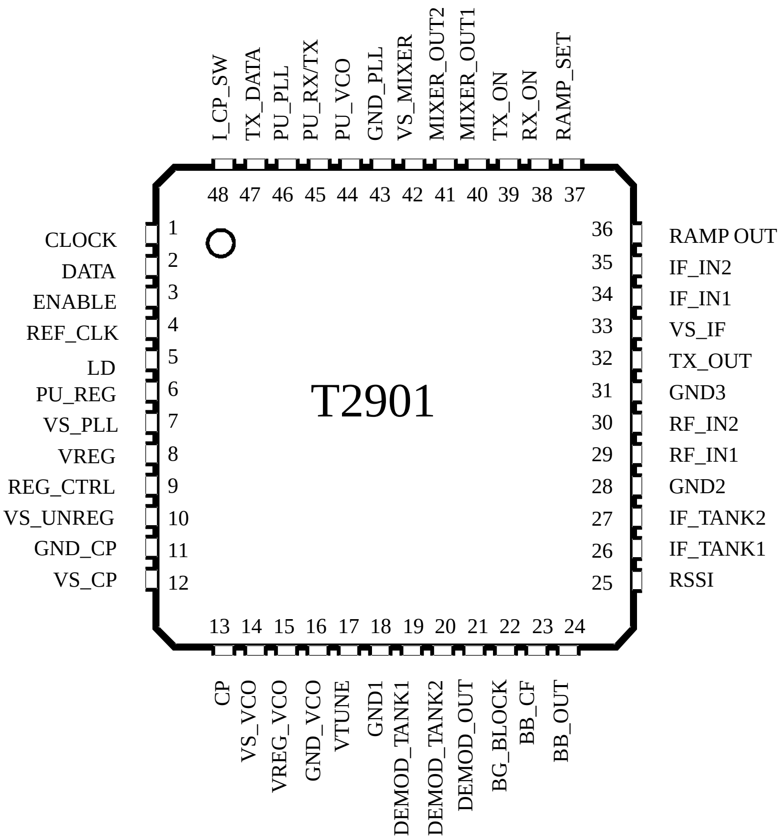


Figure 2. Pinning

Pin Description (continued)

Pin	Symbol	Function
1	CLOCK	3-wire-bus: Clock input
2	DATA	3-wire-bus: Data input
3	ENABLE	3-wire-bus: Enable input
4	REF_CLK	Reference frequency input
5	LD	Lock-detect output
6	PU_REG	Auxiliary voltage regulator power-up input
7	VS_PLL	PLL supply voltage
8	VREG	Aux. voltage regulator output
9	REG_CTRL	Aux. voltage regulator control output
10	VS_UNREG	Aux. voltage regulator supply voltage
11	GND_CP	Charge pump ground
12	VS_CP	Charge pump supply voltage
13	CP	Charge pump output
14	VS_VCO	VCO voltage regulator supply voltage
15	VREG_VCO	VCO voltage regulator control output
16	GND_VCO	VCO ground
17	VTUNE	VCO tuning voltage input
18	GND1	Ground
19	DEMOD_TANK1	Demodulator tank circuit
20	DEMOD_TANK2	Demodulator tank circuit
21	DEMOD_OUT	Demodulator output & BB_IN
22	BG_BLOCK	Bandgap blocking
23	BB_CF	Baseband filter corner frequency control input
24	BB_OUT	Baseband filter output
25	RSSI	Received signal strength indicator output
26	IF_TANK1	IF tank circuit
27	IF_TANK2	IF tank circuit
28	GND2	Ground
29	RF_IN1	RF decoupling
30	RF_IN2	RF input 2 to the image reject mixer
31	GND3	Ground
32	TX_OUT	TX PA output
33	VS_IF	IF amplifier supply voltage
34	IF_IN1	Differential IF input of the IF amplifier
35	IF_IN2	Differential IF input of the IF amplifier
36	RAMP OUT	Ramp generator output for ext. PA power ramping
37	RAMP_SET	Slew rate setting of ramping signal
38	RX_ON	RX section power up control input
39	TX_ON	TX section power up control input
40	MIXER_OUT1	Differential mixer output of the SAW
41	MIXER_OUT2	Differential mixer output of the SAW
42	VS_MIXER	Mixer supply voltage
43	GND_PLL	PLL ground
44	PU_VCO	VCO power-up input
45	PU_RX/TX	RX/TX power-up input
46	PU_PLL	PLL power-up input
47	TX_DATA	TX data input to Gaussian filter and modulation-compensation circuit
48	I_CP_SW	Charge pump current switch

Functional Description

Receiver

The RF-input signal at RF_IN is fed to an image-rejection mixer IR MIXER with its differential outputs MIXER_OUT1 and MIXER_OUT2 driving an IF-SAW filter at 110 MHz/ 111 MHz. The IF amplifiers IF_AMP1 and IF amplifier IF_AMP2 with an external IF_TANK and an integrated RSSI function fed the signal to the demodulator DEMOD working at $f = f_{IF}/2$ (55 MHz/ 55.5 MHz) and finally to an integrated baseband filter BB. For demodulator tuning in production, an integrated 5-bit Digital-to-Analog (D/A) converter is used to control the on-chip varicap diode.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian filter GF and fet to the fully integrated VCO operating at twice the output frequency. After modulation, the signal is frequency-divided by 2 and fed via a TX/RX SWITCH to the TX DRIVER. This bus-controlled driver amplifier supplies +3 dBm output power at TX_OUT. A ramp-signal generator RAMP GEN, providing ramp signals at RAMP_OUT for an external power amplifier, is also integrated. The slope of the ramp signal is controlled by a capacitor at RAMP_SET.

Synthesizer

The IR MIXER, the TX DRIVER and the programmable counter PC are driven by the fully integrated VCO (including on-chip inductors and varactors). An 3-bit Digital-to-Analog converter is used to pretune the frequency. The output signal is frequency-divided to supply the desired frequency to the TX DRIVER, 0/ 90 degreee phase shifter for the IR MIXER and to be used by the PC for the phase detector PD (f_{PD} = 1 MHz). Unlimited multi-slot operation is possible by using the integrated advanced closed-loop modulation concept based on the modulation compensation circuit MCC.

Power Supply

For minimum interference and maximum signal isolation, an integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current-saving modes are provided.

Absolute Maximum Ratings

All voltages are referred to GND (Pins 11, 16, 18, 28, 31 and 43).

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Pins 7, 10, 12, 14, 33 and 42	V_{S_xxx}			6	V
Logic input voltage Pins 1, 2, 3, 6, 38, 39, 44, 45, 46, 48	V_{IN}	– 0.3		6	V
Junction temperature	T_{jmax}			125	°C
Storage temperature	T_{stg}	–40		125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	130	K/W

Operating Range

All voltages are referred to GND (Pins 11, 16, 18, 28, 31 and 43).

Parameter	Symbol	Min.	Typ.	Max.	Unit
Regulated supply voltage Pins 7,12,14, 33 and 42	V_{S_xxx}	2.7	3.0	3.3	V
Unregulated supply voltage Pin 10	V_{S_unreg}	3.0		5.5	V
Ambient temperature	T_{amb}	–20	+25	+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified) : V_S = 3.0 V, T_{amb} = 25°C.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply	**Pins 7, 10, 12, 14, 33 and 42**					
Total supply current	TX	I_S		64		mA
	RX	I_S		69		mA
Standby current	PU = GND	I_S		1	100	µA
LNA + IR mixer	**Pins 29, 30, 40 and 41**					
Image rejection ratio	Pins 40 and 41	IRR	20	30		dB
DSB noise figure	Pins 40 and 41	NFDSB= NFSSB		12		dB
Conversion gain	R_{load} = 400 Ω (differential)	G_{conv}		17		dB
Output interception point	Pins 40 and 41	OIP3		–3		dBm
Receiver sensitivity	P_{in} @ Pin 30, BB out, Pin 24, 12 dB SINAD	P_{in}		–80		dBm
Input impedance	at 2.45 GHz, Pins 29, 30	Z_{in}		5 – j52		Ω
TX PA	**Pin 32**					
Max output power	Pwr setting = max	Pmax	0	3	5	dBm
Min output power	Pwr setting = min	Pmin		–27		dBm
RF leakage	In RX mode	Pleak	–47			dBm
IF amplifier	**Pins 26, 27, 34 and 35**					
Input impedance	Pins 34 and 35	Z_{in}		188		Ω
Lower cut-off frequency		fl_{3dB}		40		MHz
Upper cut-off frequency		fu_{3dB}		313		MHz
Power gain		G_p		85		dB
Bandwidth of external tank circuit	Pins 26 and27	BW_{3dB}		10		MHz
Noise figure		NF		12		dB
RSSI	**Pins 25, 34 and 35**					
RSSI sensitivity	at IF_IN1 , IF_IN2 Pins 34 and 35	P_{min}		20		dBµV
RSSI compression	at IF_IN1 , IF_IN2 Pins 34 and 35	P_{max}		100		dBµV
RSSI dynamic range	at IF_IN1, IF_IN2 Pin 34/35	DR		80		dB
RSSI resolution	Slope of the RSSI has to be steady	Acc		±3		dB
RSSI rise time	P_{in} < 30 to 100 dBµV, Pin 25	t_r		1		µs
RSSI fall time	P_{in} <100 to <30 dBµV, Pin 25	t_f		1		µs
Quiescent output voltage	P_{in} <20 dBµV at IF_IN1, IF_IN2, Pin 25	V_{out}		0.45		V
Maximum output voltage	P_{in} =100 dBµV at IF_IN1, IF_IN2, Pin 25	V_{out}		2.25		V

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_S = 3.0 V, T_{amb} = 25°C.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
FM demodulator	**Pins 19, 20 and 21**					
Co-channel rejection ratio	Pin = –75 dBm at IR-mixer input	CCRR		10		dB
Sensitivity	Quality factor of external tank circuit approx. 20, $f_{res} = f_{IF}/2$ Pin 21	S		0.6		V/MHz
Amplitude of recovered signal	Nominal deviation of signal ± 160 kHz, Pin 21	A		200		mV_{pp}
Output voltage DC range	Pin 21	$FMout_{DC}$	0.4		V_s–0.4	V
Output impedance	Pin 21	Z_{out}		13		kΩ
AM rejection ratio	Pin 21	AMRR		t.b.d		dB
Baseband filter	**Pins 23 and 24**					
3 dB bandwidth	C_{ext} = 56 pF Pin 24	PGBW		1.5		MHz
Output voltage range	Pin 24	Vout	1		Vs–1	V
Common-mode input voltage	Pin 22	Vin	1		Vs–1	V
Ramp generator	**Pin 36**					
Rise time	Cramp = 270 pF at Pin 37	t_r		5		µs
Fall time	Cramp = 270 pF at Pin 37	t_f		5		µs
Minimum output voltage	Accord. PA ramp input	V_{min}		t.b.d.		V
Maximum output voltage	Accord. PA ramp input	V_{max}		t.b.d.		V
Logic input levels	**Pins 1, 2, 3, 38, 39, 47 and 48**					
High input level	=‘1’	V_{iH}	1.5			V
Low input level	=‘0’	V_{iL}			0.5	V
High input current	=‘1’	I_{iH}	–5		5	µA
Low input current	=‘0’	I_{iL}	–5		5	µA
Power / standby	**Pins 6, 44, 45 and 46**					
Power up PU = ‘1’ High input level		V_{PU}	2.0			V
Standby PU = ‘0’ Low input level		$V_{PU,OFF}$			0.7	V
Power up PU = ‘1’ High input current	V_{PU} = 3 V Pin 6 Pin 46 V_{PU} = 5.5 V Pin 46 Pin 44 Pin 45	I_{PU_REG} I_{PU_PL} I_{PU_PL} I_{PU_VCO} $I_{PU\_RX/TX}$	20 100 200 60 60	30 125 300 80 80	40 150 400 100 100	µA µA µA µA µA
Standby PU = ‘0’ Low input current	V_{PU} = 0 V V_{PU} = 0.5 V	$I_{PU,OFF}$			0.1 1	µA µA
Settling time VS = 0 → active operation	Switched VS = 0 to VS = 3 V	t_{soa}		< 10		µs
Settling time standby → active operation	Switched PU = 0 to PU = 1	t_{ssa}		< 10		µs
Settling time active operation→ standby	Switched VS = 3 V to VS = 0	t_{sas}		< 2		µs

Electrical Characteristics (continued)

Test conditions (unless otherwise specified) : V_S = 3.0 V, T_{amb} = 25°C.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
PLL						
Scaling factor prescaler		S_{PSC}		32/33		
Scaling factor main counter		S_{MC}	64		79	
Scaling factor swallow counter		S_{SC}	0		31	
External reference input frequency	AC-coupled sinewave @ 20 ppm accuracy, Pin 4	f_{REF_CLK}		13		MHz
External reference input voltage	AC-coupled sinewave, Pin 4	V_{REF_CLK}	50		250	mV_{RMS}
Total scaling factor reference counter	Pin 4	S_{RC}		13		
Charge pump active when RX, TX Pin 13						
Output current	$V_{I\_CP\_SW}$ = “0” $V_{CP} \leq V_{VS\_CP}$ / 2	I_{CP_1}		±1		mA
	$V_{I\_CP\_SW}$ = “1” $V_{CP} \leq V_{VS\_CP}$ / 2	I_{CP_5}		±5		mA
Current scaling factor	I_{CP} = CPCS x I_{CP_TYP} (see bus protocol D0 ... D1)	CPCS	80		110	%
Leakage current		I_L		± 100		pA
Modulation-compensation circuit @ maximum DSV ≤ 78						
Oversampling	f_{REF_CLK}= 13 MHz	OVS		1		
Integration counter		MAC	–63		+63	
Current scaling factor	(see bus protocol E3 ... E5)	MCCS	60		130	%
3-wire bus						
Clock	Pin 1	f_{clock}			6	MHz
Gaussian transmit filter, Gaussian shape B∗T = 0.5						
Tx data filter clock	f_{REF_CLK} = 13 MHz, TX, 7 taps in filter	f_{TXFCLK}		6.5		MHz
GF adjustment range (for FM deviation adjustm.)	(see bus protocol D6 ... D8)	GFCS	60		130	%
Internal VCO						
Tuning range RX band	@ f_{IF} = 111 MHz	$f_{VCO,RX}$	2289		2389	MHz
Tuning range TX band		$f_{VCO,TX}$	2400		2500	MHz
Phase noise	@ 500 kHz offset Pin 21	N_{VCO}	–95			dBc/Hz
Phase noise, wideband	> 2 MHz offset Pin 21	N_{VCO}	–120			dBc/Hz
Tuning input sensitivity	Pin 17	$S_{VCO,mod}$		50		MHz/V

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Internal VCO PRETUNE 4-bit programming (see bus protocol D2 ... D5)						
Stepwidth		$f_{pretune}$		30		MHz
Lock-detect output	**Pin 5**					
Lock-detect output, test-mode output	locked = ‘1’ unlocked = ‘0’ (test modes see bus protocol E0 ... E2)	LD				
Leakage current	V_{OH} = 3.3 V Pin 5	I_L			5	µA
Saturation voltage	I_{OL} = 0.5 mA Pin 5	V_{SL}			0.4	V

Table of Switch Settings in Different Modes

Mode	Standby	Synthesizer	RX Mode	TX Mode	RSSI
PU_PLL, PU_REG	0	1	1	1	1
PU_RX/TX	0	0	1	1	1
RX_ON	0	0	1	0	1
TX_ON	0	X	0	1	1
PU_VCO	0	1	1	1	1
VCO, PLL, prescaler, RX/TX switch	Off	On	On	On	On
PA, Ramp Gen, MCC, Gaussian filter	Off	Off	Off	On	Off
LNA, IR mixer, IF amplifier	Off	Off	On	Off	On
Demodulator, BB-filter	Off	Off	On	Off	Off

PLL Principle

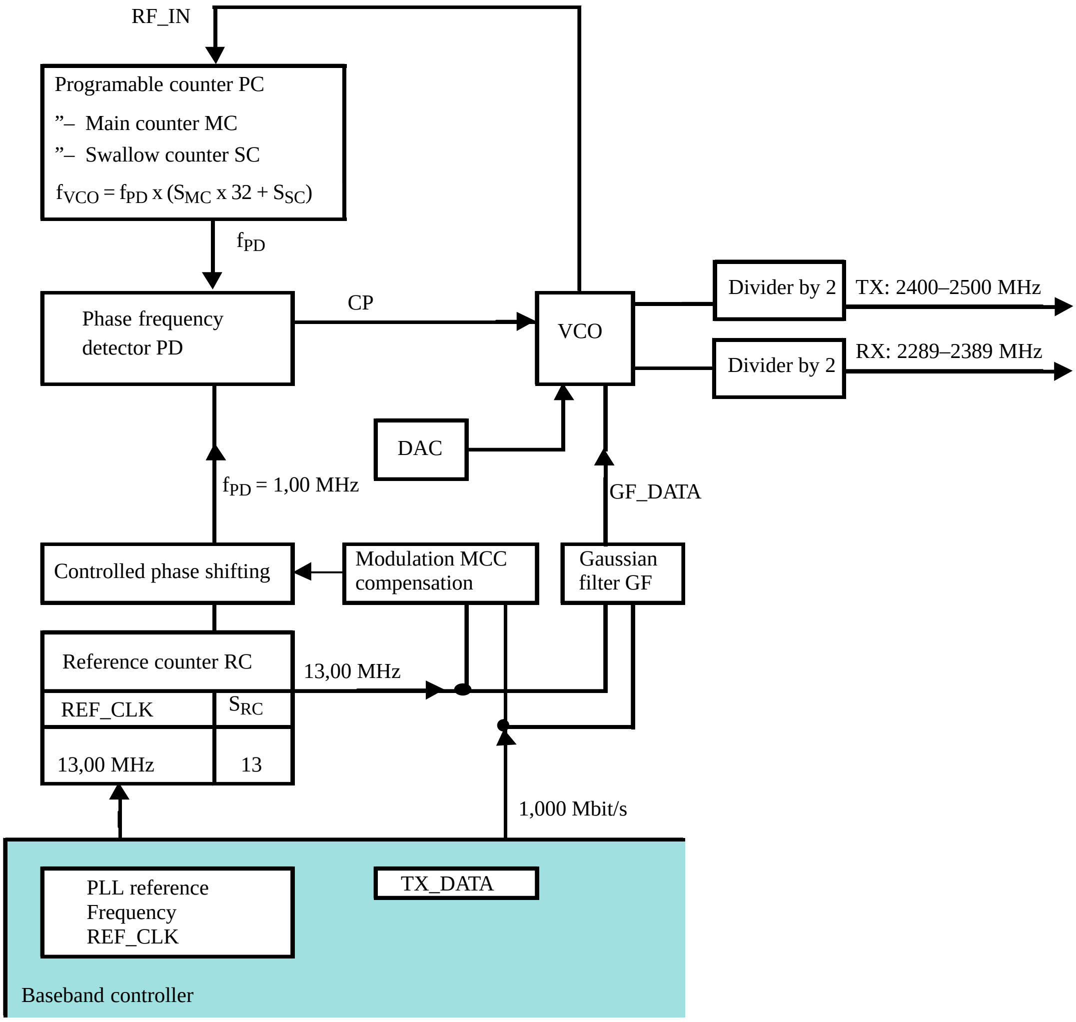


Figure 3. PLL principle

Table 1. The following table shows the maximum programmable LO frequencies for RX and TX.

	f_{IF} [MHz]	f_{RX} [MHz]	f_{TX} [MHz]	S_{MC}	S_{SC}
min	111.0	2159.0	2048.0	64	0
max	111.0	2670.0	2559.0	79	31

Preset of MCC and Gaussian Transmit Filter for TX

After programming the PLL (3-wire bus Enable input going to high level) until start of the Data preamble, it is necessary to send a symmetrical alternating 1/0-datastream.

Serial Programming Bus

Reference and programmable counters can be programmed by the 3-wire bus (CLOCK, DATA and ENABLE). In addition to this information, further control bits such as the scaling of charge pump currents as well as internal currents for the Gaussian lowpass filter and modulation-compensation circuit can be transferred.

After setting the Enable signal to low condition, the data status is transferred bit by bit on the rising edge of the clock signal into the shift register, starting with the MSB-bit. When the Enable signal has returned to high condition, the programmed information is loaded into the addressed latches according to the address-bit condition (last bit). Additional leading bits are ignored and there is no check made how many pulses arrived during Enable low condition. The bus then returns to a low-current standby mode until the Enable signal changes to low again.

Bus Protocol Formats

Standard bit setting: Word 1

MSB																							LSB
Data bits																							Address bit
D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
MC				SC					PS	PA		GF	MCC	GFCS			VCO-DAC				CPCS		1
1	1	0	0	1	0	0	1	1	1	1	0	1	1	0	1	1	1	0	0	0	1	0	1

Word 2

Data bits											Address bit
E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	A0
DEMODDAC					MCCS			TEST			0
1	0	0	0	0	1	0	0	0	0	0	0

PLL Settings

MC (Main Counter)							
			D22	D21	D20	D19	S_{MS}
1	0	0	0	0	0	0	64
1	0	0	0	0	0	1	65
1	0	0	...	...	...	...	...
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

SC (Swallow Counter)					
D18	D17	D16	D15	D14	S_{SC} *)
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	... **)
1	1	0	1	1	30
1	1	1	1	0	31

* S_{SC} = [D14] $\times 2^0$ + [D15] $\times 2^1$ + ... [D218] $\times 2^4$

** $S_{PGD} = 32 \times S_{MC} + S_{SC}$

Gauss Filter and Modulation Compensation Settings

D10	GF (Gaussian Filter)
0	OFF
1	ON

D9	MCC (Modulation Compensation Circuit)
0	OFF
1	ON

D13	PS (Phase Select Modulation-Compensation Circuit)
0	inverted
1	normal

GFCS (Gaussian Filtered Current Settings)			
D8	D7	D6	GFCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

MCCS (Modulation Compensation Current Settings)			
E5	E4	E3	MCCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

Power Amplifier and Charge Pump Settings

PA (Output Power Settings)		
D12	D11	PA
0	0	–17 dBm
0	1	–7 dBm
1	0	–1 dBm
1	1	+3 dBm

CPCS (Charge-Pump Current Settings)		
D1	D0	CPCS
1	0	80%
1	1	90%
0	0	100%
0	1	110%

Pretune DAC Voltage Settings

$V_{TUNE} = V_{CC}/2$

Pretune DAC Voltage (Internal Connection)				
D5	D4	D3	D2	f_{VCO}/%
0	0	0	0	–3.5
0	0	0	1	...
0	0	1	0	...
0	0	1	1	...
0	1	0	0	...
0	1	0	1	...
0	1	1	0	...
0	1	1	1	...
1	0	0	0	0.0
1	0	0	1	...
1	0	1	0	...
1	0	1	1	...
1	1	0	0	...
1	1	0	1	...
1	1	1	0	...
1	1	1	1	+3.5

DEMOD DAC Voltage Settings (DEMODDAC)

Demod DAC Voltage (Internal Connection)					
E10	E9	E8	E7	E6	$f_{IFcenter}$ %
0	0	0	0	0	–3.5
0	0	0	0	1	...
0	0	0	1	0	...
					...
1	1	1	0	1	...
1	1	1	1	0	...
1	1	1	1	1	3.5

Test Mode Settings

Test Output Pin (Lock Detect)			
E2	E1	E0	Signal at lock detect and PLL mode
0	0	0	Lock detect mode
0	0	1	PC out divided by two and CP active (phase changed)
0	1	0	RC out divided by two and CP active (phase changed)
0	1	1	MCCTEST (REF_CLK divided by 1664)
1	0	0	CP tristate only
1	0	1	PC out divided by two and CP high impedance
1	1	0	RC out divided by two and CP high impedance
1	1	1	GFTEST (REF_CLK divided by 4)

3-Wire Bus Protocol Pulse Diagram

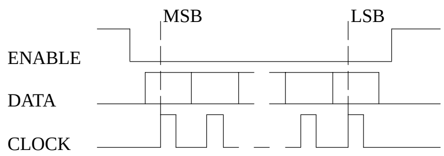


Figure 4.

3-Wire Bus Protocol Timing Diagram

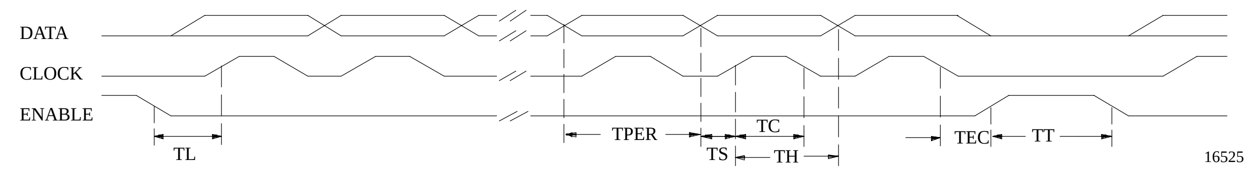
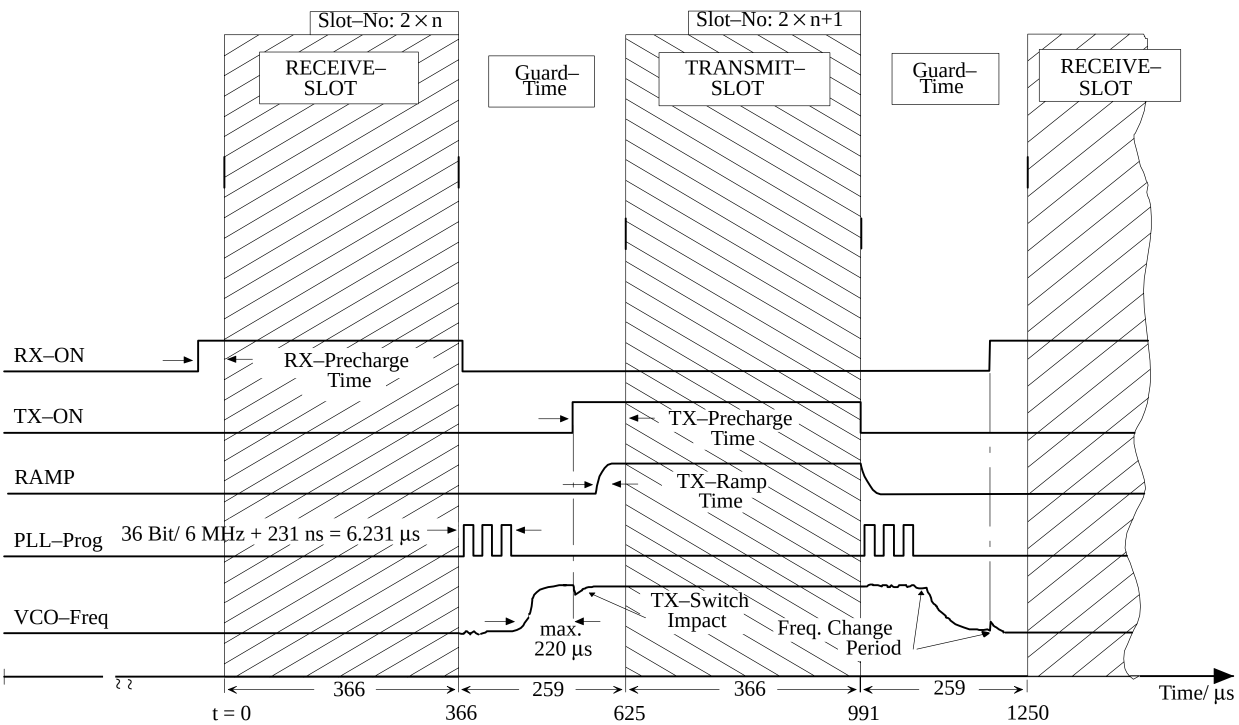


Figure 5.

Table 2. Bus signal times

Description	Symbol	Min. Value	Unit
Clock period	TPER	1/ (6.5 MHz)	µs
Set time data to clock	TS	60	ns
Hold time data to clock	TH	60	ns
Clock pulse width	TC	1/ (13 MHz)	µs
Set time enable to clock	TL	3/ (13 MHz)	µs
Hold time enable to clock	TEC	0	ns
Time between two protocols	TT	3/ (13 MHz)	µs

Bluetooth RX/TX Timing Diagram



Typical Application Circuit

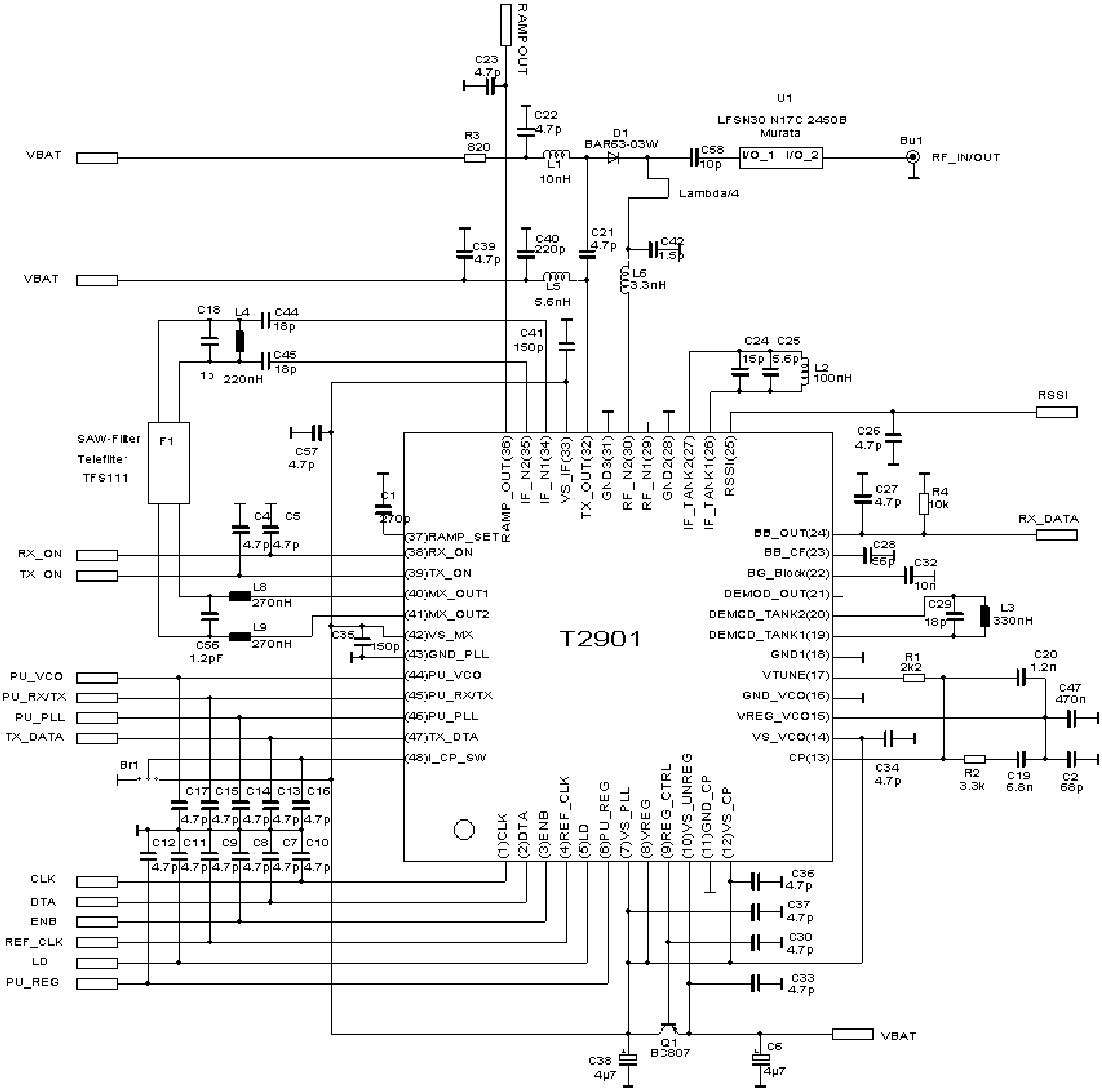


Figure 6. Application circuit

RF Board Measurements

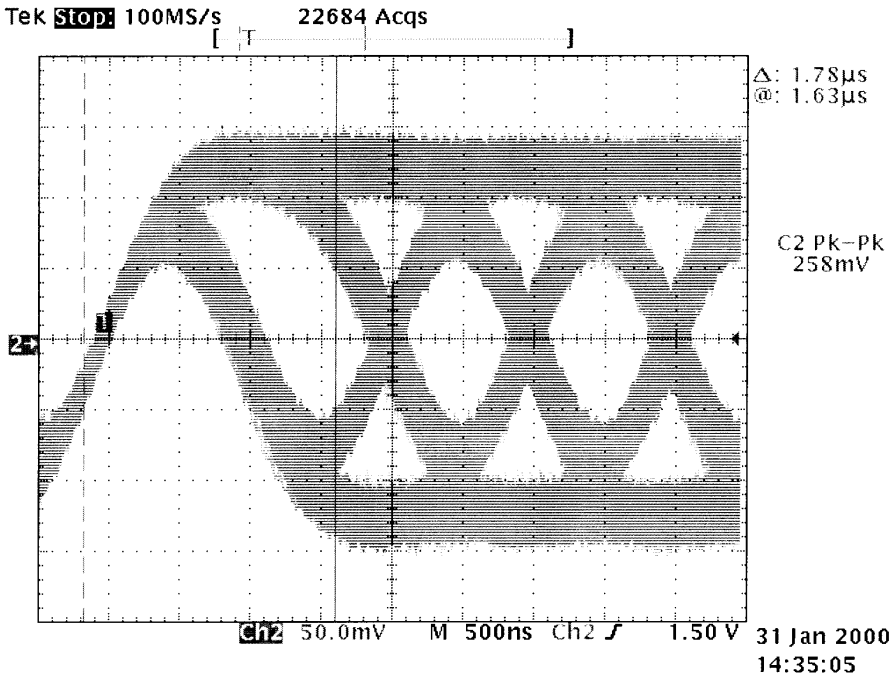


Figure 7. RX mode, Eye pattern with Telefilter TFS111
f = 2450 MHz (signal generator), Pin = –60 dBm, V_{BB} = 1.5 V ± 130 mV
(with optimal tuning of VCODAC and DEMODDAC)

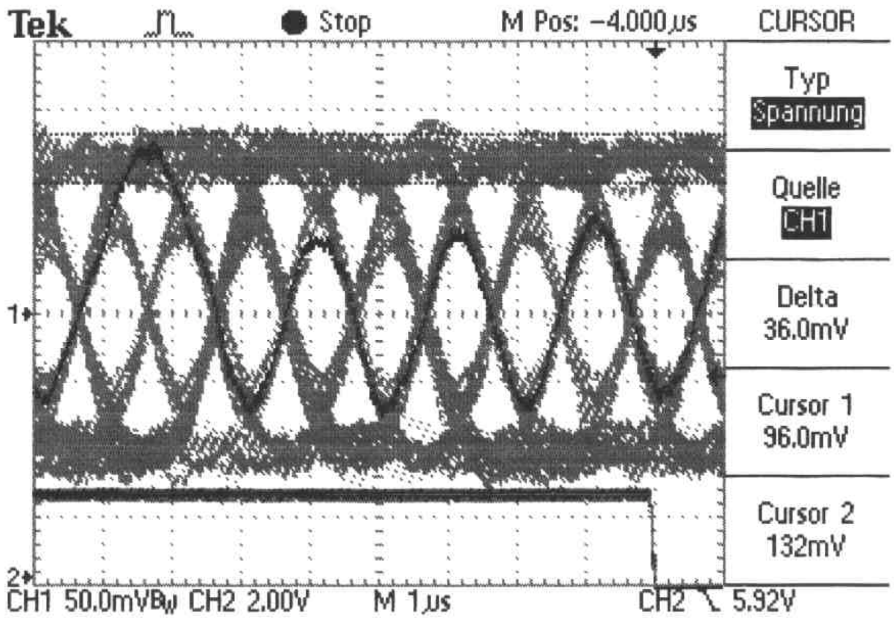


Figure 8. RX / TX mode, Eye pattern Telefilter TFS111
fin = 2450 MHz

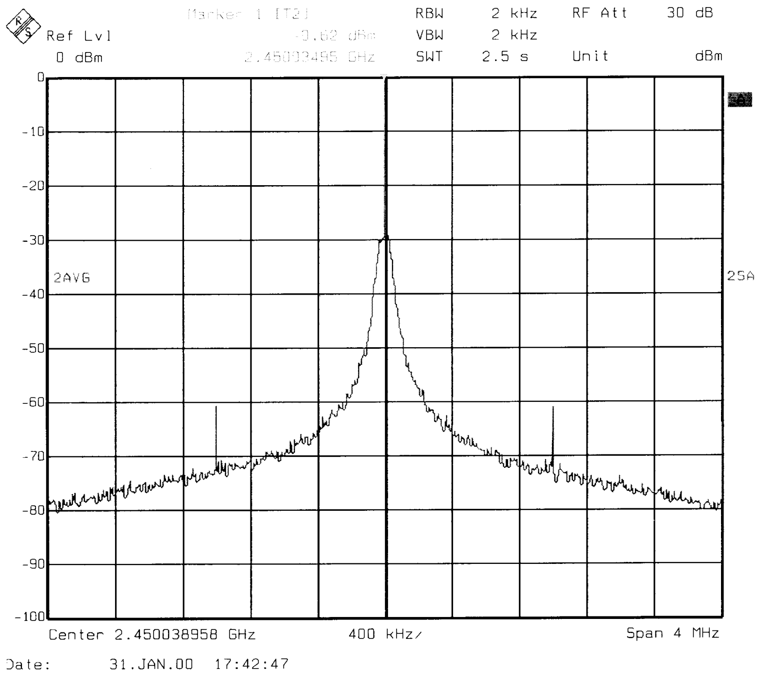


Figure 9. TX spectrum
Pout = 1.4 dBm (corrected for cable attenuation: 2 dB)
Spurious signal suppression > 60 dBc (typical)
PLL loop filter values optimized for settling time < 150 µs

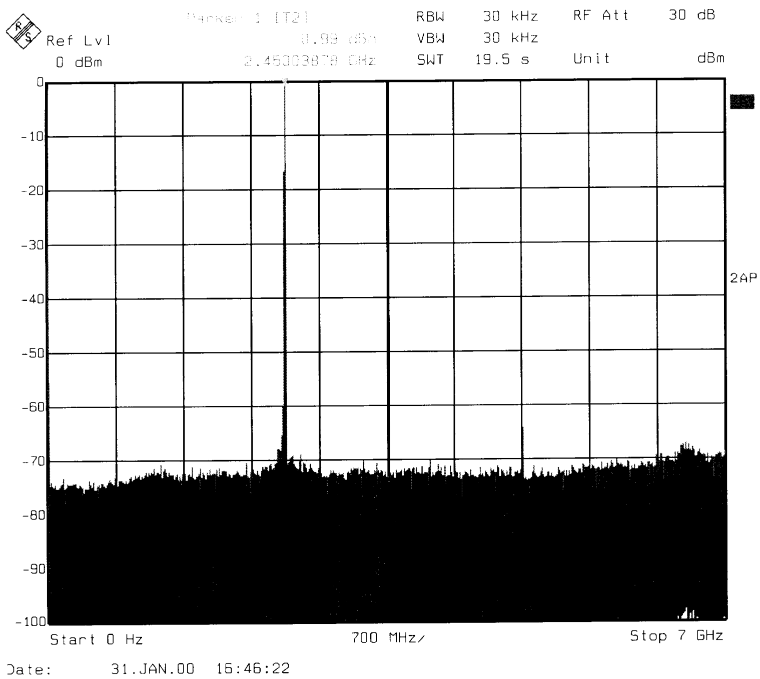
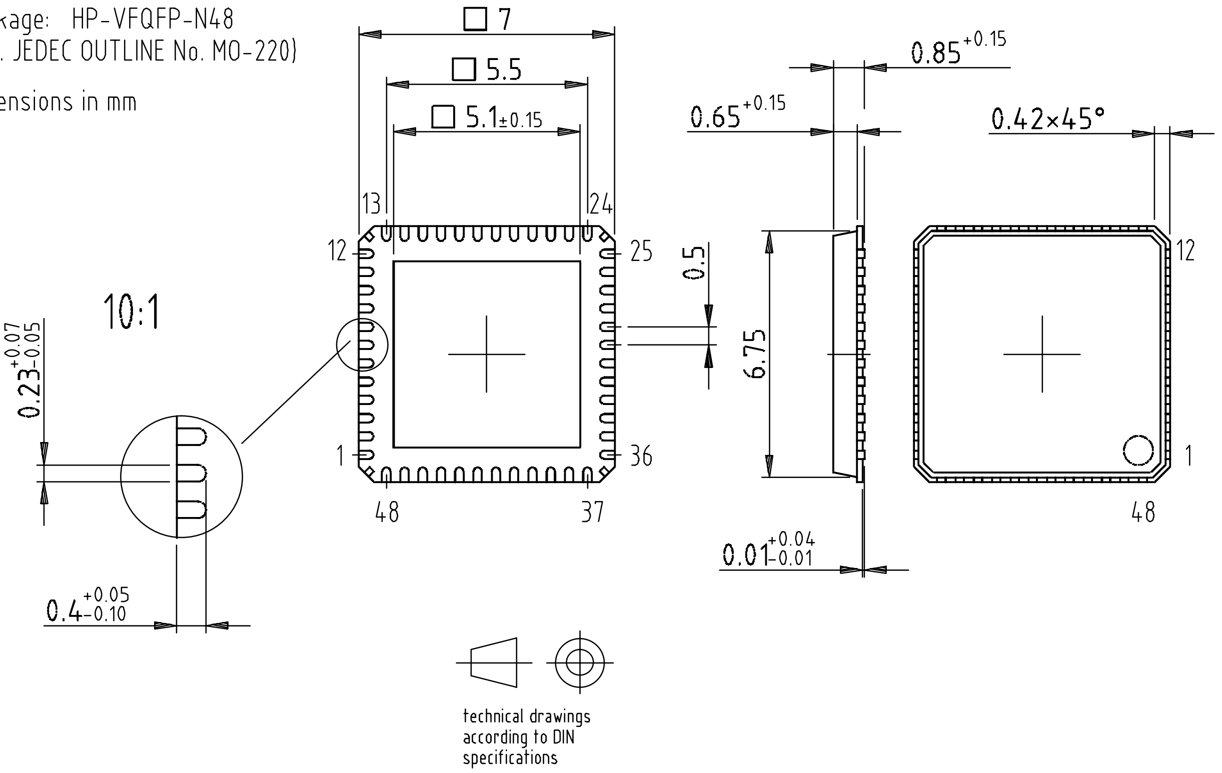


Figure 10. TX spectrum
Harmonics < 60 dBc

Package Information

Package: HP-VFQFP-N48
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423