

## 1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

### 1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

## 1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

**Table 1.1 Performance outline**

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns ( $f(X_{IN}) = 20$ MHz, $V_{CC} = 3.0$ to 5.5 V) 100 ns ( $f(X_{IN}) = 10$ MHz, $V_{CC} = 2.7$ to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler)
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial Interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high speed, low speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8)
Electrical characteristics	Power supply voltage	$V_{CC} = 3.0$ to 5.5 V ( $f(X_{IN}) = 20$ MHz) $V_{CC} = 2.7$ to 5.5 V ( $f(X_{IN}) = 10$ MHz)
	Power consumption	Typ. 9 mA ( $V_{CC} = 5.0$ V, ( $f(X_{IN}) = 20$ MHz, High-speed mode) Typ. 5 mA ( $V_{CC} = 3.0$ V, ( $f(X_{IN}) = 10$ MHz, High-speed mode) Typ. 35 $\mu$ A ( $V_{CC} = 3.0$ V, Wait mode, Peripheral clock stops) Typ. 0.7 $\mu$ A ( $V_{CC} = 3.0$ V, Stop mode)
Flash memory	Program/erase voltage	$V_{CC} = 2.7$ to 5.5 V
	Number of program/erase	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

### 1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

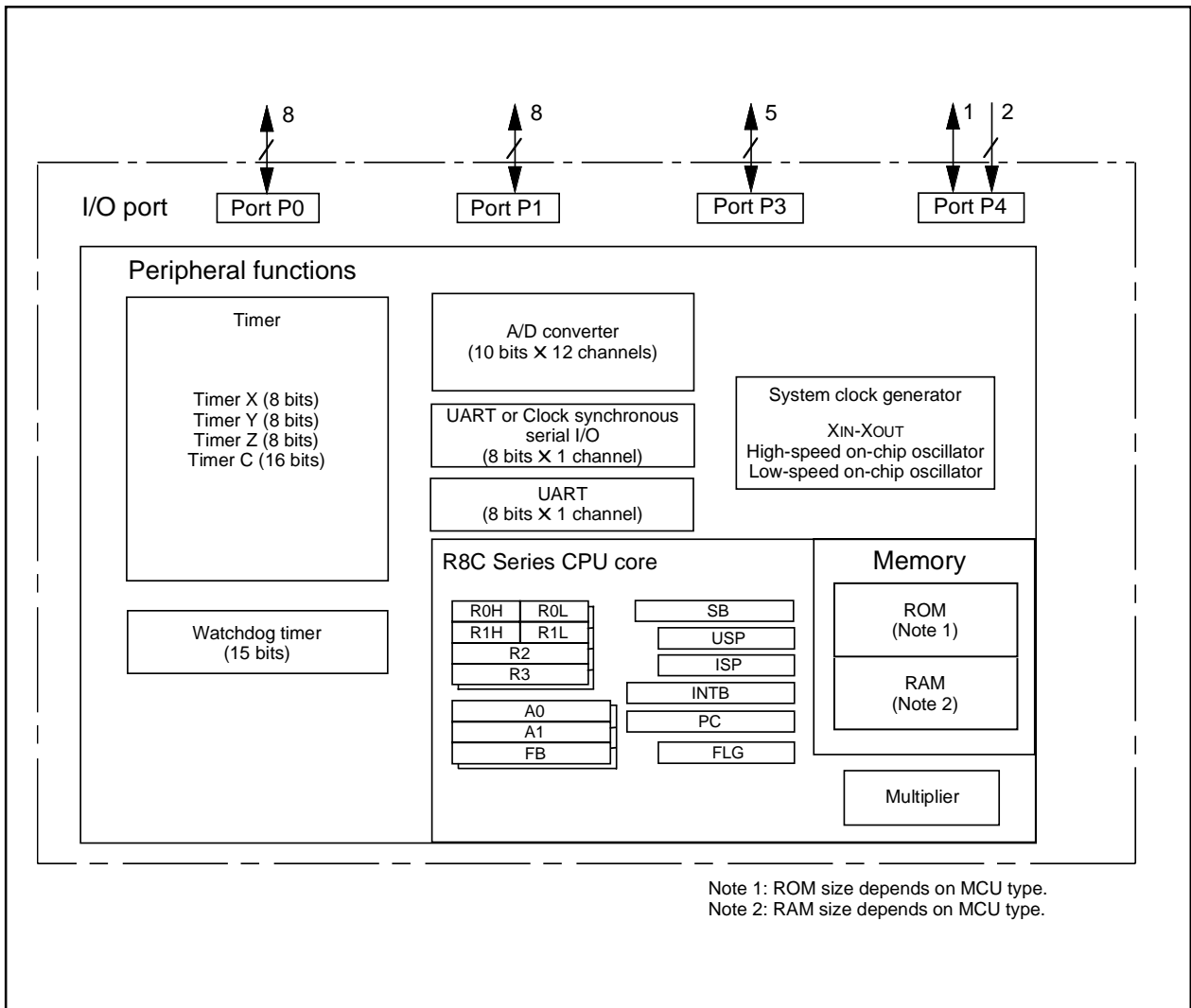


Figure 1.1 Block Diagram

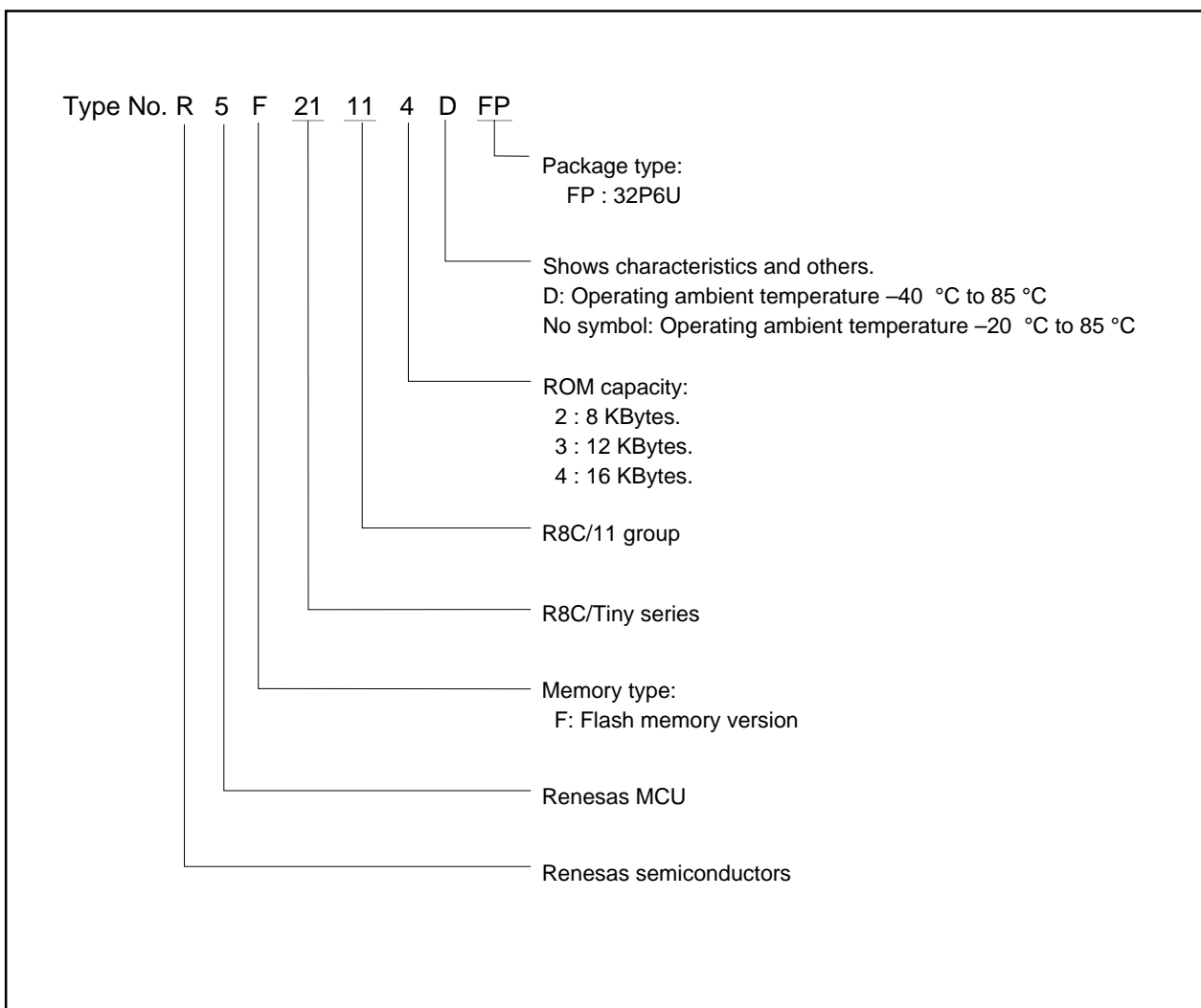
### 1.4 Product List

Table 1.2 lists the products.

**Table 1.2 Product List**

As of Sep. 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21112FP	8K bytes	512 bytes	32P6U-A	Flash memory version
R5F21113FP	12K bytes	768 bytes	32P6U-A	
R5F21114FP	16K bytes	1K bytes	32P6U-A	
R5F21112DFP	8K bytes	512 bytes	32P6U-A	D version
R5F21113DFP	12K bytes	768 bytes	32P6U-A	
R5F21114DFP	16K bytes	1K bytes	32P6U-A	



**Figure 1.2 Type No., Memory Size, and Package**

### 1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

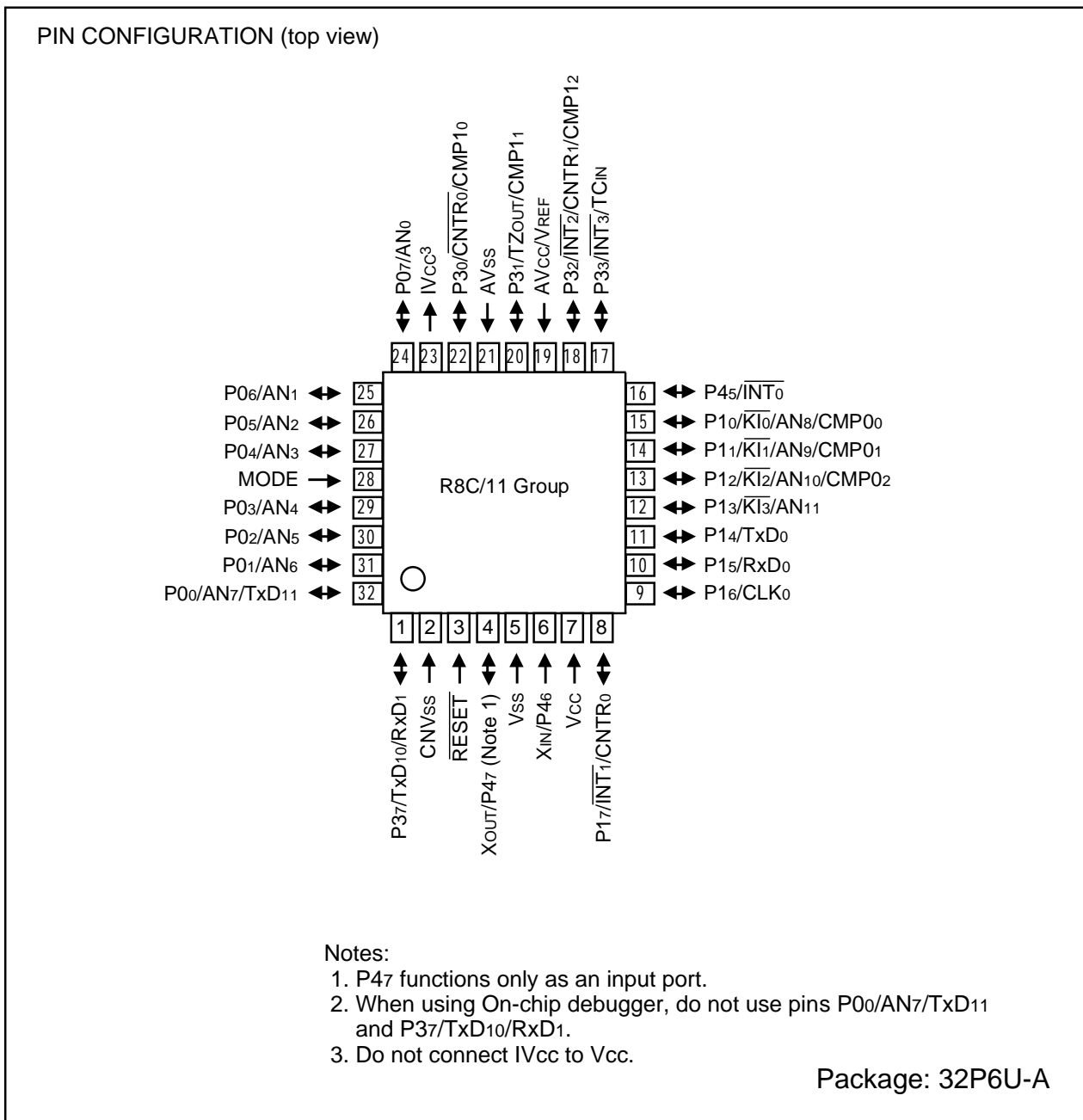


Figure 1.3 Pin Configuration (Top View)

## 1.6 Pin Description

Table 1.3 shows the pin description

**Table 1.3 Pin description**

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 $\mu$ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	These are power supply input pins for A/D converter. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	I	"L" on this input resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT $\bar{0}$ to INT $\bar{3}$	I	These are INT interrupt input pins.
Key input interrupt	KI $\bar{0}$ to KI $\bar{3}$	I	These are key input interrupt pins.
Timer X	CNTR $\bar{0}$	I/O	This is the timer X I/O pin.
	CNTR $\bar{0}$	O	This is the timer X output pin.
Timer Y	CNTR $\bar{1}$	I/O	This is the timer Y I/O pin.
Timer Z	TZOUT	O	This is the timer Z output pin.
Timer C	TCIN	I	This is the timer C input pin.
	CMP $\bar{0}$ to CMP $\bar{0}$ <sub>3</sub> , CMP $\bar{1}$ <sub>0</sub> to CMP $\bar{1}$ <sub>3</sub>	O	These are the timer C output pins.
Serial interface	CLK $\bar{0}$	I/O	This is a transfer clock I/O pin.
	RxD $\bar{0}$ , RxD $\bar{1}$	I	These are serial data input pins.
	TxD $\bar{0}$ , TxD $\bar{1}$ <sub>0</sub> , TxD $\bar{1}$ <sub>1</sub>	O	These are serial data output pins.
Reference voltage input	VREF	I	This is a reference voltage input pin for A/D converter.
A/D converter	AN $\bar{0}$ to AN $\bar{1}$ <sub>1</sub>	I	These are analog input pins for A/D converter.
I/O port	P $\bar{0}$ to P $\bar{7}$ , P $\bar{1}$ <sub>0</sub> to P $\bar{1}$ <sub>7</sub> , P $\bar{3}$ <sub>0</sub> to P $\bar{3}$ <sub>3</sub> , P $\bar{3}$ <sub>7</sub> , P $\bar{4}$ <sub>5</sub>	I/O	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P $\bar{1}$ <sub>0</sub> to P $\bar{1}$ <sub>7</sub> also function as LED drive ports.
Input port	P $\bar{4}$ <sub>6</sub> , P $\bar{4}$ <sub>7</sub>	I	These are input only pins.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

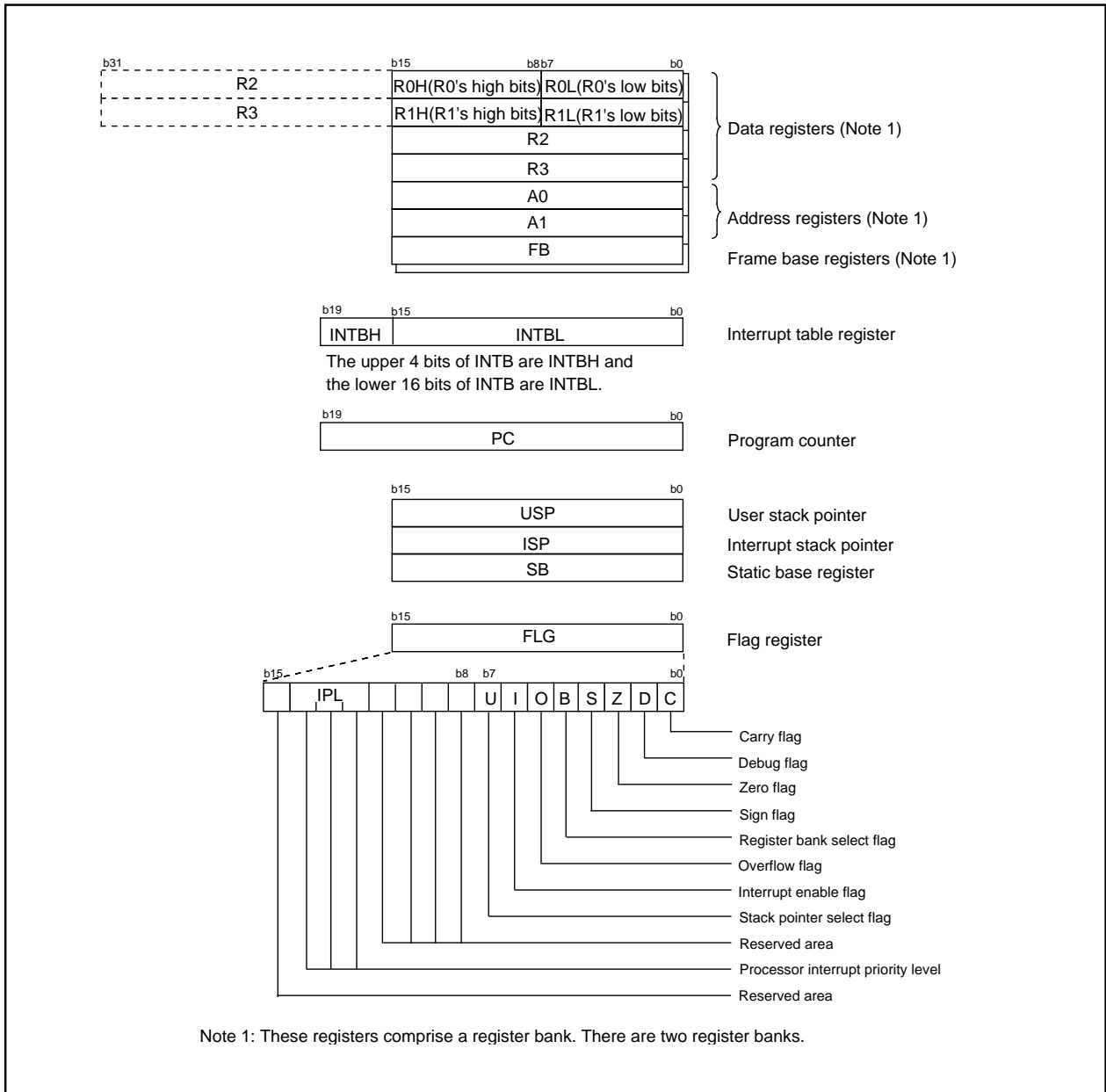


Figure 2.1. Central Processing Unit Register

### 2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

### 2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

### 2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

### 2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.



### 3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000<sub>16</sub> to FFFFF<sub>16</sub>.

The internal ROM is allocated in a lower address direction beginning with address 0FFFF<sub>16</sub>. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C000<sub>16</sub> to 0FFFF<sub>16</sub>.

The fixed interrupt vector table is allocated to the addresses from 0FFDC<sub>16</sub> to 0FFFF<sub>16</sub>. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400<sub>16</sub>. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400<sub>16</sub> to 007FF<sub>16</sub>. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. Special function registers (SFR) are allocated to the addresses from 00000<sub>16</sub> to 002FF<sub>16</sub>. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.

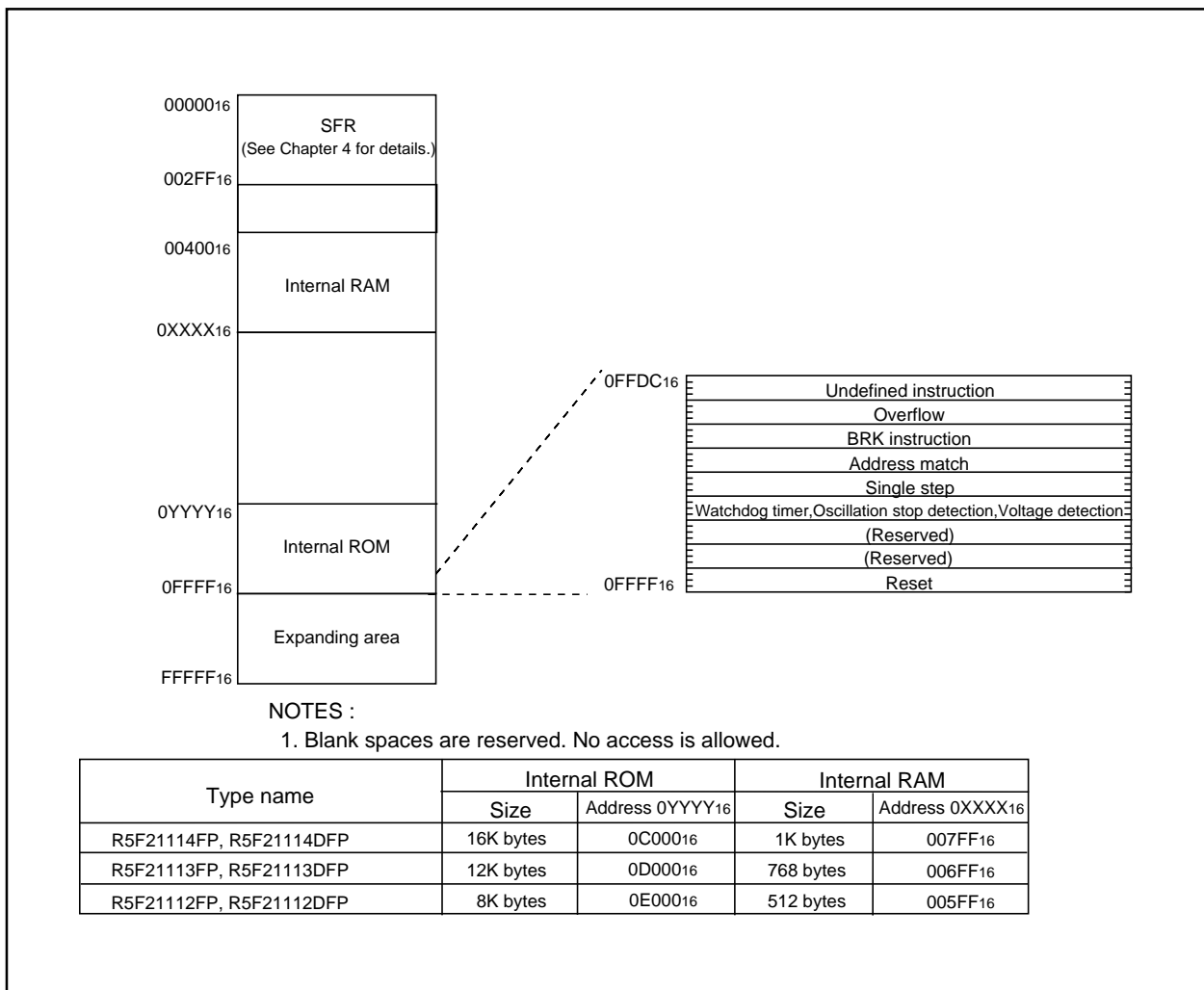


Figure 3.1 Memory Map

## 4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

**Table 4.1 SFR Information(1)(1)**

Address	Register	Symbol	After reset
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0 <sup>1</sup>	PM0	00 <sub>16</sub>
0005 <sub>16</sub>	Processor mode register 1	PM1	00 <sub>16</sub>
0006 <sub>16</sub>	System clock control register 0	CM0	011010002
0007 <sub>16</sub>	System clock control register 1	CM1	001000002
0008 <sub>16</sub>	High-speed on-chip control register 0	HR0	00 <sub>16</sub>
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXXXX002
000A <sub>16</sub>	Protect register	PRCR	00XXX0002
000B <sub>16</sub>	High-speed on-chip control register 1	HR1	40 <sub>16</sub>
000C <sub>16</sub>	Oscillation stop detection register	OCD	000001002
000D <sub>16</sub>	Watchdog timer reset register	WDTR	XX <sub>16</sub>
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog timer control register	WDC	000XXXXX2
0010 <sub>16</sub>	Address match interrupt register 0	RMAD0	00 <sub>16</sub>
0011 <sub>16</sub>			00 <sub>16</sub>
0012 <sub>16</sub>			X0 <sub>16</sub>
0013 <sub>16</sub>			
0014 <sub>16</sub>	Address match interrupt register 1	RMAD1	00 <sub>16</sub>
0015 <sub>16</sub>			00 <sub>16</sub>
0016 <sub>16</sub>			X0 <sub>16</sub>
0017 <sub>16</sub>			
0018 <sub>16</sub>			
0019 <sub>16</sub>	Voltage detection register 1 <sup>2</sup>	VCR1	00 <sub>16</sub>
001A <sub>16</sub>	Voltage detection register 2 <sup>2</sup>	VCR2	XXX00000 <sub>16</sub>
001B <sub>16</sub>			
001C <sub>16</sub>			
001D <sub>16</sub>			
001E <sub>16</sub>	INT0 input filter select register	INT0F	XXXXX0002
001F <sub>16</sub>	Voltage detection interrupt register <sup>2</sup>	D4INT	0016 <sup>3</sup>
0020 <sub>16</sub>			
0021 <sub>16</sub>			
0022 <sub>16</sub>			
0023 <sub>16</sub>			
0024 <sub>16</sub>			
0025 <sub>16</sub>			
0026 <sub>16</sub>			
0027 <sub>16</sub>			
0028 <sub>16</sub>			
0029 <sub>16</sub>			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>			
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			
0030 <sub>16</sub>			
0031 <sub>16</sub>			
0032 <sub>16</sub>			
0033 <sub>16</sub>			
0034 <sub>16</sub>			
0035 <sub>16</sub>			
0036 <sub>16</sub>			
0037 <sub>16</sub>			
0038 <sub>16</sub>			
0039 <sub>16</sub>			
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>			
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

010000012 <sup>4</sup>

X : Undefined

NOTES:

- Blank columns are all reserved space. No access is allowed.
- Software reset or the watchdog timer reset does not affect this register.
- Owing to Reset input.
- In the case of RESET pin = H retaining.

Table 4.2 SFR Information(2)<sup>(1)</sup>

Address	Register	Symbol	After reset
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>			
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>			
0049 <sub>16</sub>			
004A <sub>16</sub>			
004B <sub>16</sub>			
004C <sub>16</sub>			
004D <sub>16</sub>	Key input interrupt control register	KUPIC	XXXXX0002
004E <sub>16</sub>	A/D conversion interrupt control register	ADIC	XXXXX0002
004F <sub>16</sub>			
0050 <sub>16</sub>	Compare 1 interrupt control register	CMP1IC	XXXXX0002
0051 <sub>16</sub>	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 <sub>16</sub>	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 <sub>16</sub>	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 <sub>16</sub>	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 <sub>16</sub>	INT2 interrupt control register	INT2IC	XXXXX0002
0056 <sub>16</sub>	Timer X interrupt control register	TXIC	XXXXX0002
0057 <sub>16</sub>	Timer Y interrupt control register	TYIC	XXXXX0002
0058 <sub>16</sub>	Timer Z interrupt control register	TZIC	XXXXX0002
0059 <sub>16</sub>	INT1 interrupt control register	INT1IC	XXXXX0002
005A <sub>16</sub>	INT3 interrupt control register	INT3IC	XXXXX0002
005B <sub>16</sub>	Timer C interrupt control register	TCIC	XXXXX0002
005C <sub>16</sub>	Compare 0 interrupt control register	CMP0IC	XXXXX0002
005D <sub>16</sub>	INT0 interrupt control register	INT0IC	XX00X0002
005E <sub>16</sub>			
005F <sub>16</sub>			
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>			
0069 <sub>16</sub>			
006A <sub>16</sub>			
006B <sub>16</sub>			
006C <sub>16</sub>			
006D <sub>16</sub>			
006E <sub>16</sub>			
006F <sub>16</sub>			
0070 <sub>16</sub>			
0071 <sub>16</sub>			
0072 <sub>16</sub>			
0073 <sub>16</sub>			
0074 <sub>16</sub>			
0075 <sub>16</sub>			
0076 <sub>16</sub>			
0077 <sub>16</sub>			
0078 <sub>16</sub>			
0079 <sub>16</sub>			
007A <sub>16</sub>			
007B <sub>16</sub>			
007C <sub>16</sub>			
007D <sub>16</sub>			
007E <sub>16</sub>			
007F <sub>16</sub>			

X : Undefined

NOTES :

1. Blank columns are all reserved space. No access is allowed.

Table 4.3 SFR Information(3)<sup>(1)</sup>

Address	Register	Symbol	After reset
0080 <sub>16</sub>	Timer Y, Z mode register	TYZMR	00 <sub>16</sub>
0081 <sub>16</sub>	Prescaler Y	PREY	FF <sub>16</sub>
0082 <sub>16</sub>	Timer Y secondary	TYSC	FF <sub>16</sub>
0083 <sub>16</sub>	Timer Y primary	TYPR	FF <sub>16</sub>
0084 <sub>16</sub>	Timer Y, Z waveform output control register	PUM	00 <sub>16</sub>
0085 <sub>16</sub>	Prescaler Z	PREZ	FF <sub>16</sub>
0086 <sub>16</sub>	Timer Z secondary	TZSC	FF <sub>16</sub>
0087 <sub>16</sub>	Timer Z primary	TZPR	FF <sub>16</sub>
0088 <sub>16</sub>			
0089 <sub>16</sub>			
008A <sub>16</sub>	Timer Y, Z output control register	TYZOC	00 <sub>16</sub>
008B <sub>16</sub>	Timer X mode register	TXMR	00 <sub>16</sub>
008C <sub>16</sub>	Prescaler X	PREX	FF <sub>16</sub>
008D <sub>16</sub>	Timer X register	TX	FF <sub>16</sub>
008E <sub>16</sub>	Timer count source setting register	TCSS	00 <sub>16</sub>
008F <sub>16</sub>			
0090 <sub>16</sub>	Timer C register	TC	00 <sub>16</sub>
0091 <sub>16</sub>			00 <sub>16</sub>
0092 <sub>16</sub>			
0093 <sub>16</sub>			
0094 <sub>16</sub>			
0095 <sub>16</sub>			
0096 <sub>16</sub>	External input enable register	INTEN	00 <sub>16</sub>
0097 <sub>16</sub>			
0098 <sub>16</sub>	Key input enable register	KIEN	00 <sub>16</sub>
0099 <sub>16</sub>			
009A <sub>16</sub>	Timer C control register 0	TCC0	00 <sub>16</sub>
009B <sub>16</sub>	Timer C control register 1	TCC1	00 <sub>16</sub>
009C <sub>16</sub>	Capture, compare 0 register	TM0	FF <sub>16</sub>
009D <sub>16</sub>			FF <sub>16</sub>
009E <sub>16</sub>	Compare 1 register	TM1	FF <sub>16</sub>
009F <sub>16</sub>			FF <sub>16</sub>
00A0 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	00 <sub>16</sub>
00A1 <sub>16</sub>	UART0 bit rate register	U0BRG	XX <sub>16</sub>
00A2 <sub>16</sub>	UART0 transmit buffer register	U0TB	XX <sub>16</sub>
00A3 <sub>16</sub>			XX <sub>16</sub>
00A4 <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	00001000 <sub>2</sub>
00A5 <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	00000010 <sub>2</sub>
00A6 <sub>16</sub>	UART0 receive buffer register	U0RB	XX <sub>16</sub>
00A7 <sub>16</sub>			XX <sub>16</sub>
00A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	00 <sub>16</sub>
00A9 <sub>16</sub>	UART1 bit rate register	U1BRG	XX <sub>16</sub>
00AA <sub>16</sub>	UART1 transmit buffer register	U1TB	XX <sub>16</sub>
00AB <sub>16</sub>			XX <sub>16</sub>
00AC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	00001000 <sub>2</sub>
00AD <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	00000010 <sub>2</sub>
00AE <sub>16</sub>	UART1 receive buffer register	U1RB	XX <sub>16</sub>
00AF <sub>16</sub>			XX <sub>16</sub>
00B0 <sub>16</sub>	UART transmit/receive control register 2	UCON	00 <sub>16</sub>
00B1 <sub>16</sub>			
00B2 <sub>16</sub>			
00B3 <sub>16</sub>			
00B4 <sub>16</sub>			
00B5 <sub>16</sub>			
00B6 <sub>16</sub>			
00B7 <sub>16</sub>			
00B8 <sub>16</sub>			
00B9 <sub>16</sub>			
00BA <sub>16</sub>			
00BB <sub>16</sub>			
00BC <sub>16</sub>			
00BD <sub>16</sub>			
00BE <sub>16</sub>			
00BF <sub>16</sub>			

X : Undefined

NOTES :

1. Blank columns are all reserved space. No access is allowed.

Table 4.4 SFR Information(4)<sup>(1)</sup>

Address	Register	Symbol	After reset
00C0 <sub>16</sub>	A/D register	AD	XX <sub>16</sub>
00C1 <sub>16</sub>			XX <sub>16</sub>
00C2 <sub>16</sub>			
00C3 <sub>16</sub>			
00C4 <sub>16</sub>			
00C5 <sub>16</sub>			
00C6 <sub>16</sub>			
00C7 <sub>16</sub>			
00C8 <sub>16</sub>			
00C9 <sub>16</sub>			
00CA <sub>16</sub>			
00CB <sub>16</sub>			
00CC <sub>16</sub>			
00CD <sub>16</sub>			
00CE <sub>16</sub>			
00CF <sub>16</sub>			
00D0 <sub>16</sub>			
00D1 <sub>16</sub>			
00D2 <sub>16</sub>			
00D3 <sub>16</sub>			
00D4 <sub>16</sub>	A/D control register 2	ADCON2	00 <sub>16</sub>
00D5 <sub>16</sub>			
00D6 <sub>16</sub>	A/D control register 0	ADCON0	00000XX <sub>2</sub>
00D7 <sub>16</sub>	A/D control register 1	ADCON1	00 <sub>16</sub>
00D8 <sub>16</sub>			
00D9 <sub>16</sub>			
00DA <sub>16</sub>			
00DB <sub>16</sub>			
00DC <sub>16</sub>			
00DD <sub>16</sub>			
00DE <sub>16</sub>			
00DF <sub>16</sub>			
00E0 <sub>16</sub>	Port P0 register	P0	XX <sub>16</sub>
00E1 <sub>16</sub>	Port P1 register	P1	XX <sub>16</sub>
00E2 <sub>16</sub>	Port P0 direction register	PD0	00 <sub>16</sub>
00E3 <sub>16</sub>	Port P1 direction register	PD1	00 <sub>16</sub>
00E4 <sub>16</sub>			
00E5 <sub>16</sub>	Port P3 register	P3	XX <sub>16</sub>
00E6 <sub>16</sub>			
00E7 <sub>16</sub>	Port P3 direction register	PD3	00 <sub>16</sub>
00E8 <sub>16</sub>	Port P4 register	P4	XX <sub>16</sub>
00E9 <sub>16</sub>			
00EA <sub>16</sub>	Port P4 direction register	PD4	00 <sub>16</sub>
00EB <sub>16</sub>			
00EC <sub>16</sub>			
00ED <sub>16</sub>			
00EE <sub>16</sub>			
00EF <sub>16</sub>			
00F0 <sub>16</sub>			
00F1 <sub>16</sub>			
00F2 <sub>16</sub>			
00F3 <sub>16</sub>			
00F4 <sub>16</sub>			
00F5 <sub>16</sub>			
00F6 <sub>16</sub>			
00F7 <sub>16</sub>			
00F8 <sub>16</sub>			
00F9 <sub>16</sub>			
03FA <sub>16</sub>			
00FB <sub>16</sub>			
00FC <sub>16</sub>	Pull-up control register 0	PUR0	00XX0000 <sub>2</sub>
00FD <sub>16</sub>	Pull-up control register 1	PUR1	XXXXXX0X <sub>2</sub>
00FE <sub>16</sub>	Port P1 drive capacity control register	DRR	00 <sub>16</sub>
00FF <sub>16</sub>	Timer C output control register	TCOUT	00 <sub>16</sub>
⋈			
01B3 <sub>16</sub>	Flash memory control register 4	FMR4	01000000 <sub>2</sub>
01B4 <sub>16</sub>			
01B5 <sub>16</sub>	Flash memory control register 1	FMR1	0100XX0X <sub>2</sub>
01B6 <sub>16</sub>			
01B7 <sub>16</sub>	Flash memory control register 0	FMR0	00000001 <sub>2</sub>

X : Undefined

NOTES :

1. The blank areas, 0100<sub>16</sub> to 01B2<sub>16</sub> and 01B8<sub>16</sub> to 02FF<sub>16</sub> are reserved and cannot be used by users.

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter	Condition	Rated value	Unit
V <sub>CC</sub>	Supply voltage	V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.5	V
AV <sub>CC</sub>	Analog supply voltage	V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.5	V
V <sub>I</sub>	Input voltage		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage		-0.3 to V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>opr</sub> =25 °C	300	mW
T <sub>opr</sub>	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature		-65 to 150	°C

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter	Conditions	Standard			Unit	
			Min.	Typ.	Max.		
V <sub>CC</sub>	Supply voltage		2.7	—	5.5	V	
AV <sub>CC</sub>	Analog supply voltage		—	V <sub>CC</sub> <sup>3</sup>	—	V	
V <sub>SS</sub>	Supply voltage		—	0	—	V	
AV <sub>SS</sub>	Analog supply voltage		—	0	—	V	
V <sub>IH</sub>	"H" input voltage		0.8V <sub>CC</sub>	—	V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage		0	—	0.2V <sub>CC</sub>	V	
I <sub>OH (sum)</sub>	"H" peak all output currents	Sum of all pins' IOH (peak)	—	—	-60.0	mA	
I <sub>OH (peak)</sub>	"H" peak output current		—	—	-10.0	mA	
I <sub>OH (avg)</sub>	"H" average output current		—	—	-5.0	mA	
I <sub>OL (sum)</sub>	"L" peak all output currents	Sum of all pins' IOL (peak)	—	—	60	mA	
I <sub>OL (peak)</sub>	"L" peak output current	Except P1 <sub>0</sub> to P1 <sub>7</sub>	—	—	10	mA	
		P1 <sub>0</sub> to P1 <sub>7</sub>	Drive capacity HIGH	—	—	30	mA
			Drive capacity LOW	—	—	10	mA
I <sub>OL (avg)</sub>	"L" average output current	Except P1 <sub>0</sub> to P1 <sub>7</sub>	—	—	5	mA	
		P1 <sub>0</sub> to P1 <sub>7</sub>	Drive capacity HIGH	—	—	15	mA
			Drive capacity LOW	—	—	5	mA
f (XIN)	Main clock input oscillation frequency	3.0V ≤ V <sub>CC</sub> ≤ 5.5V	0	—	20	MHz	
		2.7V ≤ V <sub>CC</sub> < 3.0V	0	—	10	MHz	

**Note**

1: Referenced to V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C unless otherwise specified.

2: The mean output current is the mean value within 100ms.

3: Hold V<sub>CC</sub>=AV<sub>CC</sub>.

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{ref} = V_{CC}$			10	Bit
–	Absolute accuracy	10 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0V$			$\pm 3$	LSB
		8 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0V$			$\pm 2$	LSB
		10 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 3.3V$			$\pm 5$	LSB
		8 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 3.3V$			$\pm 2$	LSB
$R_{LADDER}$	Ladder resistance		$V_{REF} = V_{CC}$	10		40	$k\Omega$
$t_{CONV}$	Conversion time	10 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0V$	3.3			$\mu s$
		8 bit mode	$f(XIN) = \emptyset AD = 10 \text{ MHz}$ , $V_{ref} = V_{CC} = 5.0V$	2.8			$\mu s$
$V_{REF}$	Reference voltage				$V_{CC}^4$		V
$V_{IA}$	Analog input voltage			0		$V_{ref}$	V
–	A/D operation clock frequency <sup>2</sup>	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

## Note

- 1: Referenced to  $V_{CC} = AV_{CC} = 2.7$  to  $5.5V$  at  $T_{opr} = -20$  to  $85 \text{ }^\circ C$  /  $-40$  to  $85 \text{ }^\circ C$  unless otherwise specified.
- 2: When  $f_{AD}$  is 10 MHz more, divide the  $f_{AD}$  and make A/D operation clock frequency ( $\emptyset AD$ ) lower than 10 MHz.
- 3: When the  $V_{CC}$  is less than 4.2V, divide the  $f_{AD}$  and make A/D operation clock frequency ( $\emptyset AD$ ) lower than  $f_{AD}/2$ .
- 4: Hold  $V_{CC} = V_{ref}$ .

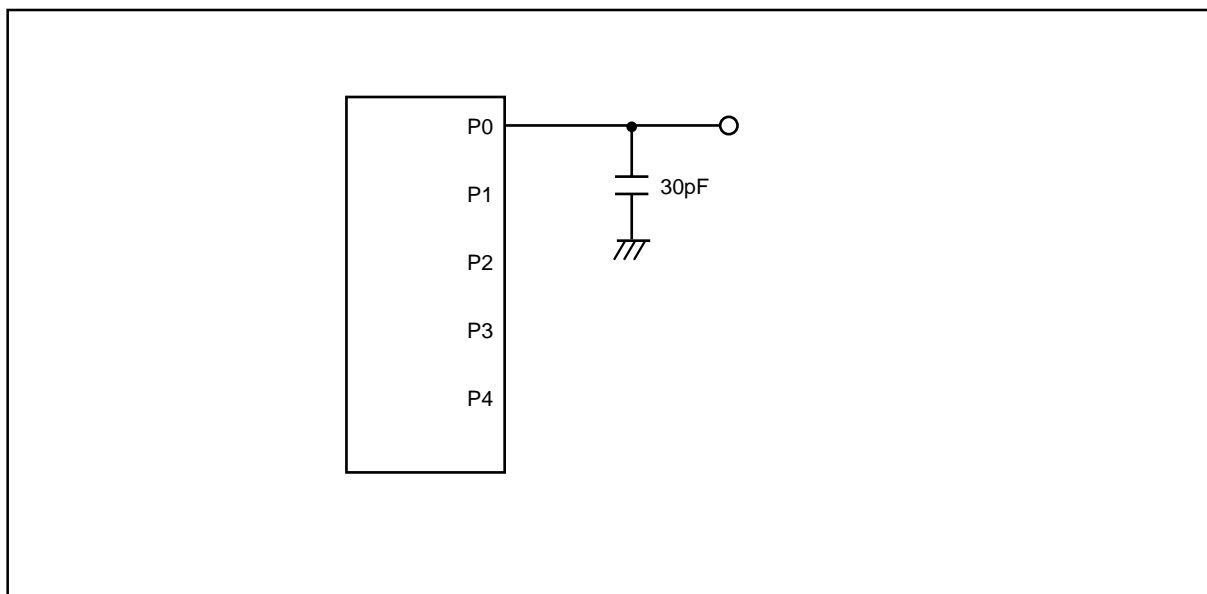


Figure 5.1 Port P0 to P4 measurement circuit

**Table 5.4 Flash Memory Version Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase cycle		100	—	—	cycle
—	Byte program time	V <sub>cc</sub> =5.0V, Topr=25 °C	—	50	400	μs
—	Block erase time	V <sub>cc</sub> =5.0V, Topr=25 °C	—	0.4	9	s
td(SR-ES)	Time delay from suspend request until erase suspend		—	—	8	ms
—	Program, Erase voltage		2.7	—	5.5	V
—	Read voltage		2.7	—	5.5	V
—	Program, Erase temperature		0	—	60	°C
—	Data-retention duration	Topr=55 °C	20	—	—	year

**Note**

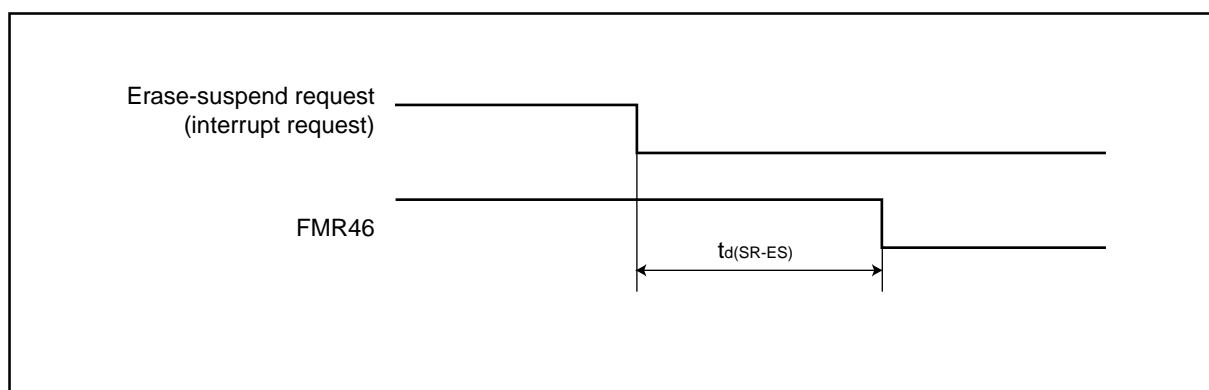
1: Referenced to V<sub>cc1</sub>=AV<sub>cc</sub>=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.

**Table 5.5 Voltage Detection Circuit Electrical Characteristics**

Symbol	Parameter	Measuring condition	Min.	Standard		Unit
				Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time <sup>2</sup>			40		μs
	Voltage detection circuit self consumption current	V <sub>C27</sub> =1, V <sub>CC</sub> =5.0V		600		nA
td(E-A)	Waiting time till voltage detection circuit operation starts <sup>3</sup>				20	μs
V <sub>ccmin</sub>	Minimum value of microcomputer operation voltage		2.7			V

**NOTES:**

1. The measuring condition is V<sub>cc</sub>=AV<sub>cc</sub>=2.7V to 5.5V and Topr= -40°C to 85 °C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0"

**Figure 5.2 Time delay from Suspend Request until Erase Suspend**



**Table 5.6 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2)**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage				Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled <sup>2</sup>				100	ms
tw(por2)	Time to hold external power below valid voltage		0			s

NOTES:

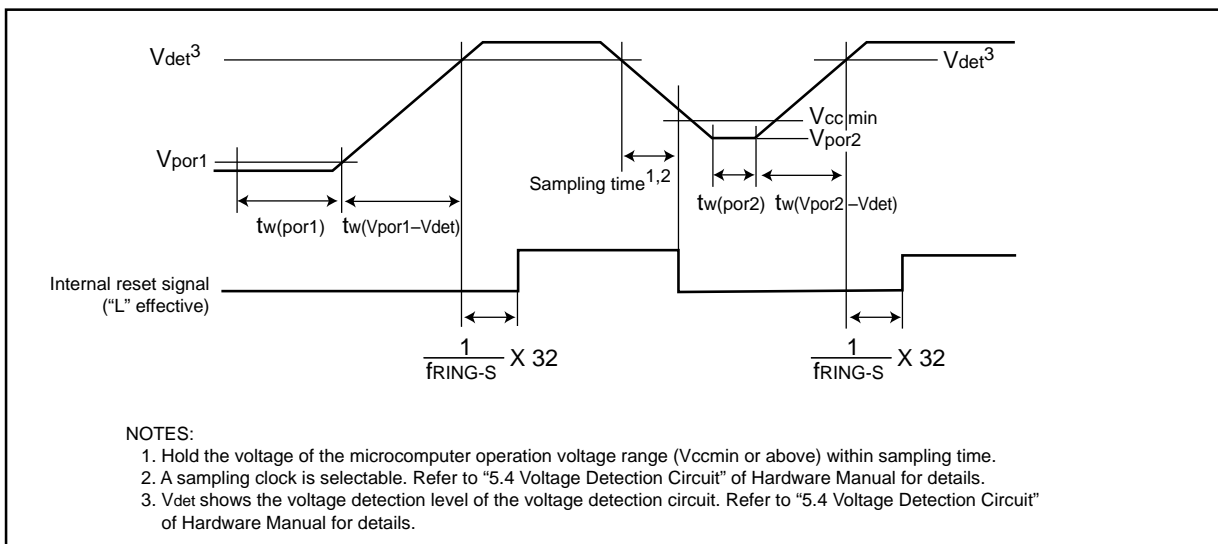
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual.
2. This condition is not applicable when using with Vcc ≥ 1.0V.
3. When turning power on after the time to hold the external power below effective voltage exceeds 10s, refer to Table 16.8 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset).

**Table 5.7 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage				0.1	V
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C			100	ms
tw(por1)	Time to hold external power on below valid voltage	0°C ≤ Topr ≤ 85°C	10			s
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr ≤ 0°C			100	ms
tw(por1)	Time to hold external power on below valid voltage	-20°C ≤ Topr ≤ 0°C	30			s
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr ≤ 0°C			1	ms
tw(por1)	Time to hold external power on below valid voltage	-20°C ≤ Topr ≤ 0°C	10			s
tw(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C			0.5	ms
tw(por1)	Time to hold external power on below valid voltage	0°C ≤ Topr ≤ 85°C	1			s

NOTES:

1. When not the sing hardware reset 2, use with Vcc ≥ 2.7V.



**Figure 5.3 Reset Circuit Electrical Characteristics**

**Table 5.8 High-speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
	High-speed on-chip oscillator frequency 1 / (td(HRoffset)+td(HR)) when the reset is released	VCC=5.0V, Topr=25 °C Set "4016" in the HR1 register	6	8	10	MHz
td(HRoffset)	Settable high-speed on-chip oscillator minimum period	VCC=5.0V, Topr=25 °C Set "0016" in the HR1 register		61		ns
td(HR)	High-speed on-chip oscillator period adjusted unit	Differences when setting "0116" and "0016" in the HR register		1		ns
	High-speed on-chip oscillator temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C		±5		%
	High-speed on-chip oscillator temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 85 °C		±10		%

## NOTES:

1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

**Table 5.9 Power Circuit Timing Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on <sup>2</sup>				2	ms
td(R-S)	STOP release time <sup>3</sup>				150	µs

## Note

1: The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.

2: This shows the wait time until the internal power supply generating circuit is stabilized during power-on.

3: This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

**Table 5.10 Electrical Characteristics (1) [Vcc=5V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VoH	"H" output voltage	Except XOUT	IOH=-5mA	Vcc-2.0		Vcc	V
			IOH=-200µA	Vcc-0.3		Vcc	V
		XOUT	Drive ability HIGH IOH=-1 mA	Vcc-2.0		Vcc	V
			Drive ability LOW IOH=-500µA	Vcc-2.0		Vcc	V
VoL	"L" output voltage	P10 to P17 Except XOUT	IOH= 5 mA			2.0	V
			IOH= 200 µA			0.45	V
		P10 to P17	Drive capacity HIGH IOL= 15 mA			2.0	V
			Drive capacity LOW IOL= 5 mA			2.0	V
			Drive capacity LOW IOL= 200 µA			0.45	V
		XOUT	Drive capacity HIGH IOL= 1 mA			2.0	V
			Drive capacity LOW IOL=500 µA			2.0	V
		VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1		0.2	
RESET				0.2		2.2	V
IiH	"H" input current		Vi=5V			5.0	µA
IiL	"L" input current		Vi=0V			-5.0	µA
RPULLUP	Pull-up resistance		Vi=0V	30	50	167	kΩ
RiXIN	Feedback resistance	XIN			1.0		MΩ
fRING-S	Low-speed on-chip oscillator frequency			40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage		At stop mode	2.0			V

## Note

1 : Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

Table 5.11 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		9	15	mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	14	mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		4		mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		470	900	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>1</sup> Peripheral clock operation VC27="0"		40	80	μA
Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock off VC27="0"		38	76	μA		
Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	μA		

## NOTES

- 1: The power supply current measuring is executed using the measuring program on flash memory.
- 2: Timer Y is operated with timer mode.

**Timing requirements (Unless otherwise noted: VCC = 5V, VSS = 0V at Ta = 25 °C) [VCC=5V]****Table 5.12 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	50		ns
tWH(XIN)	XIN input HIGH pulse width	25		ns
tWL(XIN)	XIN input LOW pulse width	25		ns

**Table 5.13 CNTR0 input, CNTR1 input,  $\overline{\text{INT2}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

**Table 5.14 TCIN input,  $\overline{\text{INT3}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400 <sup>(1)</sup>		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 <sup>(2)</sup>		ns
tWL(TCIN)	TCIN input LOW pulse width	200 <sup>(2)</sup>		ns

**NOTES**

- 1 :When using the Timer C input capture mode, adjust the cycle time above ( 1/ Timer C count source frequency x 3).
- 2 : When using the Timer C input capture mode, adjust the pulse width above ( 1/ Timer C count source frequency x 1.5).

**Table 5.15 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	200		ns
tW(CKH)	CLKi input HIGH pulse width	100		ns
tW(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

**Table 5.16 External interrupt  $\overline{\text{INT0}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	250 <sup>(1)</sup>		ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	250 <sup>(2)</sup>		ns

**NOTES**

- 1 : When selecting the digital filter by the  $\overline{\text{INT0}}$  input filter select bit, use the  $\overline{\text{INT0}}$  input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.
- 2 : When selecting the digital filter by the  $\overline{\text{INT0}}$  input filter select bit, use the  $\overline{\text{INT0}}$  input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.

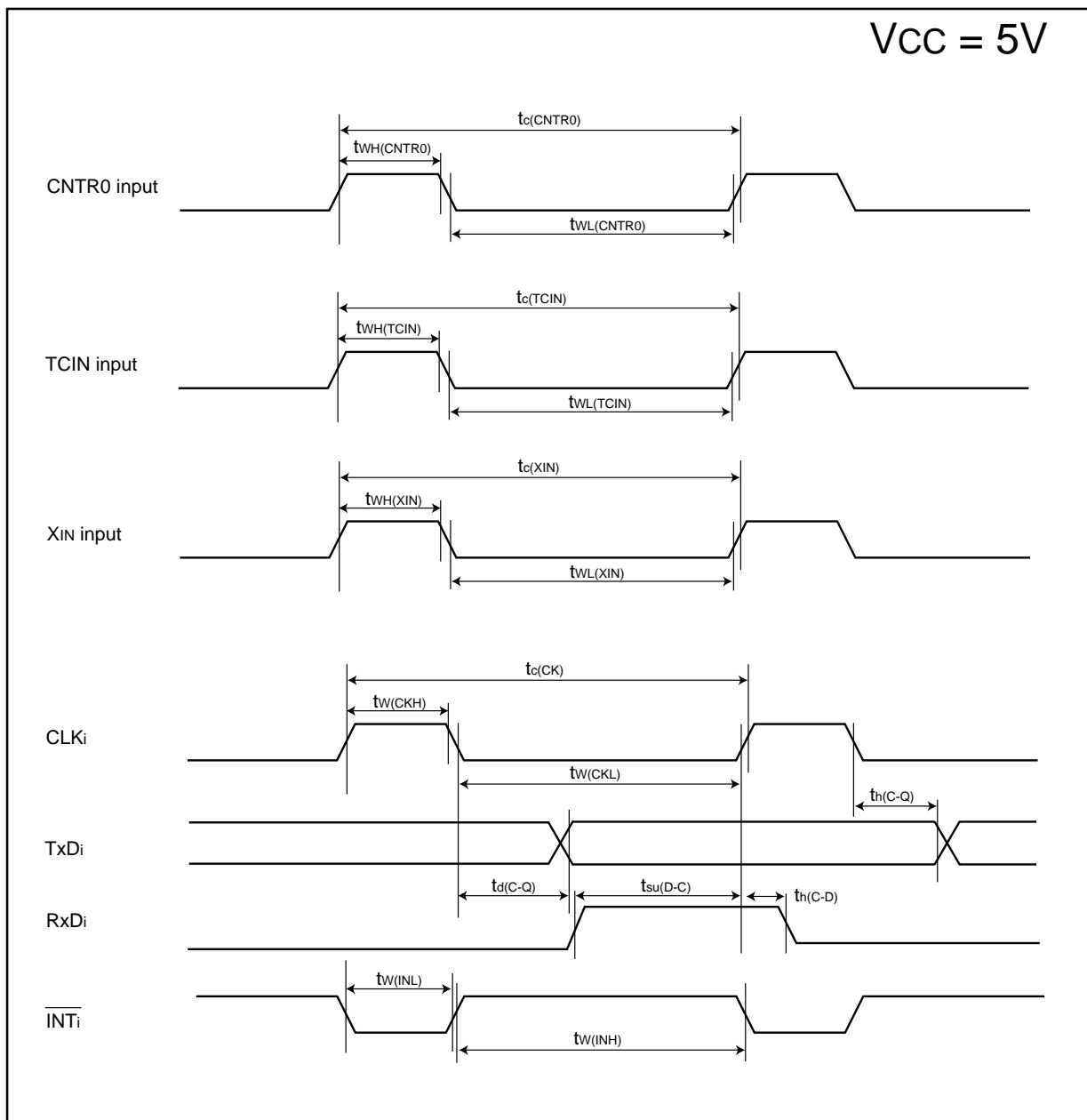


Figure 5.4 Vcc=5V timing diagram

**Table 5.17 Electrical Characteristics (3) [Vcc=3V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	I <sub>OH</sub> =-1mA	V <sub>CC</sub> -0.5		V <sub>CC</sub>	V
		XOUT	Drive capacity HIGH I <sub>OH</sub> =-0.1 mA	V <sub>CC</sub> -0.5		V <sub>CC</sub>	V
			Drive capacity LOW I <sub>OH</sub> =-50 μA	V <sub>CC</sub> -0.5		V <sub>CC</sub>	V
VOL	"L" output voltage	P10 to P17 Except XOUT	I <sub>OH</sub> = 1 mA			0.5	V
		P10 to P17	Drive capacity HIGH I <sub>OL</sub> = 2 mA			0.5	V
			Drive capacity LOW I <sub>OL</sub> = 1 mA			0.5	V
		XOUT	Drive capacity HIGH I <sub>OL</sub> = 0.1 mA			0.5	V
			Drive capacity LOW I <sub>OL</sub> =50 μA			0.5	V
VT+·VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1		0.2		0.8	V
		RESET		0.2		1.8	V
I <sub>IH</sub>	"H" input current		V <sub>I</sub> =3V			4.0	μA
I <sub>IL</sub>	"L" input current		V <sub>I</sub> =0V			-4.0	μA
R <sub>PULLUP</sub>	Pull-up resistance		V <sub>I</sub> =0V	66	160	500	kΩ
R <sub>XIN</sub>	Feedback resistance	XIN			3.0		MΩ
f <sub>RING-S</sub>	Low-speed on-chip oscillator frequency			40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage		At stop mode	2.0			V

**Note**

1 : Referenced to V<sub>CC</sub>=AV<sub>CC</sub>=2.7 to 3.3V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

**Table 5.18 Electrical Characteristics (4) [Vcc=3V]**

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	High-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	13	mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		7	12	mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2.5		mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		1.6		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		420	800	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock operation VC27="0"		37	74	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock off VC27="0"		35	70	μA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off OM10="1" Peripheral clock off VC27="0"		0.7	3.0	μA

## Note

- 1: The power supply current measuring is executed using the measuring program on frash memory.
- 2: Timer Y is operated with timer mode.

**Timing requirements (Unless otherwise noted:  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = 25\text{ }^\circ\text{C}$ ) [ $V_{CC}=3V$ ]****Table 5.19 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	100		ns
tWH(XIN)	XIN input HIGH pulse width	40		ns
tWL(XIN)	XIN input LOW pulse width	40		ns

**Table 5.20 CNTR0 input, CNTR1 input, INT2 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

**Table 5.21 TCIN input, INT3 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 <sup>(1)</sup>		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 <sup>(2)</sup>		ns
tWL(TCIN)	TCIN input LOW pulse width	600 <sup>(2)</sup>		ns

**NOTES**

- 1 : When using the Timer C input capture mode, adjust the cycle time above ( 1/ Timer C count source frequency x 3).
- 2 : When using the Timer C input capture mode, adjust the pulse width above ( 1/ Timer C count source frequency x 1.5).

**Table 5.22 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CLK)	CLKi input cycle time	300		ns
tW(CLKH)	CLKi input HIGH pulse width	150		ns
tW(CLKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

**Table 5.23 External interrupt INT0 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	INT0 input HIGH pulse width	380 <sup>(1)</sup>		ns
tW(INL)	INT0 input LOW pulse width	380 <sup>(2)</sup>		ns

**NOTES**

- 1 : When selecting the digital filter by the INT0 input filter select bit, use the INT0 input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.
- 2 : When selecting the digital filter by the INT0 input filter select bit, use the INT0 input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.



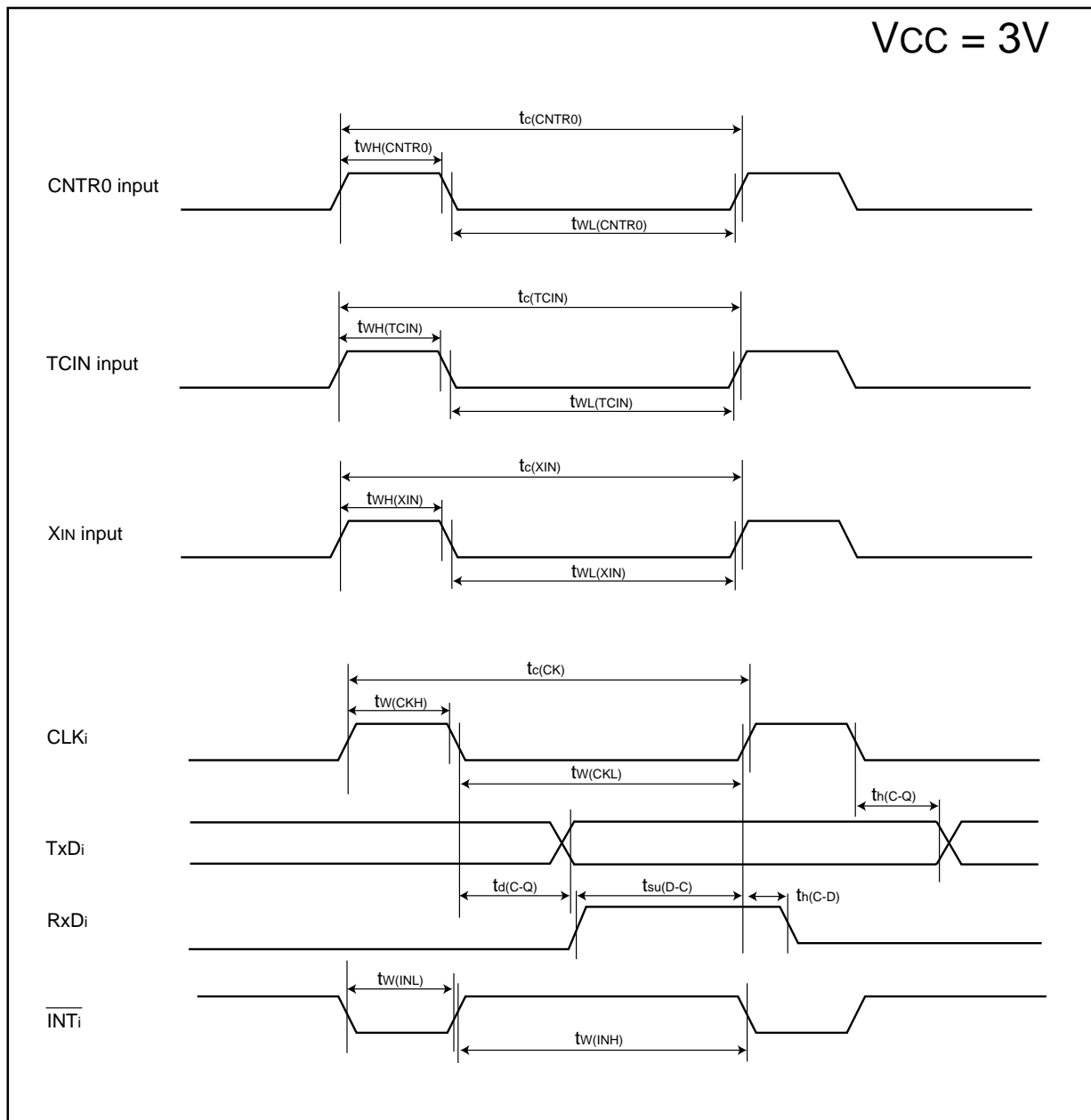


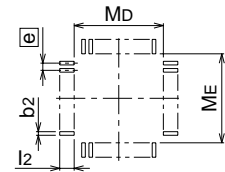
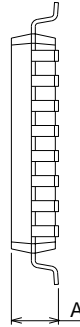
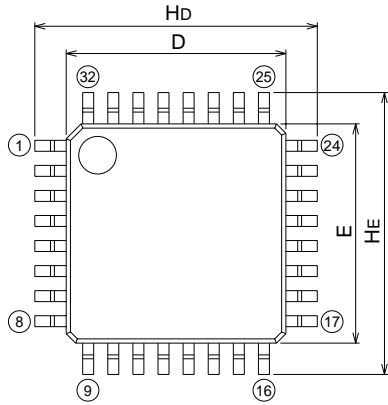
Figure 5.5 Vcc=3V timing diagram

Package Dimensions

32P6U-A

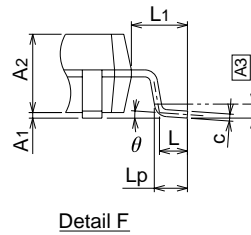
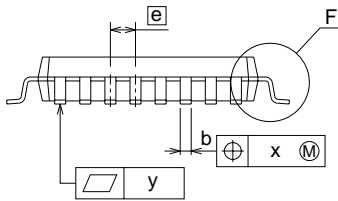
Plastic 32pin 7X7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	—		Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.8	—
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0 <sub>i</sub>	—	10 <sub>i</sub>
b2	—	0.5	—
l2	1.0	—	—
Md	—	7.4	—
ME	—	7.4	—



REVISION HISTORY

R8C/11 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 10 12 14	Table 1.1: Shortest instruction execution time and $f(X_{IN})$ changed Figure 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ Table 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ The value of HR1 register after reset changed The value of TC register after reset changed Chapter "5. Electrical Characteristics" added
1.20	Oct. 31, 2003	2 6 11  14 15 17 19  20 21 22 23  24 25	Table 1.1: Power consumption values added Table 1.3: Resistor value for $CNV_{SS}$ and MODE deleted Register name of address 0050 <sub>16</sub> modified from CMP2IC to CMP1IC, register name of address 005C <sub>16</sub> modified from CMP1IC to CMP0IC Table 5.2: Note 3 and Note 4 deleted $t_{smp}$ in Table 5.3 deleted Figure 5.1 added Table 5.10: $V_{CC}$ changed from "4.2 to 5.5V" to "3.3V to 5.5V", low-power ring oscillator changed from "on 100kHz" to "125kHz", $X_{IN}=5\text{MHz}$ deleted and $X_{IN}=10\text{MHz}$ added in high-speed mode and medium-speed mode, $VC27="0"$ added in stop mode measuring condition, data added and modified Table 11 to Table 15 added Figure 5.2 added Table 5.16: Note 1, $f_{(BCLK)}=5\text{ MHz}$ changed to 10 MHz Table 5.17: low-power ring oscillator changed from "on 100kHz" to "125kHz", $X_{IN}=5\text{MHz}$ deleted and $X_{IN}=10\text{MHz}$ added in high-speed mode and medium-speed mode, $VC27="0"$ added in stop mode measuring condition, data added and modified Table 5.18 to Table 5.22 added Figure 5.3 added
1.30	Dec 05, 2003	4 15	Table 1.2 : ** deleted Table 5.4 revised
1.40	Sep 30, 2004	all pages 2 5 6 9 10-13 12 14 15 16 17 18	Words standardized (on-chip oscillator, serial interface, A/D) Table 1.1 revised Figure 1.3, NOTES 3 added Table 1.3 revised Figure 3.1, NOTES added One body sentence in chapter 4 added ; Title of Table 4.1 to 4.4 added Table 4.3 revised ; Table 4.4 revised Table 5.2 revised Table 5.3 revised Table 5.4 revised ; Table 16.5 revised Table 5.6, 5.7 adn 5.8 revised ; Figure 5.3 revised Table 5.9 revised ; Table 5.10 revised

REVISION HISTORY

R8C/11 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.40	Sep 30, 2004	20	Table 5.12 revised ; Table 5.16 revised
		22	Table 16.17 revised
		24	Table 16.19 revised

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