

General Description

The Extended Line Card Controller (ELIC) PEB 20550-H is a device to allow the control, supervision and processing of voice, data and signaling information. It also provides access for the microcontroller to write/read data to/from the IOM and PCM interfaces and gives control over layer-1 devices. Revolutionary is the multiplexing concept allowing to use only one implemented HDLC controller to process the signaling information for up to 32 digital subscribers.

The switching part of the ELIC controls space and times switching functions between subscriber line devices and time division multiplex highways. Furthermore it controls the flow of information between the subscriber interface ports and a processor.

For processing signaling information two different HDLC controllers are implemented. The **SACCO A** is a Serial Access Communication Controller (HDLC) which allows extracting D-Channel information transported on the IOM interface. The data is then passed to the microcontroller. In the downstream direction, the SACCO A passes data, packed in the HDLC protocol, from the microcontroller to the IOM interface.

With 4 IOM interfaces, and 8 digital subscribers possible per interface, former designs needed 32 HDLC controllers (one for the D-channel of every subscriber). The SACCO A of the ELIC can serve all 32 channels in a time-multiplexing manner. This process is controlled by the **BUS ARBITER**. This part of the ELIC monitors all D-channels of the IOM interface and locks the SACCO A onto one D-channel as soon as the start of a HDLC frame is detected. After the end-flag of the HDLC frame has been received, the SACCO A is released again and can lock onto the next D-channel as soon as a new request is detected. During the assignment of the HDLC controller to a certain channel the other subscribers are not allowed to send information on their D-channels. To assure this a blocking mechanism is implemented which indicates to corresponding terminals that they may not use the D-channel. This mechanism works as well for the standard ISDN S_0 as for the proprietary U_P interface, a two wire ISDN capable interface for PBXs. Any ISDN Telephone can be connected to a PBX because the standard arbitration mechanism is used for blocking the phones.

This concept saves the space and the costs of up to 32 HDLC controllers. Due to the bursty characteristic of the signaling data, one HDLC controller is sufficient to process this data flow. For central office applications the ELIC is not recommended when the arbiter is used, as PTTs require transparent D-channels. In this case the SACCO A can be used as an independent HDLC controller.

If the design needs higher D-channel data rates additional HDLC controllers (IDEC, PEB 2075) can be connected. This can either be done on the IOM interface and is then fixed for a certain subscriber or via the PCM interface which makes this extra HDLC controller flexibly assignable.

Type	Package
PEB 20550-H	P-MQFP-80-1 (SMD)

The **SACCO B** is a second integrated HDLC controller behaving like an external device. It is mainly intended for signaling information between the line card and the group processor on the main board. This can be done either via a dedicated signaling highway or via the PCM highway. The SACCO B can also be used for music on hold, conferencing access and other features. The HDLC information handling between SACCO A and SACCO B always has to go via a microprocessor.

Features

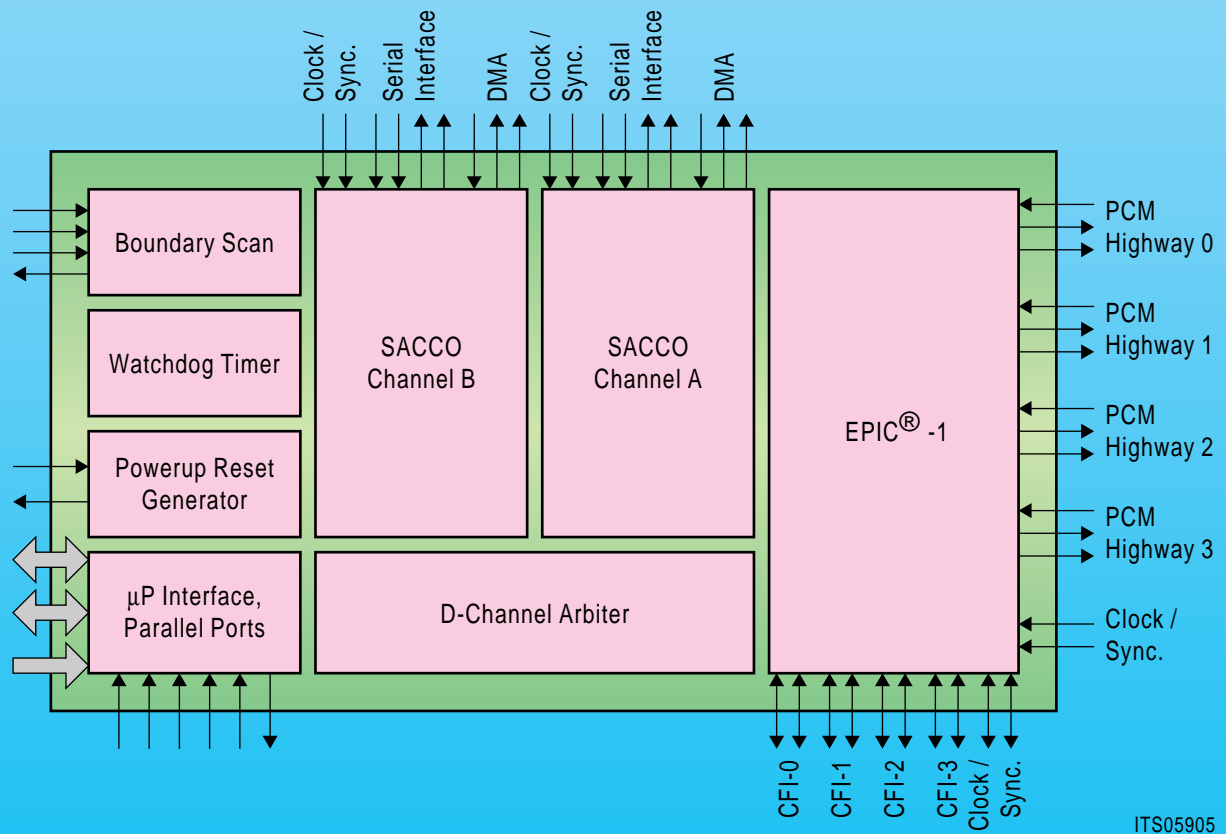
- Configurable interface (CFI) programmable for IOM-2, IOM-1, SLD or PCM
- Switching between configurable interface (e.g. IOM-2) and PCM ports
- Switching of 64 B-channels (32 digital or 64 analog subscribers) without blocking (128×128 matrix)
- Two HDLC controllers with 64-byte FIFOs implemented
- Arbiter logic to use one of the HDLC-controllers time multiplexed for a maximum of 32 digital subscribers
- Full-duplex signaling protocols (LAPD or proprietary)
- HDLC broadcast messages
- DMA access to HDLC data
- Boundary scan

Application Areas

- PBX:
 - analog line cards
 - digital line cards
- CO:
 - analog line cards (with disabled arbiter)
 - digital line cards (with disabled arbiter)

Interfaces

- 4 configurable interfaces (individually programmable for IOM, SLD, PCM)
- 4 PCM interfaces (maximum combined data rate of 8 Mbit/s)
- μP interface (Siemens/Intel and Motorola interface, multiplexed and demultiplexed address/data bus)
- Boundary scan (for on-board tests)
- DMA interface



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Block Diagram