LTC1418

Low Power, 14-Bit, 200ksps ADC with Serial and Parallel I/O

January 1998

FEATURES

- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 200ksps**
- **±1.5LSB INL and ±1LSB DNL Max**
- **Power Dissipation: 15mW (Typ)**
- **Parallel or Serial Data Output**
- No Missing Codes Over Temperature
- Power Shutdown: Nap and Sleep
- External or Internal Reference
- Differential High Impedance Analog Input
- Input Range: 0V to 4.096V or ±2.048V
- 82dB S/(N + D) and 95dB THD at Nyquist
- 28-Pin SSOP Package

APPLICATIONS

- Remote Data Acquisition
- Battery Operated Systems
- Digital Signal Processing
- Isolated Data Acquisition Systems
- Audio and Telecom Processing
- Medical Instrumentation

DESCRIPTION

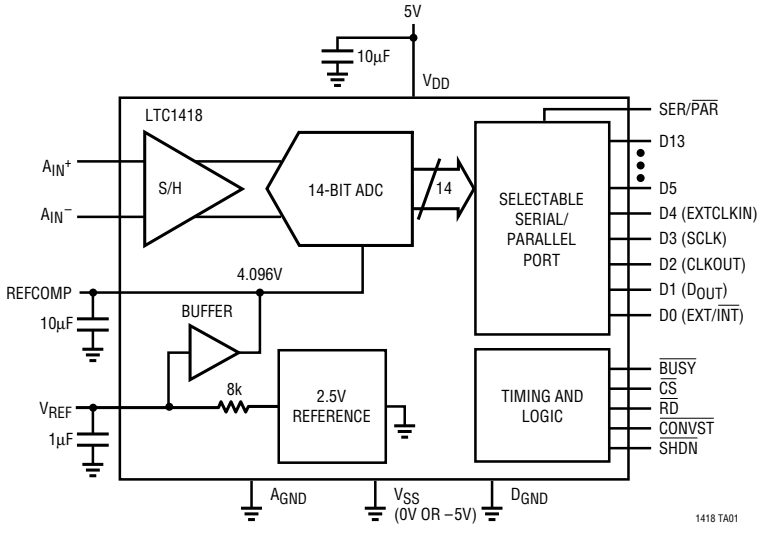
The LTC®1418 is a low power, 200ksps, 14-bit A/D converter. Data output is selectable for 14-bit parallel or serial format. This versatile device can operate from a single 5V or ±5V supply. An onboard high performance sample-and-hold, a precision reference and internal timing minimize external circuitry requirements. The low 15mW power dissipation is made even more attractive with two user selectable power shutdown modes.

The LTC1418 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. DC specs include ±1.5LSB INL, ±1LSB DNL and no missing codes over temperature. Outstanding AC performance includes 82dB S/(N + D) and 95dB THD at the Nyquist input frequency of 100kHz.

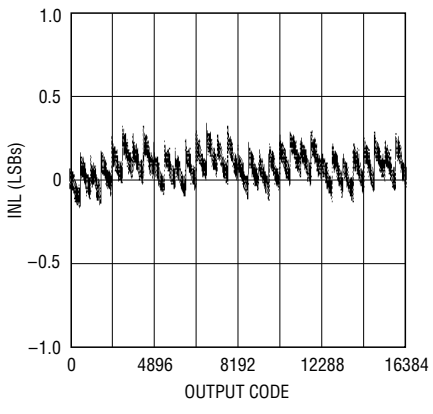
The flexible output format allows either parallel or serial I/O. The SPI/MICROWIRE™ compatible serial I/O port can operate as either master or slave and can support clock frequencies from DC to 10MHz. A separate convert start input and a data ready signal ($\overline{BUSY}$) allow easy control of conversion start and data transfer.

TYPICAL APPLICATION

Low Power, 200kHz, 14-Bit Sampling A/D Converter



Typical INL Curve

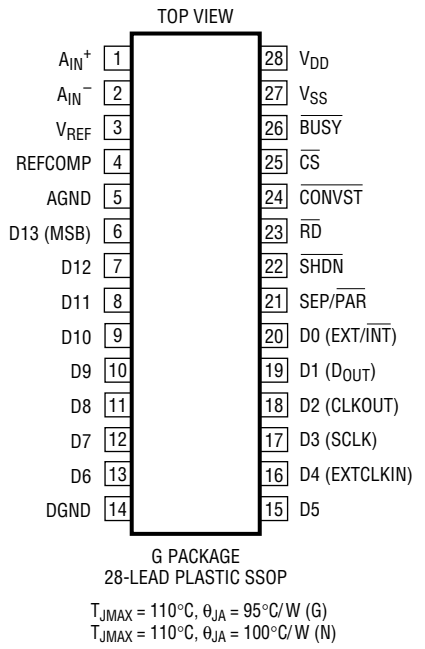


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... –0.3V to (V_{DD} + 0.3V)
  Bipolar Operation ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4)
  Unipolar Operation ..... –0.3V to 10V
  Bipolar Operation ..... (V_{SS} – 0.3V) to 10V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to (V_{DD} + 0.3V)
  Bipolar Operation ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operation Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 110°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)

ORDER PART NUMBER
LTC1418ACG
LTC1418CG

Consult factory for Industrial grade, Military grade and N package parts.

CONVERTER CHARACTERISTICS

With internal reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1418 MIN	LTC1418 TYP	LTC1418 MAX	LTC1418A MIN	LTC1418A TYP	LTC1418A MAX	UNITS
Resolution (No Missing Codes)		●	13			14			Bits
Integral Linearity Error	(Note 7)	●		±0.8	±2		±0.5	±1.25	LSB
Differential Linearity Error		●		±0.7	±1.5		±0.35	±1	LSB
Offset Error	(Note 8)	●		±5	±20		±2	±10	LSB
Full-Scale Error	Internal Reference External Reference = 2.5V			±10 ±5	±60 ±30		±20 ±5	±60 ±15	LSB LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0, Internal Reference $I_{OUT(REF)}$ = 0, External Reference	●		±15 ±5			±10 ±1	±45	ppm/°C ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V (Unipolar) 4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V (Bipolar)	● ●		0 to 4.096 ±2.048		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			25 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time	Commercial Industrial	● ●		300 300	1000 1000	ns ns

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal	●	79	82		dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics	●		–95	–86	dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal	●	86	95		dB
IMD	Intermodulation Distortion	f_{IN1} = 97.7kHz, f_{IN2} = 104.2kHz			–90		dB
	Full Power Bandwidth				5		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 77dB			0.5		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.05 0.05		LSB/V LSB/V
V_{REF} Output Resistance	0.1mA ≤ $\lvert I_{OUT} \rvert$ ≤ 0.1mA			8		kΩ

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA V_{DD} = 4.75V, I_O = –200µA	 ●	 4.0	4.74		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA V_{DD} = 4.75V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D13 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D13 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 10, 11)			4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 10)	Bipolar Only (V_{SS} = 0V for Unipolar)		–4.75		–5.25	V
I_{DD}	Positive Supply Current	Unipolar, $\overline{RD}$ High (Note 5)	●		3	4	mA
		Bipolar, $\overline{RD}$ High (Note 5)	●		3.4	4	mA
	Nap Mode	$\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V (Note 12)			570		µA
	Sleep Mode	$\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V (Note 12)			2		µA
I_{SS}	Negative Supply Current	Bipolar, $\overline{RD}$ High (Note 5)	●		1.4	1.8	mA
	Nap Mode	$\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V (Note 12)			0.1		µA
	Sleep Mode	$\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V (Note 12)			0.1		µA
P_{DIS}	Power Dissipation	Unipolar	●		15	20	mW
		Bipolar	●		24	29	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	200			kHz
t_{CONV}	Conversion Time		●		3.4	4	µs
t_{ACQ}	Acquisition Time		●		0.3	1	µs
$t_{ACQ} + t_{CONV}$	Acquisition Plus Conversion Time		●		3.7	5	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	40			ns
t_3	$\overline{CS}\downarrow$ to $\overline{SHDN}\downarrow$ Setup Time to Ensure Nap Mode	(Notes 9, 10)	●	40			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time from Nap Mode	(Note 10)			500		ns
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	CL = 25pF	●		35	70	ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$		 ●	20 15	35		ns ns
t_8	Delay Between Conversions	(Note 10)	●	500			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$		●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF	 ●		15	30 40	ns ns
		C_L = 100pF	 ●		20	40 55	ns ns
t_{11}	Bus Relinquish Time	 Commercial Industrial	 ● ●		8	20 25 30	ns ns ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time			40			ns
t_{14}	Delay Time, SCLK$\downarrow$ to D_{OUT} Valid	C_L = 25pF (Note 9)	●		35	70	ns
t_{15}	Time from Previous Data Remain Valid After SCLK$\downarrow$	C_L = 25pF (Note 9)	●	15	25		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{CC} without latchup.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = 0V or –5V, f_{SAMPLE} = 200kHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended input with A_{IN}^- grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: The falling edge of $\overline{CONVST}$ starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion, it can create small errors. For best performance ensure that $\overline{CONVST}$ returns high either within 2.1µs after the conversion starts or after BUSY rises.

Note 12: Pins 16 (D4/EXTCLKIN), 17 (D3/SCLK) and 20 (DO/EXT/$\overline{INT}$) at 0V or 5V. See Power Shutdown.

PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input.

A_{IN}^- (Pin 2): Negative Analog Input.

V_{REF} (Pin 3): 2.50V Reference Output. Bypass to AGND with 1µF.

REFCOMP (Pin 4): 4.096V Reference Bypass Pin. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

AGND (Pin 5): Analog Ground.

D13 to D6 (Pins 6 to 13): Three-State Data Outputs (Parallel). D13 is the most significant bit.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D5 (Pin 15): Three-State Data Output (Parallel).

D4 (EXTCLKIN) (Pin 16): Three-State Data Output (Parallel). Conversion clock input (serial) when Pin 20 (EXT/$\overline{INT}$) is tied to high.

D3 (SCLK) (Pin 17): Three-State Data Output (Parallel). Data clock input (serial).

D2 (CLKOUT) (Pin 18): Three-State Data Output (Parallel). Conversion clock output (serial).

D1 (D_{OUT}) (Pin 19): Three-State Data Output (Parallel). Serial data output (serial).

D0 (EXT/$\overline{INT}$) (Pin 20): Three-State Data Output (Parallel). Conversion clock selector (serial). An input low enables the internal conversion clock. An input High indicates an external conversion clock will be assigned to Pin 16 (EXTCLKIN).

SER/$\overline{PAR}$ (Pin 21): Date Output Mode.

$\overline{SHDN}$ (Pin 22): Power Shutdown Input. Low selects shutdown. Shutdown mode selected by $\overline{CS}$. $\overline{CS}$ = 0 for nap mode and $\overline{CS}$ = 1 for sleep mode.

$\overline{RD}$ (Pin 23): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CONVST}$ (Pin 24): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

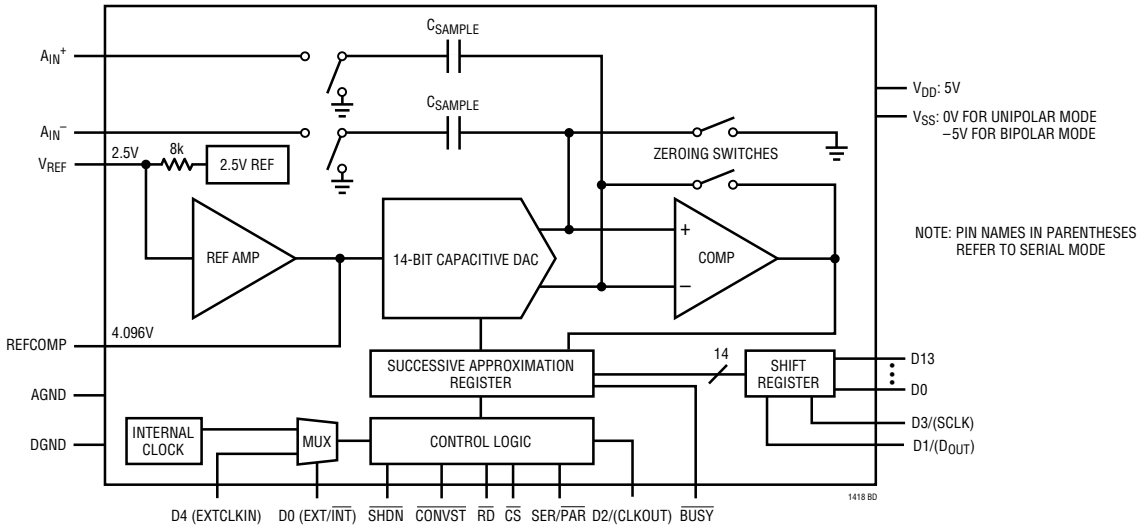
$\overline{CS}$ (Pin 25): Chip Select. This input must be low for the ADC to recognize the $\overline{CONVST}$ and $\overline{RD}$ inputs. $\overline{CS}$ also sets the shutdown mode when $\overline{SHDN}$ goes low. $\overline{CS}$ and $\overline{SHDN}$ low select the quick wake-up nap mode. $\overline{CS}$ high and $\overline{SHDN}$ low select sleep mode.

$\overline{BUSY}$ (Pin 26): The $\overline{BUSY}$ Output Shows the Converter Status. It is low when a conversion is in progress.

V_{SS} (Pin 27): Negative Supply, –5V for Bipolar Operation. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic. Analog ground for unipolar operation.

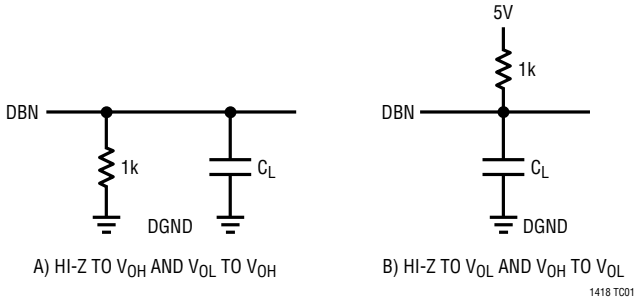
V_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

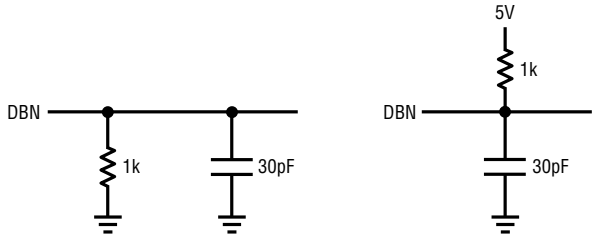
Load Circuits for Access Timing



A) HI-Z TO V_{OH} AND V_{OL} TO V_{OH} B) HI-Z TO V_{OL} AND V_{OH} TO V_{OL}

1418 TC01

Load Circuits for Output Float Delay



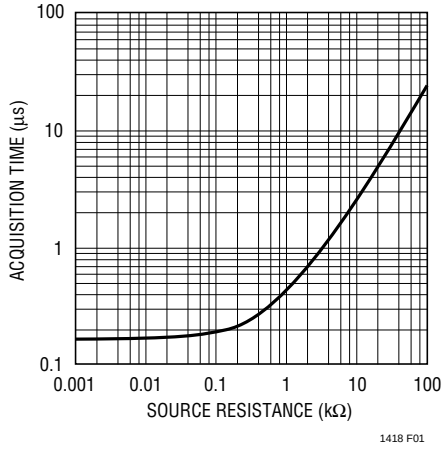
A) V_{OH} TO HI-Z B) V_{OL} TO HI-Z

1418 TC02

APPLICATIONS INFORMATION

Driving the Analog Input

The differential analog inputs of the LTC1418 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1418 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 1). For minimum acquisition time, with high source impedance, a buffer amplifier must be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts—1μs for full throughput rate.



1418 F01

Figure 1. t_{ACQ} vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a closed-loop bandwidth of 10MHz, then the output impedance at 10MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 5MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

Suitable devices capable of driving the ADC's input include the LT®1354 and LT1357 op amps. The noise and the distortion of the input amplifier must also be considered, since they will add to the LTC1418 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 6MHz. Any noise that is present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. For AC applications a simple 1-pole RC filter is usually sufficient. For example, a 1000pF capacitor

APPLICATIONS INFORMATION

from the input to ground and a 100Ω source resistor will limit the input bandwidth to 1.6MHz. Simple RC filters work well for AC applications, but they will limit the transient response. For full speed operation, a fast settling, low noise amplifier should be chosen.

Internal Reference

The LTC1418 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.500V. It is internally connected to a reference amplifier and is available at Pin 3. A 8k resistor is in series with the output so that it can be easily overdriven in applications where an external reference is required, see Figure 2. The reference amplifier compensation pin (REFCOMP, Pin 4) must be connected to a capacitor to ground. The reference is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The reference should be kept in the range of 2.25V to 2.75V for specified linearity.

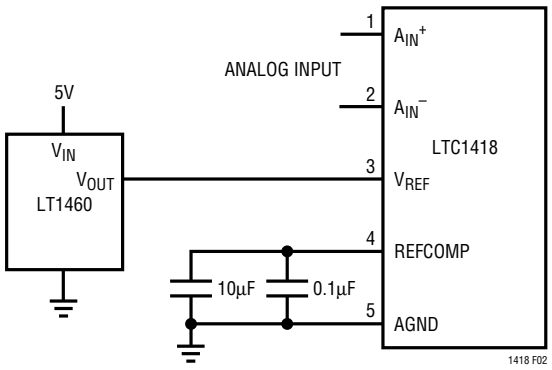


Figure 2. Using the LT1460 as an External Reference

UNIPOLAR / BIPOLAR OPERATION AND ADJUSTMENT

Figure 3a shows the ideal input/output characteristics for the LTC1418. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, … FS – 1.5LSB). The output code is natural binary with 1LSB = FS/16384 = 4.096V/16384 = 250µV. Figure 3b shows the input/output transfer characteristics for the bipolar mode in two's complement format.

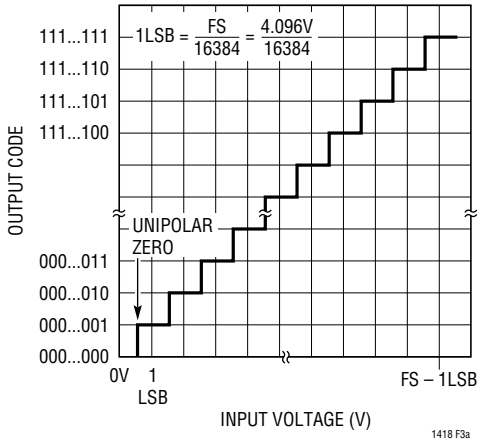


Figure 3a. LTC1418 Unipolar Transfer Characteristics

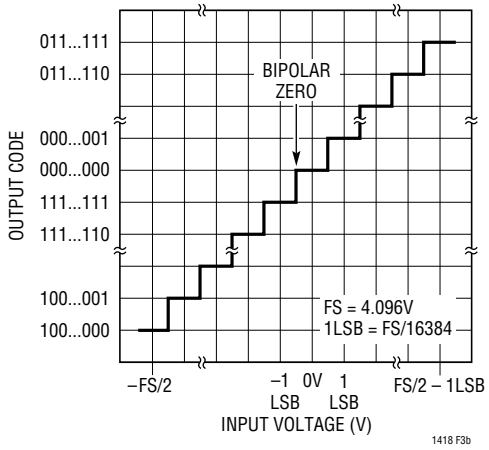


Figure 3b. LTC1418 Bipolar Transfer Characteristics

Unipolar Offset and Full-Scale Error Adjustment

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figures 4a and 4b show the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply 125µV (i.e., 0.5LSB) at the input and adjust the offset at the A_{IN}^- input until the output code flickers between 0000 0000 0000 00 and 0000 0000 0000 01. For full-scale adjustment, an input voltage of 4.095625V (FS – 1.5LSBs) is applied to A_{IN}^+ and R2 is adjusted until the output code flickers between 1111 1111 1111 10 and 1111 1111 1111 11.

APPLICATIONS INFORMATION

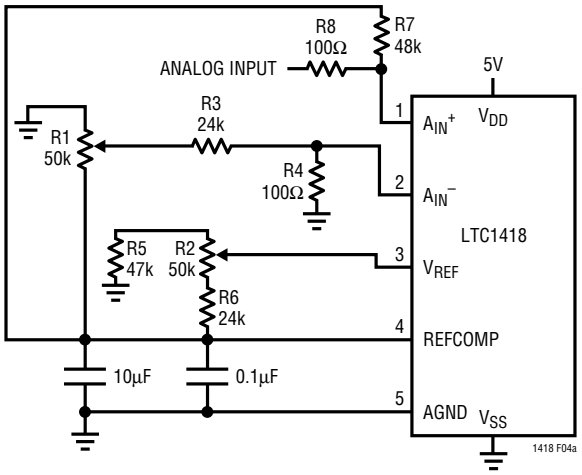


Figure 4a. Offset and Full-Scale Adjust Circuit if –5V is Not Available

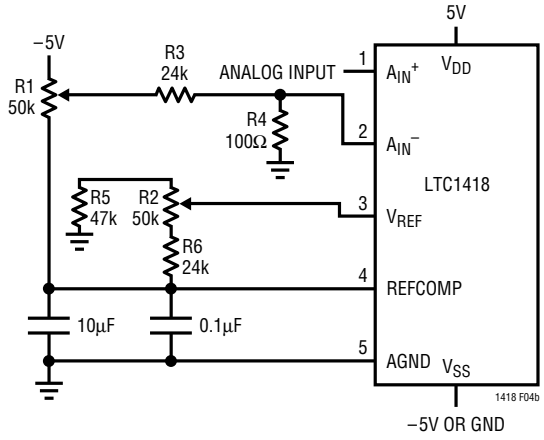


Figure 4b. Offset and Full-Scale Adjust Circuit if –5V is Available

Bipolar Offset and Full-Scale Error Adjustment

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset error must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply –125µV (i.e., –0.5LSB) at A_{IN}^+ and adjust the offset at the A_{IN}^- input until the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 2.047625V (FS – 1.5LSBs) is applied to A_{IN}^+ and R2 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.

BOARD LAYOUT AND GROUNDING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1418, a printed circuit board with ground plane is required. The ground plane under the ADC area should be as free of breaks and holes as possible, such that a low impedance path between all ADC grounds and all ADC decoupling capacitors is provided. It is critical to prevent digital noise from being coupled to the analog input, reference or analog power supply lines. Layout should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND) and Pin 14 (DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the V_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1418 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1418 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 1) and A_{IN}^- (Pin 2) should be kept as short as possible. In applications where this is not

APPLICATIONS INFORMATION

possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Power Shutdown

The LTC1418 provides two power shutdown modes, nap and sleep, to save power during inactive periods. The nap mode reduces the power by 80% and leaves only the digital logic and reference powered up. The wake-up time from nap to active is 500ns (see Figure 5a). In sleep mode all bias currents are shut down and only leakage current remains—about 2µA. Wake-up time from sleep mode is much slower since the reference circuit must power up and settle to 0.005% for full 14-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 30ms with the recommended 10µF capacitor. Shutdown is controlled by Pin 22 ($\overline{SHDN}$); the ADC is in shutdown when it is low. The shutdown mode is selected with

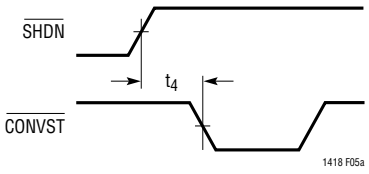


Figure 5a. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

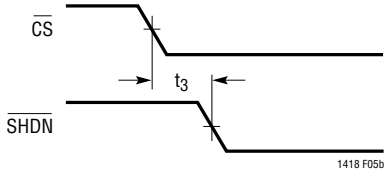


Figure 5b. $\overline{CS}$ to $\overline{SHDN}$ Timing

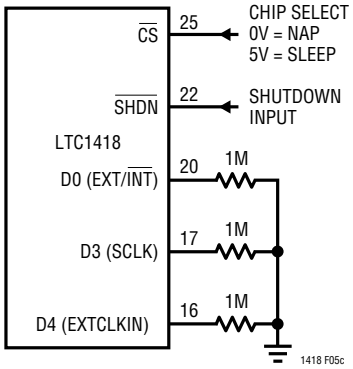


Figure 5c. Shutdown Circuit When Pins 16, 17 and 20 Are Not Driven

Pin 25 ($\overline{CS}$); low selects nap (see Figure 5b), high selects sleep.

Pins 16 (D4/EXTCLKIN), 17 (D3/SCLK) and 20 (D0/EXT/$\overline{INT}$) must be high (= V_{DD}) or low (0V) during shutdown to avoid unwanted supply current from input buffers tied to these pins. If the pins are driven high or low during shutdown, unwanted current is avoided. If not, 1M pull-down resistors can be used as in Figure 5c.

DIGITAL INTERFACE

The LTC1418 can operate in serial or parallel mode. In parallel mode the ADC is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. In serial mode only four digital interface lines are required, SCLK, $\overline{CONVST}$, EXTCLKIN and D_{OUT}. SCLK, the serial data shift clock can be an external input or supplied by the LTC1418 internal clock.

Internal Clock

The ADC has an internal clock. In parallel output mode the internal clock is always used as the conversion clock. In serial output mode either the internal clock or an external clock may be used as the conversion clock (see Figure 12). The internal clock is factory trimmed to achieve a typical conversion time of 3.4µs and a maximum conversion time over the full operating temperature range of 4µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 1µs, throughput performance of 200ksps is assured.

APPLICATIONS INFORMATION

Conversion Control

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. A logic "0" applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low, see Figure 6). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

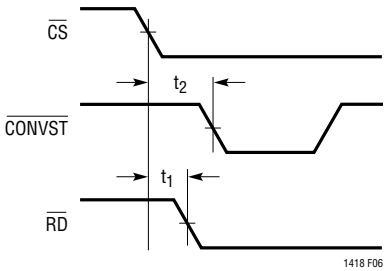


Figure 6. $\overline{CS}$ to $\overline{CONVST}$ Set-Up Timing

Data Output

The data format is controlled by the SER/$\overline{PAR}$ input pin; logic low selects parallel output format. In parallel mode the 14-bit data output word D0 to D13 is updated at the end of each conversion on Pins 6 to 13 and Pins 15 to 20. A logic high applied to SER/$\overline{PAR}$ selects the serial formatted data output and Pins 16 to 20 assume their serial function, Pins 6 to 13 and 15 are in the Hi-Z state. In either parallel or serial data formats, outputs will be active only when $\overline{CS}$ and $\overline{RD}$ are low. Any other combination of $\overline{CS}$ and $\overline{RD}$ will three-state the output. In unipolar mode (V_{SS} = 0V) the data will be in straight binary format (corresponding to the unipolar input range). In bipolar mode (V_{SS} = –5V), the data will be in two's complement format (corresponding to the bipolar input range).

Parallel Output Mode

Parallel mode is selected with a logic 0 applied to the SER/$\overline{PAR}$ pin. Figures 7 through 11 show different modes of parallel output operation. In modes 1a and 1b (Figures 7 and 8) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 9) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared databus.

In slow memory and ROM modes (Figures 10 and 11), $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low and starts the conversion. $\overline{BUSY}$ goes low forcing the processor into a wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

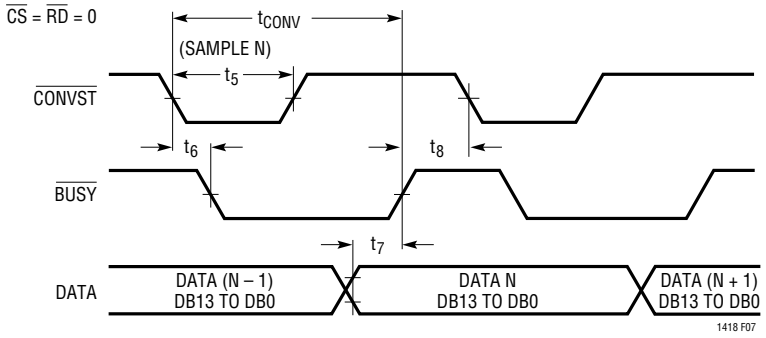


Figure 7. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⊓⊓⊓)

APPLICATIONS INFORMATION

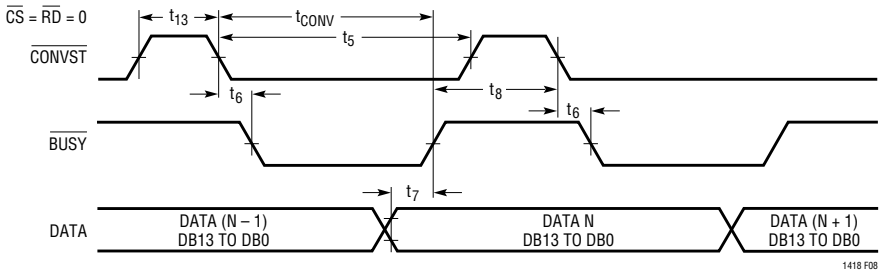


Figure 8. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⎍⎍⎍)

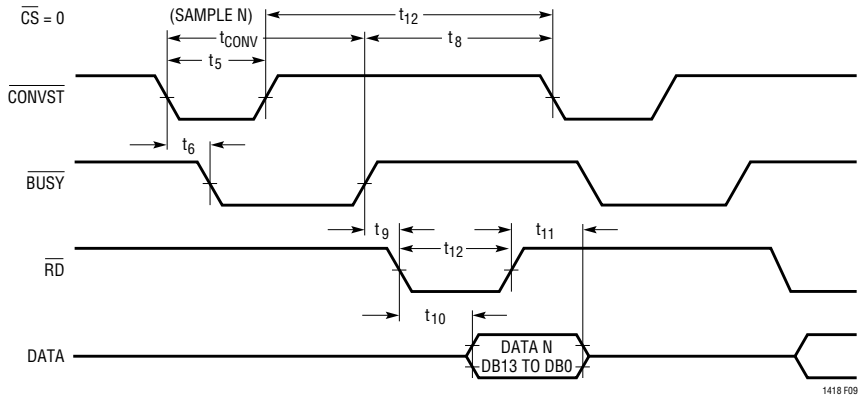


Figure 9. Mode 2. $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

APPLICATIONS INFORMATION

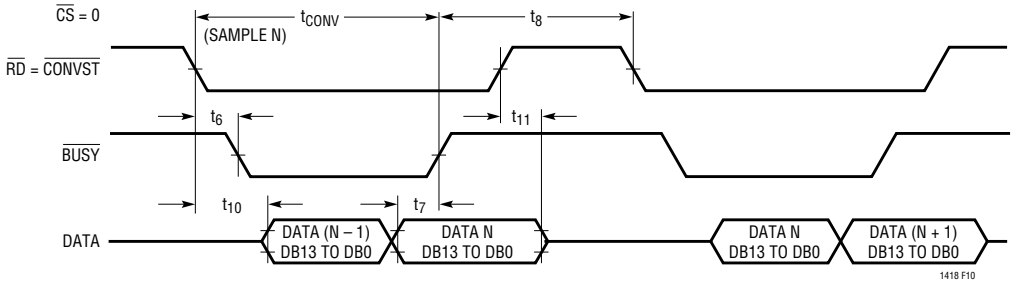


Figure 10. Slow Memory Mode Timing

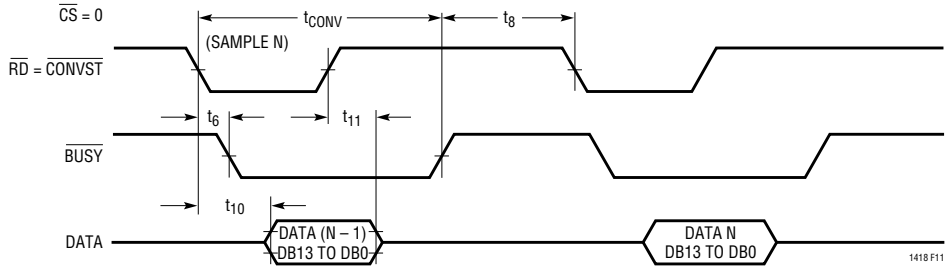


Figure 11. ROM Mode Timing

APPLICATIONS INFORMATION

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

Serial Output Mode

Serial output mode is selected when the SER/$\overline{PAR}$ input pin is high. In this mode, Pins 16 to 20, D0 (EXT/$\overline{INT}$), D1 (D_{OUT}), D2 (CLKOUT), D3 (SCLK) and D4 (EXTCLKIN) assume their serial functions as shown in Figure 12. (During this discussion these pins will be referred to by their serial function names: EXT/$\overline{INT}$, D_{OUT}, CLKOUT, SCLK and EXTCLKIN.) As in parallel mode, conversions are started by a falling $\overline{CONVST}$ edge with $\overline{CS}$ low. After a conversion is completed and the output shift register has been updated, $\overline{BUSY}$ will go high and valid data will be available on D_{OUT} (Pin 19). This data can be clocked out either before the next conversion starts or it can be clocked out during the next conversion. To enable the serial data output buffer and shift clock, $\overline{CS}$ and $\overline{RD}$ must be low.

Figure 12 shows a function block diagram of the LTC1418 in serial mode. There are two pieces to this circuitry: the conversion clock selection circuit (EXT/$\overline{INT}$, EXTCLKIN and CLKOUT) and the serial port (SCLK, D_{OUT}, $\overline{CS}$ and $\overline{RD}$).

Conversion Clock Selection (Serial Mode)

In Figure 12, the conversion clock controls the internal ADC operation. The conversion clock can be either internal or external. By connecting EXT/$\overline{INT}$ low, the internal clock is selected. This clock generates 16 clock cycles which feed into the SAR for each conversion.

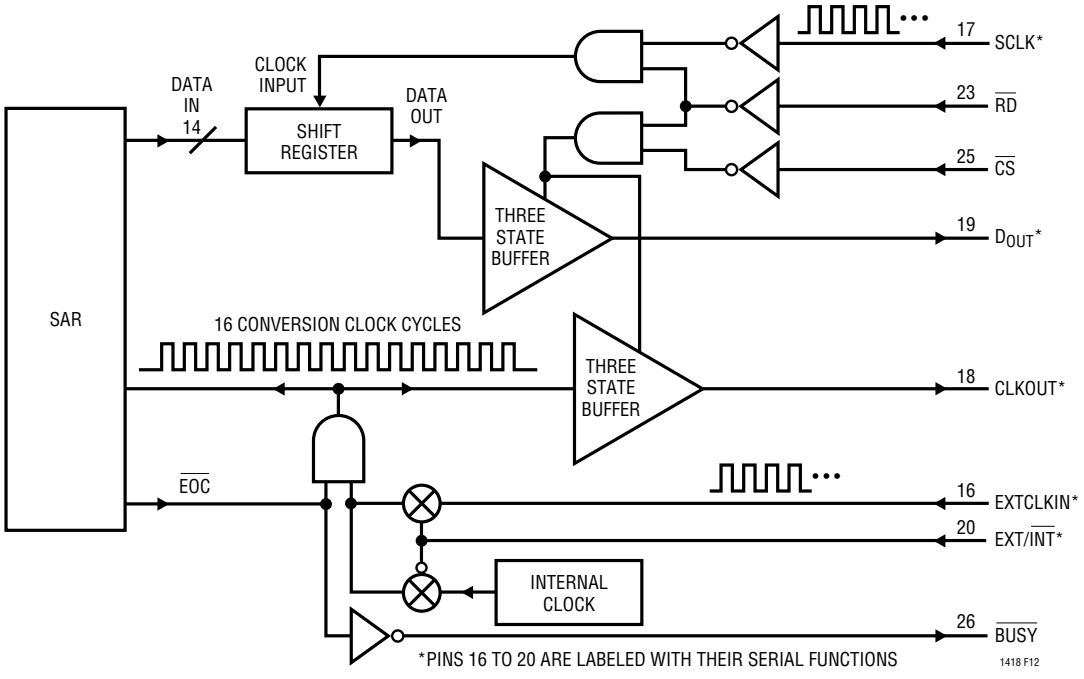


Figure 12. Functional Block Diagram for Serial Mode (SER/$\overline{PAR}$ = High)

APPLICATIONS INFORMATION

To select an external conversion clock, tie EXT/$\overline{INT}$ high and apply an external conversion clock to EXTCLKIN (Pin 16). (When an external shift clock (SCLK) is used during a conversion, the SCLK should be used as the external conversion clock to avoid the noise generated by the asynchronous clocks. To maintain accuracy the external conversion clock frequency must be between 30kHz and 4.5MHz.) The SAR sends an end of conversion signal, $\overline{EOC}$, that gates the external conversion clock so that only 16 clock cycles can go into the SAR, even if the external clock, EXTCLKIN, contains more than 16 cycles.

When $\overline{CS}$ and $\overline{RD}$ are low, these 16 cycles of conversion clock (whether internally or externally generated) will appear on CLKOUT during each conversion and then CLKOUT will remain low until the next conversion. If desired, CLKOUT can be used as a master clock to drive the serial port. Because CLKOUT is running during the conversion, it is important to avoid excessive loading that can cause large supply transients and create noise. For the best performance, limit CLKOUT loading to 20pF.

Serial Port

The serial port in Figure 12 is made up of a 16-bit shift register and a three-state output buffer that are controlled by three inputs: SCLK, $\overline{RD}$ and $\overline{CS}$. The serial port has one output, D_{OUT}, that provides the serial output data.

The SCLK is used to clock the shift register. Data may be clocked out with the internal conversion clock operating as a master by connecting CLKOUT (Pin 18) to SCLK (Pin 17) or with an external data clock applied to D3 (SCLK). The minimum number of SCLK cycles required to transfer a data word is 14. Normally, SCLK contains 16 clock cycles for a word length of 16 bits; 14 bits with MSB first, followed by two trailing zeros.

A logic high on $\overline{RD}$ disables SCLK and three-states D_{OUT}. In case of using a continuous SCLK, $\overline{RD}$ can be controlled to limit the number of shift clocks to the desired number (i.e., 16 cycles) and to three-state D_{OUT} after the data transfer.

A logic high on $\overline{CS}$ three-states the D_{OUT} output buffer. It also inhibits conversion when it is tied high. In power shutdown mode ($\overline{SHDN}$ = low), a high $\overline{CS}$ selects sleep mode while a low $\overline{CS}$ selects nap mode. For normal serial port operation, $\overline{CS}$ can be grounded.

D_{OUT} outputs the serial data; 14 bits, MSB first, on the falling edge of each SCLK (see Figures 13 and 14). If 16 SCLKs are provided, the 14 data bits will be followed by two zeros. The MSB (D13) will be valid on the first rising and the first falling edge of the SCLK. D12 will be valid on the second rising and the second falling edge as will all the remaining bits. The data may be captured on either edge. The largest hold time margin is achieved if data is captured on the rising edge of SCLK.

$\overline{BUSY}$ gives the end of conversion indication. When the LTC1418 is configured as a master serial device, $\overline{BUSY}$ can be used as a framing pulse and to three-state the serial port after transferring the serial output data by tying it to the $\overline{RD}$ pin.

Figures 14 to 17 show several serial modes of operation, demonstrating the flexibility of the LTC1418 serial port.

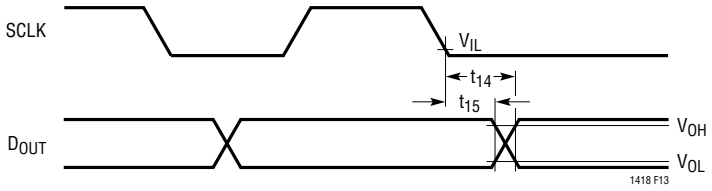


Figure 13. SCLK to D_{OUT} Delay

APPLICATIONS INFORMATION

Serial Data Output During a Conversion

Using Internal Conversion Clock for Conversion and Data Transfer. Figure 14 shows data from the previous conversion being clocked out during the conversion with the LTC1418 internal clock providing both the conversion clock and the SCLK. The internal clock has been optimized for the fastest conversion time, consequently this mode can provide the best overall speed performance. To select an internal conversion clock, tie EXT/$\overline{INT}$ (Pin 20) low. The internal clock appears on CLKOUT (Pin 18) which can be tied to SCLK (Pin 17) to supply the SCLK.

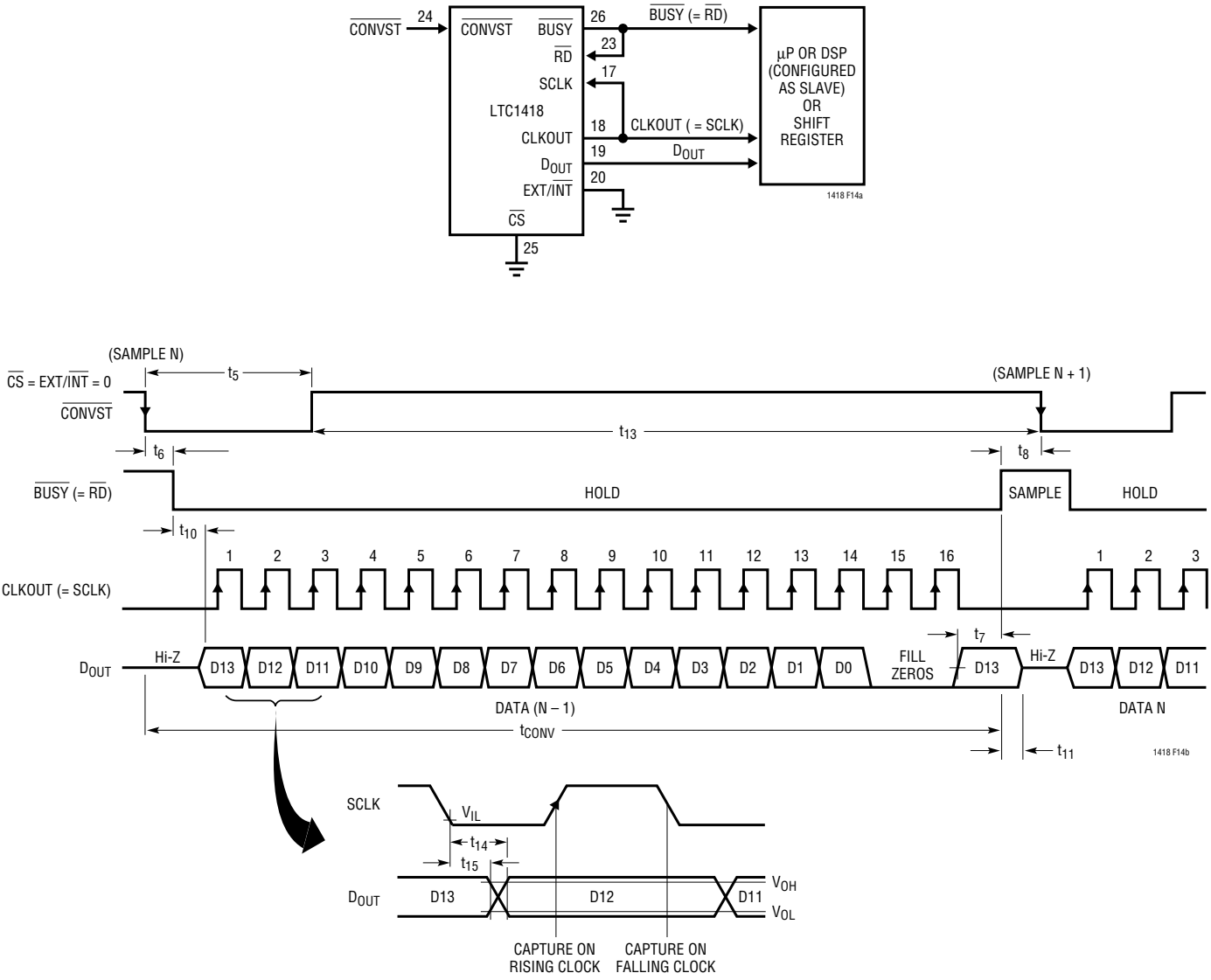


Figure 14. Internal Conversion Clock Selected. Data Transferred During Conversion Using the ADC Clock Output as a Master Shift Clock (SCLK Driven from CLKOUT)

APPLICATIONS INFORMATION

Using External Clock for Conversion and Data Transfer. In Figure 15, data from the previous conversion is output during the conversion with an external clock providing both the conversion clock and the shift clock. To select an external conversion clock, tie EXT/$\overline{INT}$ high and apply the clock to EXTCLKIN. The same clock is also applied to SCLK to provide a data shift clock. To maintain accuracy the conversion clock frequency must be between 30kHz and 4.5MHz.

It is not recommended to clock data with an external clock during a conversion that is running on an internal clock because the asynchronous clocks may create noise.

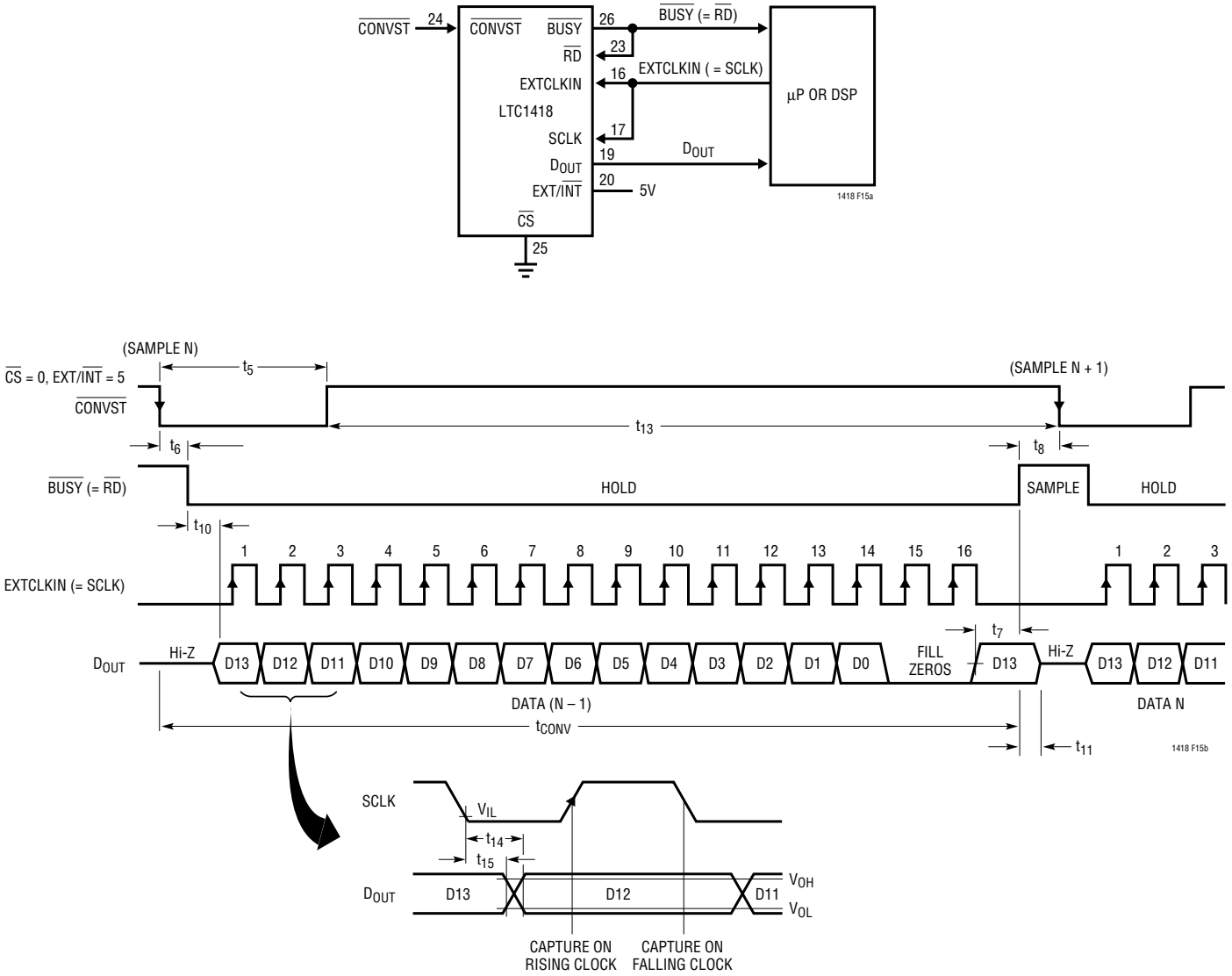


Figure 15. External Conversion Clock Selected. Data Transferred During Conversion Using the External Clock (External Clock Drives Both EXTCLKIN and SCLK)

APPLICATIONS INFORMATION

Serial Data Output After a Conversion

Using Internal Conversion Clock and External Data Clock. In this mode, data is output after the end of each conversion but before the next conversion is started (Figure 16). The internal clock is used as the conversion clock and an external clock is used for the SCLK. This mode is useful in applications where the processor acts as a master serial device. This mode is SPI and MICROWIRE compatible. It also allows operation when the SCLK frequency is very low (less than 30kHz). To select the internal conversion clock tie EXT/$\overline{INT}$ low. The external SCLK is applied to SCLK. $\overline{RD}$ can be used to gate the external SCLK, such that data will clock only after $\overline{RD}$ goes low and to three-state D_{OUT} after data transfer. If more than 16 SCLKs are provided, more zeros will be filled in after the data word indefinitely.

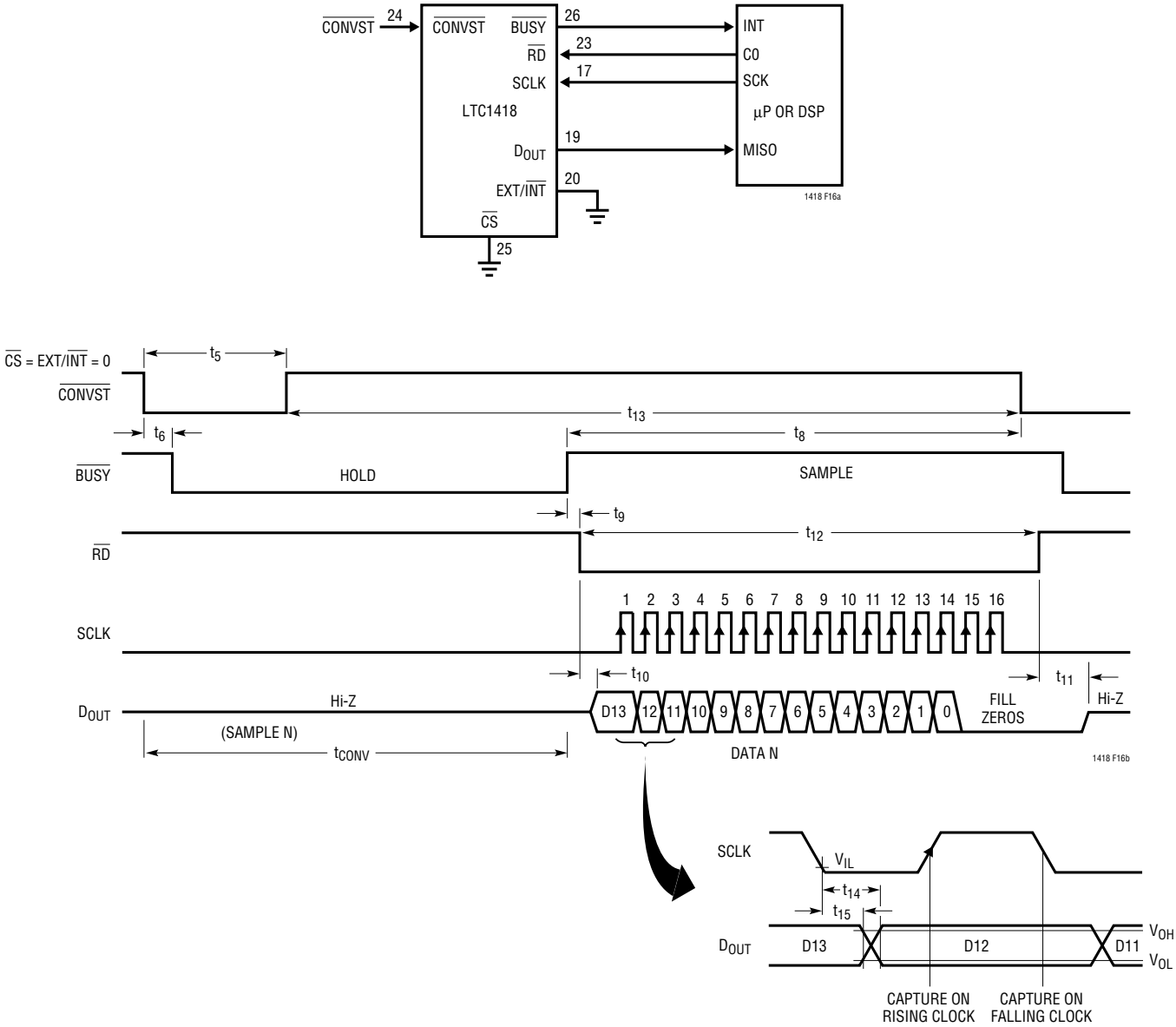


Figure 16. Internal Conversion Clock Selected. Data Transferred After Conversion Using an External SCLK. $\overline{BUSY}\uparrow$ Indicates End of Conversion

APPLICATIONS INFORMATION

Using External Conversion Clock and External Data Clock. In Figure 17, data is also output after each conversion is completed and before the next conversion is started. An external clock is used for the conversion clock and either another or the same external clock is used for the SCLK. This mode is identical to Figure 16 except that an external clock is used for the conversion. This mode allows the user to synchronize the A/D conversion to an external clock either to have precise control of the internal bit test timing or to provide a precise conversion time. As in Figure 16, this mode works when the SCLK frequency is very low (less than 30kHz). However, the external conversion clock must be between 30kHz and 4.5MHz to maintain accuracy. If more than 16 SCLKs are provided, more zeros will be filled in after the data word indefinitely. To select the external conversion clock tie $\overline{EXT}$/INT high. The external SCLK is applied to SCLK. $\overline{RD}$ can be used to gate the external SCLK such that data will clock only after $\overline{RD}$ goes low.

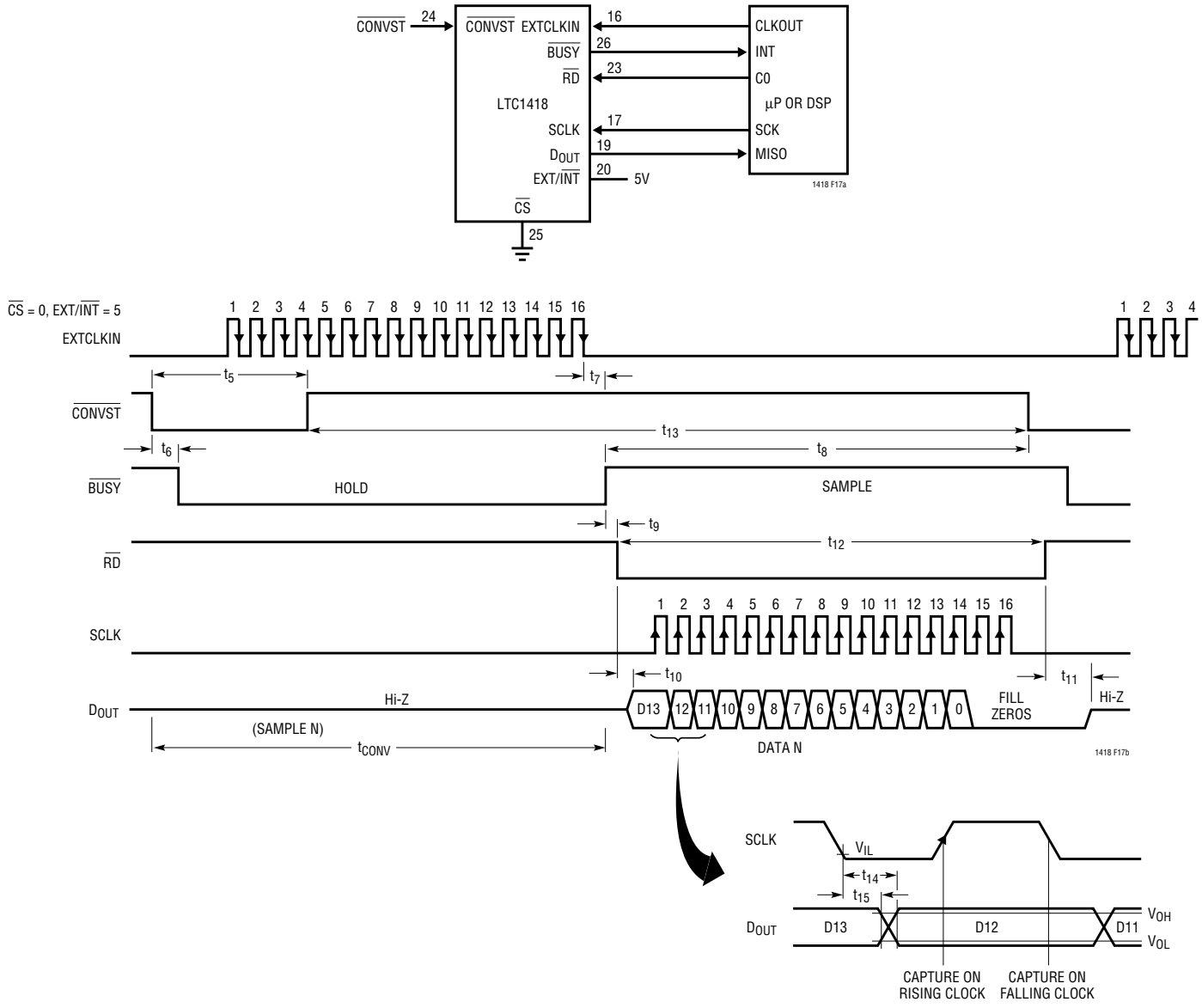
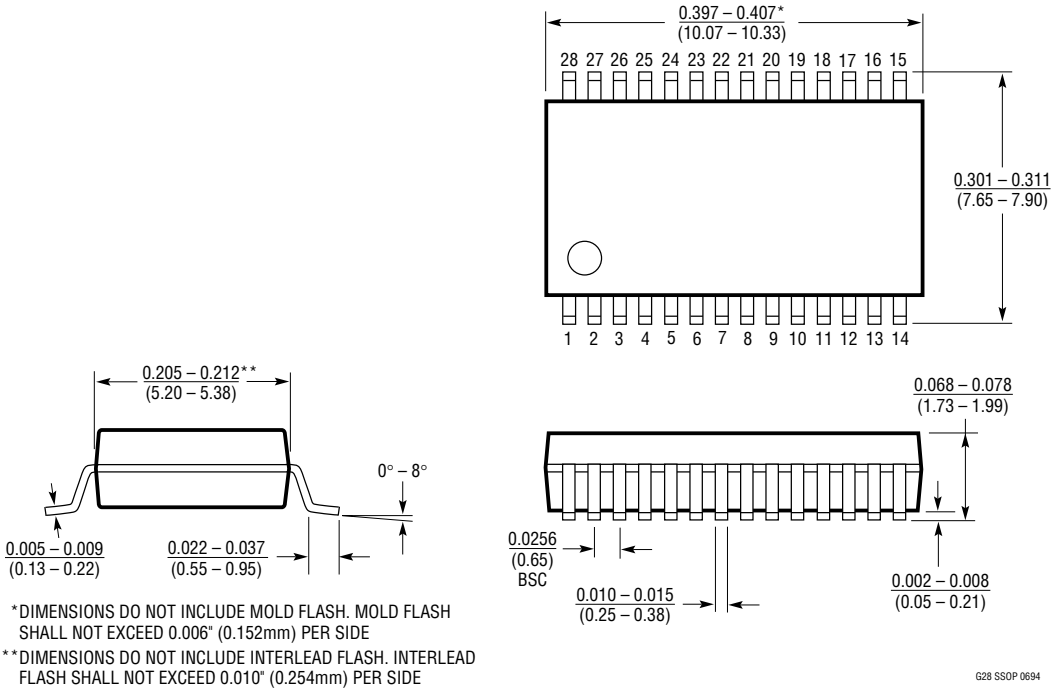


Figure 17. External Conversion Clock Selected. Data Transferred After Conversion Using an External SCLK. $\overline{BUSY}\uparrow$ Indicates End of Conversion

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1274/LTC1277	Low Power, 12-Bit, 100ksps ADCs	10mW Power Dissipation, Parallel/Byte Interface
LTC1415	Single 5V, 12-Bit, 1.25Msps ADC	55mW Power Dissipation, 72dB SINAD
LTC1416	Low Power, 14-Bit, 400ksps ADC	75mW Power Dissipation, 80.5dB SINAD
LTC1419	Low Power, 14-Bit, 800ksps ADC	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation
LTC1605	Single 5V, 16-Bit, 100ksps ADC	Low Power, ±10V Inputs, Parallel/Byte Interface
DACs		
LTC1595	16-Bit CMOS Multiplying DAC in SO-8	±1LSB Max INL/DNL, 1nV • sec Glitch, DAC8043 Upgrade
LTC1596	16-Bit CMOS Multiplying DAC	±1LSB Max INL/DNL, DAC8143/AD7543 Upgrade
Reference		
LT1019-2.5	Precision Bandgap Reference	0.05% Max, 5ppm/°C Max

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417• (408) 432-1900
FAX: (408) 434-0507•TELEX: 499-3977 • www.linear-tech.com
1418i LT/TP 0198 4K • PRINTED IN USA