# LT6220/LT6221/LT6222

## Single/Dual/Quad 60MHz, 20V/µs Low Power, Rail-to-Rail Input and Output Precision Op Amp

July 2003

## FEATURES

- **Gain-Bandwidth Product: 60MHz**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Quiescent Current: 1mA Max**
- **Input Offset Voltage: 350µV Max**
- **Input Bias Current: 150nA Max**
- Wide Supply Range: 2.2V to 12.6V
- Large Output Current: 50mA Typ
- Low Voltage Noise: 10nV√Hz Typ
- Slew Rate: 20V/µs Typ
- Common Mode Rejection: 102dB Typ
- Power Supply Rejection: 105dB Typ
- Open Loop Gain: 100V/mV Typ
- Operating Temperature Range – 40°C to 85°C
- Single in the 8-Pin SO and 5-Pin Low Profile (1mm) ThinSOT Packages
- Dual in the 8-Pin SO and (3mm x 3mm) DFN Packages
- Quad in the 16-Pin SSOP Package

## APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Amplifiers
- Fast Current Sensing Amplifiers

## DESCRIPTION

The LT®6220/LT6221/LT6222 are single/dual/quad, low power, high speed rail-to-rail input and output operational amplifiers with excellent DC performance. The LT6220/LT6221/LT6222 feature reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth.

Typically, the LT6220/LT6221/LT6222 have an input offset voltage of less than 100µV, an input bias current of less than 15nA and an open-loop gain of 100V/mV. The parts have an input range that includes both supply rails and an output that swings within 10mV of either supply rail to maximize the signal dynamic range in low supply applications.

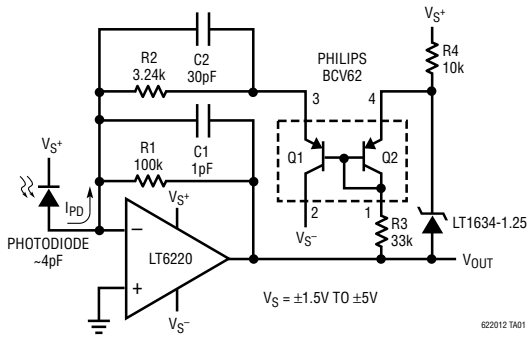
The LT6220/LT6221/LT6222 maintains performance for supplies from 2.2V to 12.6V and are specified at 3V, 5V and ±5V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

The LT6220 is housed in the 8-pin SO package with the standard op amp pinout as well as the 5-pin SOT-23 package. The LT6221 is available in 8-pin SO and DFN (3mm × 3mm low profile dual fine pitch leadless) packages with the standard op amp pinout. The LT6222 features the standard quad op amp configuration and is available in the 16-Pin SSOP package. The LT6220/LT6221/LT6222 can be used as plug-in replacements for many op amps to improve input/output range and performance.

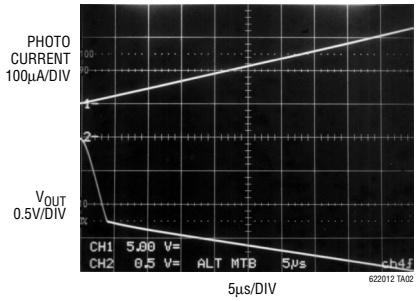


## TYPICAL APPLICATION

**Stepped-Gain Photodiode Amplifier**




**Stepped-Gain Photodiode Amplifier Response**



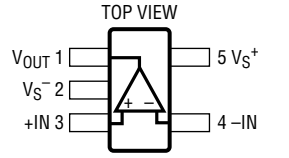

5µs/DIV

622012i

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V_S^-$ to $V_S^+$) ..... 12.6V
Input Voltage (Note 2) ..... $\pm V_S$
Input Current (Note 2) ..... ±10mA
Output Short Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ...–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Maximum Junction Temperature ..... 150°C
(DD Package) ..... 125°C
Storage Temperature .....–65°C to 150°C
(DD Package) .....–65°C to 125°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

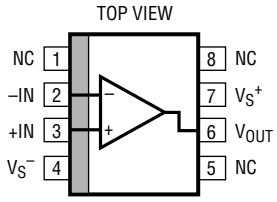
## PACKAGE/ORDER INFORMATION




S5 PACKAGE
5-LEAD PLASTIC SOT-23

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 250°C/W (NOTE 10)

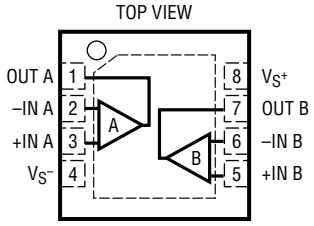
| ORDER PART NUMBER |
|---|
| LT6220CS5<br>LT6220IS5 |
| S5 PART* MARKING |
| LTAFP |




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 190°C/W

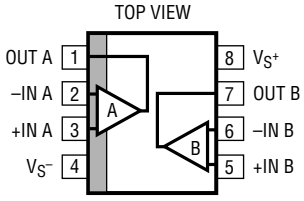
| ORDER PART NUMBER |
|---|
| LT6220CS8<br>LT6220IS8 |
| S8 PART MARKING |
| 6220<br>6220I |




DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 160°C/W (NOTE 10)
UNDERSIDE METAL INTERNALLY CONNECTED TO $V^-$
(PCB CONNECTION OPTIONAL)

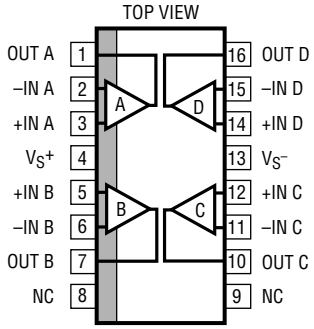
| ORDER PART NUMBER | DD PART* MARKING |
|---|---|
| LT6221CDD<br>LT6221IDD | LADZ |




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 190°C/W

| ORDER PART NUMBER | S8 PART MARKING |
|---|---|
| LT6221CS8<br>LT6221IS8 | 6221<br>6221I |




GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 135°C/W

| ORDER PART NUMBER | SSOP PART MARKING |
|---|---|
| LT6222CGN<br>LT6222IGN | 6222<br>6222I |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grades are identified by a label on the shipping container.

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, $V_S$ = 5V, 0V; $V_S$ = 3V, 0V; $V_{CM}$ = $V_{OUT}$ = half supply, unless otherwise noted**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = 0V<br>$V_{CM}$ = 0V (DD Package)<br>$V_{CM}$ = 0V (S5 Package)<br>$V_{CM}$ = $V_S$<br>$V_{CM}$ = $V_S$ (S5 Package) | | 70<br>150<br>200<br>0.5<br>0.5 | 350<br>700<br>850<br>2.5<br>3 | µV<br>µV<br>µV<br>mV<br>mV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V<br>$V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | | 30<br>15 | 195<br>120 | µV<br>µV |
| | Input Offset Voltage Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = 0V<br>$V_{CM}$ = 0V (DD Package) | | 100<br>150 | 600<br>1100 | µV<br>µV |
| $I_B$ | Input Bias Current | $V_{CM}$ = 1V<br>$V_{CM}$ = $V_S$ | | 15<br>250 | 150<br>600 | nA<br>nA |
| | Input Bias Current Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = 1V<br>$V_{CM}$ = $V_S$ | | 15<br>20 | 175<br>250 | nA<br>nA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 1V<br>$V_{CM}$ = $V_S$ | | 15<br>15 | 100<br>100 | nA<br>nA |
| | Input Noise Voltage | 0.1Hz to 10Hz | | 0.5 | | $\mu V_{P-P}$ |
| $e_n$ | Input Noise Voltage Density | f = 10kHz | | 10 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Noise Current Density | f = 10kHz | | 0.8 | | $pA/\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S$ = 5V, $V_O$ = 0.5V to 4.5V, $R_L$ = 1k at $V_S$/2<br>$V_S$ = 5V, $V_O$ = 1V to 4V, $R_L$ = 100Ω at $V_S$/2<br>$V_S$ = 3V, $V_O$ = 0.5V to 2.5V, $R_L$ = 1k at $V_S$/2 | 35<br>3.5<br>30 | 100<br>10<br>90 | | V/mV<br>V/mV<br>V/mV |
| CMRR | Common Mode Rejection Ratio | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V<br>$V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | 85<br>82 | 102<br>102 | | dB<br>dB |
| | CMRR Match (Channel-to-Channel) (Note 9) | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V<br>$V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | 79<br>76 | 100<br>100 | | dB<br>dB |
| | Input Common Mode Range | | 0 | | $V_S$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5V to 10V, $V_{CM}$ = 0V | 84 | 105 | | dB |
| | PSRR Match (Channel-to-Channel) (Note 9) | | 79 | 105 | | dB |
| | Minimum Supply Voltage (Note 6) | | | 2.2 | 2.5 | V |
| $V_{OL}$ | Output Voltage Swing LOW (Note 7) | No Load<br>$I_{SINK}$ = 5mA<br>$I_{SINK}$ = 20mA | | 5<br>100<br>325 | 40<br>200<br>650 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing HIGH (Note 7) | No Load<br>$I_{SOURCE}$ = 5mA<br>$I_{SOURCE}$ = 20mA | | 5<br>130<br>475 | 40<br>250<br>900 | mV<br>mV<br>mV |
| $I_{SC}$ | Short-Circuit Current | $V_S$ = 5V<br>$V_S$ = 3V | 20<br>20 | 45<br>35 | | mA<br>mA |
| $I_S$ | Supply Current Per Amplifier | | | 0.9 | 1 | mA |
| GBW | Gain-Bandwidth Product | $V_S$ = 5V, Frequency = 1MHz | 35 | 60 | | MHz |
| SR | Slew Rate | $V_S$ = 5V, $A_V$ = –1, $R_L$ = 1k, $V_O$ = 4V | 10 | 20 | | V/µs |
| FPBW | Full Power Bandwidth | $V_S$ = 5V, $A_V$ = 1, $V_O$ = $4V_{p-p}$ | | 1.6 | | MHz |
| HD | Harmonic Distortion | $V_S$ = 5V, $A_V$ = 1, $R_L$ = 1k, $V_O$ = $2V_{P-P}$, $f_C$ = 500kHz | | 77.5 | | dBc |
| $t_S$ | Settling Time | 0.01%, $V_S$ = 5V, $V_{STEP}$ = 2V, $A_V$ = 1, $R_L$ = 1k | | 300 | | ns |
| ΔG | Differential Gain (NTSC) | $V_S$ = 5V, $A_V$ = 2, $R_L$ = 1k | | 0.3 | | % |
| Δθ | Differential Phase (NTSC) | $V_S$ = 5V, $A_V$ = 2, $R_L$ = 1k | | 0.3 | | Deg |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the 0°C ≤ $T_A$ ≤ 70°C temperature range. $V_S$ = 5V, 0V; $V_S$ = 3V, 0V; $V_{CM}$ = $V_{OUT}$ = half supply, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = 0V | ● | | 90 | 500 | µV |
| | | $V_{CM}$ = 0V (DD Package) | ● | | 180 | 850 | µV |
| | | $V_{CM}$ = 0V (S5 Package) | ● | | 230 | 1250 | µV |
| | | $V_{CM}$ = $V_S$ | ● | | 0.5 | 3 | mV |
| | | $V_{CM}$ = $V_S$ (S5 Package) | ● | | 0.5 | 3.5 | mV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V | ● | | 30 | 280 | µV |
| | | $V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | ● | | 15 | 190 | µV |
| | Input Offset Voltage Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = 0V | ● | | 110 | 850 | µV |
| | | $V_{CM}$ = 0V (DD Package) | ● | | 180 | 1400 | µV |
| $V_{OS}$ TC | Input Offset Voltage Drift (Note 8) | | ● | | 1.5 | 5 | µV/°C |
| | | (S5 Package) | ● | | 3.5 | 10 | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM}$ = 1V | ● | | 20 | 175 | nA |
| | | $V_{CM}$ = $V_S$ – 0.2V | ● | | 275 | 800 | nA |
| | Input Bias Current Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = 1V | ● | | 15 | 200 | nA |
| | | $V_{CM}$ = $V_S$ – 0.2V | ● | | 20 | 300 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 1V | ● | | 15 | 125 | nA |
| | | $V_{CM}$ = $V_S$ – 0.2V | ● | | 15 | 125 | nA |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S$ = 5V, $V_O$ = 0.5V to 4.5V, $R_L$ = 1k at $V_S$/2 | ● | 30 | 90 | | V/mV |
| | | $V_S$ = 5V, $V_O$ = 1V to 4V, $R_L$ = 100Ω at $V_S$/2 | ● | 3 | 9 | | V/mV |
| | | $V_S$ = 3V, $V_O$ = 0.5V to 2.5V, $R_L$ = 1k at $V_S$/2 | ● | 25 | 80 | | V/mV |
| CMRR | Common Mode Rejection Ratio | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V | ● | 82 | 100 | | dB |
| | | $V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | ● | 78 | 100 | | dB |
| | CMRR Match (Channel-to-Channel) (Note 9) | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V | ● | 77 | 100 | | dB |
| | | $V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | ● | 73 | 100 | | dB |
| | Input Common Mode Range | | ● | 0 | | $V_S$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5V to 10V, $V_{CM}$ = 0V | ● | 81 | 104 | | dB |
| | PSRR Match (Channel-to-Channel) (Note 9) | | ● | 76 | 104 | | dB |
| | Minimum Supply Voltage (Note 6) | | ● | | 2.2 | 2.5 | V |
| $V_{OL}$ | Output Voltage Swing LOW (Note 7) | No Load | ● | | 8 | 50 | mV |
| | | $I_{SINK}$ = 5mA | ● | | 110 | 220 | mV |
| | | $I_{SINK}$ = 20mA | ● | | 375 | 750 | mV |
| $V_{OH}$ | Output Voltage Swing HIGH (Note 7) | No Load | ● | | 8 | 50 | mV |
| | | $I_{SOURCE}$ = 5mA | ● | | 150 | 300 | mV |
| | | $I_{SOURCE}$ = 20mA | ● | | 600 | 1100 | mV |
| $I_{SC}$ | Short-Circuit Current | $V_S$ = 5V | ● | 20 | 40 | | mA |
| | | $V_S$ = 3V | ● | 20 | 30 | | mA |
| $I_S$ | Supply Current Per Amplifier | | ● | | 1 | 1.4 | mA |
| GBW | Gain-Bandwidth Product | $V_S$ = 5V, Frequency = 1MHz | ● | 30 | 60 | | MHz |
| SR | Slew Rate | $V_S$ = 5V, $A_V$ = –1, $R_L$ = 1k, $V_O$ = 4$V_{P-P}$ | ● | 9 | 18 | | V/µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the –40°C ≤ $T_A$ ≤ 85°C temperature range. $V_S$ = 5V, 0V; $V_S$ = 3V, 0V; $V_{CM}$ = $V_{OUT}$ = half supply unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = 0V | ● | | 125 | 700 | µV |
| | | $V_{CM}$ = 0V (DD Package) | ● | | 300 | 1300 | µV |
| | | $V_{CM}$ = 0V (S5 Package) | ● | | 350 | 2000 | µV |
| | | $V_{CM}$ = $V_S$ | ● | | 0.75 | 3.5 | mV |
| | | $V_{CM}$ = $V_S$ (S5 Package) | ● | | 1 | 4.5 | mV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V | ● | | 30 | 300 | µV |
| | | $V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | ● | | 30 | 210 | µV |
| | Input Offset Voltage Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = 0V | ● | | 175 | 1200 | µV |
| | | $V_{CM}$ = 0V (DD Package) | ● | | 300 | 2200 | µV |
| $V_{OS}$ TC | Input Offset Voltage Drift (Note 8) | | ● | | 1.5 | 7.5 | µV/°C |
| | | (S5 Package) | ● | | 3.5 | 15 | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM}$ = 1V | ● | | 25 | 200 | nA |
| | | $V_{CM}$ = $V_S$ – 0.2V | ● | | 300 | 900 | nA |
| | Input Bias Current Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = 1V | ● | | 15 | 250 | nA |
| | | $V_{CM}$ = $V_S$ – 0.2V | ● | | 20 | 350 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 1V | ● | | 20 | 150 | nA |
| | | $V_{CM}$ = $V_S$ – 0.2V | ● | | 20 | 150 | nA |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S$ = 5V, $V_O$ = 0.5V to 4.5V, $R_L$ = 1k at $V_S$/2 | ● | 25 | 70 | | V/mV |
| | | $V_S$ = 5V, $V_O$ = 1.5V to 3.5V, $R_L$ = 100Ω at $V_S$/2 | ● | 2.5 | 8 | | V/mV |
| | | $V_S$ = 3V, $V_O$ = 0.5V to 2.5V, $R_L$= 1k at $V_S$/2 | ● | 20 | 60 | | V/mV |
| CMRR | Common Mode Rejection Ratio | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V | ● | 81 | 100 | | dB |
| | | $V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | ● | 77 | 100 | | dB |
| | CMRR Match (Channel-to-Channel) (Note 9) | $V_S$ = 5V, $V_{CM}$ = 0V to 3.5V | ● | 76 | 100 | | dB |
| | | $V_S$ = 3V, $V_{CM}$ = 0V to 1.5V | ● | 72 | 100 | | dB |
| | Input Common Mode Range | | ● | 0 | | $V_S$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5V to 10V, $V_{CM}$ = 0V | ● | 79 | 104 | | dB |
| | PSRR Match (Channel-to-Channel) (Note 9) | | ● | 74 | 104 | | dB |
| | Minimum Supply Voltage (Note 6) | $V_{CM}$ = $V_O$ = 0.5V | ● | | 2.2 | 2.5 | V |
| $V_{OL}$ | Output Voltage Swing LOW (Note 7) | No Load | ● | | 10 | 60 | mV |
| | | $I_{SINK}$ = 5mA | ● | | 120 | 240 | mV |
| | | $I_{SINK}$ = 10mA | ● | | 220 | 450 | mV |
| $V_{OH}$ | Output Voltage Swing HIGH (Note 7) | No Load | ● | | 10 | 60 | mV |
| | | $I_{SOURCE}$ = 5mA | ● | | 160 | 325 | mV |
| | | $I_{SOURCE}$ = 10mA | ● | | 325 | 650 | mV |
| $I_{SC}$ | Short-Circuit Current | $V_S$ = 5V | ● | 12.5 | 30 | | mA |
| | | $V_S$ = 3V | ● | 12.5 | 25 | | mA |
| $I_S$ | Supply Current Per Amplifier | | ● | | 1.1 | 1.5 | mA |
| GBW | Gain-Bandwidth Product | $V_S$ = 5V, Frequency = 1MHz | ● | 25 | 50 | | MHz |
| SR | Slew Rate | $V_S$ = 5V, $A_V$ = –1, $R_L$ = 1k, $V_O$ = 4V | ● | 8 | 15 | | V/µs |

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, $V_S$ = ±5V, $V_{CM}$ = 0V, $V_{OUT}$ = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = –5V<br>$V_{CM}$ = –5V (DD Package)<br>$V_{CM}$ = –5V (S5 Package)<br>$V_{CM}$ = 5V<br>$V_{CM}$ = 5V (S5 Package) | | 80<br>150<br>200<br>0.7<br>0.7 | 500<br>750<br>900<br>2.5<br>3 | µV<br>µV<br>µV<br>mV<br>mV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift | $V_{CM}$ = –5V to 3.5V | | 70 | 675 | µV |
| | Input Offset Voltage Match (Channel-to-Channel) | $V_{CM}$ = –5V<br>$V_{CM}$ = –5V (DD Package) | | 100<br>150 | 850<br>1300 | µV<br>µV |
| $I_B$ | Input Bias Current | $V_{CM}$ = –4V<br>$V_{CM}$ = 5V | | 20<br>250 | 150<br>700 | nA<br>nA |
| | Input Bias Current Match (Channel-to-Channel) | $V_{CM}$ = –4V<br>$V_{CM}$ = 5V | | 15<br>20 | 175<br>250 | nA<br>nA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = –4V<br>$V_{CM}$ = 5V | | 15<br>15 | 100<br>100 | nA<br>nA |
| | Input Noise Voltage | 0.1Hz to 10Hz | | 0.5 | | $\mu V_{P-P}$ |
| $e_n$ | Input Noise Voltage Density | f = 10kHz | | 10 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Noise Current Density | f = 10kHz | | 0.8 | | $pA/\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | f = 100kHz | | 2 | | pF |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = –4V to 4V, $R_L$ = 1k<br>$V_O$ = –2V to 2V, $R_L$ = 100Ω | 35<br>3.5 | 95<br>10 | | V/mV<br>V/mV |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = –5V to 3.5V | 82 | 102 | | dB |
| | CMRR Match (Channel-to-Channel) | | 77 | 100 | | dB |
| | Input Common Mode Range | | $V_S^-$ | | $V_S^+$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S^+$ = 2.5V to 10V, $V_S^-$ = 0V, $V_{CM}$ = 0V | 84 | 105 | | dB |
| | PSRR Match (Channel-to-Channel) | | 79 | 105 | | dB |
| $V_{OL}$ | Output Voltage Swing LOW (Note 7) | No Load<br>$I_{SINK}$ = 5mA<br>$I_{SINK}$ = 20mA | | 5<br>100<br>325 | 40<br>200<br>650 | mV<br>mV<br>mV |
| $V_{OH}$ | Output Voltage Swing HIGH (Note 7) | No Load<br>$I_{SOURCE}$ = 5mA<br>$I_{SOURCE}$ = 20mA | | 5<br>130<br>475 | 40<br>250<br>900 | mV<br>mV<br>mV |
| $I_{SC}$ | Short-Circuit Current | | 25 | 50 | | mA |
| $I_S$ | Supply Current Per Amplifier | | | 1 | 1.5 | mA |
| GBW | Gain-Bandwidth Product | Frequency = 1MHz | | 60 | | MHz |
| SR | Slew Rate | $A_V$ = –1, $R_L$ = 1k, $V_O$ = ±4V,<br>Measure at $V_O$ = ±2V | | 20 | | V/µs |
| FPBW | Full Power Bandwidth | $V_O = 8V_{P-P}$ | | 0.8 | | MHz |
| HD | Harmonic Distortion | $A_V$ = 1, $R_L$= 1k, $V_O = 2V_{p-p}$, $f_c$ = 500kHz | | 77.5 | | dBc |
| $t_S$ | Settling Time | 0.01%, $V_{STEP}$ = 5V, $A_V$ = 1, $R_L$ = 1k | | 375 | | ns |
| ΔG | Differential Gain (NTSC) | $A_V$ = 2, $R_L$ = 1k | | 0.15 | | % |
| Δθ | Differential Phase (NTSC) | $A_V$ = 2, $R_L$ = 1k | | 0.6 | | Deg |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the 0°C ≤ $T_A$ ≤ 70°C temperature range. $V_S$ = ±5V, $V_{CM}$ = 0V, $V_{OUT}$ = 0V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = –5V | ● | | 100 | 650 | µV |
| | | $V_{CM}$ = –5V (DD Package) | ● | | 180 | 900 | µV |
| | | $V_{CM}$ = –5V (S5 Package) | ● | | 230 | 1300 | µV |
| | | $V_{CM}$ = 5V | ● | | 0.75 | 3 | mV |
| | | $V_{CM}$ = 5V (S5 Package) | ● | | 0.75 | 3.5 | mV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift | $V_{CM}$ = –5V to 3.5V | ● | | 90 | 850 | µV |
| | Input Offset Voltage Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = –5V | ● | | 90 | 1100 | µV |
| | | $V_{CM}$ = –5V (DD Package) | ● | | 180 | 1500 | µV |
| $V_{OS}$ TC | Input Offset Voltage Drift (Note 8) | | ● | | 1.5 | 5 | µV/°C |
| | | (S5 Package) | ● | | 3.5 | 10 | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM}$ = –4V | ● | | 20 | 175 | nA |
| | | $V_{CM}$ = 4.8V | ● | | 275 | 800 | nA |
| | Input Bias Current Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = –4V | ● | | 15 | 200 | nA |
| | | $V_{CM}$ = 4.8V | ● | | 20 | 300 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = –4V | ● | | 15 | 125 | nA |
| | | $V_{CM}$ = 4.8V | ● | | 15 | 125 | nA |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = –4V to 4V, $R_L$ = 1k | ● | 30 | 90 | | V/mV |
| | | $V_O$ = –2V to 2V, $R_L$ =100Ω | ● | 3 | 9 | | V/mV |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = –5V to 3.5V | ● | 80 | 100 | | dB |
| | CMRR Match (Channel-to-Channel) (Note 9) | | ● | 75 | 100 | | dB |
| | Input Common Mode Range | | ● | $V_S^-$ | | $V_S^+$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S^+$ = 2.5V to 10V, $V_S^-$ = 0V, $V_{CM}$ = 0V | ● | 81 | 104 | | dB |
| | PSRR Match (Channel-to-Channel) (Note 9) | | ● | 76 | 104 | | dB |
| $V_{OL}$ | Output Voltage Swing LOW (Note 7) | No Load | ● | | 8 | 50 | mV |
| | | $I_{SINK}$ = 5mA | ● | | 110 | 220 | mV |
| | | $I_{SINK}$ = 20mA | ● | | 375 | 750 | mV |
| $V_{OH}$ | Output Voltage Swing HIGH (Note 7) | No Load | ● | | 8 | 50 | mV |
| | | $I_{SOURCE}$ = 5mA | ● | | 150 | 300 | mV |
| | | $I_{SOURCE}$ = 20mA | ● | | 600 | 1100 | mV |
| $I_{SC}$ | Short-Circuit Current | | ● | 20 | 40 | | mA |
| $I_S$ | Supply Current Per Amplifier | | ● | | 1.2 | 2 | mA |
| GBW | Gain-Bandwidth Product | Frequency = 1MHz | | | 60 | | MHz |
| SR | Slew Rate | $A_V$ = –1, $R_L$ = 1k, $V_O$ = ±4V, Measure at $V_O$ = ±2V | | | 18 | | V/µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the –40°C ≤ $T_A$ ≤ 85°C temperature range. $V_S$ = ±5V, $V_{CM}$ = 0V, $V_{OUT}$ = 0V, unless otherwise noted. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = –5V | ● | | 150 | 800 | µV |
| | | $V_{CM}$ = –5V (DD Package) | ● | | 300 | 1300 | µV |
| | | $V_{CM}$ = –5V (S5 Package) | ● | | 350 | 2000 | µV |
| | | $V_{CM}$ = 5V | ● | | 0.75 | 3.5 | mV |
| | | $V_{CM}$ = 5V (S5 Package) | ● | | 1 | 4.5 | mV |
| $\Delta V_{OS}$ | Input Offset Voltage Shift | $V_{CM}$ = – 5V to 3.5V | ● | | 90 | 950 | µV |
| | Input Offset Voltage Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = –5V | ● | | 175 | 1350 | µV |
| | | $V_{CM}$ = –5V (DD Package) | ● | | 300 | 2200 | µV |
| $V_{OS}$ TC | Input Offset Voltage Drift (Note 8) | | ● | | 1.5 | 7.5 | µV/°C |
| | | (S5 Package) | ● | | 3.5 | 15 | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM}$ = –4V | ● | | 25 | 200 | nA |
| | | $V_{CM}$ = 4.8V | ● | | 300 | 900 | nA |
| | Input Bias Current Match (Channel-to-Channel) (Note 9) | $V_{CM}$ = –4V | ● | | 15 | 250 | nA |
| | | $V_{CM}$ = 4.8V | ● | | 20 | 350 | nA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = –4V | ● | | 20 | 150 | nA |
| | | $V_{CM}$ = 4.8V | ● | | 20 | 150 | nA |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = –4V to 4V, $R_L$ = 1k | ● | 25 | 70 | | V/mV |
| | | $V_O$ = –1V to 1V, $R_L$ = 100Ω | ● | 2.5 | 8 | | V/mV |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = –5V to 3.5V | ● | 79 | 100 | | dB |
| | CMRR Match (Channel-to-Channel) (Note 9) | | ● | 74 | 100 | | dB |
| | Input Common Mode Range | | ● | –5 | | 5 | V |
| PSRR | Power Supply Rejection Ratio | $V_S^+$ = 2.5V to 10V, $V_S^-$ = 0V, $V_{CM}$ = 0V | ● | 79 | 104 | | dB |
| | PSRR Match (Channel-to-Channel) (Note 9) | | ● | 74 | 104 | | dB |
| $V_{OL}$ | Output Voltage Swing LOW (Note 7) | No Load | ● | | 10 | 60 | mV |
| | | $I_{SINK}$ = 5mA | ● | | 120 | 240 | mV |
| | | $I_{SINK}$ = 10mA | ● | | 220 | 450 | mV |
| $V_{OH}$ | Output Voltage Swing HIGH (Note 7) | No Load | ● | | 10 | 60 | mV |
| | | $I_{SOURCE}$ = 5mA | ● | | 160 | 325 | mV |
| | | $I_{SOURCE}$ = 10mA | ● | | 325 | 650 | mV |
| $I_{SC}$ | Short-Circuit Current | | ● | 12.5 | 30 | | mA |
| $I_S$ | Supply Current | | ● | | 1.4 | 2.25 | mA |
| GBW | Gain-Bandwidth Product | Frequency = 1MHz | | | 50 | | MHz |
| SR | Slew Rate | $A_V$ = –1, $R_L$ = 1k, $V_O$ = ±4V, Measure at $V_O$ = ±2V | | | 15 | | V/µs |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 4:** The LT6220C/LT6221C/LT6222C and LT6220I/LT6221I/LT6222I are guaranteed functional over the temperature range of –40°C and 85°C.

**Note 5:** The LT6220C/LT6221C/LT6222C are guaranteed to meet specified performance from 0°C to 70°C. The LT6220C/LT6221C/LT6222C are designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT6220I/LT6221I/LT6222I are guaranteed to meet specified performance from –40°C to 85°C.

**Note 6:** Minimum supply voltage is guaranteed by power supply rejection ratio test.

**Note 7:** Output voltage swings are measured between the output and power supply rails.

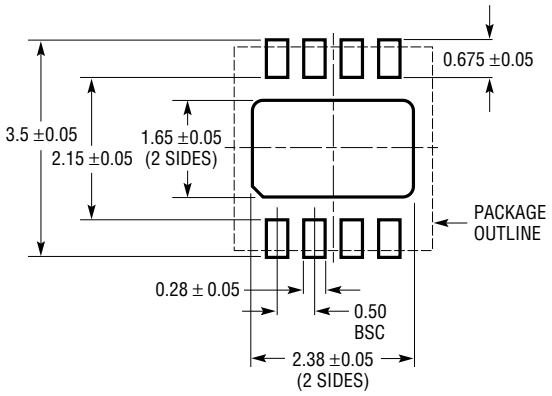
**Note 8:** This parameter is not 100% tested.

**Note 9:** Matching parameters are the difference between amplifiers A and D and between B and C on the LT6222; between the two amplifiers on the LT6221.

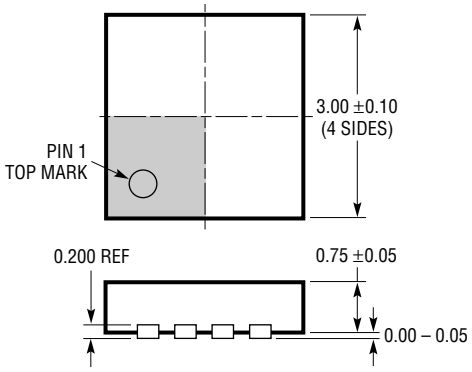
**Note 10:** Thermal resistance ($\theta_{JA}$) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be substantially reduced by connecting Pin 2 of the LT6220CS5/LT6220IS5 or the underside metal of DD packages to a larger metal area ($V_S^-$ trace).

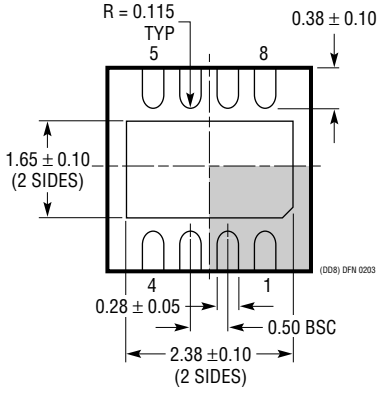
# PACKAGE DESCRIPTION

**DD Package**
**8-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1698)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



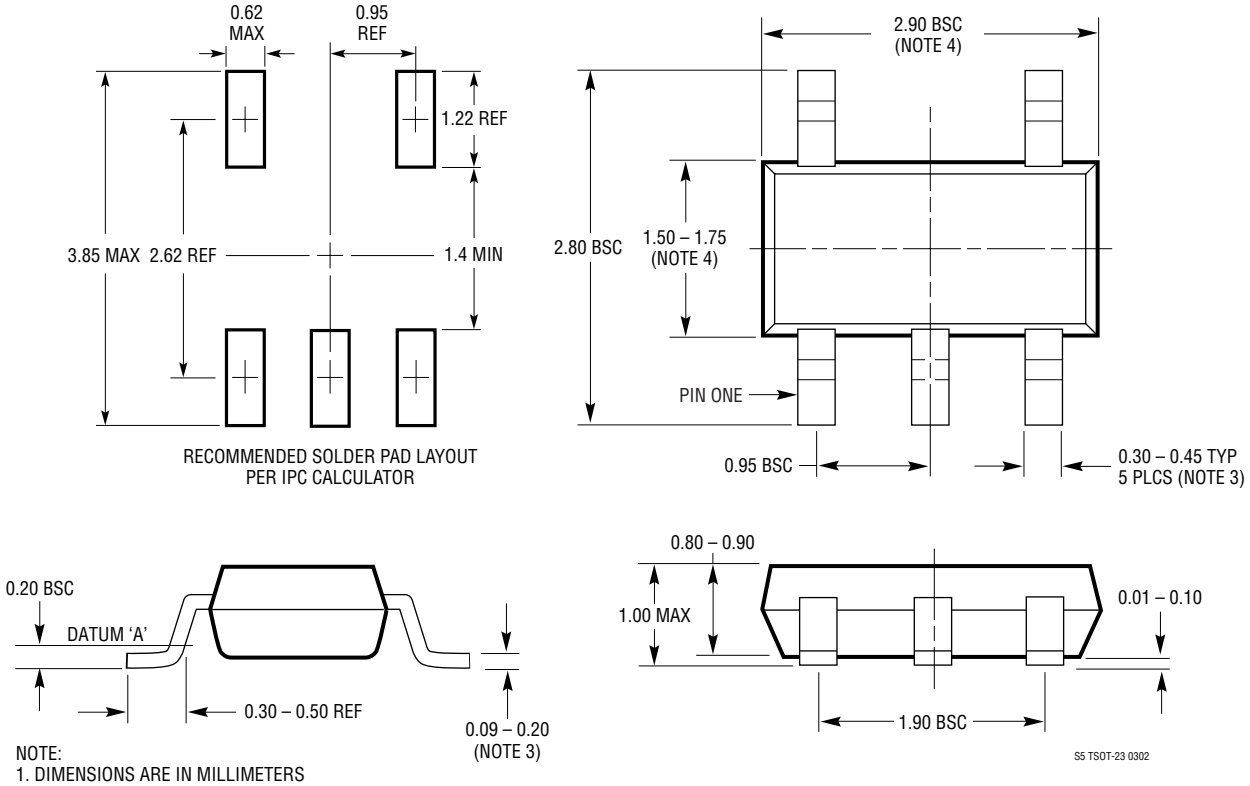




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

# PACKAGE DESCRIPTION

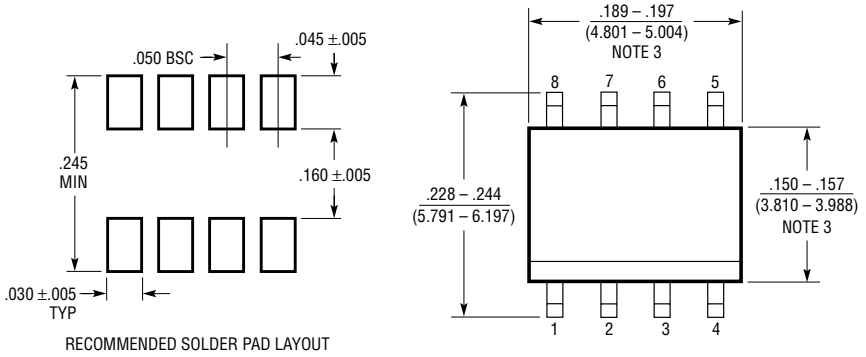
**S5 Package**
**5-Lead Plastic SOT-23**
(Reference LTC DWG # 05-08-1633)




NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

# PACKAGE DESCRIPTION

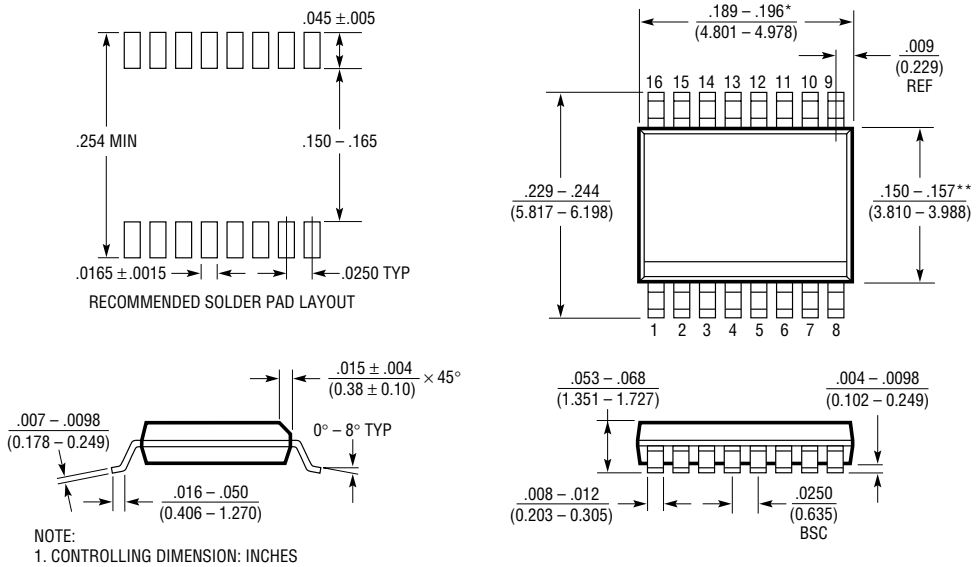
**S8 Package**
**8-Lead Plastic Small Outline (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1610)




NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

**GN Package**
**16-Lead Plastic SSOP (Narrow .150 Inch)**
(Reference LTC DWG # 05-08-1641)




NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

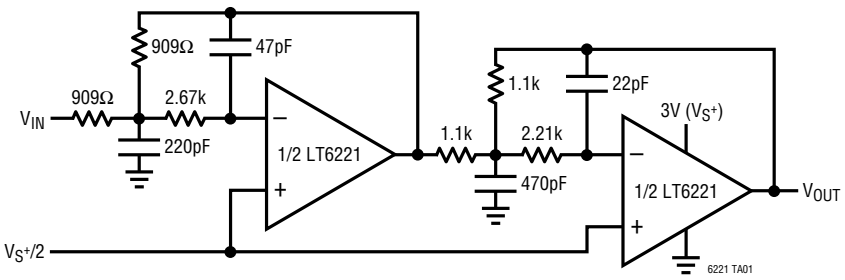
## TYPICAL APPLICATION

The circuit on the front page of this data sheet is a stepped gain transimpedance photodiode amplifier. At low signal levels, the circuit has a high 100kΩ gain, but at high signal levels the circuit automatically and smoothly changes to a low 3.2kΩ gain. The benefit of a stepped gain approach is that it maximizes dynamic range, which is very useful on limited supplies. Put another way, in order to get 100kΩ sensitivity and still handle a 1mA signal level without resorting to gain reduction, the circuit would need a 100V negative voltage supply.

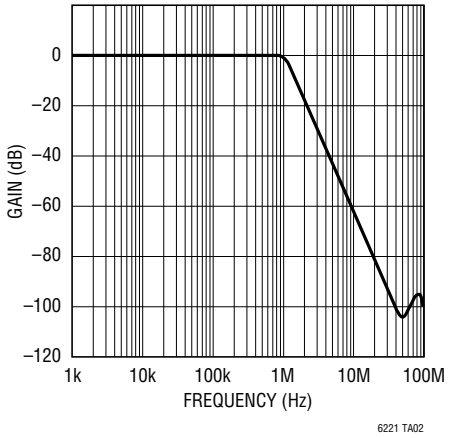
The operation of the circuit is quite simple. At low photodiode currents (below 10μA) the output and inverting input of the op amp will be no more than 1V below ground. The LT1634 in parallel with R3 and Q2 keep a constant current though Q2 of about 20μA. R4 maintains quiescent current through the LT1634 and pulls Q2's emitter above ground, so Q1 is reverse biased and no current flows through R2. So for small signals, the only feedback path is R1 (and C1) and the circuit is a simple transimpedance amplifier with 100kΩ gain.

As the signal level increases though, the output of the op amp goes more negative. At 12.5μA of photodiode current, the 100kΩ gain dictates that the LT6220 output will be about 1.25V below ground. However, at that point the emitter of Q2 will be at ground, and the base of Q1 will be 1V below ground. Thus, Q1 turns on and photodiode current starts to flow through R2. The transimpedance gain is therefore now reduced to R1||R2, or about 3.1kΩ. The circuit response is shown in the oscillogram to the right of the schematic. Note the smooth transition between the two operating gains, as well as the linearity.

**3V, 1MHz, 4th Order Butterworth Filter**




**1MHz Filter Frequency Response**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT1498/LT1499 | Dual/Quad 10MHz, 6V/μs Rail-to-Rail Input/ Output $C_{LOAD}$ Op Amps | High DC Accuracy, 475μV $V_{OS(MAX)}$ Max Supply Current 2.2mA/Amp |
| LT1800/LT1801/LT1802 | Single/Dual/Quad 80MHz, 25V/μs, Low Power Rail-to-Rail Input/Output Precision Op Amps | 350μV $V_{OS(MAX)}$, 250nA $I_{BIAS(MAX)}$, Max Supply Current 2mA/Amp |
| LT1803/LT1804/LT1805 | Single/Dual/Quad 85MHz, 100V/μs Rail-to-Rail Input/Output Op Amps | 2mV $V_{OS(MAX)}$, Max Supply Current 3mA/Amp |
| LT1806/LT1807 | Single/Dual 325MHz, 140V/μs Rail-to-Rail Input/ Output Op Amps | High DC Accuracy, 550μV $V_{OS(MAX)}$ Max Low Noise 3.5nV/$\sqrt{Hz}$ Low Distortion –80dBc at 5MHz, Power Down (LT1806) |
| LT1809/LT1810 | Single/Dual 180MHz, Rail-to-Rail Input/Output Op Amps | 350V/μs Slew Rate, Low Distortion –90dBc at 5MHz, Power Down (LT1809) |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