SPEC No. EL101010

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SPECIFICATIONS

Product Type DIGITAL SIGNAL PROCESSOR FOR COLOR CCD CAMERA

Model No. LR38269

※This specification contains 24 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: K. Misawa
K. MISAWA
Dept. General Manager

REVIEWED BY: G. Yoshikawa

PREPARED BY: T. Yata

Engineering Dept. 3
Logic IC Engineering Center
First Integrated Circuits Group
Integrated Circuits Group
SHARP CORPORATION

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●When using the products covered herein, please observe the conditions written herein and
the precautions outlined in the following paragraphs. In no event shall the company be liable
for any damages resulting from failure company be liable for any damages resulting
from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following applications areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales
representative of the company.

CONTENTS

1. GENERAL

This is the digital signal processor for color CCD camera system of 270K and 320K pixels CCD with the complementary color filter. The camera system consists of CDS·AGC·AD IC (IR3Y38M), DSP IC (LR38269), and Vdriver IC (LR36685).

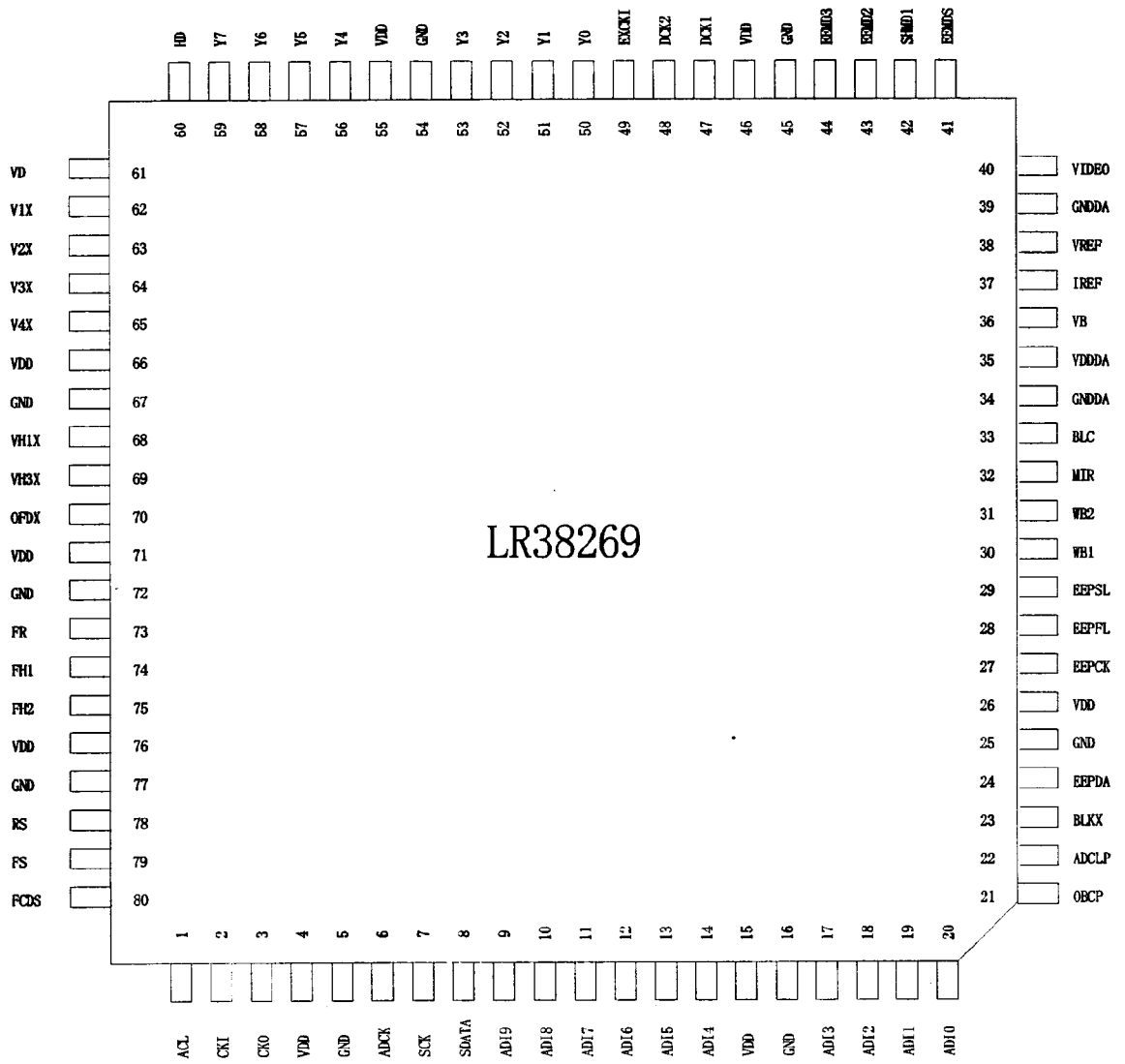
1-1. FEATURES

- The process (structure) is CMOS.
- A P-type silicon circuit board is used.
- The package type is 80-pin QFP.
- The package material is plastic.
- Not designed or rated as radiation hardened.

1-2. FUNCTIONS

- Single +3.3V power supply
- Available for 270K and 320K CCD with Mg, Cy, Ye and Gr color filter
- Available for NTSC and PAL
- External performance control
- Chioce out of 4 kinds of GAMMA and KNEE response
- 8 ~ 10 bits digital input
- Analog NTSC/PAL composite output by built-in 9 bits DA converter
- Either Y & U / V (16 bits) ~~or U / Y / V / Y (8 bits)~~ output in digital
- External control interface Input / Output
- Auto Exposure and Auto White Balance.

2. PIN ASSIGNMENT

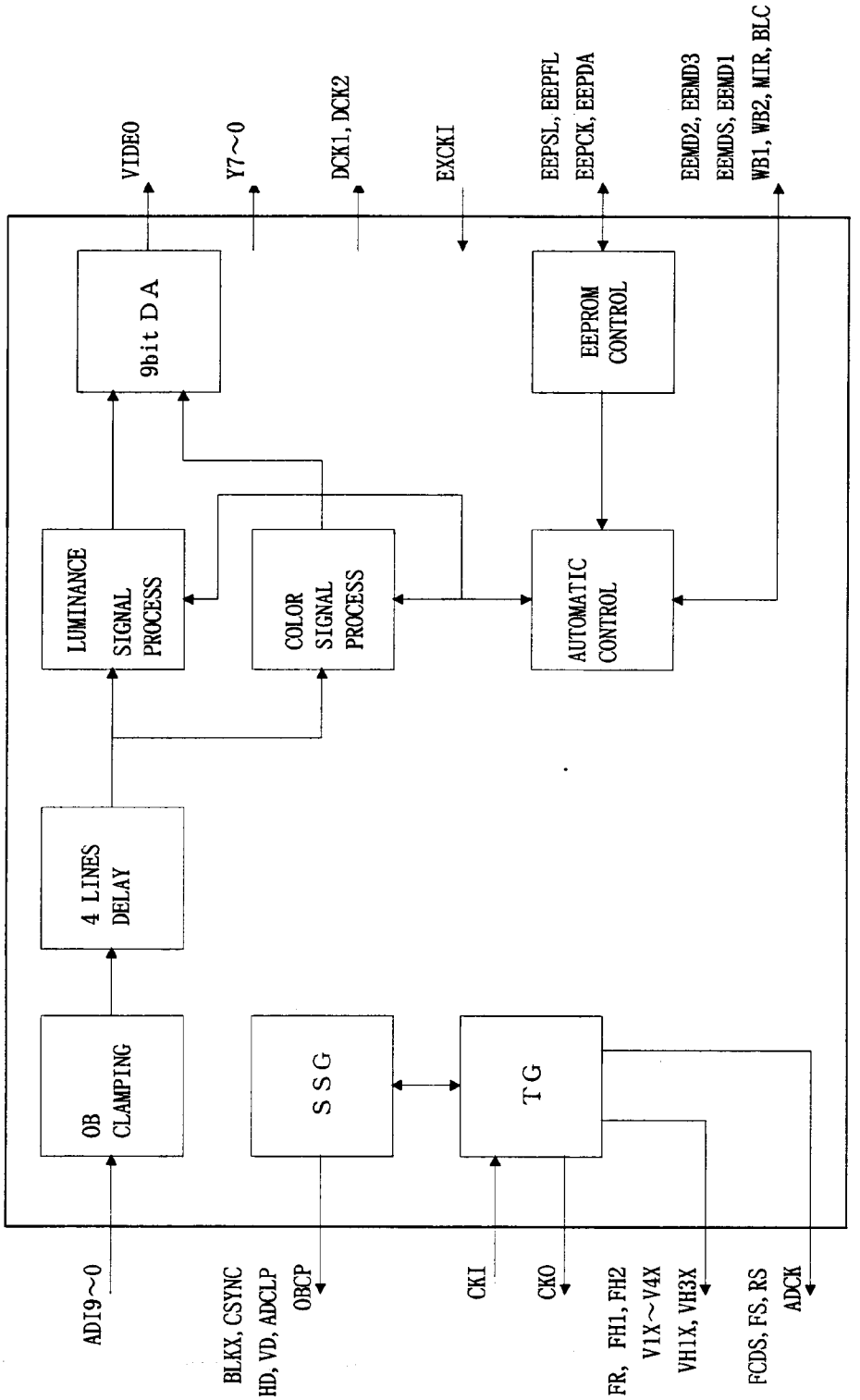


2-2. PIN TABLE

NO	I/O	SIGNAL	NO	I/O	SIGNAL
1	IC	ACL	41	IO4MU	EEMDS
2	OSCI	CKI	42	IO4MU	EEMD1
3	OSCO	CKO	43	IO4MU	EEMD2
4	–	VDD	44	IO4MU	EEMD3
5	–	GND	45	–	GND
6	OBF6M	ADCK	46	–	VDD
7	IO4M	SCK	47	OBF4M	DCK1
8	IO4M	SDATA	48	OBF4M	DCK2
9	IC	ADI9	49	IC	EXCKI
10	IC	ADI8	50	OBF4M	Y0
11	IC	ADI7	51	OBF4M	Y1
12	IC	ADI6	52	OBF4M	Y2
13	IC	ADI5	53	OBF4M	Y3
14	IC	ADI4	54	–	GND
15	–	VDD	55	–	VDD
16	–	GND	56	OBF4M	Y4
17	IC	ADI3	57	OBF4M	Y5
18	IC	ADI2	58	OBF4M	Y6
19	IC	ADI1	59	OBF4M	Y7
20	IC	ADI0	60	IO4M	HD
21	IO4M	OBCP	61	IO4M	VD
22	IO4M	ADCLP	62	IO4M	V1X
23	IO4M	BLKX	63	IO4M	V2X
24	IO4M	EEPDA	64	IO4M	V3X
25	–	GND	65	IO4M	V4X
26	–	VDD	66	–	VDD
27	IO4MU	EEPCK	67	–	GND
28	IC	EEPFL	68	IO4M	VH1X
29	IC	EEPSL	69	IO4M	VH3X
30	IO4M	WB1	70	OBF6M	OFDX
31	IO4M	WB2	71	–	VDD
32	IO4M	MIR	72	–	GND
33	IO4M	BLC	73	OBF12M	FR
34	–	GNDDA	74	OBF12M	FH1
35	–	VDDDA	75	OBF12M	FH2
36	DAO	VB	76	–	VDD
37	DAO	IREF	77	–	GND
38	DAI	VREF	78	OBF6M	RS
39	–	GNDDA	79	OBF6M	FS
40	DAO	VIDEO	80	OBF6M	FCDS

ICU : CMOS INPUT WITH PULL-UP
IC : CMOS INPUT
DAI : DA CONVERTER INPUT
IO4M : INPUT/OUTPUT
OBF4M/OBF6M/OBF12M : OUTPUT PIN
OSCI : OSCILLATTER INPUT
OSCO : OSCILLATTTER OUTPUT

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

No	SYMBOL	I/O	POLARITY	CONTENTS
1	ACL	ICU	⎍	Initializing input
2	CKI	IC	⎍⎍	Clock input. Connected XTAL between pin 3 and pin 2.
3	CKO	O	⎍⎍	Clock output
4	VDD	−		+3.3 V power supply input
5	GND	−		Ground pin
6	ADCK	O	⎍⎍	Clock output of AD converter to be connected to pin 13 of IR3Y38M.
7	SCK	O	⎍⎍	Clock output of Serial data to be connected to pin 16 of IR3Y38M.
8	SDATA	O	⨉	Serial data output to be connected to pin 19 of IR3Y38M.
9	ADI9	IC	⨉	Digital signal input to be fed from pin 12 of IR3Y38M(MSB).
10	ADI8	IC	⨉	Digital signal input to be fed from pin 11 of IR3Y38M.
11	ADI7	IC	⨉	Digital signal input to be fed from pin 10 of IR3Y38M.
12	ADI6	IC	⨉	Digital signal input to be fed from pin 9 of IR3Y38M.
13	ADI5	IC	⨉	Digital signal input to be fed from pin 8 of IR3Y38M.
14	ADI4	IC	⨉	Digital signal input to be fed from pin 5 of IR3Y38M.
15	VDD	−		+3.3 V power supply input
16	GND	−		Ground pin
17	ADI3	IC	⨉	Digital signal input to be fed from pin 4 of IR3Y38M.
18	ADI2	IC	⨉	Digital signal input to be fed from pin 3 of IR3Y38M.
19	ADI1	IC	⨉	Digital signal input to be fed from pin 2 of IR3Y38M.
20	ADI0	IC	⨉	Digital signal input to be fed from pin 1 of IR3Y38M.
21	OBCP	O	⎍	Optical clamp pulse output to be connected to pin 32 of IR3Y38M.

No	SYMBOL	I/O	POLARITY	CONTENTS
22	ADCLP	O	⊓	Clamp pulse output to be connected to pin 45 of IR3Y38M.
23	BLKX	O	⊓	Blanking pulse output to be connected to pin 35 of IR3Y38M.
24	EEPDA	IC	⋈	DATA input from EEPROM output pin.
25	GND	—		+3.3 V power supply input
26	VDD	—		Ground pin
27	EEPCK	I/O	⊓⊔	Clock output to EEPROM clock input pin. This pin keeps High-impeadance under High level of pin 29.
28	EEPFL	IC	⋈	Control pin of EEPROM.
29	EEPSL	IC	⋈	Control pin of EEPROM. A pull-down register should be connected between pin 29 and GND. High level of pin 29 can make data-setting from outside available.
30	WB1	I/O		White balance mode setting by both WB1 and WB2. Please see another table in detail. In digital output mode, this pin is assigned to bit 0 (LSB) of U/V signal.
31	WB2	I/O		White balance mode setting by both WB1 and WB2. Please see another table in detail. In digital output mode, this pin is assigned to bit 1 of U/V signal.
32	MIR	I/O		Video output mode setting. L : Normal H : Mirror In digital output mode, this pin is assigned to bit 2 of U/V signal.
33	BLC	I/O		Backlight compensation choice. L : OFF H : ON In digital output mode, this pin is assigned to bit 3 of U/V signal.
34	GNDDA	—		Grounding pin of built-in DA converter.
35	VDDDA	—		+3.3V power supply input of built-in DA converter.
36	VB	DAO		Bias voltage output of built-in DA converter to be connected to GND through a capacitor.

No	SYMBOL	I/O	POLARITY	CONTENTS
37	IREF	DAO		Bias current output of built-in DA converter to be connected to GND through a register.
38	VREF	DAI		Bias voltage input of built-in DA converter to be connected to +1.0V power supply.
39	GNDDA	—		Grounding pin of built-in DA converter.
40	VIDEO	DAO		Analog video signal output.
41	EEMDS	I/O		Electronic exposure mode setting by EEMDS, SHMD1, SHMD2 and SHMD3. Please see another page in detail. In digital output mode, this pin is assigned to bit 7 of U/V signal.
42	SHMD1	I/O		
43	SHMD2	I/O		
44	SHMD3	I/O		
45	GND	—		+3.3 V power supply input
46	VDD	—		Ground pin
47	DCK1	O	⎍⎍	Clock output of 13.5Mhz for digital signal output. Output mode setting switches to CSYNC output.
48	DCK2	O	⎍⎍	ID pulse output for U/V output signal.
49	EXCKI	IC	⎍⎍	Clock input of 13.5MHz.
50	Y0	O	⋈	Bit 0 (LSB) of Digital luminance signal output
51	Y1	O	⋈	Bit 1 of Digital luminance signal output
52	Y2	O	⋈	Bit 2 of Digital luminance signal output
53	Y3	O	⋈	Bit 3 of Digital luminance signal output
54	GND	—		Ground pin
55	VDD	—		+3.3 V power supply input
56	Y4	O	⋈	Bit 4 of Digital luminance signal output
57	Y5	O	⋈	Bit 5 of Digital luminance signal output
58	Y6	O	⋈	Bit 6 of Digital luminance signal output
59	Y7	O	⋈	Bit 7 (MSB) of Digital luminance signal output

No	SYMBOL	I/O	POLARITY	CONTENTS
60	HD	0	⎍	Horizontal driving pulse output. Either Driving timing or Video output timing is selectable by Output mode setting.
61	VD	0	⎍	Vertical driving pulse output. Either VD or CSYNC with either Driving timing or Video output timing is selectable by Output mode setting.
62	V1X	0	⎍	Vertical driving pulse output to be connected to Vertical driver IC. Either V3X or V4X should be connected to pin 45 of IR3Y38M.
63	V2X	0	⎍	
64	V3X	0	⎎	
65	V4X	0	⎎	
66	VDD	—		+3.3 V power supply input
67	GND	—		Ground pin
68	VH1X	0	⎎	Vertical driving pulse output to be connected to Vertical driver IC.
69	VH3X	0	⎎	Vertical driving pulse output to be connected to Vertical driver IC.
70	OFDX	0	⎎	OFD driving pulse output to be connected to Vertical driver IC.
71	VDD	—		+3.3 V power supply input
72	GND	—		Ground pin
73	FR	0	⎎	Reset pulse output to be connected to CCD through a capacitor.
74	FH1	0	⎍⎍	Horizontal driving pulse output to be connected to CCD.
75	FH2	0	⎎⎍	Horizontal driving pulse output to be connected to CCD.
76	VDD	—		+3.3 V power supply input
77	GND	—		Ground pin
78	RS	0	⎎	Sample-hold pulse output to be connected to pin 31 of IR3Y38M.
79	FS	0	⎎	Sample-hold pulse output to be connected to pin 30 of IR3Y38M.
80	FCDS	0	⎎	Sample-hold pulse output to be connected to both pin 28 and pin 29 of IR3Y38M.

5. INTERNAL COEFFICIENT TABLE

ADDRESS	NAME	bit	CONTENTS
00			Not used
01	MODE1	7	TVMD 0 : NTSC 1 : PAL
		6	INPUT SIGNAL DELAY 0 : NO DELAY 1 : 1 CLOCK DELAY
		5	COCK POLARITY TO LATCH INPUT SIGNAL
			0 : NORMAL 1 : INVERTED
		4	YL KILLER 0 : NORMAL 1 : KILLED
		3	PIN MODE SELECT 0 : MODE INPUT 1 : U/V OUTPUT (NOTE:2)
		2	VD OUTPUT CHOICE (NOTE:1)
		1	HD OUTPUT CHOICE 0 : TG 1 : VIDEO OUTPUT
		0	DCK1 OUTPUT CHOICE (NOTE:1)
02	MODE2	6-7	LUMINANCE GAMMA CHOICE
		4-5	COLOR GAMMA CHOICE
		3	VERTICAL APERTURE 0 : ON 1 : OFF
		2	HORIZONTAL APERTURE 0 : ON 1 : OFF
		1	COLOR KILLER 0 : ON 1 : OFF
		0	FLICKER CANCELLER 0 : ON 1 : OFF
03	MODE3	7	POLARITY CHOICE OF SP1, SP2
		6	POLARITY INVERTER OF HG
		5	VIDEO FORMAT CHOICE
			0 : INTERLACE 1 : NON-INTERLACE
		4	UV DOT-SEQUENCE CHOICE (OUTPUT STAGE)
		3	UV DOT-SEQUENCE CHOICE
		2	CARRIER BALANCE TUNING 0 : ON 1 : OFF
		1	AGC 0 : AUTO 1 : FIXED (GAIN at address 15)
		0	DIGITAL OUTPUT CLOCK 0 : 9.6MHz 1 : 13.5MHz
04	REF_IRIS1	0-7	EXPOSURE LEVEL (TARGET OF IRIS CONTROL)
05	CTLD_01	0-7	HIGHER LEVEL OF EXPOSURE LEVEL
06	CTLD_02	0-7	LOWER LEVEL OF EXPOSURE LEVEL
07	REF_IRIS2	0-7	EXPOSURE LEVEL WITH BACKLIGHT COMPENSATION
08	UW_E1	0-7	IRIS CONTROL WEIGHTING FACTOR 1
09	UW_E2	0-7	IRIS CONTROL WEIGHTING FACTOR 2
0A	UW_E3	0-7	IRIS CONTROL WEIGHTING FACTOR 3

ADDRESS	NAME	bit	CONTENTS
0B	UW_E4	0-7	IRIS CONTROL WEIGHTING FACTOR 4
0C	UW_E5	0-7	IRIS CONTROL WEIGHTING FACTOR 5
0D	UW_E6	0-7	IRIS CONTROL WEIGHTING FACTOR 6
0E	UW_E7	0-7	IRIS CONTROL WEIGHTING FACTOR 7
0F	UW_E8	0-7	IRIS CONTROL WEIGHTING FACTOR 8
10	CW_E	0-7	WEIGHTING FACTOR OF IRIS WINDOW AREA
11	CWP_E	0-6	UPPER-LEFT POINT OF IRIS WINDOW AREA
12	CWA_E	0-6	LOWER-RIGHT POINT OF IRIS WINDOW AREA
13	EE_DIV_STP	4-6	ELECTRNIC SHUTTER SPEED PITCH
	LPFE_F	2-3	IRIS RESPONSE SPEED CHOICE WITH FLICKER CANCELLER
	LPFE_N	0-1	IRIS RESPONSE SPEED CHOICE
14	P_HEE_IRIS	0-7	MAXIMUM LUMINANCE LEVEL TO CONTROL IRIS
15	P_LEE_IRIS	0-7	MINIMUM LUMINANCE LEVEL TO CONTROL IRIS
16	INT_PEAK	6	INTEGRATED PIXELS 0 : 8 PIXELS 1 : 4 PIXELS
	IRIS_DLY		CONDITION OF LOCKED EXPOSURE CONTROL
		5	NUMBER OF FILTERS 0 : 1 TIMES INTEGRATION 1 : 3 TIMES
		4	VALID SIGNAL TO CONTROL IRIS 00 : EVERY FIELD
		3	01 : EVERY 2 FIELD 10 : EVERY 3 FIELD 11 : EVERY 7 FIELD
			CONDITION OF UNLOCKED EXPOSURE CONTROL
		2	NUMBER OF FILTERS 0 : 1 TIMES INTEGRATION 1 : 3 TIMES
		1	VALID SIGNAL TO CONTROL IRIS 00 : EVERY FIELD
		0	01 : EVERY 2 FIELD 10 : EVERY 3 FIELD 11 : EVERY 7 FIELD
17	AG_DIV_STP	5-7	AGC CONTROL DATA
	AG_GAIN	0-4	MINIMUM PITCH OF AGC VARIABLE GAIN
18			NOT USED
19	I_AGC_D8	0-7	AGC BIAS GAIN
1A	REF_AGC_D8	0-7	AGC REFERENCE GAIN
1B	S_38M_GA	0-7	FIXED AGC GAIN
1C	S_38M_MAX	0-2	AGC MAX GAIN
1D	S_38M_OFS	6	OFFSET CONTROL 0 : AUTO 1 : FIXED
		0-5	OFFSET DATA

ADDRESS	NAME	bit	CONTENTS
1E	CSEPR	0-7	RED COLOR SIGNAL SEPARATOR
1F	CSEPB	0-7	BLUE COLOR SIGNAL SEPARATOR
20	CB_R	0-7	RED SIGNAL CARRIER BALANCE
21	CB_B	0-7	BLUE SIGNAL CARRIER BALANCE
22	K_T_R	0-7	BASIC RED WB GAIN
23	K_T_B	0-7	BASIC BLUE WB GAIN
24	MAX_WBR	0-7	RED WB GAIN AT MAXIMUM COLOR TEMPERATURE
25	MIN_WBR	0-7	RED WB GAIN AT MINIMUM COLOR TEMPERATURE
26	MAX_WBB	0-7	BLUE WB GAIN AT MAXIMUM COLOR TEMPERATURE
27	MIN_WBB	0-7	BLUE WB GAIN RED AT MINIMUM COLOR TEMPERATURE
28	WBR1	0-7	RED WB DATA (PRESET 1)
29	WBB1	0-7	BLUE WB DATA (PRESET 1)
2A	WBR2	0-7	RED WB DATA (PRESET 2)
2B	WBB2	0-7	BLUE WB DATA (PRESET 2)
2C	WBR3	0-7	RED WB DATA (PRESET 3)
2D	WBB3	0-7	BLUE WB DATA (PRESET 3)
2E	K_GA_R	0-7	CORRECTION COEFFICIENT OF R-Y GAIN
2F	K_GA_B	0-7	CORRECTION COEFFICIENT OF B-Y GAIN
30	REF_GA_R	0-5	BASIC GAIN OF R-Y SIGNAL
31	REF_GA_B	0-5	BASIC GAIN OF B-Y SIGNAL
32	GA_R1	0-5	R-Y GAIN DATA (PRESET 1)
33	GA_B1	0-5	B-Y GAIN DATA (PRESET 1)
34	GA_R2	0-5	R-Y GAIN DATA (PRESET 2)
35	GA_B2	0-5	B-Y GAIN DATA (PRESET 2)
36	GA_R3	0-5	R-Y GAIN DATA (PRESET 3)
37	GA_B3	0-5	B-Y GAIN DATA (PRESET 3)
38	MAX_IQAREA	7	AWB IQ AREA CHOICE 0 : SET DATA 1 : FIXED
	LPFIQ_F	5-6	RESPONSE SPEED CHOICE WITH FLICKER CANCELLER
	LPFIQ_N	3-4	RESPONSE SPEED
	FINE	2	FINE-TUNING MODE
	AWB_WAIT_C	0-1	AWB TIME CONSTANT AFTER LOCK-IN (UPPER 2 BITS)
39	AWB_WAIT_C	0-7	AWB TIME CONSTANT AFTER LOCK-IN (LOWER 8 BITS)
3A	CMP_CT	0-7	AWB TIME CONSTANT V PERIOD MULTIPLIED BY DATA

ADDRESS	NAME	bit	CONTENTS
3B	AWB_HCL	0-7	HIGHEST LUMINANCE LEVEL TO BE AVAILABLE FOR AWB CONTROL
3C	AWB_LCL	0-7	LOWEST LUMINANCE LEVEL TO BE AVAILABLE FOR AWB CONTROL
3D	REF_WBPK	0-7	MAXIMUM LUMINANCE LEVEL FOR AWB
3E	K_CL	0-7	MINIMUM LUMINANCE LEVEL FOR AWB
3F	K_WBCL	0-7	VARIABLE PITCH FOR MINIMUM LUMINANCE LEVEL FOR AWB
40	UW_IQ1	0-7	AWB CONTROL WEIGHTING FACTOR 1
41	UW_IQ2	0-7	AWB CONTROL WEIGHTING FACTOR 2
42	UW_IQ3	0-7	AWB CONTROL WEIGHTING FACTOR 3
43	UW_IQ4	0-7	AWB CONTROL WEIGHTING FACTOR 4
44	INT_I_R-Y	7	AWB CONTROL DATA 0 : I/Q 1 : R-Y/B-Y
	CW_IQ	0-6	WEIGHTING FACTOR OF AWB WINDOW AREA
45	CWPA_IQ	4-7	UPPER-LEFT POINT OF AWB WINDOW AREA
		0-3	LOWER-RIGHT POINT OF AWB WINDOW AREA
46	CTLD_AWO	0-7	IRIS LEVEL TO ERASE THE AREA TO DETECT WHITE COLOR
47	AWB_IP_L	0-7	OUTSIDE AWB DETECTOR AREA I-PLUS
48	AWB_IM_L	0-7	OUTSIDE AWB DETECTOR AREA I-MINUS
49	AWB_QP_L	0-7	OUTSIDE AWB DETECTOR AREA Q-PLUS
4A	AWB_QM_L	0-7	OUTSIDE AWB DETECTOR AREA Q-MINUS
4B	AWB_IP_S	0-7	INSIDE AWB DETECTOR AREA I-PLUS
4C	AWB_IM_S	0-7	INSIDE AWB DETECTOR AREA I-MINUS
4D	AWB_QP_S	0-7	INSIDE AWB DETECTOR AREA Q-PLUS
4E	AWB_QM_S	0-7	INSIDE AWB DETECTOR AREA Q-MINUS
4F	AWB_I_WH_L	0-6	AWB WHITE ZONE I-PLUS
50	AWB_Q_WH_L	0-6	AWB WHITE ZONE Q-PLUS
51	AWB_I_WH_S	0-6	AWB WHITE ZONE I-MINUS
52	AWB_Q_WH_S	0-6	AWB WHITE ZONE Q-MINUS
53	K_MAT_R	0-7	R-Y GAIN FOR COLOR MATRIX CORRECTION
54	K_MAT_B	0-7	B-Y GAIN FOR COLOR MATRIX CORRECTION
55	REF_MAT_R	0-5	BASIC R-Y DATA OF COLOR MATRIX CORRECTION
56	REF_MAT_B	0-5	BASIC B-Y DATA OF COLOR MATRIX CORRECTION
57	MAT1	0-7	COLOR MATRIX DATA (PRESET 1) R-Y 4 bits, B-Y 4 bits
58	MAT2	0-7	COLOR MATRIX DATA (PRESET 2) R-Y 4 bits, B-Y 4 bits
59	MAT3	0-7	COLOR MATRIX DATA (PRESET 3) R-Y 4 bits, B-Y 4 bits
5A	COL_S	0-7	AGC GAIN TO START SUPPRESSING COLOR LEVEL

ADDRESS	NAME	bit	CONTENTS
5B	COL_H	0-5	PITCH OF COLOR LEVEL SUPPRESSING
5C	CKI_HCL	0-7	HIGHER LUMINANCE LEVEL TO START SUPPRESSING COLOR SIGNAL
5D	CKI_LCL	0-7	LOWER LUMINANCE LEVEL TO START SUPPRESSING COLOR SIGNAL
5E	CKI_HLGA	4-7	COLOR SIGNAL SUPPRESSION GAIN FOR HIGHER LUMINANCE SIGNAL
		0-3	COLOR SIGNAL SUPPRESSION GAIN FOR LOWER LUMINANCE SIGNAL
5F	CKI_HLTI	4-7	HILIGHT LUMINANCE SIGNAL POSITION TO SUPPRESS COLOR -2～+2
		0-3	LOWEST LUMINANCE SIGNAL POSITION TO SUPPRESS COLOR -2～+2
60	CKI_HECL	0-7	HORIZONTAL APERTURE LEVEL TO SUPPRESS COLOR SIGNAL
61	CKI_EVCL	0-7	VERTICAL APERTURE LEVEL TO SUPPRESS COLOR SIGNAL
62	CKI_EGA	4-7	HORIZONTAL APERTURE GAIN TO SUPPRESS COLOR SIGNAL
		0-3	VERTICAL APERTURE GAIN TO SUPPRESS COLOR SIGNAL
63	APT_S	0-7	AGC GAIN TO START SUPPRESSING APERTURE SIGNAL
64	APT_H	0-5	GAIN TO SUPPRESS APERTURE SIGNAL
65	NSUP_R	0-7	R-Y SIGNAL CORING LEVEL
66	NSUP_B	0-7	B-Y SIGNAL CORING LEVEL
67	CKI_IEL	7	COLOR-KILLER LEVEL 0: UNITY GAIN 1: 1/4 GAIN
	CKI_ETI	4-6	HORIZONTAL EDGE SIGNAL POSITION TO KILL COLOR SIGNAL -2～+2
		1-3	VERTICAL EDGE SIGNAL POSITION TO KILL COLOR SIGNAL -2～+2
68	APT_HTIM	6-7	HORIZONTAL APERTURE SIGNAL POSITION -1～+1
	APT_HGA	1-5	HORIZONTAL APERTURE GAIN
69	APT_HCL	0-6	HORIZONTAL APERTURE SIGNAL CORING
6A	APT_VGA	0-4	VERTICAL APERTURE GAIN
6B	APT_VCL	0-6	VERTICAL APERTURE SIGNAL CORING
6C	CBLK_LV	7	CBLK LEVEL CHOICE 0 : 0 1 : 10H
	SETUP	1-6	SET UP LEVEL
6D	VARI_Y	0-4	LUMINANCE SIGNAL POSITION
6E	SW_CTRL	0-7	BELOW DATA IS AVAILABLE UNDER BOTH EEPSL=H AND DIGITAL OUTPUTMODE
			WB1、WB2、BACK、EEMD、SHMD1、SHMD2、SHMD3、MIR
6F	TG_SEL1	5-7	ADCK PHASE SETTING (6 STEPS PER 60 DEGREE)
		2-4	FS PHASE SETTING (±2 nS× 3)
70	TG_SEL2	5-7	FCDS PHASE SETTING (±2 nS× 3)
		2-4	FR PHASE SETTING (±2 nS× 3)

6. Electric characteristics

6-1. Absolute maximum operating condition

ITEM	SYMBOL	RATING	UNIT
POWER SUPPLY VOLTAGE	VDD	- 0.3 ~ + 4.3	V
INPUT VOLTAGE	Vi	- 0.3 ~ VDD + 0.3	V
OUTPUT VOLTAGE	Vo	- 0.3 ~ VDD + 0.3	V
STORAGE TEMPERATURE	Tstg	- 55 ~ + 150	℃

6-2. Operating condition

ITEM	SYMBOL	RATING	UNIT
POWER SUPPLY VOLTAGE	VDD	+ 3.0 ~ + 3.6	V
OPERATING TEMPERATURE	Topr	- 10 ~ + 70	℃
input CLOCK FREQUENCY	Fck	28.6MHz	MHz

6-3. Electric characteristics VDD = + 3.0 ~ + 3.6V Topr = - 10 ~ + 70 ℃

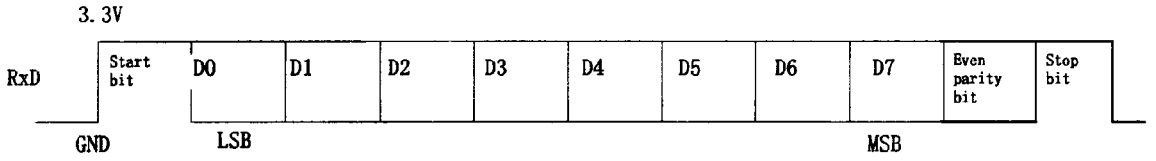
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Low level input voltage	VIL				0.2VDD	V	1
Hlevel input voltage	VIH		0.8VDD			V	
Input current by register	IOL1	VIN = 0 V		10		μA	2
High output voltage	VOH1	IOH = 4 mA	0.9VDD			V	3
Low output voltage	VOL1	IOL = - 4 mA			0.1VDD	V	
High output voltage	VOH2	IOH = 6 mA	0.9VDD			V	4
Low output voltage	VOL2	IOL = - 6 mA			0.1VDD	V	
High output voltage	VOH3	IOH = 12 mA	0.9VDD			V	5
Low output voltage	VOL3	IOL = -12 mA			0.1VDD	V	
RESOLUTION	RES			9		bit	6
Linearity error	EL	Vref = 1.0 V			±3.0	LSB	
Differential error	ED	Rref = 2.4 Kohm			±1.0	LSB	
Full scale current	IFS	Rout = 75 ohm		13		mA	
Reference voltage	Vref			1.0		V	7
Reference register	Rref			4.8		KΩ	8
Output load register	Rout			75		Ω	9

NOTE 1: PIN with IC, ICU
NOTE 2: PIN WITH ICU
NOTE 3: PIN WITH OBF4M, IO4M
NOTE 4: PIN WITH OBF6M
NOTE 5: PIN WITH OBF12M
NOTE 6: PIN OF VIDEO
NOTE 7: PIN OF VREF
NOTE 8: PIN OF IREF
NOTE 9: PIN OF VIDEO

6-4. DATA INTERFACE

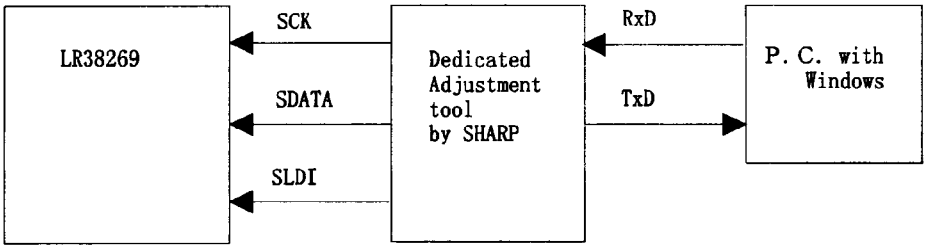
(1) Format of data transfers

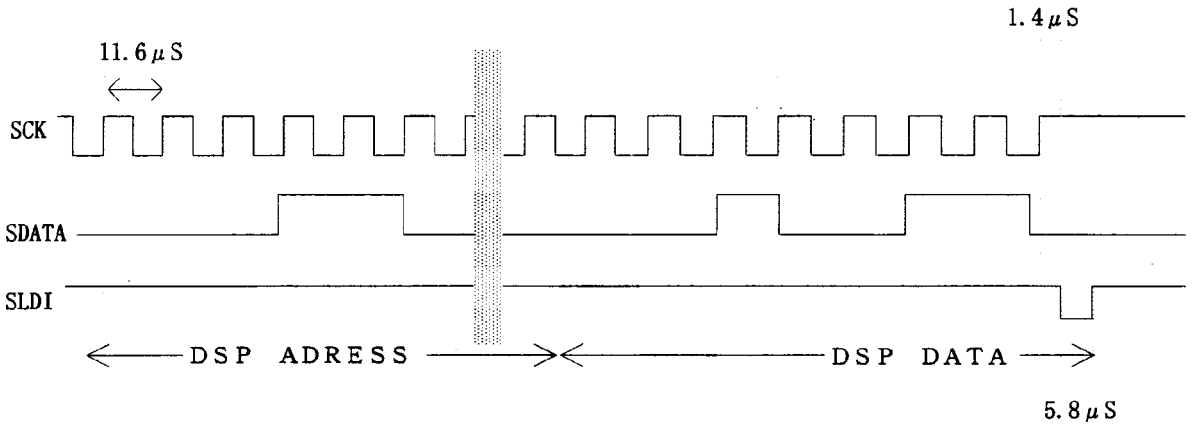
- Format of transfers : Asynchronous (Based on RS-232C standard)
- Bit rate : 9600 bps
- Data length : 8 bit
- Parity check : 1 even parity bit
- Start bit : 1 bit
- Stop bit : 1 bit
- Signal voltage level (CMOS)



Data bit

- System Connection





Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1114

2. Markings

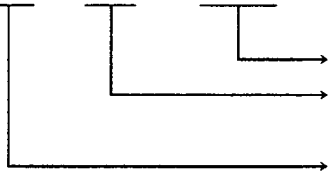
2－1. Marking contents

(1) Product name : LR38269

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××



Indicates the product was manufactured in the WWth week of 19YY.

Denotes the production ref.code (1~3)

Denotes the production week. (01,02,03, ・・・・・52,53)

Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No.AA1114

(This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (60devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P Band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (600devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

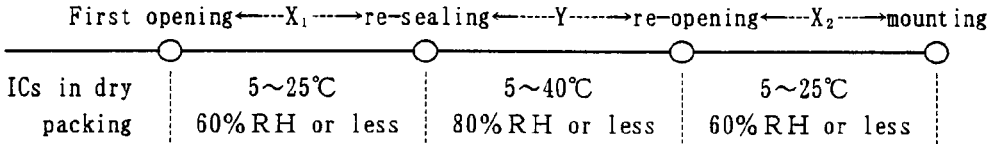
3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 4 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 4 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 4 days, and store the ICs in the same environment as section 4-3.(1).



$X_1 + X_2$: within 4 days
Y : within 2 weeks

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃.
Heat resistance tray is used for shipping tray.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.(1).

5. Surface Mount Conditions

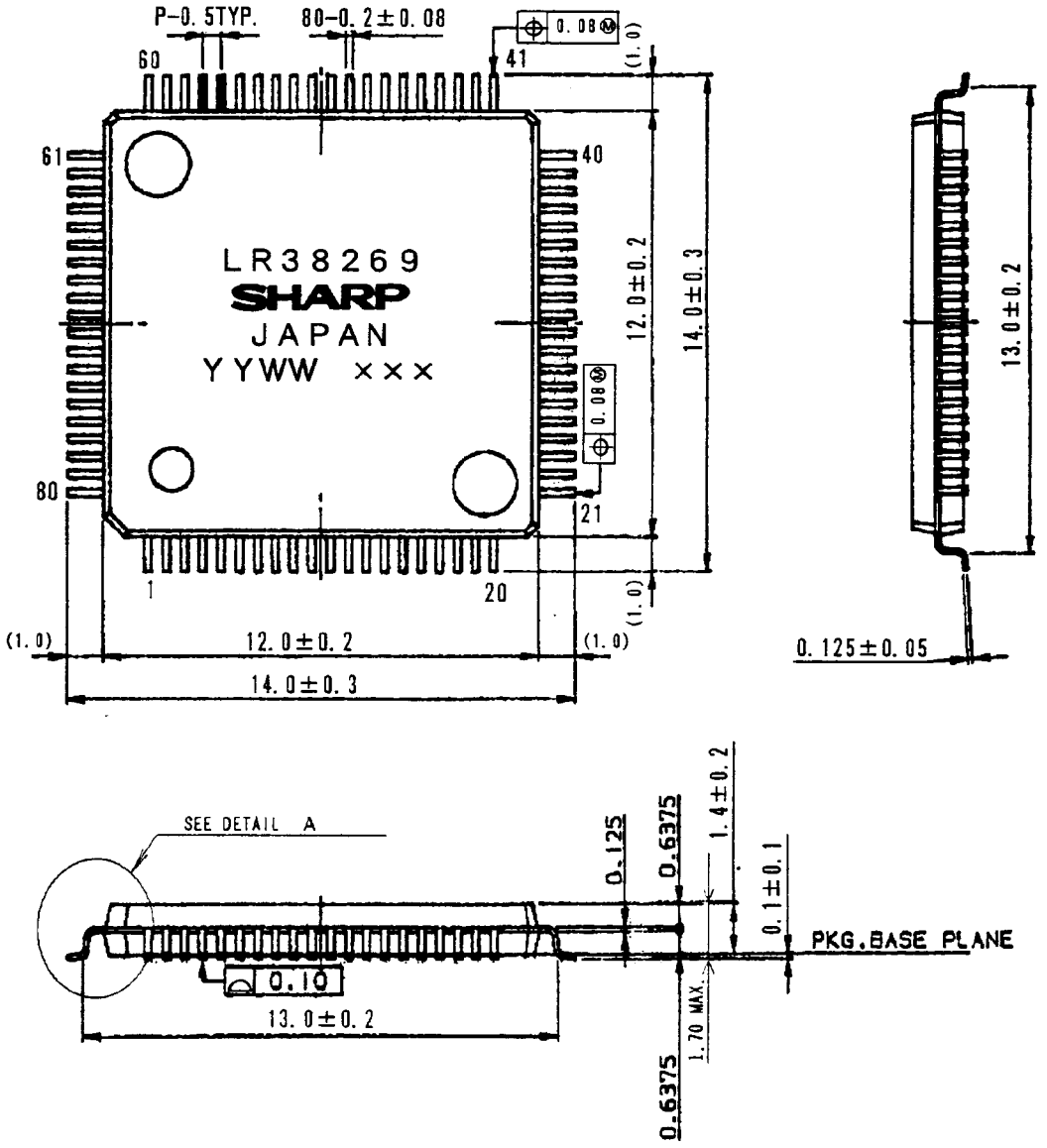
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

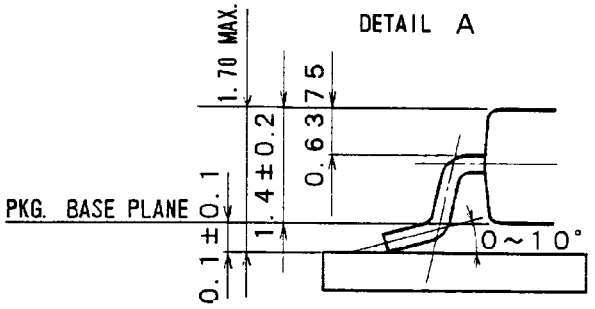
5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230℃ or less, duration of less than 15 seconds. 200℃ or over, duration of less than 40 seconds. Temperature increase rate of 1～4℃/second.	IC package surface
Vapor phase soldering	215℃ or less, duration of less than 40 seconds above 200℃.	Steam
Manual soldering (soldering iron)	260℃ or less, duration of less than 10 seconds.	IC outer lead

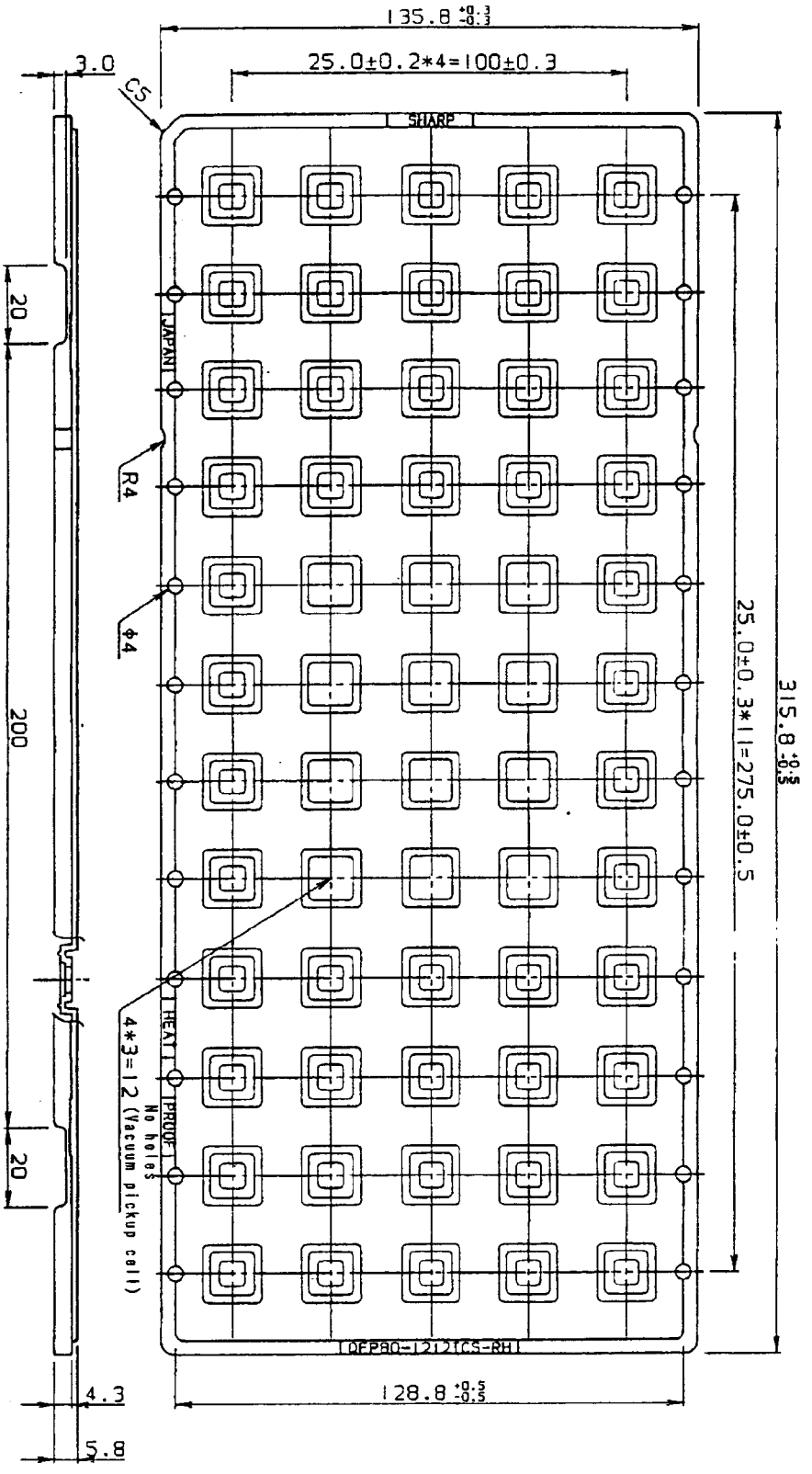
5－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃





名称 NAME	LQFP80-P-1212	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1114	単位 UNIT	mm	



名称 NAME	QFP80−1212TCS−RH			備考 NOTE
DRAWING NO.	CV626	単位 UNIT	mm	

DSP, LR38269