



# 3.3V CMOS 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, AND BUS-HOLD

**IDT74LVCH162244A**

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$ , Normal Range
- $V_{cc} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4 $\mu$ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Available in SSOP, TSSOP, and TVSOP packages

## DRIVE FEATURES:

- Balanced Output Drivers:  $\pm 12mA$
- Full internal series termination

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

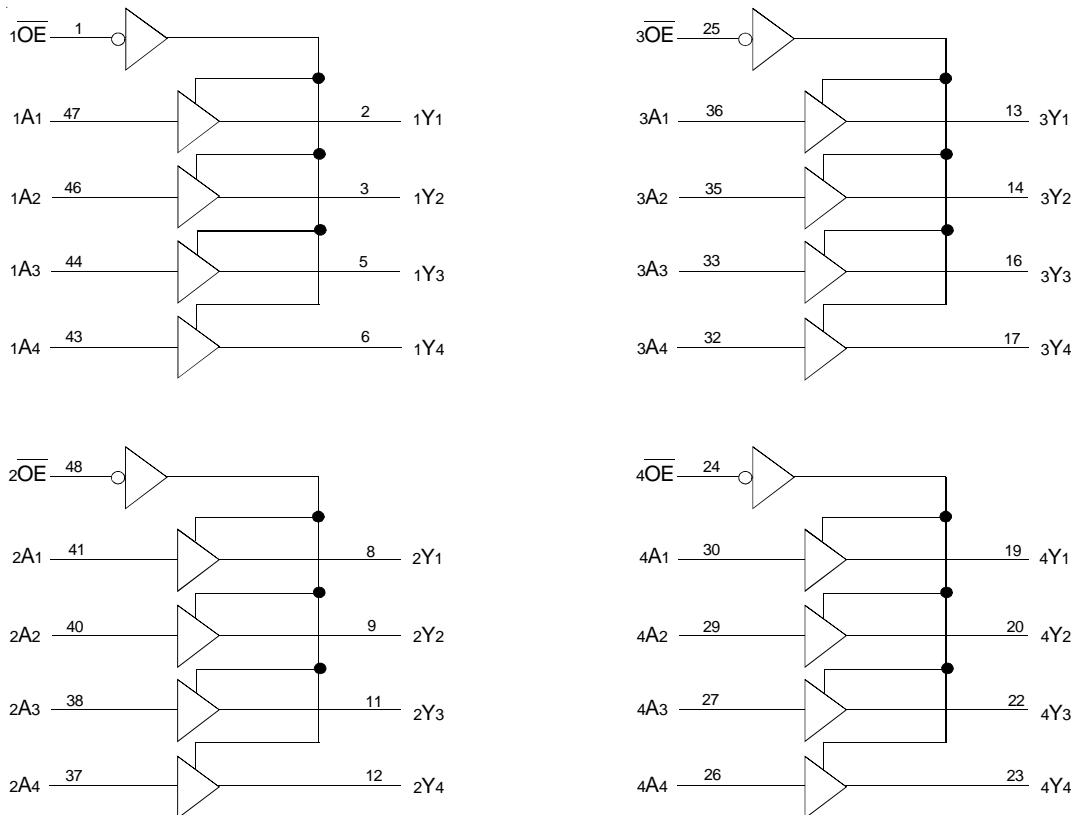
The LVCH162244A 16-bit buffer/driver is built using advanced dual metal CMOS technology. The LVCH162244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

All pins of this 16-bit buffer/driver can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH162244A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive  $\pm 12mA$  at the designated threshold levels.

The LVCH162244A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM

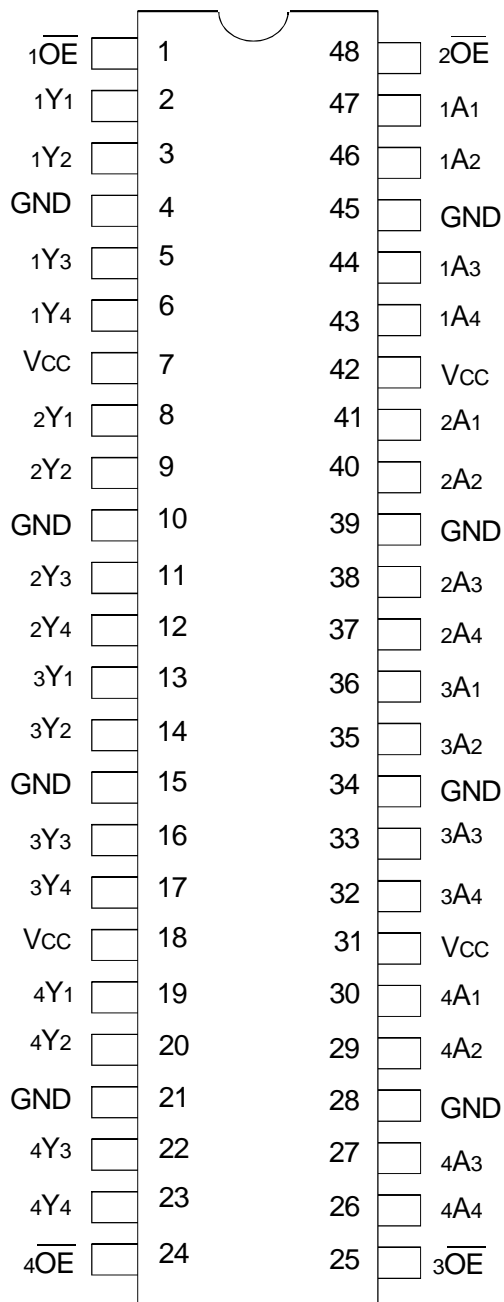


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

MARCH 1999

## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
x $\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs <sup>(1)</sup>
xYx	3-State Outputs

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH 4-BIT BUFFER)<sup>(1)</sup>

Inputs		Outputs
x $\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

### NOTE:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = 0 to 5.5V	—	—	±10	μA
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 5.5V		—	—	±50	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5V^{(2)}$	—	—	10	
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	500	μA

### NOTES:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>BH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
I <sub>BH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	—	—	—	μA
			V <sub>I</sub> = 0.7V	—	—	—	
I <sub>BHO</sub> I <sub>BHLO</sub>	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

### NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = - 0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = - 4mA	1.9	—	
			I <sub>OH</sub> = - 6mA	1.7	—	
		V <sub>CC</sub> = 2.7V	I <sub>OH</sub> = - 4mA	2.2	—	
			I <sub>OH</sub> = - 8mA	2	—	
		V <sub>CC</sub> = 3V	I <sub>OH</sub> = - 6mA	2.4	—	
I <sub>OH</sub> = - 12mA	2		—			
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 4mA	—	0.4	
			I <sub>OL</sub> = 6mA	—	0.55	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 4mA	—	0.4	
			I <sub>OL</sub> = 8mA	—	0.6	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 6mA	—	0.55	
I <sub>OL</sub> = 12mA	—		0.8			

**NOTE:**  
1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Buffer/Driver Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	35	pF
CPD	Power Dissipation Capacitance per Buffer/Driver Outputs disabled		4	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

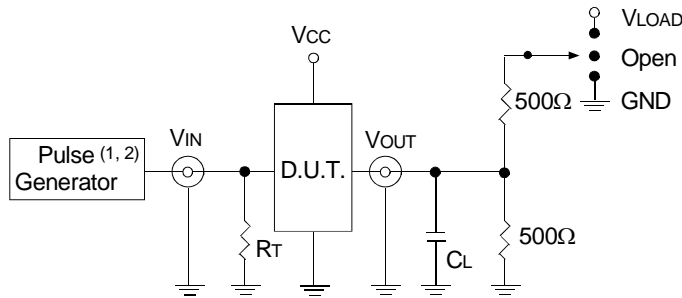
Symbol	Parameter	V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay	—	5.6	1.1	4.4	ns
t <sub>PHL</sub>	xAx to xYx					
t <sub>PZH</sub>	Output Enable Time	—	6.9	1	5.5	ns
t <sub>PZL</sub>	x $\overline{OE}$ to xYx					
t <sub>PHZ</sub>	Output Disable Time	—	6.8	1.8	6.3	ns
t <sub>PLZ</sub>	x $\overline{OE}$ to xYx					
t <sub>SK(0)</sub>	Output Skew <sup>(2)</sup>	—	—	—	500	ps

**NOTES:**  
1. See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = - 40°C to + 85°C.  
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ± 0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

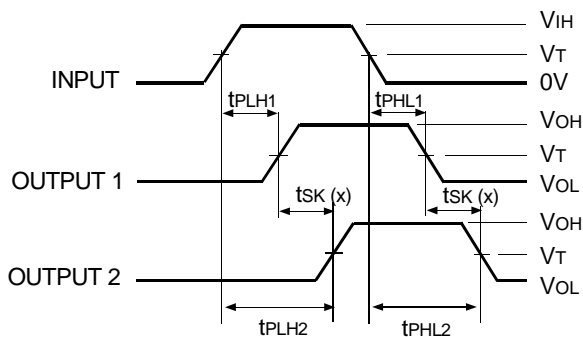
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

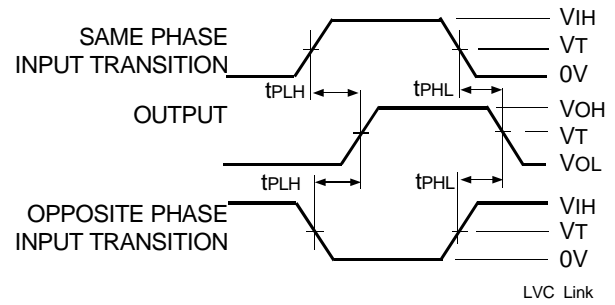


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

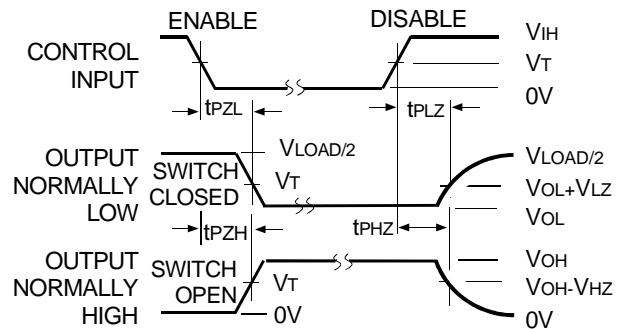
Output Skew - tsk(x)

#### NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



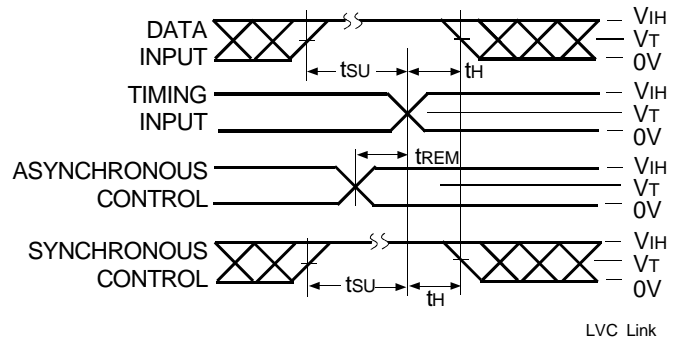
#### Propagation Delay



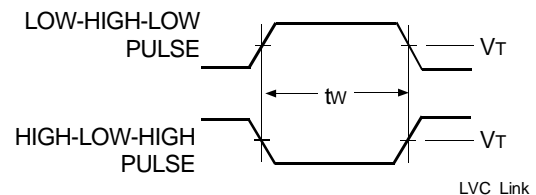
#### Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

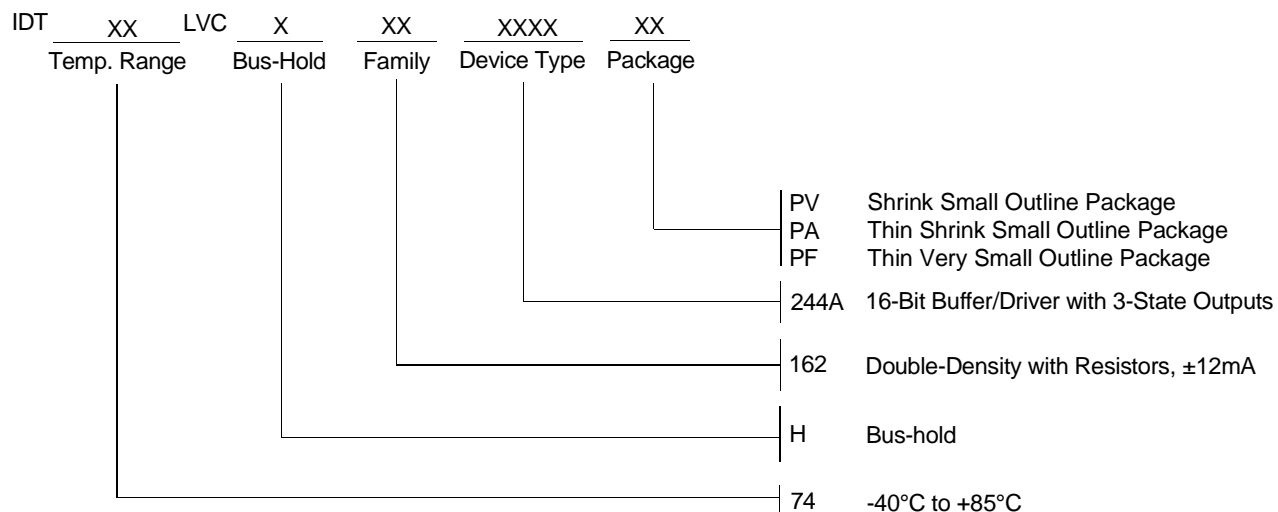


#### Set-up, Hold, and Release Times



#### Pulse Width

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
 www.idt.com

**for Tech Support:**  
 logichelp@idt.com  
 (408) 654-6459