



June 2001  
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## FSTD162861 20-Bit Bus Switch with Level Shifting and 25Ω Series Resistors in Outputs (Preliminary)

### General Description

The Fairchild Switch FSTD162861 provides 20-bits of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to  $V_{CC}$  has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device is organized as a 10-bit or 20-bit bus switch. When  $\overline{OE}_1$  is LOW, the switch is ON and Port 1A is connected to Port 1B. When  $\overline{OE}_2$  is LOW, Port 2A is connected to Port 2B. When  $\overline{OE}_X$  is HIGH, a high impedance state exists between the A and B Ports. The FSTD162861 has equivalent 25Ω series resistors to reduce signal-reflection noise, eliminating the need for external terminating resistors.

### Features

- 25Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low  $I_{CC}$
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- TruTranslation™ voltage translation from 5.0V inputs to 3.3V outputs

### Ordering Code:

Order Number	Package Number	Package Description
FSTD162861MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

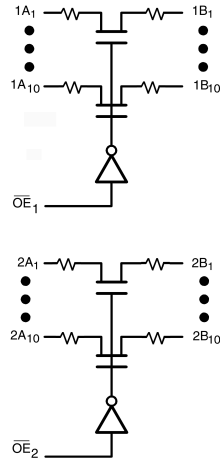
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

TruTranslation™ is a trademark of Fairchild Semiconductor Corporation.

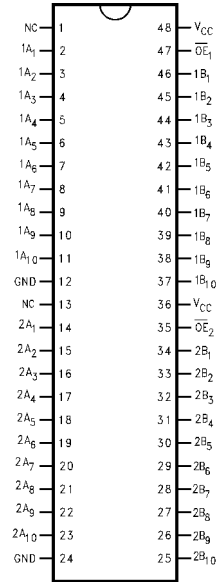
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**Logic Diagram**



**Connection Diagram**



**Truth Table**

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

**Pin Descriptions**

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

### Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ ) (Note 2)	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ ) (Note 3)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output ( $I_{OUT}$ ) Current	128 mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150 °C

### Recommended Operating Conditions (Note 4)

Power Supply Operating ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to 5.5V
Input Rise and Fall Time ( $t_r, t_f$ )	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature ( $T_A$ )	-40 °C to +85 °C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:**  $V_S$  is the voltage observed/applied at either the A or B Port across the switch.

**Note 3:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 4:** Unused control inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$			Units	Conditions
			Min	Typ (Note 5)	Max		
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18\text{ mA}$
$V_{IH}$	HIGH Level Input Voltage	4.5 - 5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.5 - 5.5			0.8	V	
$V_{OH}$	HIGH Level	4.5 - 5.5	See Figure 3			V	
$I_I$	Input Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq V_{IN} \leq 5.5V$
		0			10	$\mu\text{A}$	$V_{IN} = 5.5V$
$I_{OZ}$	OFF-STATE Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 6)	4.5	20	26	38	$\Omega$	$V_{IN} = 0V, I_{IN} = 64\text{ mA}$
		4.5	20	27	40	$\Omega$	$V_{IN} = 0V, I_{IN} = 30\text{ mA}$
		4.5	20	28	48	$\Omega$	$V_{IN} = 2.4V, I_{IN} = 15\text{ mA}$
$I_{CC}$	Quiescent Supply Current	5.5			1.5	mA	$OE_1 = OE_2 = GND$ $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
					3	mA	$OE_1 = OE_2 = V_{CC}$ $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	5.5			2.5	mA	One Input at 3.4V Other Inputs at $V_{CC}$ or GND

**Note 5:** Typical values are at  $V_{CC} = 5.0V$  and  $T_A = +25^\circ\text{C}$

**Note 6:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

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### AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40 °C to +85 °C, C <sub>L</sub> = 50 pF, R <sub>U</sub> = R <sub>D</sub> = 500Ω		Units	Conditions	Figure Number
		V <sub>CC</sub> = 4.5 – 5.5V				
		Min	Max			
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus (Note 7)		1.25	ns	V <sub>I</sub> = OPEN	Figures 1, 2
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	1.0	6.0	ns	V <sub>I</sub> = 7V for t <sub>PZL</sub> V <sub>I</sub> = OPEN for t <sub>PZH</sub>	Figures 1, 2
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	1.0	7.0	ns	V <sub>I</sub> = 7V for t <sub>PLZ</sub> V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	Figures 1, 2

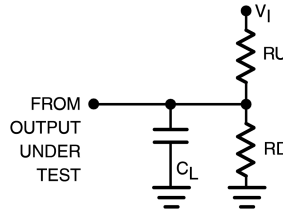
**Note 7:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

### Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C <sub>IN</sub>	Control Pin Input Capacitance	3.5		pF	V <sub>CC</sub> = 5.0V, V <sub>IN</sub> = 0V
C <sub>I/O</sub>	Input/Output Capacitance "OFF State"	6.0		pF	V <sub>CC</sub> , $\overline{OE}$ = 5.0V, V <sub>IN</sub> = 0V

**Note 8:** T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

### AC Loading and Waveforms



- Note:** Input driven by 50Ω source terminated in 50Ω
- Note:** C<sub>L</sub> includes load and stray capacitance
- Note:** Input PRR = 1.0 MHz, t<sub>W</sub> = 500 ns

FIGURE 1. AC Test Circuit

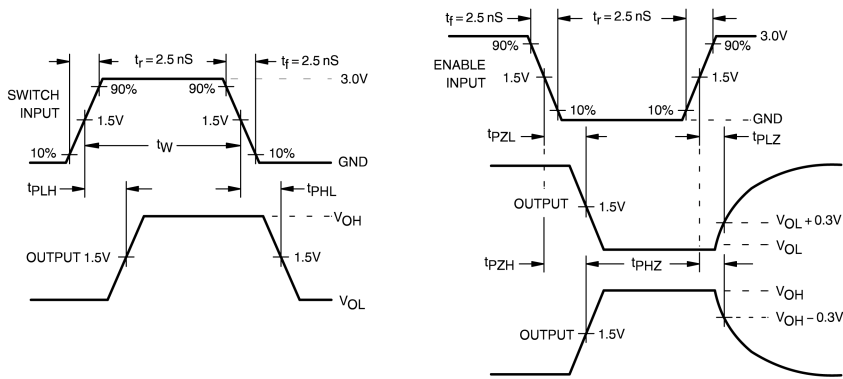


FIGURE 2. AC Waveforms

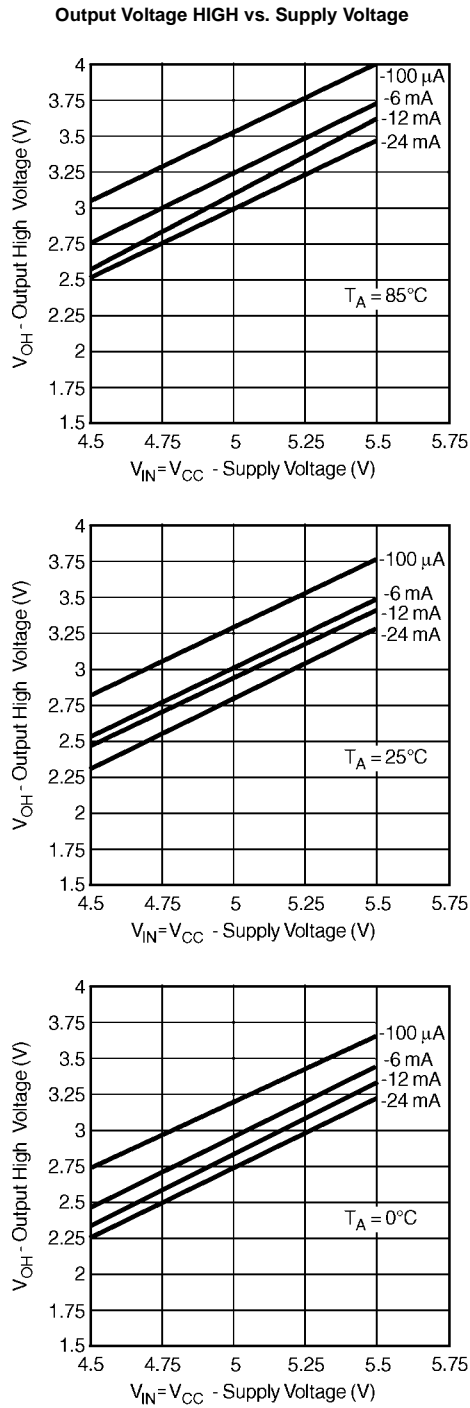
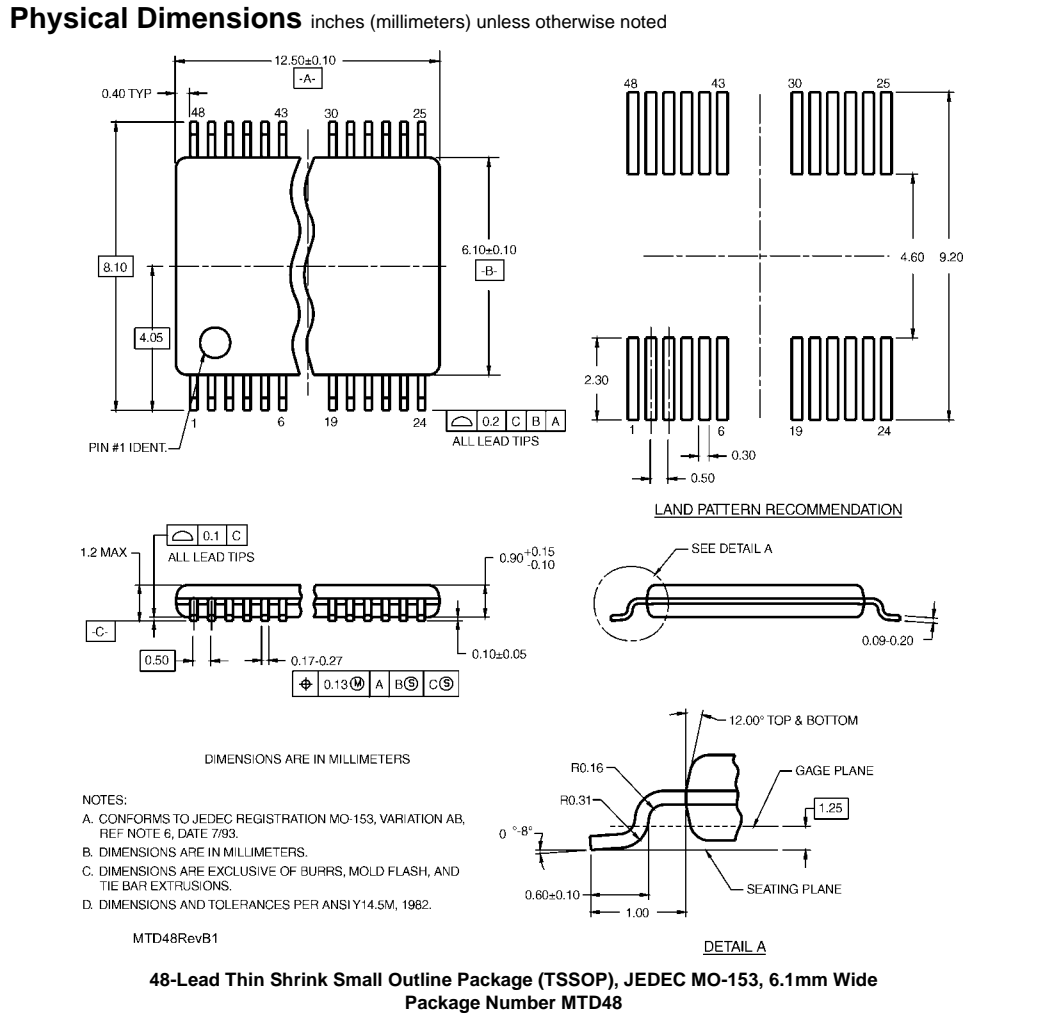


FIGURE 3.



**Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

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