

Power Amplifier/Antenna Switch + Low Noise Down Conversion Mixer for PHS

Description

The CXG7001FN is a MMIC consisting of the power amplifier, antenna switch and low noise down conversion mixer.

This IC is designed using the Sony's GaAs J-FET process featuring a single positive power supply operation.

Features

- Operates at a single positive power supply: $V_{DD} = 3V$
- Small mold package: 26-pin HSOF

<Power amplifier/antenna switch transmitter block >

- Low current consumption: $I_{DD} = 150mA$
($P_{OUT} = 20.2dBm, f = 1.9GHz$)
- High power gain: $G_p = 39dB$ Typ.
($P_{OUT} = 20.2dBm, f = 1.9GHz$)

**<Antenna switch receiver block/
low noise down conversion mixer>**

- Low current consumption: $I_{DD} = 5.5mA$ Typ.
(When no signal)
- High conversion gain: $G_c = 20.5dB$ Typ. ($f = 1.9GHz$)
- Low distortion: Input $IP_3 = -13dBm$ Typ. ($f = 1.9GHz$)
- High image suppression ratio: $IMR = 40dBc$ Typ.
($f = 1.9GHz$)
- High 1/2 IF suppression ratio: $1/2IFR = 44dBc$ Typ.
($f = 1.9GHz$)

Applications

Japan digital cordless telephones (PHS)

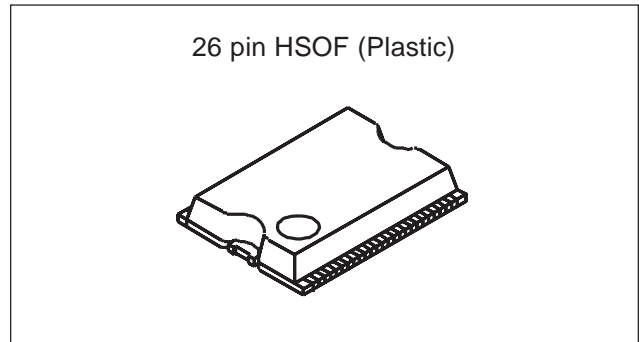
Structure

GaAs J-FET MMIC

Notes on Handling

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Absolute Maximum Ratings

<Power amplifier block>

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	V_{GSO}	1.5	V
• Gain control voltage	V_{PCTL}	2.5	V
• Drain current	I_{DD}	550	mA
• Allowable power dissipation	P_D	3	W

<Switch block>

Control voltage	V_{CTL}	6	V
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<Front-end block>

• Supply voltage	V_{DD}	6	V
• Input power	P_{RF}	+10	dBm

<Common to each block>

• Channel temperature	T_{ch}	150	°C
• Operating temperature	T_{opr}	-35 to +85	°C
• Storage temperature	T_{stg}	-65 to +150	°C

Recommended Operating Conditions

<Common to each block>

• Supply voltage	V_{DD}	2.7 to 3.3	V
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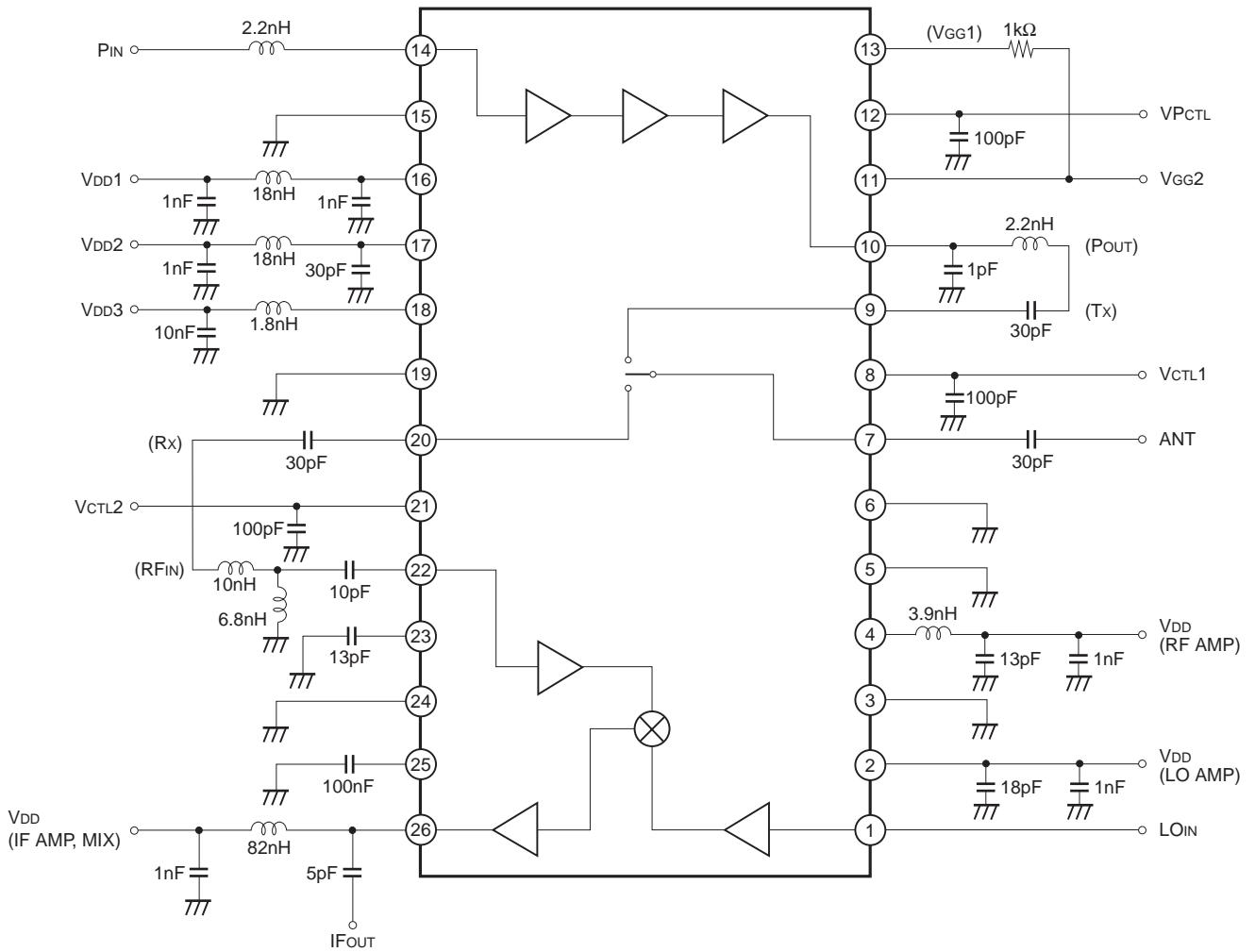
<Power amplifier block>

• Gain control voltage	V_{PCTL}	to $V_{DD}-1.0$	V
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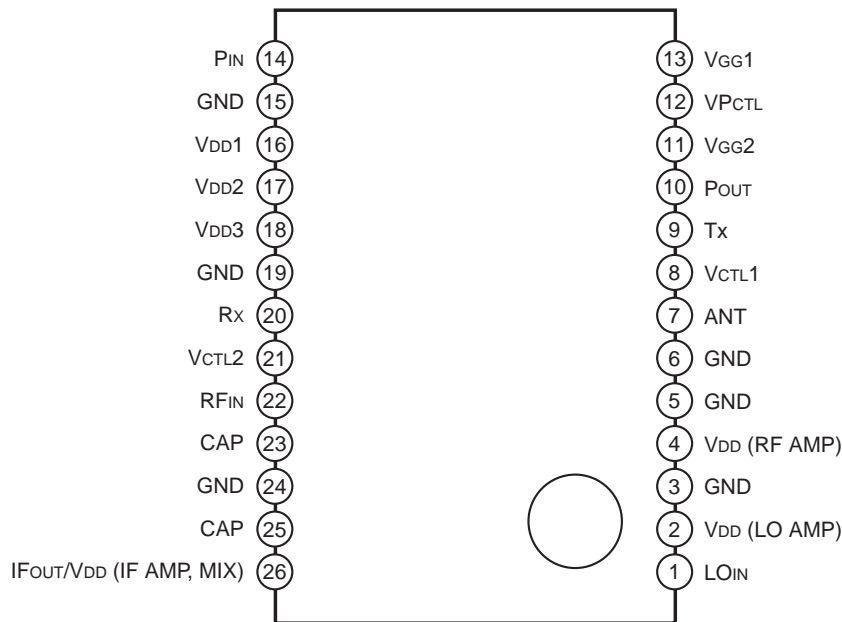
<Switch block>

• Control voltage (H)	$V_{CTL}(H)$	2.9 to 3.3	V
• Control voltage (L)	$V_{CTL}(L)$	0 to 0.2	V

Block Diagram and External Circuit



Pin Configuration



26 pin – HSOF (Plastic)

Pin Description

Pin No.	Symbol	Description
1	LO _{IN}	LO signal input.
2	V _{DD} (LO AMP)	LO AMP V _{DD} .
3	GND	GND.
4	V _{DD} (RF AMP)	RF AMP V _{DD} .
5	GND	GND.
6	GND	GND.
7	ANT	Antenna switch. Either ANT-Tx or ANT-Rx is depending on whether the setting is VCTL1 or VCTL 2.
8	VCTL1	Antenna switch control Pin 1.
9	T _X	T _X . Input the signal into the antenna switch when ANT-Tx.
10	P _{OUT}	Power amplifier output.
11	V _{GG2}	Power amplifier (the final-stage FET) gate voltage adjustment Pin 2.
12	V _{PCTL}	The first-stage FET control pin for the power amplifier.
13	V _{GG1}	Power amplifier (the first-stage FET, the second-stage FET) gate voltage adjustment Pin 1.
14	P _{IN}	Signal input into the power amplifier.
15	GND	GND.
16	V _{DD1}	Power amplifier (the first-stage FET) V _{DD1} .
17	V _{DD2}	Power amplifier (the second-stage FET) V _{DD2} .
18	V _{DD3}	Power amplifier (the final-stage FET) V _{DD3} .
19	GND	GND.
20	R _X	R _X . Output ANT input signal into Rx when ANT-Rx.
21	VCTL2	Antenna switch control Pin 2.
22	R _{FIN}	RF signal input.
23	CAP	Connector for the external capacitor. Connected to LNA FET source. Self-vibration frequency becomes 1.9GHz by this capacitor (Typ. 13pF).
24	GND	GND.
25	CAP	Connector for the external capacitor. IF AMP distortion is corrected by this capacitor.
26	IF _{OUT} /V _{DD} (IF AMP, MIX)	IF output and IF AMP, MIX V _{DD} .

Electrical Characteristics

1. Control Pin Logic for Antenna Switch

Conditions of control pins	ANT – Tx	ANT – Rx
$V_{CTL1} = 3V, V_{CTL2} = 0V$	ON	OFF
$V_{CTL1} = 0V, V_{CTL2} = 3V$	OFF	ON

2. Power Amplifier Block + Antenna Switch Transmitter Block

These specifications are those when the Sony's recommended evaluation board, shown on page 7, is used.

Unless otherwise specified: $V_{DD} = 3V, V_{PCTL} = 2V, V_{CTL1} = 3V, V_{CTL2} = 0V,$

$I_{DD} = 150mA, P_{OUT} = 20.2dBm, f = 1.9GHz, T_a = 25^{\circ}C$

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}			150		mA
Gate voltage adjustment value	V_{GG}		0.04	0.25	0.60	V
Output power	P_{OUT}	Measured with the ANT pin	20.2			dBm
Power gain	G_P		36	39		dB
Adjacent channel leak power ratio (600 ± 100kHz)	ACPR600kHz	Measured with the ANT pin		-63	-55	dBc
Adjacent channel leak power ratio (900 ± 100kHz)	ACPR900kHz	Measured with the ANT pin		-70	-60	dBc
Occupied bandwidth	OBW	Measured with the ANT pin		250	275	kHz
2nd-order harmonic level	—	Measured with the ANT pin			-25	dBc
3rd-order harmonic level	—	Measured with the ANT pin			-25	dBc

3. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer Block

These specifications are those when the Sony's recommended evaluation board, shown on page 7, is used.

Unless otherwise specified: $V_{DD} = 3V, V_{CTL1} = 0V, V_{CTL2} = 3V, RF1 = 1.90GHz/-35dBm,$

$LO = 1.66GHz/-15dBm, T_a = 25^{\circ}C$

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}	When no signal		5.5	7.5	mA
Conversion gain	G_C	When a small signal	17	20.5		dB
Noise figure	NF	When a small signal		4.2	5.5	dB
Input IP3	IIP3	*1	-17.5	-13		dBm
Image suppression ratio	IMR	$RF2 = 1.42GHz/-35dBm$	30	40		dBc
1/2 IF suppression ratio	1/2IFR	$RF2 = 1.78GHz/-35dBm$	39	44		dBc
2 × LO-IF suppression ratio	—	$RF2 = 3.08GHz/-35dBm$	39	47		dBc
2 × LO+IF suppression ratio	—	$RF2 = 3.56GHz/-35dBm$	24	62		dBc
LO to ANT leak	P_{LK}			-42	-37	dBm

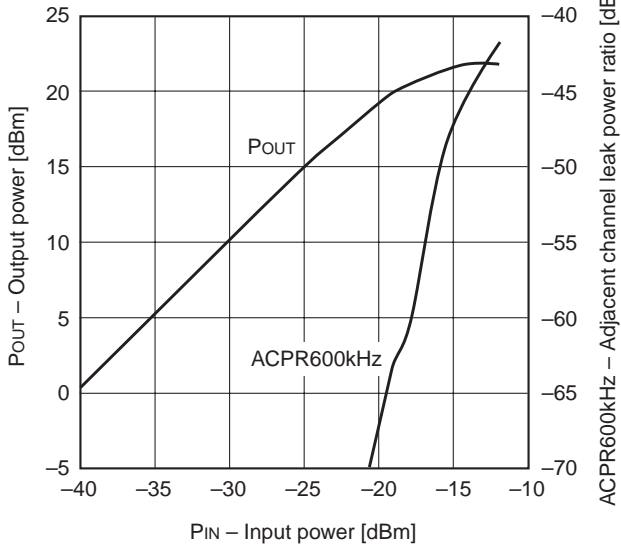
*1 Conversion from IM3 suppression ratio during $FR1 = 1.9000GHz/-35dBm$ and $FR2 = 1.9006GHz/-35dBm$ input.

Example of Representative Characteristics

1. Power Amplifier + Antenna Switch Transmitter Block (f = 1.9GHz, Ta = 25°C)

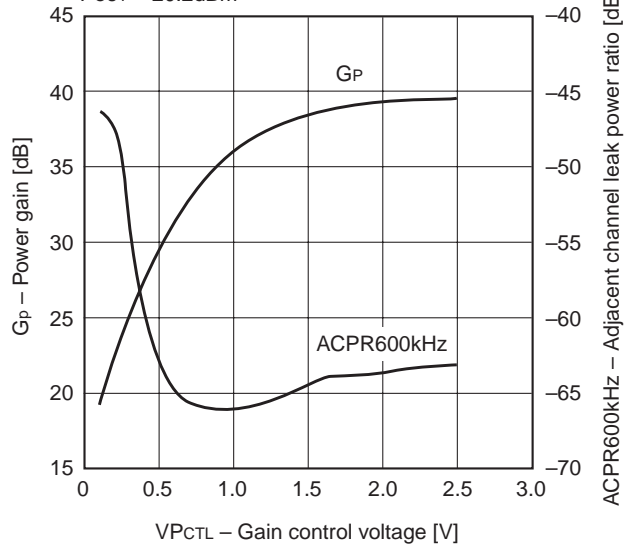
P_{OUT}, ACPR600kHz vs. P_{IN}

V_{DD} = 3V, V_{PCTL} = 2V, V_{GG} = const., V_{CTL1} = 3V,
V_{CTL2} = 0V
I_{DD} = 150mA (@P_{OUT} = 20.2dBm), P_{IN} = var.



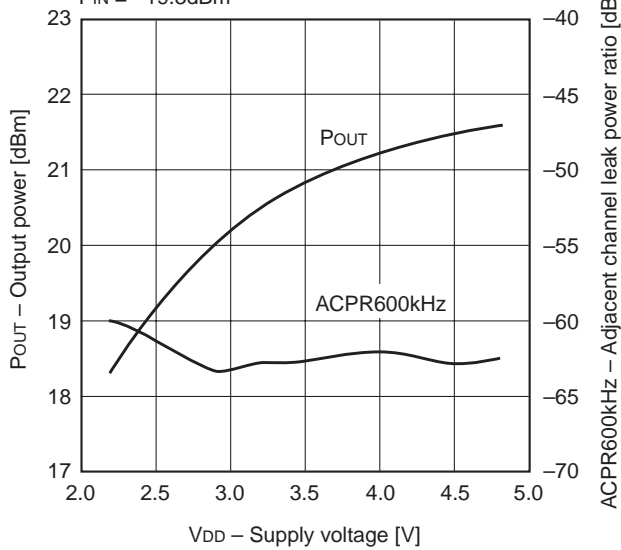
G_p, ACPR600kHz vs. V_{PCTL}

V_{DD} = 3V, V_{PCTL} = var., V_{GG} = const., V_{CTL1} = 3V,
V_{CTL2} = 0V
I_{DD} = 150mA (@V_{PCTL} = 2V), P_{IN} = var.,
P_{OUT} = 20.2dBm



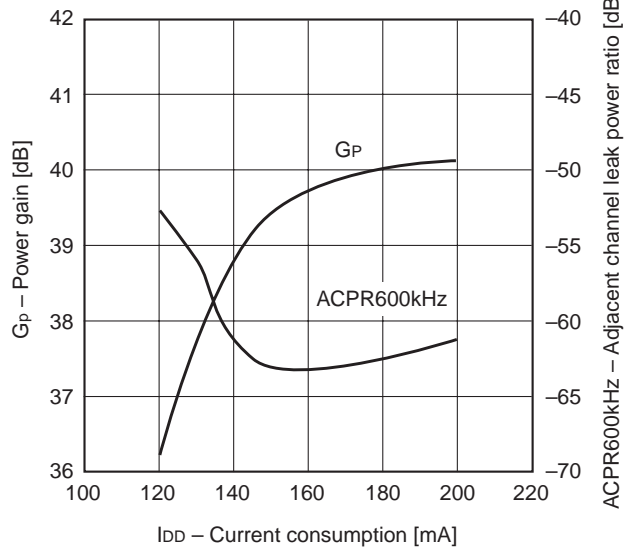
P_{OUT}, ACPR600kHz vs. V_{DD}

V_{DD} = var., V_{PCTL} = 2V, V_{GG} = const., V_{CTL1} = 3V,
V_{CTL2} = 0V
I_{DD} = 150mA (@V_{DD} = 3V, P_{OUT} = 20.2dBm),
P_{IN} = -19.3dBm



G_p, ACPR600kHz vs. I_{DD}

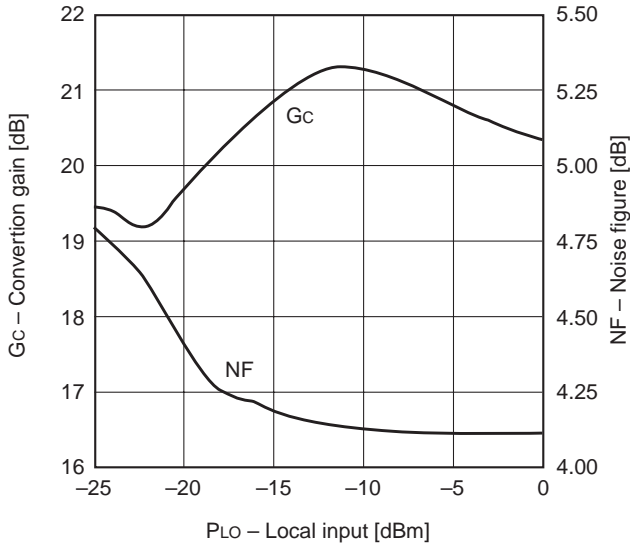
V_{DD} = 3V, V_{PCTL} = 2V, V_{GG} = var., V_{CTL1} = 3V,
V_{CTL2} = 0V
I_{DD} = var., P_{IN} = var., P_{OUT} = 20.2dBm



2. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer (Ta = 25°C)

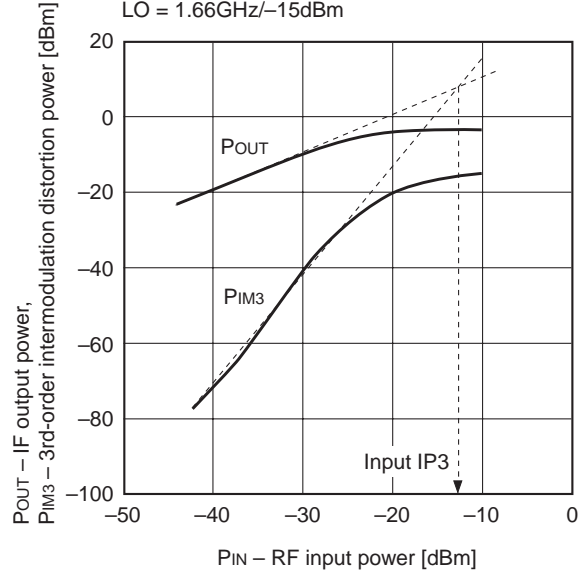
Gc, NF vs. PLO

VDD = 3V, VCTL1 = 0V, VCTL2 = 3V,
RF = 1.90GHz/small signal, LO = 1.66GHz



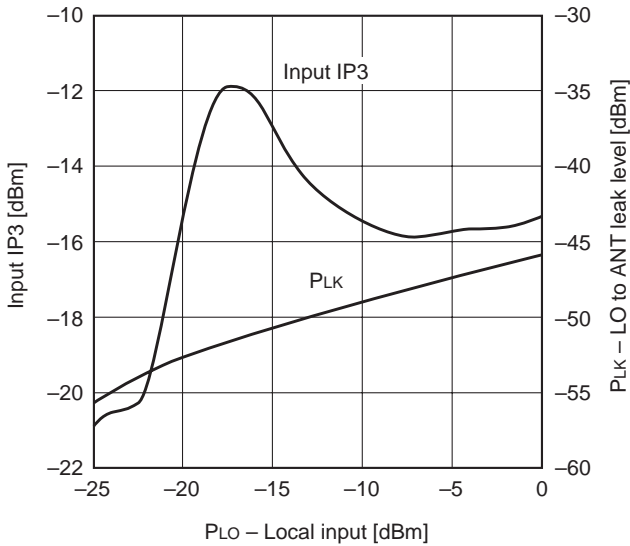
POUT, PIM3 vs. PIN

VDD = 3V, VCTL1 = 0V, VCTL2 = 3V,
RF1 = 1.9000GHz, RF2 = 1.9006GHz,
LO = 1.66GHz/-15dBm

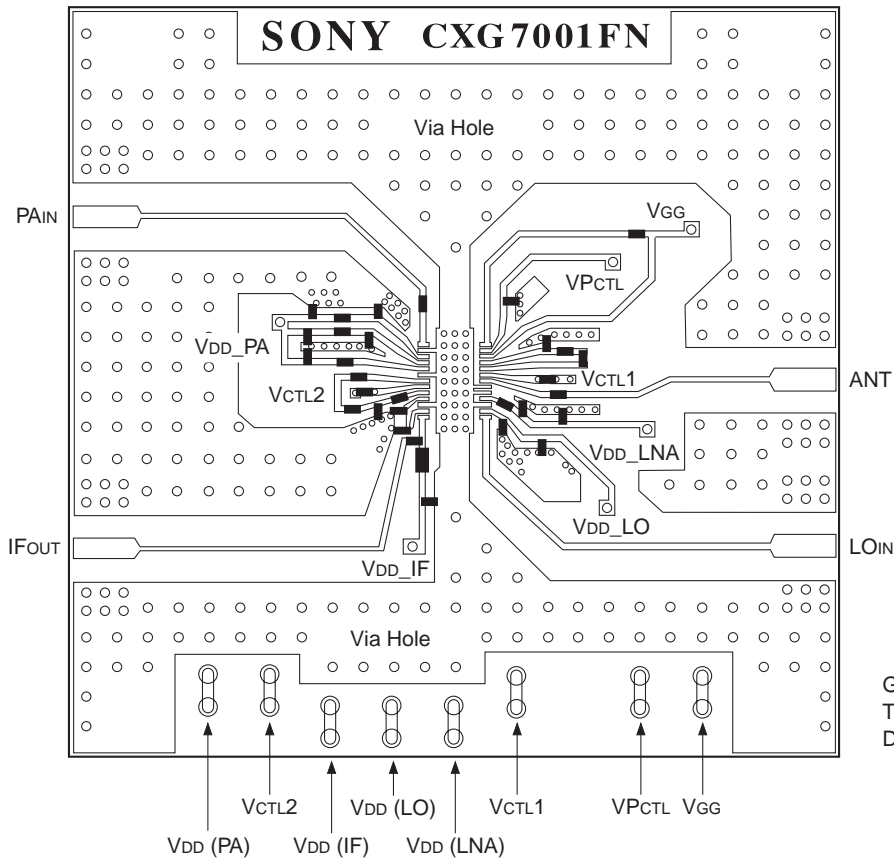


Input IP3, PLK vs. PLO

VDD = 3V, VCTL1 = 0V, VCTL2 = 3V,
RF = 1.90GHz/-35dBm, LO = 1.66GHz

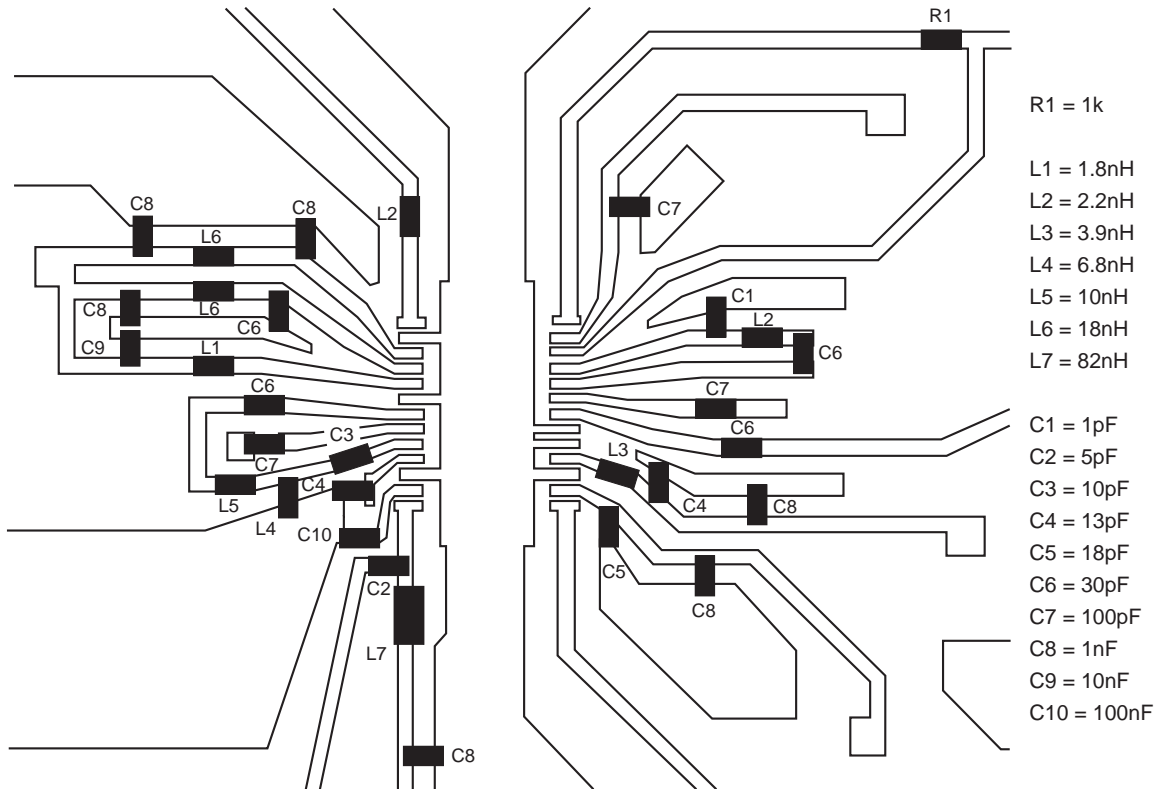


Recommended Evaluation Board



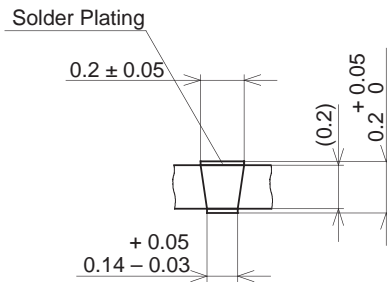
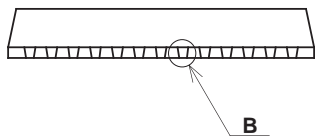
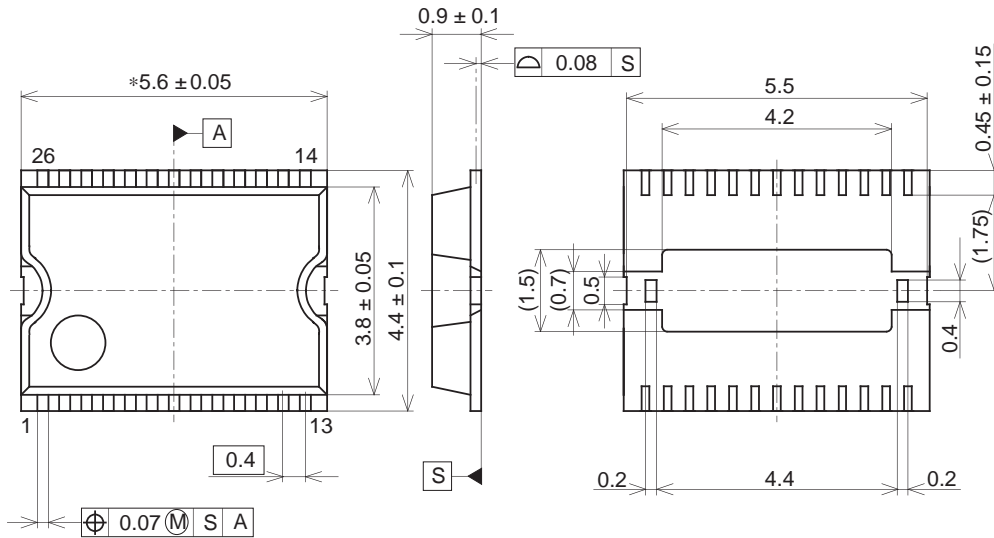
Glass fabric-base epoxy board (4 layers)
 Thickness between 1 and 2: 0.2mm
 Dimensions: 50mm × 50mm

Enlarged Diagram of External Circuit Block



Package Outline Unit: mm

HSOF 26PIN (PLASTIC)



DETAIL B

NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

SONY CODE	HSOF-26P-01
EIAJ CODE	_____
JEDEC CODE	_____

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm