SONY

CXD2540Q-2

CD Digital Signal Processor

Description

The CXD2540Q-2 is a digital signal processor LSI for CD players and is equipped with the following functions.

- Playback mode supporting CAV (Constant Angular Velocity)
  - Frame jitter-free
  - Low external clock allowing 0.5 to octuple-speed continuous playback
  - Allows relative rotational velocity readout
  - Supports external spindle control
- Wide capture range playback mode
  - Spindle rotational velocity following method
  - Supports normal-speed, double-speed and quadruple-speed playback
  - High-speed fine search which performs high-precision track jumps
- Wide frame jitter margin (±28 frames) due to a built-in 32K RAM
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error detection
  C1: double correction, C2: quadruple correction
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub Q data error correction
- Digital spindle servo (built-in oversampling filter)
- Asymmetry compensation circuit
- Error correction monitor signals are output from a new CPU interface.
- Servo auto sequencer
- Digital level meter, peak meter
- Bilingual compatible

Features

- Processes all digital signals for playback with this LSI alone
- High-integrated mounting possible due to a built-in RAM

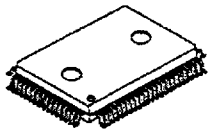
Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_I	−0.3 to +7.0	V
		(V_{SS}−0.3V to V_{DD}+0.3V)	
• Output voltage	V_O	−0.3 to +7.0	V
• Storage temperature	Tstg	−40 to +125	°C
• Supply voltage difference			
	V_{SS}—AV_{SS}	−0.3 to +0.3	V
	V_{DD}—AV_{DD}	−0.3 to +0.3	V

80 pin QFP (Plastic)



Recommended Operating Conditions

• Supply voltage	V_{DD}*	4.75 to 5.25	V
• Operating temperature	Topr	−20 to +75	°C

* The V_{DD} (min.) for the CXD2540Q varies according to the playback speed and built-in VCO1 selection.

Playback speed	V_{DD} (min.) [V]	
	VCO1 high-speed	VCO1 normal-speed
x 8	4.75	—
x 6	4.50	—
x 4	4.50	—
x 2*1	4.00	—
x 2	3.40	4.00
x 1	3.40	3.40
x 1*2	3.40	3.40

*1 When this LSI is set to normal-speed playback mode internally and the operating clock of this LSI is doubled, double-speed playback results.

*2 When this LSI is set to double-speed playback mode internally and the operating clock of this LSI is halved, normal-speed playback results. (Low power consumption mode)

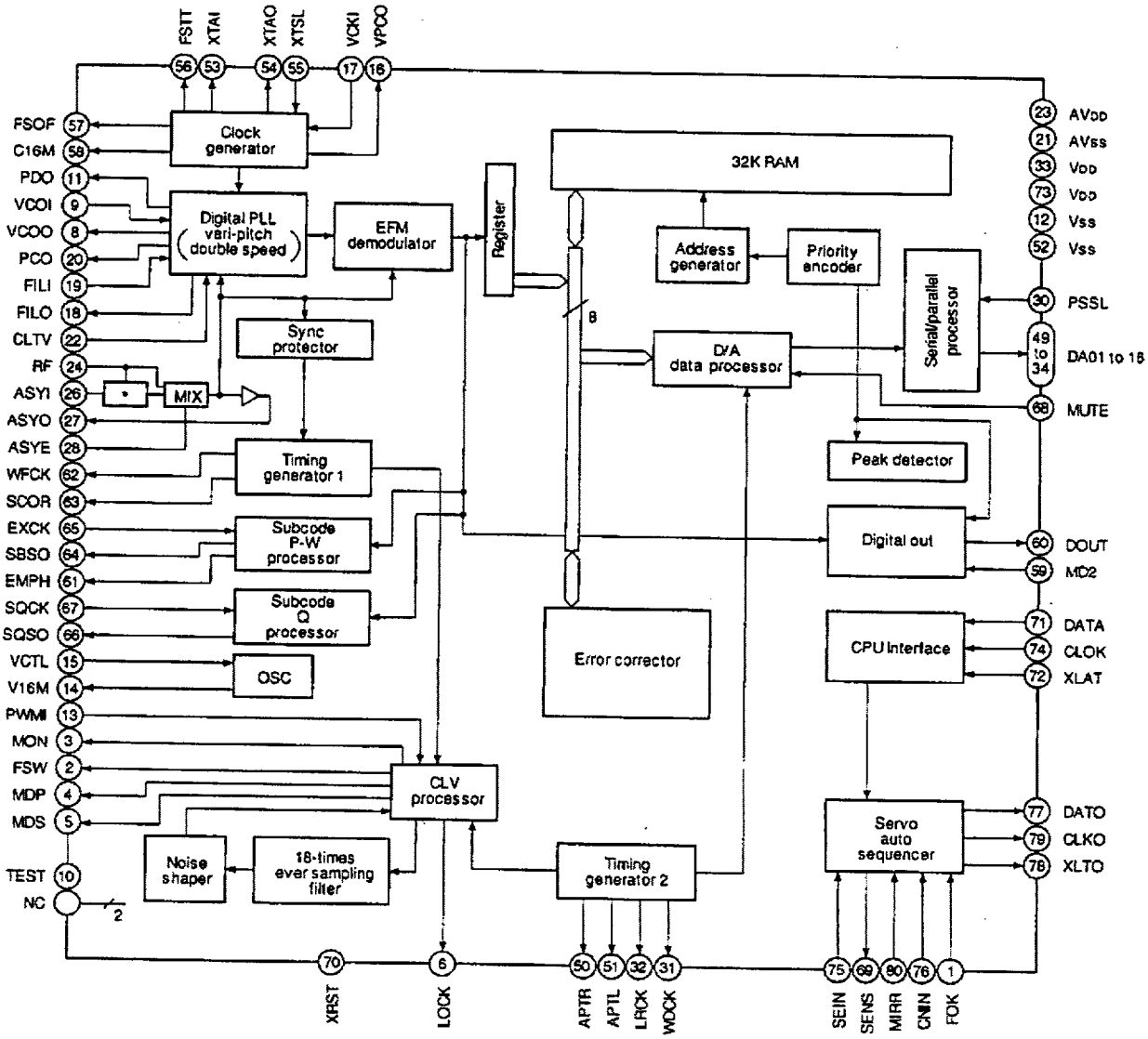
Input/output Capacitances*

• Input capacitance	C_I	12 (max.)	pF
• Output capacitance	C_O	12 (max.)	pF

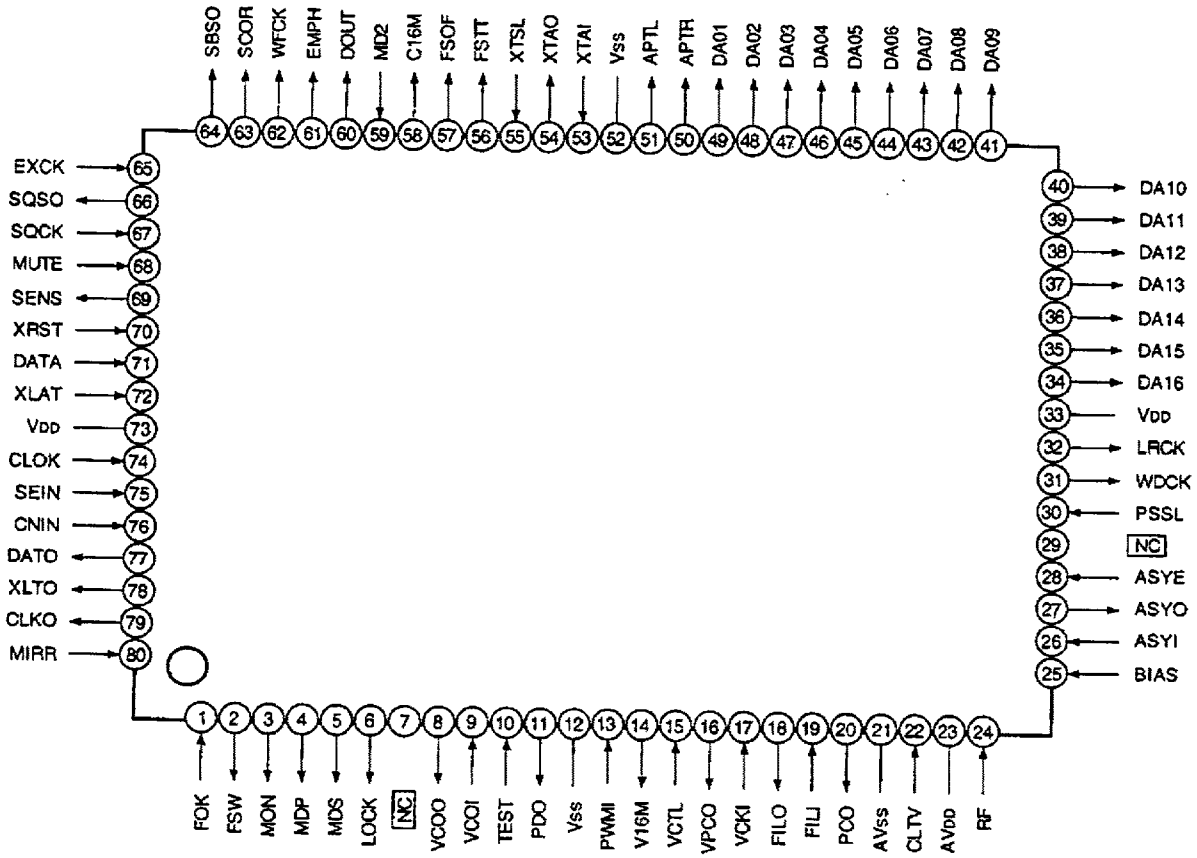
* Measurement conditions $V_{DD} = V_I = 0V$, $f_M = 1MHz$

E96129—ST

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
1	FOK	I		Focus OK input. Used for SENS output and the servo auto sequencer.
2	FSW	O	Z, 0	Spindle motor output filter switching output.
3	MON	O	1, 0	Spindle motor on/off control output.
4	MDP	O	1, Z, 0	Spindle motor servo control.
5	MDS	O	1, Z, 0	Spindle motor servo control.
6	LOCK	O	1, 0	High, when sampled value of GFS at 460Hz is high. Low, when sampled value of GFS at 460Hz is low by 8 times succesively.
7	NC			
8	VCOO	O	1, 0	Analog EFM PLL oscillation circuit output.
9	VCOI	I		Analog EFM PLL oscillation circuit input. fLOCK = 8.6436MHz.
10	TEST	I		TEST pin.
11	PDO	O	1, Z, 0	Analog EFM PLL charge pump output.
12	Vss			GND
13	PWMI	I		Spindle motor external control input.
14	V16M	O	1, 0	VCO2 oscillation output for the wide-band EFM PLL.
15	VCTL	I		VCO2 control voltage input for the wide-band EFM PLL.
16	VPCO	O	1, Z, 0	Wide-band EFM PLL charge pump output.
17	VCKI	I		VCO2 oscillation input for the wide-band EFM PLL.
18	FILO	O	Analog	Multiplier PLL (slave = digital PLL) filter output.
19	FILI	I		Multiplier PLL filter input.
20	PCO	O	1, Z, 0	Multiplier PLL charge pump output.
21	AVss			Analog GND.
22	CLTV	I		Multiplier VCO1 control voltage input.
23	AVDD			Analog power supply (5V).
24	RF	I		EFM signal input.
25	BIAS	I		Constant current input of the asymmetry circuit.
26	ASYI	I		Asymmetry comparator voltage input.
27	ASYO	O	1, 0	EFM full-swing output.
28	ASYE	I		Low: asymmetry circuit off; high: asymmetry circuit on
29	NC			
30	PSSL	I		Audio data output mode switching input. Low: serial output; high: parallel output.
31	WDCK	O	1, 0	D/A interface for 48-bit slot. Word clock f = 2Fs.
32	LRCK	O	1, 0	D/A interface for 48-bit slot. LR clock f = Fs.
33	VDD			Power supply (5V).

Pin No.	Symbol	I/O		Description
34	DA16	O	1, 0	DA16 (MSB) output when PSSL = 1. 48-bit slot serial data (two's complement, MSB first) when PSSL = 0.
35	DA15	O	1, 0	DA15 output when PSSL = 1. 48-bit slot bit clock when PSSL = 0.
36	DA14	O	1, 0	DA14 output when PSSL = 1. 64-bit slot serial data (two's complement, LSB first) when PSSL = 0.
37	DA13	O	1, 0	DA13 output when PSSL = 1. 64-bit slot bit clock when PSSL = 0.
38	DA12	O	1, 0	DA12 output when PSSL = 1. 64-bit slot LR clock when PSSL = 0.
39	DA11	O	1, 0	DA11 output when PSSL = 1. GTOP output when PSSL = 0.
40	DA10	O	1, 0	DA10 output when PSSL = 1. XUGF output when PSSL = 0.
41	DA09	O	1, 0	DA09 output when PSSL = 1. XPLCK output when PSSL = 0.
42	DA08	O	1, 0	DA08 output when PSSL = 1. GFS output when PSSL = 0.
43	DA07	O	1, 0	DA07 output when PSSL = 1. RFCK output when PSSL = 0.
44	DA06	O	1, 0	DA06 output when PSSL = 1. C2PO output when PSSL = 0.
45	DA05	O	1, 0	DA05 output when PSSL = 1. XRAOF output when PSSL = 0.
46	DA04	O	1, 0	DA04 output when PSSL = 1. MNT3 output when PSSL = 0.
47	DA03	O	1, 0	DA03 output when PSSL = 1. MNT2 output when PSSL = 0.
48	DA02	O	1, 0	DA02 output when PSSL = 1. MNT1 output when PSSL = 0.
49	DA01	O	1, 0	DA01 output when PSSL = 1. MNT0 output when PSSL = 0.
50	APTR	O	1, 0	Aperture compensation control output. This pin outputs a high signal when the right channel is used.
51	APTL	O	1, 0	Aperture compensation control output. This pin outputs a high signal when the left channel is used.
52	Vss			GND
53	XTAI	I		Crystal oscillation circuit input.
54	XTAO	O	1, 0	Crystal oscillation circuit output.
55	XTSL	I		Crystal selector input.
56	FSTT	O	1, 0	2/3 frequency divider output for Pins 53 and 54.
57	FSOF	O	1, 0	1/4 frequency divider output for Pins 53 and 54.
58	C16M	O	1, 0	16.9344MHz output. (V16M output in CLV-W and CAV-W modes)
59	MD2	I		Digital-out on/off control. High: on; low: off
60	DOUT	O	1, 0	Digital-out output.
61	EMPH	I		Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
62	WFCK	I		WFCK (write frame clock) output.
63	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
64	SBSO	O	1, 0	Sub P to W serial output.
65	EXCK	I		SBSO readout clock input.
66	SQSO	O	1, 0	Sub Q 80-bit and PCM peak, level metter and internal status outputs.
67	SQCK	I		SQSO readout clock input.

Pin No.	Symbol	I/O		Description
68	MUTE	I	1, Z, 0	High: mute; low: release
69	SENS	—		SENS output to CPU.
70	XRST	I		System reset. Reset when low.
71	DATA	O	1, 0	Serial data input from CPU.
72	XLAT	O	1, 0	Latch input from CPU. Serial data is latched at the falling edge.
73	V_{DD}			Power supply (5V).
74	CLOK	O	1, 0	Serial data transfer clock input from CPU.
75	SEIN	I	1, 0	SENS input from SSP.
76	CNIN	I	1, 0	Track jump count signal input.
77	DATO	O	1, 0	Serial data output to SSP.
78	XLTO	O	1, 0	Serial data latch output to SSP. Latched at the falling edge.
79	CLKO	O	1, 0	Serial data transfer clock output to SSP.
80	MIRR	I	1, 0	Mirror signal input. Used when the number of tracks is 128 or more for the 2N-track jump and M track move of the auto sequencer.

Notes)

- The 64-bit slot is an LSB first, two's complement output, and the 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136μ.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

Electrical Characteristics

DC Characteristics

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = −1mA	V_{DD}−0.5		V_{DD}	V	*4
	Low level output voltage	V_{OL} (1)	I_{OL} = 1mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = −1mA	V_{DD}−0.5		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 2mA	0		0.4	V	
Output voltage (3)	Low level output voltage	V_{OL} (3)	I_{OL} = 0.2mA	0		0.4	V	*6
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = −0.28mA	V_{DD}−0.5		V_{DD}	V	*7
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Input leak current		I_{LI}	V_I = 0 to 5.50V	−5		5	μA	*1, 2, 3
Tri-state pin output leak current		I_{LO}	V_O = 0 to 5.50V	−5		5	μA	*8

Applicable pins

*1 XTSL, DATA, XLAT, MD2, PSSL, PWM1

*2 CLOK, XRST, EXCK, SQCK, MUTE, FOK, SEIN, CNIN, MIRR, VCKI, ASYE

*3 CLTV, FILI, RF, VCTL

*4 MDP, PDO, PCO, VPCO

*5 ASYO, DOUT, FSTT, FSOF, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO, CLKO, XLTO, SENS, MDS, DA01 to DA16, APTR, APTL, LRCK, WFCK, V16M

*6 FSW

*7 FILO

*8 SENS, MDS, MDP, FSW, PDO, PCO, VPCO

AC Characteristics

1. XTAI pin, VCOI pin

(1) When using self-oscillation

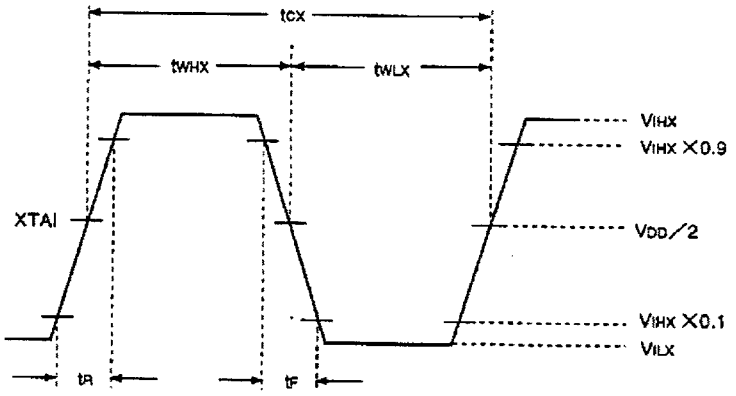
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(2) When inputting pulses to XTAI and VCOI

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 10%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1,000	ns
Input high level	V_{IHX}	V_{DD}–1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(3) When inputting sine waves to XTAI and VCOI pins via a capacitor

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 10%)

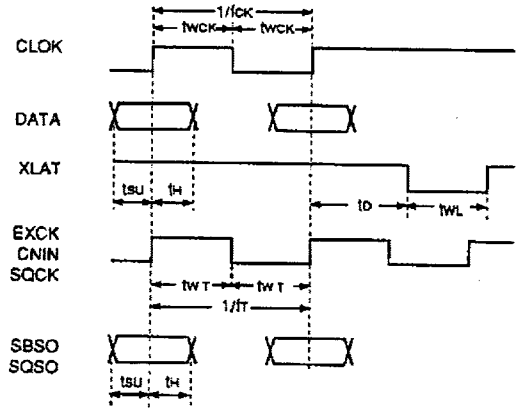
Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

2. CLOK, DATA, XLAT, CNIN, SQCK EXCK pins

(V_{DD} = AV_{DD} = 5.0V ± 10%, Vss = AVss = 0V, Topr = −20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65	MHz
EXCK SQCK pulse width	t_{WT}	750			ns
CNIN freqency *	f_T			65	kHz
CNIN pulse width *	t_{WT}	7.5			µs

* When $44 and $45 are excuted.



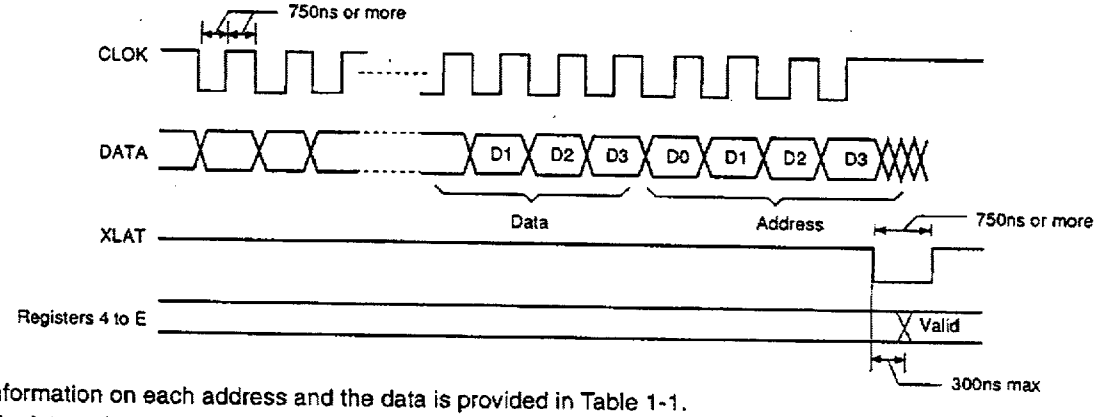
Description of Functions

§1. CPU Interface and Instructions

• CPU interface

This interface uses DATA, CLOK, and XLAT to set the modes.

The interface timing chart is shown below.



• Information on each address and the data is provided in Table 1-1.

• The internal registers are initialized by a reset when XRST = 0; the initialization data is shown in Table 1-2.

Command Table

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	–	–	–	–	–	–	–
5	Blind (A, E), Overflow (C, G)	0	1	0	1	0.18ms	0.09ms	0.05ms	0.02ms	–	–	–	–	–	–	–	–	–	–	–	–
	Brake (B)					0.36ms	0.18ms	0.09ms	0.05ms												
6	Sled_kick, Brake (D) Kick (F)	0	1	1	0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	–	–	–	–	–	–	–	–
7	Auto sequence (N) track jump count setting	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0	–	–	–	–
9	Function specification	1	0	0	1	DCLV ON/OFF	DSPB ON/OFF	ASEQ ON/OFF	DPLL ON/OFF	BiliGL MAIN	BiliGL SUB	FLFC	0	–	–	–	–	–	–	–	–
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	PCT1	PCT2	0	0	–	–	–	–	–	–	–	–
B	Traverse monitor counter setting	1	0	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
C	Servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	0	0	–	–	–	–	–	–	–	–
D	CLV CTRL	1	1	0	1	DCLV PWM mod	TB	TP	CLVS Gain	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	–	–	–	–
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	–	–	–	–

Table 1-1.

Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C, G) Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	Sled_kick, Brake (D) Kick (F)	0	1	1	0	0	1	1	1	0	0	0	0	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	—	—	—	—
9	Function specification	1	0	0	1	1	0	0	1	0	0	0	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Servo coefficient setting	1	1	0	0	0	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—

Table 1-2.

The meaning of the data for each address is explained below.

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
Fine Search	0	1	0	RXF
Focus-On	0	1	1	1
1 Track Jump	1	0	0	RXF
10 Track Jump	1	0	1	RXF
2N Track Jump	1	1	0	RXF
M Track Move	1	1	1	RXF

RXF = 0 Forward
RXF = 1 Reverse

- When the FOCUS-ON command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the TRACK JUMP commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

Max. timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

- To disable the MAX timer, set the MAX timer value to 0.
- The timer value is doubled when DSPB = high, in any operation modes.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

- The timer value is doubled when DSPB = high, in any operation modes.

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

• The timer value is doubled when DSPB = high, in any operation modes.

$7X commands

Auto sequence track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is to set N when a 2N track jump is executed, to set M when an M track move is executed and to set the jump count when fine search is executed for auto sequence.

• The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.

• When the track jump count is from 0 to 15, the CNIN signal is used to count tracks for 2N-track jump/M track move; when the count is 16 or over, the MIRR signal is used. For fine search, the CNIN signal is used to count tracks.

$8X commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0

Command bit	C2PO timing	Processing
CDROM = 1	See the Timing Chart 1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See the Timing Chart 1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital out is either on or off.

MD2	Other mute conditions*	DOUT Mute	D.out Mute F	DOUT output	DA output
0	0	0	0	off	0dB
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		−∞dB
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	0dB	0dB
1	0	0	1		−∞dB
1	0	1	0	−∞dB	0dB
1	0	1	1		−∞dB
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

* See mute conditions (1), (2), and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

Command bit	Function	Use
ASHS = 0	The command transfer rate to SSP is set to normal-speed.	Used for normal-speed and double-speed playback (double correction).
ASHS = 1	The command transfer rate to SSP is set to half-speed.	Used for quadruple-speed and double-speed playback (quadruple correction).

Command bit	Function
SOCT = 0	Sub Q is output from the SQSO pin.
SOCT = 1	Each output signal is output from the SQSO pin. Input the readout clock to SQCK. (See the Timing Chart 2-4.)

Command bit			Processing
VCOSEL1	KSL3	KSL2	
0	0	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Multiplier PLL VCO1 is set to high speed*, and the output is 1/1 frequency-divided.
1	0	1	Multiplier PLL VCO1 is set to high speed*, and the output is 1/2 frequency-divided.
1	1	0	Multiplier PLL VCO1 is set to high speed*, and the output is 1/4 frequency-divided.
1	1	1	Multiplier PLL VCO1 is set to high speed*, and the output is 1/8 frequency-divided.

* Approximately twice the normal speed

Command bit			Processing
VCOSEL2	KSL1	KSL0	
0	0	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/3 frequency-divided.
0	1	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/4 frequency-divided.
1	0	0	Wide-band PLL VCO2 is set to high speed*, and the output is 1/1 frequency-divided.
1	0	1	Wide-band PLL VCO2 is set to high speed*, and the output is 1/2 frequency-divided.
1	1	0	Wide-band PLL VCO2 is set to high speed*, and the output is 1/3 frequency-divided.
1	1	1	Wide-band PLL VCO2 is set to high speed*, and the output is 1/4 frequency-divided.

* Approximately twice the normal speed

$9X commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Function specifications	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	0

Command bit	CLV mode	Contents	
DCLV on/off = 0	During CLVS mode	FSW = low, MON = high, MDS = Z; MDP = servo control signal, carrier frequency of 230Hz at T_B = 0, and 460Hz at T_B = 1.	
	During CLVP mode	FSW = Z, MON = high; MDS = speed control signal, carrier frequency of 7.35kHz; MDP = phase control signal, carrier frequency of 1.8kHz.	
DCLV on/off = 1 (FSW, MON not required)	During CLVS and CLVP modes	When DCLV PWM and MD = 1 (Prohibited in CLV-W and CAV-W modes)	MDS = PWM polarity signal, carrier frequency of 132kHz. MDP = PWM absolute value output (binary), carrier frequency of 132kHz.
		When DCLV PWM and MD = 0	MDS = Z MDP = ternary PWM output, carrier frequency of 132kHz.

When DCLV on/off = 1 for the Digital CLV servo, the sampling frequency of the internal digital filter switches simultaneously with the CLVP/CLVS switching.
Therefore, the cut-off frequency for the CLVS is fc = 70Hz when T_B = 0, and fc = 140Hz when T_B = 1.

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error correction quadruple correction.
DSPB = 1	Double-speed playback, C2 error correction double correction.

FLFC is normally 0.
FLFC is 1 for CAV-W mode, in any playback speed.

SENS output

Microcomputer serial register value (latching not required)	ASEQ = 0	ASEQ = 1
$0X	Z	SEIN (FZC)
$1X	Z	SEIN (A.S)
$2X	Z	SEIN (T.Z.C)
$3X	Z	SEIN (SSTOP)
$4X	Z	XBUSY
$5X	Z	FOK
$6X	Z	SEIN (Z)
$AX	GFS	GFS
$BX	COMP	COMP
$CX	COUT	COUT
$EX	$\overline{OV64}$	$\overline{OV64}$
$7X, 8X, 9X, DX, FX	Z	0

Description of SENS signals

SENS output	Meaning
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the played back frame sync is obtained with the correct timing.
COMP	Measures the number of tracks set with Reg B. High when Reg B is latched, low when the initial Reg B number is input by CNIN.
COUT	Measures the number of tracks set with Reg B. High when Reg B is latched, toggles each time the Reg B number is input by CNIN. While $44 and $45 are being executed, toggles with each CNIN 8-count instead of the Reg B number.
$\overline{OV64}$	Low when the EFM signal, after passing through the sync detection filter, is lengthened by 64 channel clock pulses or more.

Command bit	Meaning
DPLL = 0*	RFPLL is analog. PDO, VCOI and VCOO are used.
DPLL = 1	RFPLL is digital. PDO is impedance.

* External parts for Pins 18 to 20 are required even when analog PLL is selected.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO:

The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

$AX commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Audio CTRL	0	0	Mute	ATT	PCT1	PCT2	0	0

Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off.
ATT = 1	–12dB

Mute conditions

(1) When register A mute = 1.
(2) When MUTE pin = 1.
(3) When register 8 D.out mute = 1 and the Digital out is on (MD2 pin = 1).
(4) When GFS stays low for over 35ms (at normal speed).
(5) When register 9 BiliGL MAIN = Sub = 1.
(6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1ms time limit.

Command bit		Meaning	PCM Gain	ECC correction ability
PCT1	PCT2			
0	0	Normal mode	×0dB	C1: double; C2: quadruple
0	1	Level meter mode	×0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	×0dB	C1: double; C2: double

Description of level meter mode (see the Timing Chart 1-4.)

- When this LSI is set to this mode, it can possess digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits of data are Sub Q data (see §2. Subcode Interface). The last 16 bits are LSB first 15-bit PCM data (absolute values). The final bit is L/R flag, it is high when the PCM data is generated by the left channel and low when generated by the right channel.
- PCM data is reset to zero and the L/R flag is reversed after one readout.
  The maximum value for this status is then measured until the next readout.

Description of peak meter mode (see the Timing Chart 1-5.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the LSI internal register is set the value again.
  In other words, the PCM maximum value detection register is not reset to zero by the readout.
- To reset the PCM maximum value register to zero, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Relative time operates as normal.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level (−∞) for this mode.

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set when the traverse status is monitored by the SENS output COMP and COUT.

$CX commands

Command	Data 1				Data 2				Explanation
	D3	D2	D1	D0	D3	D2	D1	D0	
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	0	0	Valid only when DCLV = 1.
CLV CTRL ($DX)				Gain CLVS					Valid when DCLV = 1 or 0.

The spindle servo gain is externally set when DCLV = 1.

- CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	−12dB
0	0	1	−6dB
0	1	0	−6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note) When DCLV = 0, the CLVS gain is as follows.
When Gain CLVS = 0, GCLVS = −12dB.
When Gain CLVS = 1, GCLVS = 0dB.

• CLVP mode gain setting: GMDP: GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV1	Gain DCLV0	GDCLV
0	0	0dB
0	1	+6dB
1	0	+12dB

$DX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	Gain CLVS	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0

└— See the $CX commands

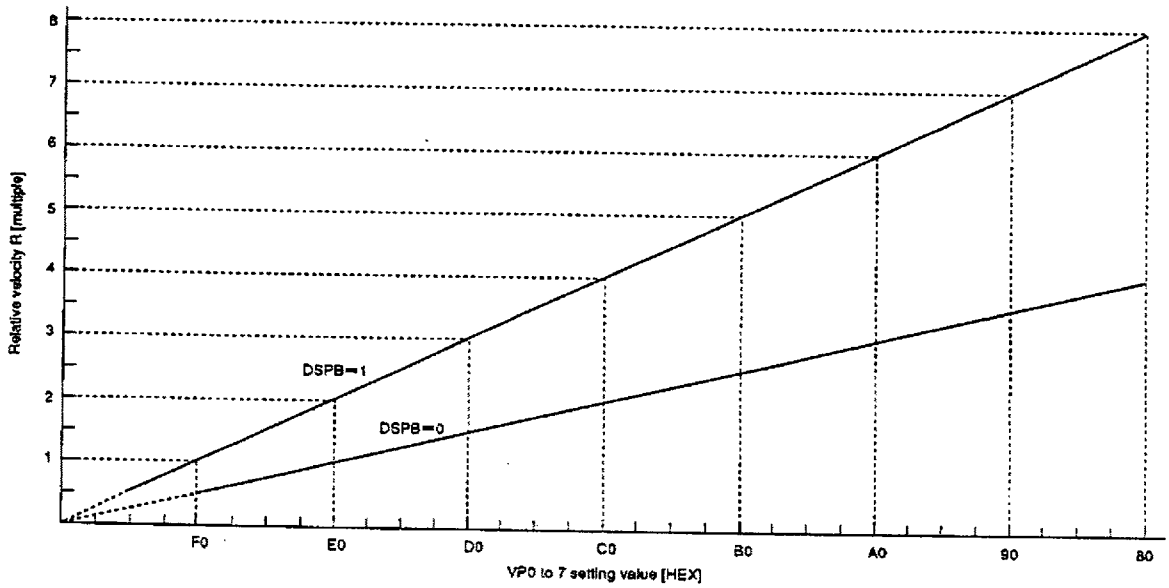
Command bit	Explanation
DCLV PWM MD = 1	Digital CLV PWM mode specified. Both MDS and MDP are used. CLV-W and CAV-W modes can not be used.
DCLV PWM MD = 0	Digital CLV PWM mode specified. Ternary MDP values are output. CLV-W and CAV-W modes can be used.

Command bit	Explanation
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS and CLVH modes.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS and CLVH modes.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

Command bit	Description
VP0 to 7 = F0 (H)	Playback at normal (double) speed
⋮	to
VP0 to 7 = E0 (H)	Playback at normal (double) speed
⋮	to
VP0 to 7 = C0 (H)	Playback at double (quadruple) speed
⋮	to
VP0 to 7 = A0 (H)	Playback at (sextuple) speed
⋮	to
VP0 to 7 = 80 (H)	Playback at (octuple) speed

Note)

1. Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTSL is high.
2. Values in parentheses are for when DSPB is 1.



$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Explanation
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.*
1	0	0	0	KICK	Spindle forward rotation mode.*
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR=0, in any modes.*
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

* See the Timing Charts 1-6 to 1-12.

Command bit								Mode	Explanation
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON		
0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	CLV-W	Used for playback in CLV-W mode.*
0	1	1	0	0	1	0	1	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	CAV-W	Spindle control with the external PWM.

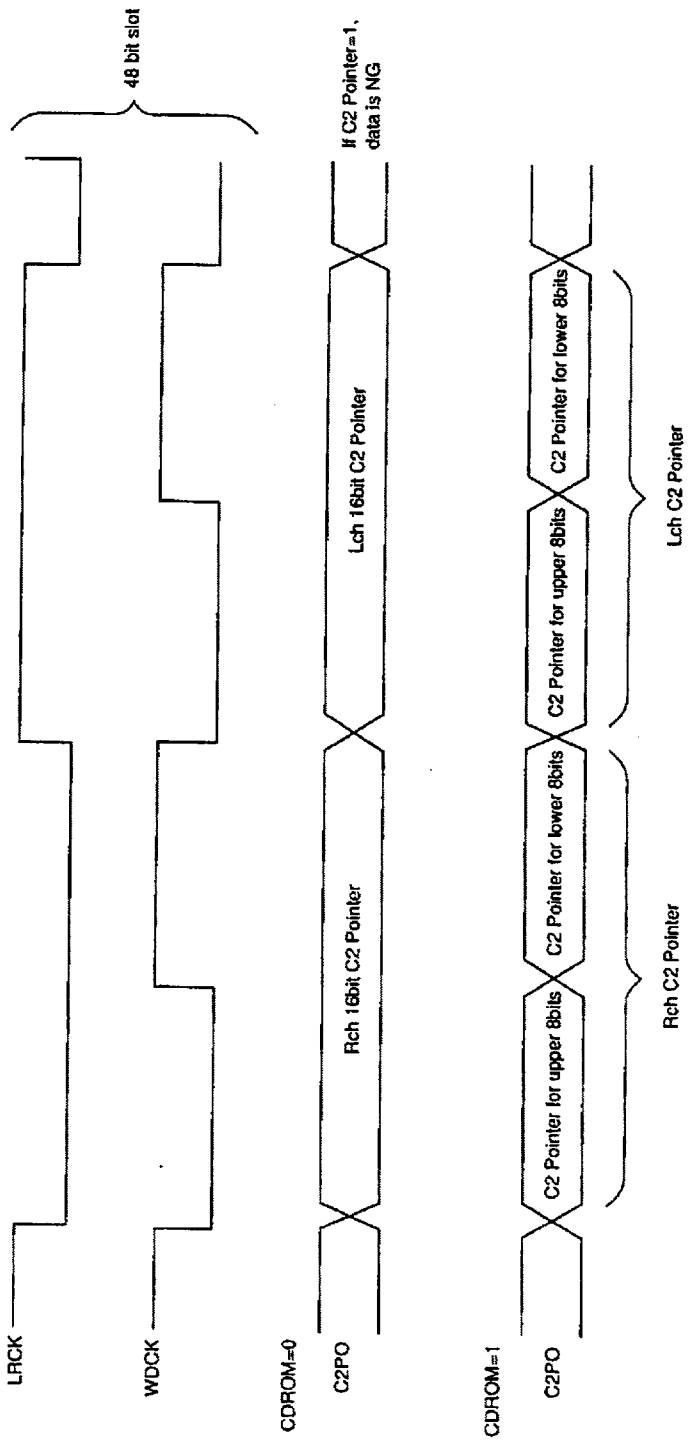
* Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

Mode	DCLV	DCLV PWM MD	LPWR	Command	Timing chart
CLV-N	0	0	0	KICK	1-6 (a)
				BRAKE	1-6 (b)
				STOP	1-6 (c)
	1	0	0	KICK	1-7 (a)
				BRAKE	1-7 (b)
				STOP	1-7 (c)
		1	0	KICK	1-8 (a)
				BRAKE	1-8 (b)
				STOP	1-8 (c)
CLV-W	1	0	0	KICK	1-9 (a)
				BRAKE	1-9 (b)
				STOP	1-9 (c)
			1	KICK	1-10 (a)
				BRAKE	1-10 (b)
				STOP	1-10 (c)
CAV-W	1	0	0	KICK	1-11 (a)
				BRAKE	1-11 (b)
				STOP	1-11 (c)
			1	KICK	1-12 (a)
				BRAKE	1-12 (b)
				STOP	1-12 (c)

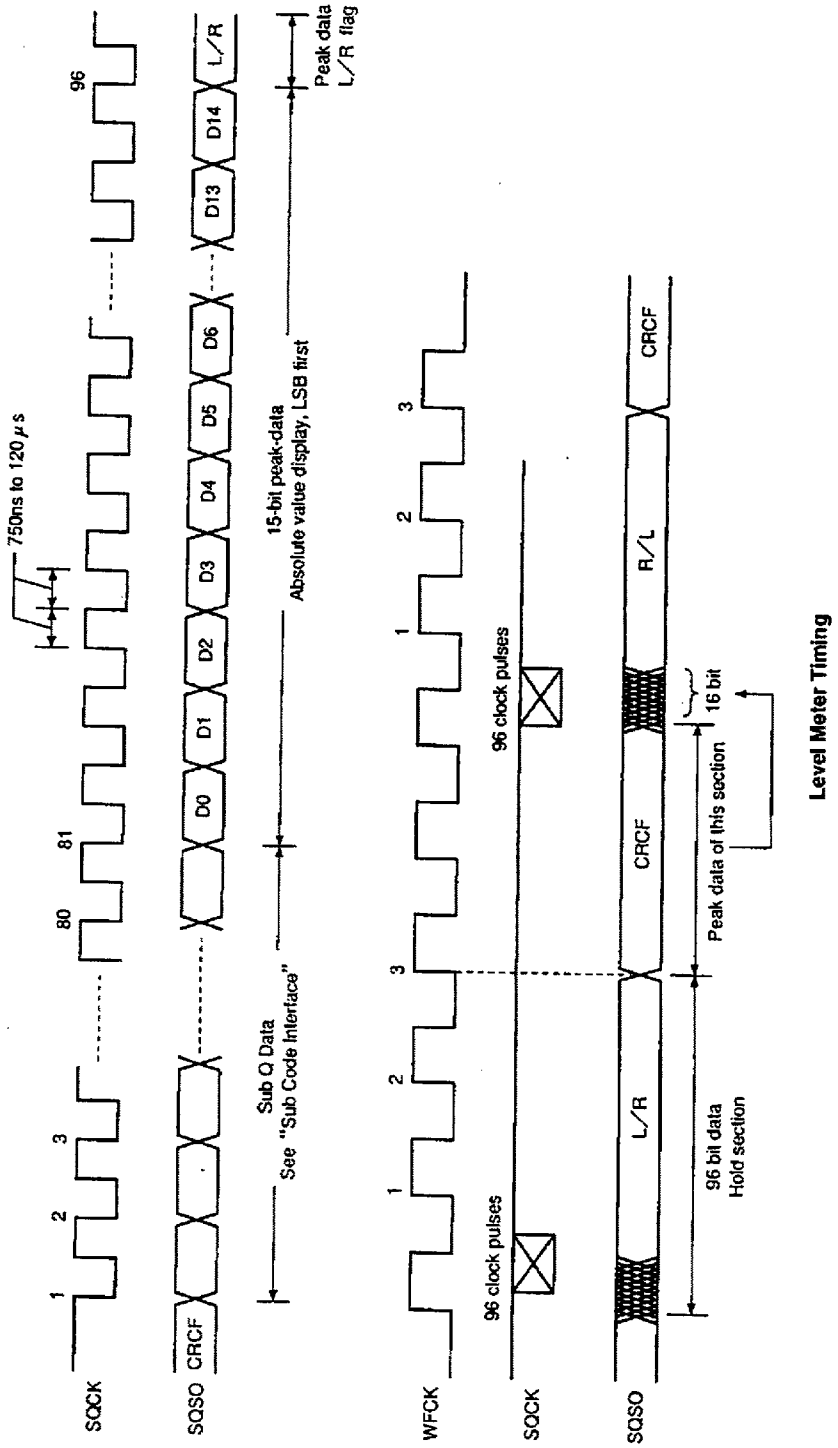
Mode	DCLV	DCLV PWM MD	LPWR	Timing chart
CLV-N	1	0	0	1-13
		1	0	1-14
CLV-W	1	0	0	1-15
			1	1-16
CAV-W	1	0	0	1-17 (CAV = 0)
			1	1-18 (CAV = 0)
			0	1-19 (CAV = 1)
			1	1-20 (CAV = 1)

Note) The CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, when using the CLV-W and CAV-W modes, set DCLV to 1 and DCLV PWM MD to 0.

Timing Chart 1-3

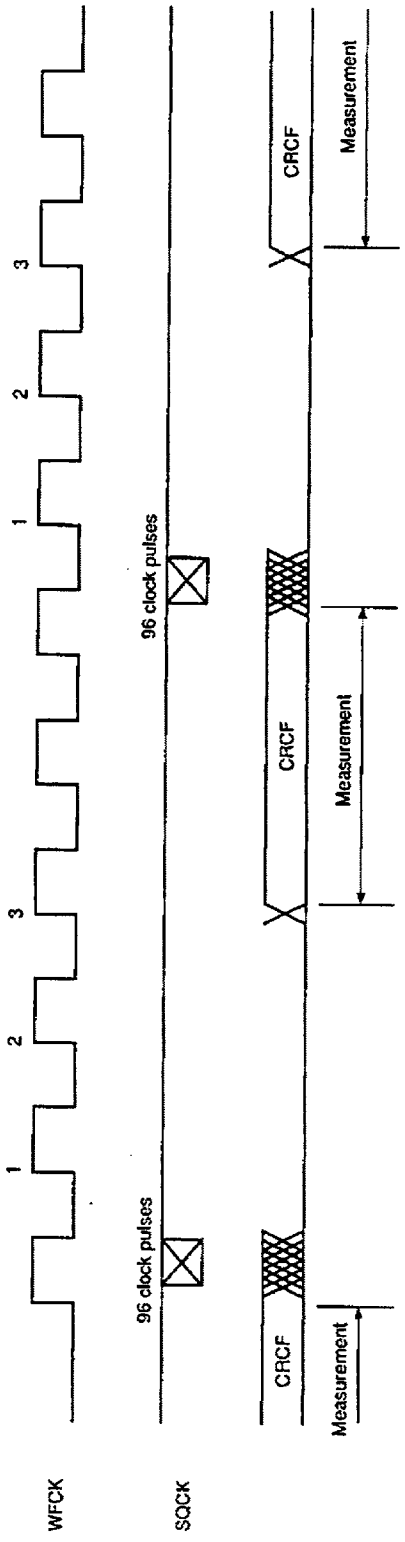


Timing Chart 1-4



Level Meter Timing

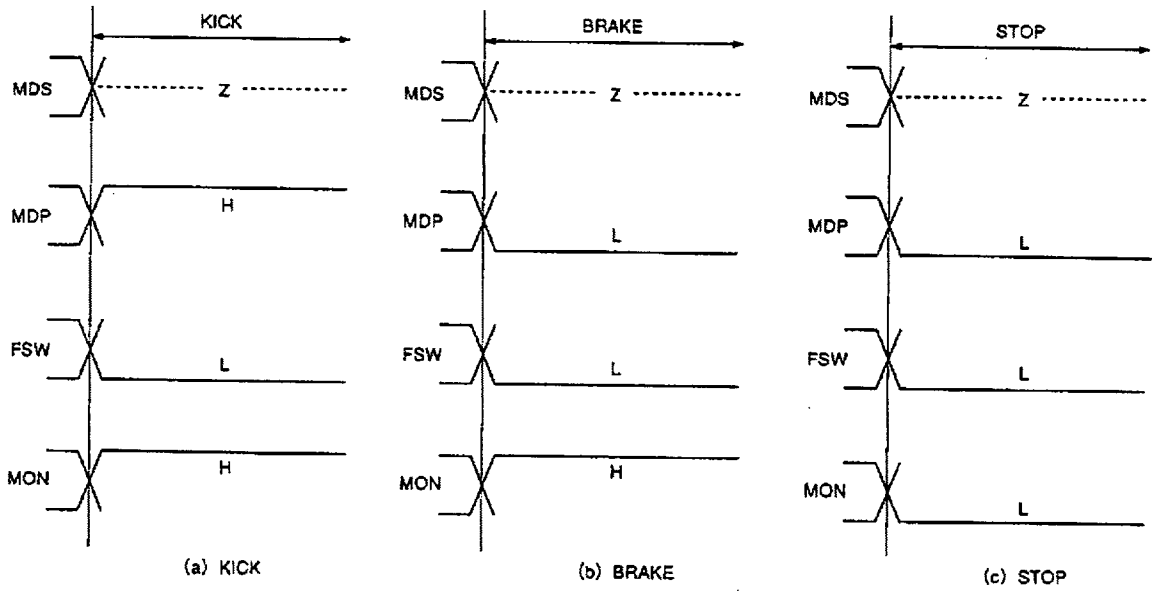
Timing Chart 1-5



Peak Meter Timing

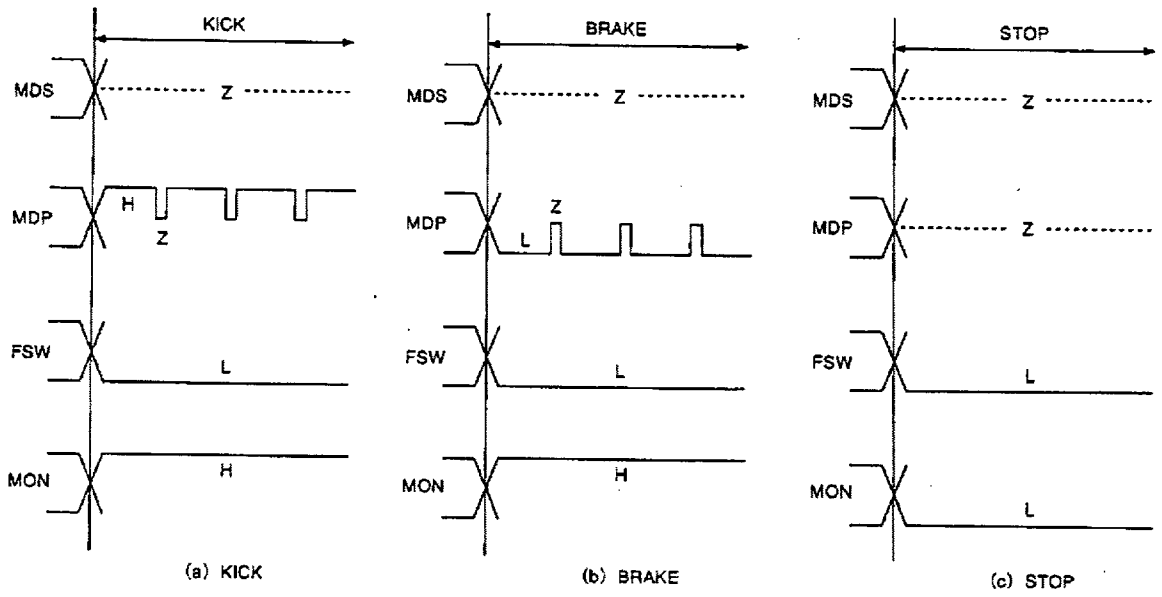
Timing Chart 1-6

CLV-N mode DCLV = DCLV PWM MD = LPWR = 0



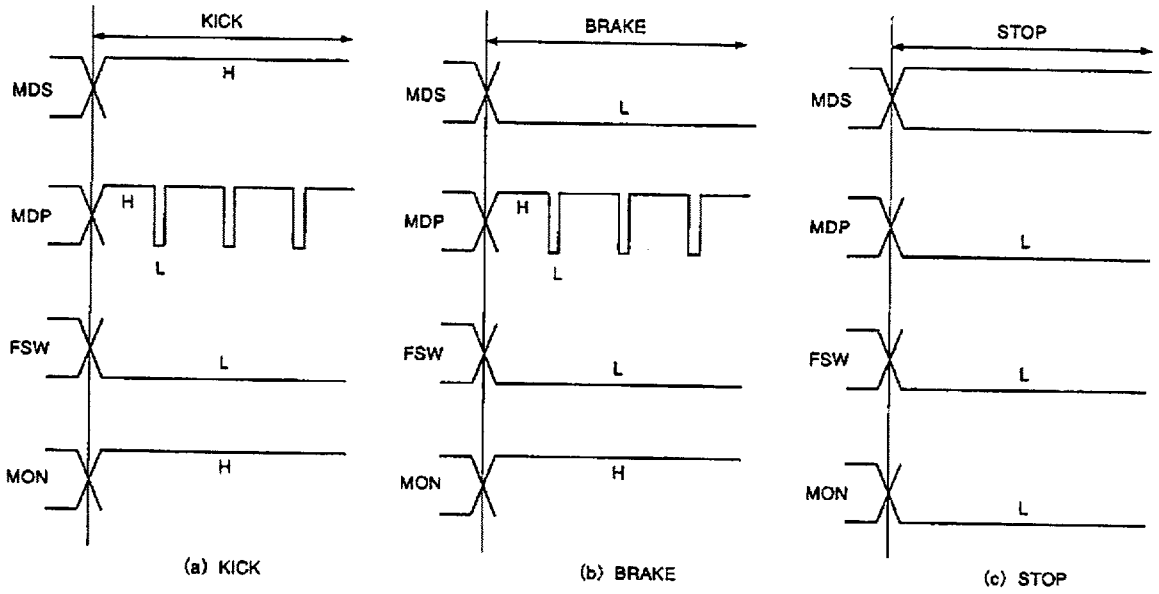
Timing Chart 1-7

CLV-N mode DCLV = 1, DCLV PWM MD = LPWR = 0



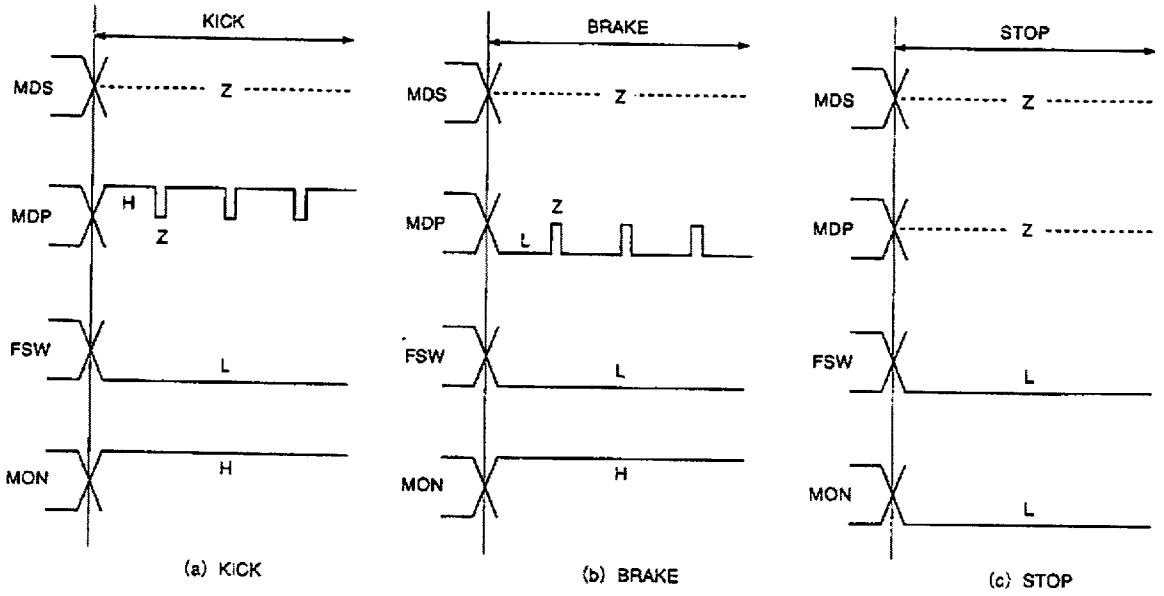
Timing Chart 1-8

CLV-N mode DCLV = DCLV PWM MD = 1, LPWR = 0



Timing Chart 1-9

CLV-W mode (when following the spindle rotational velocity) DCLV = 1, DCLV PWM MD = LPWR = 0

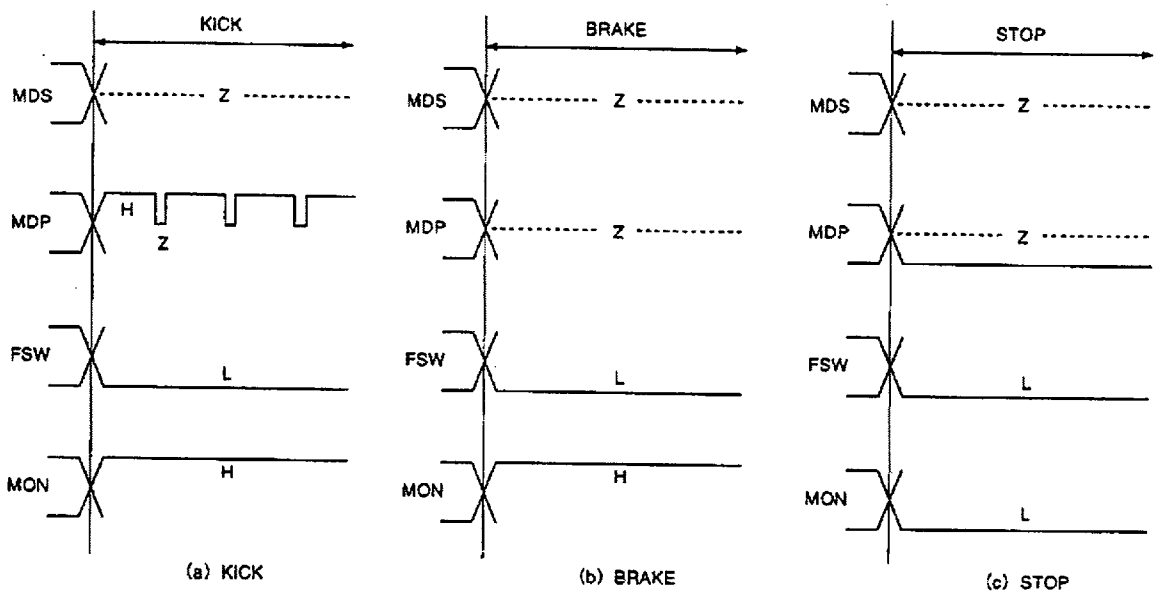


Other than when following the velocity, the timing is the same as Timing Chart 1-6 (a).

Other than when following the velocity, the timing is the same as Timing Chart 1-6 (b).

Timing Chart 1-10

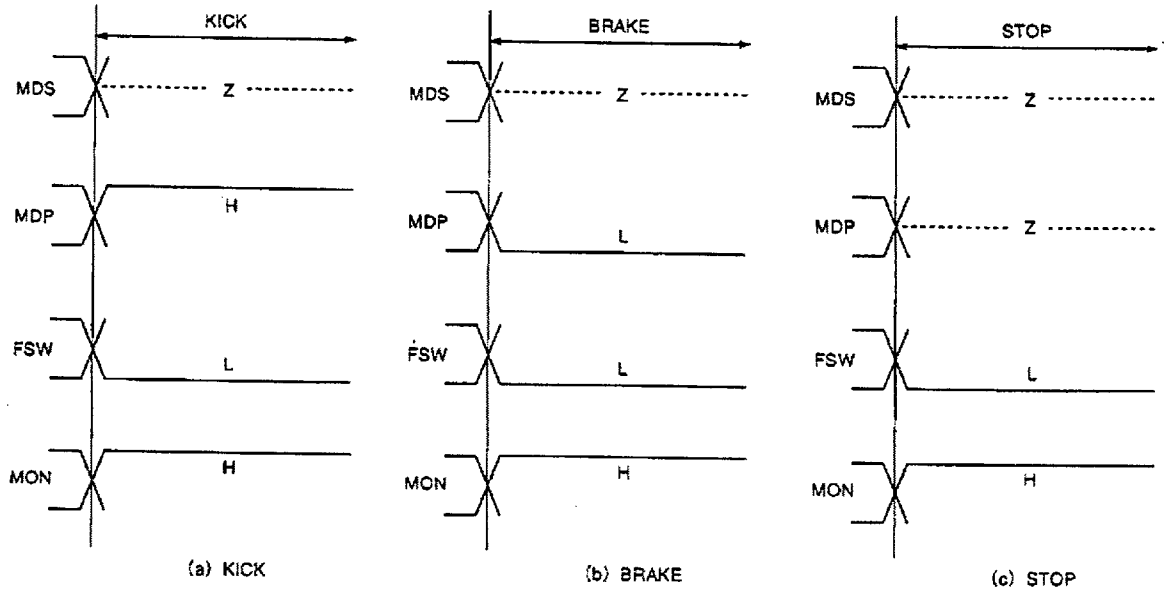
CLV-W mode (when following the spindle rotational velocity) DCLV = 1, DCLV PWM MD = 0, LPWR = 1



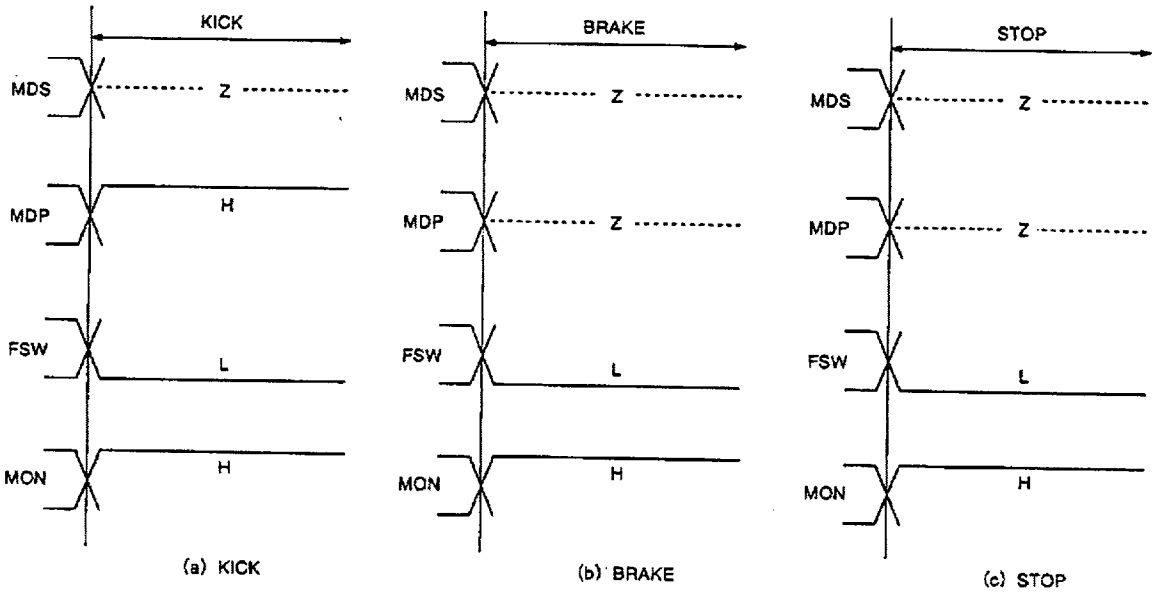
Other than when following the velocity, the timing is the same as Timing Chart 1-6 (a).

Timing Chart 1-11

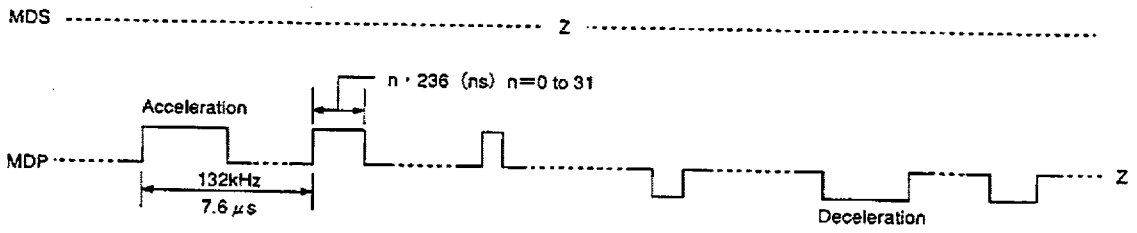
CAV-W mode DCLV = 1, DCLV PWM MD = LPWR = 0



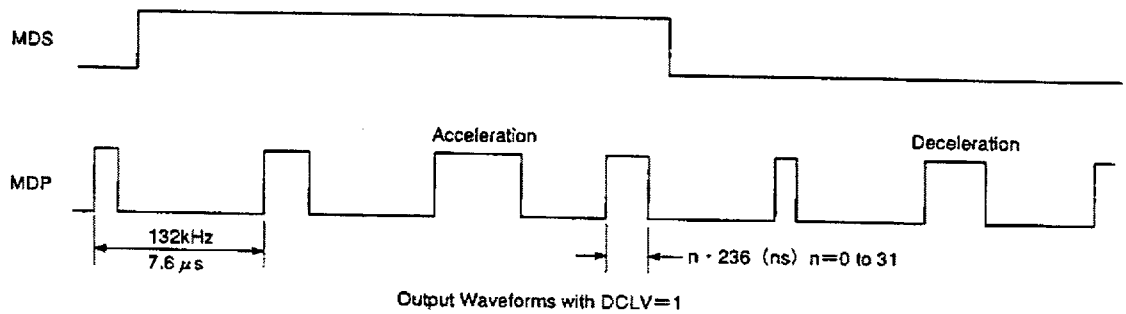
Timing Chart 1-12
CAV-W mode DCLV = 1, DCLV PWM MD = 0, LPWR = 1



Timing Chart 1-13
CLV-N mode DCLV PWM MD = LPWR = 0



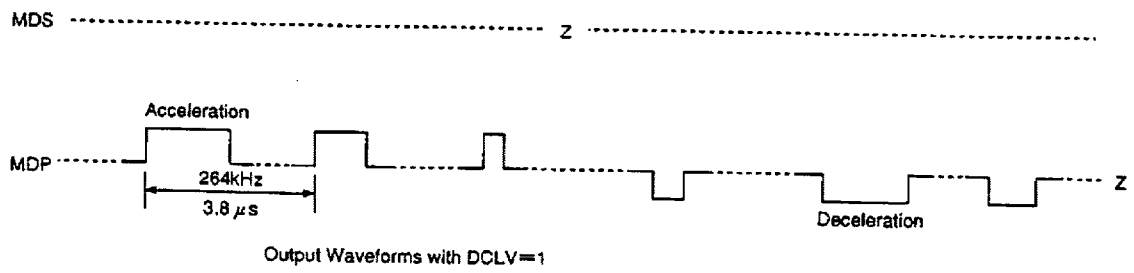
Timing Chart 1-14
CLV-N mode DCLV PWM MD = 1, LPWR = 0



Output Waveforms with DCLV=1

Timing Chart 1-15

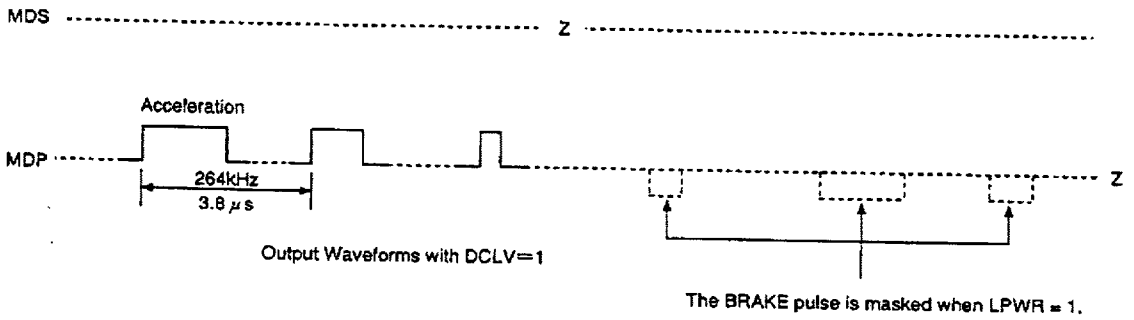
CLV-W mode DCLV PWM MD = LPWR = 0



Output Waveforms with DCLV=1

Timing Chart 1-16

CLV-W mode DCLV PWM MD = 0, LPWR = 1

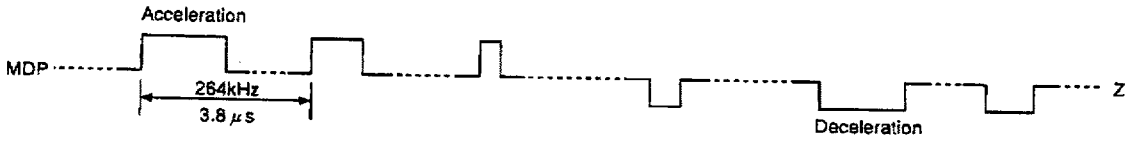


Output Waveforms with DCLV=1

The BRAKE pulse is masked when LPWR = 1.

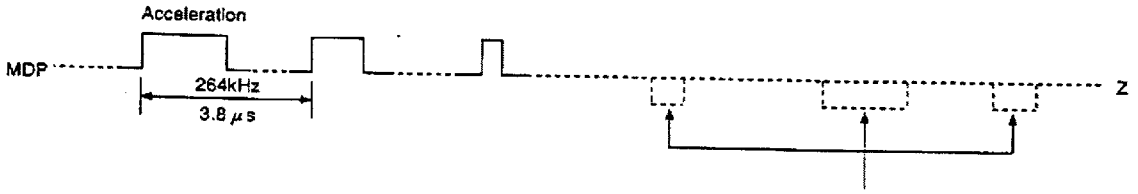
Timing Chart 1-17

CAV-W mode EPWM = DCLV PWM MD = LPWR = 0



Timing Chart 1-18

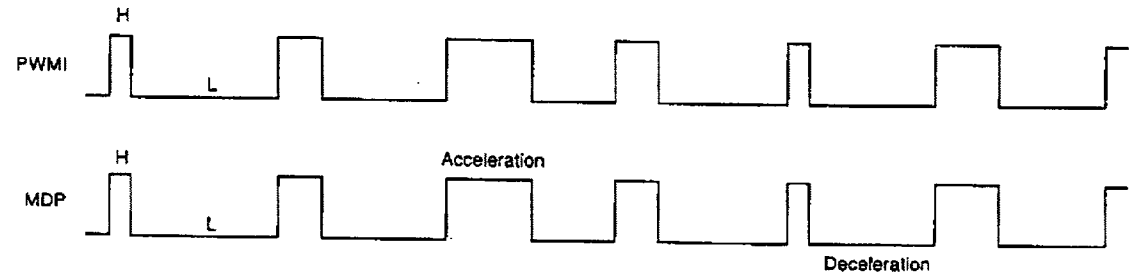
CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



The BRAKE pulse is masked when LPWR = 1.

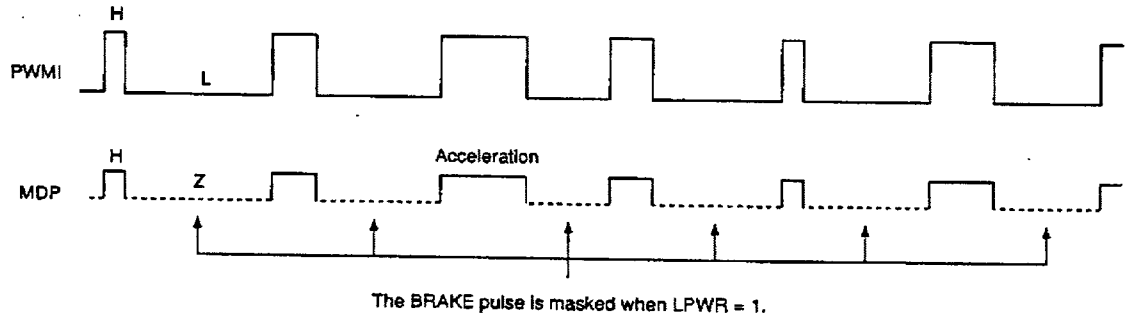
Timing Chart 1-19

CAV-W mode EPWM = 1, DCLV PWM MD = LPWR = 0



Timing Chart 1-20

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



Note) The CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, when using the CLV-W and CAV-W modes, set DCLV PWM MD to 0.

§2. Subcode Interface

This section explains the subcode interface.
There are two methods for reading out a subcode externally. The 8-bit subcodes P to W can be read from SBSO by inputting EXCK.
Sub Q can be read out after checking CRC of the 80 bits of information in the subcode frame.
Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to SQCK pin when SCOR comes correctly and CRCF is high.

§2-1. P to W Subcode Read

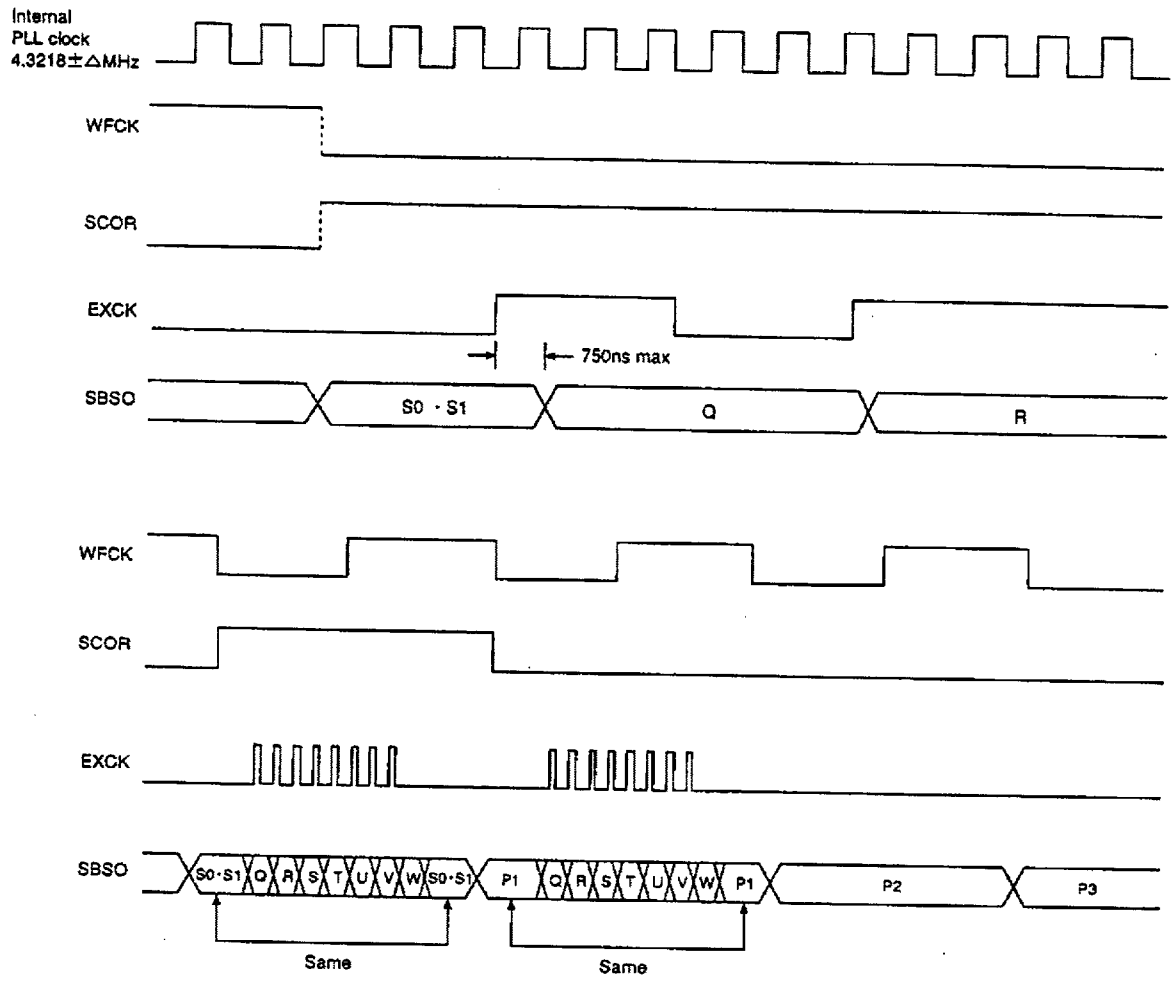
Data can be read out by inputting EXCK immediately after WFCK falls. (See the Timing Chart 2-1.)

§2-2. 80-bit Sub Q Read

Fig. 2-2 shows the peripheral block of the 80-bit Sub Q register.

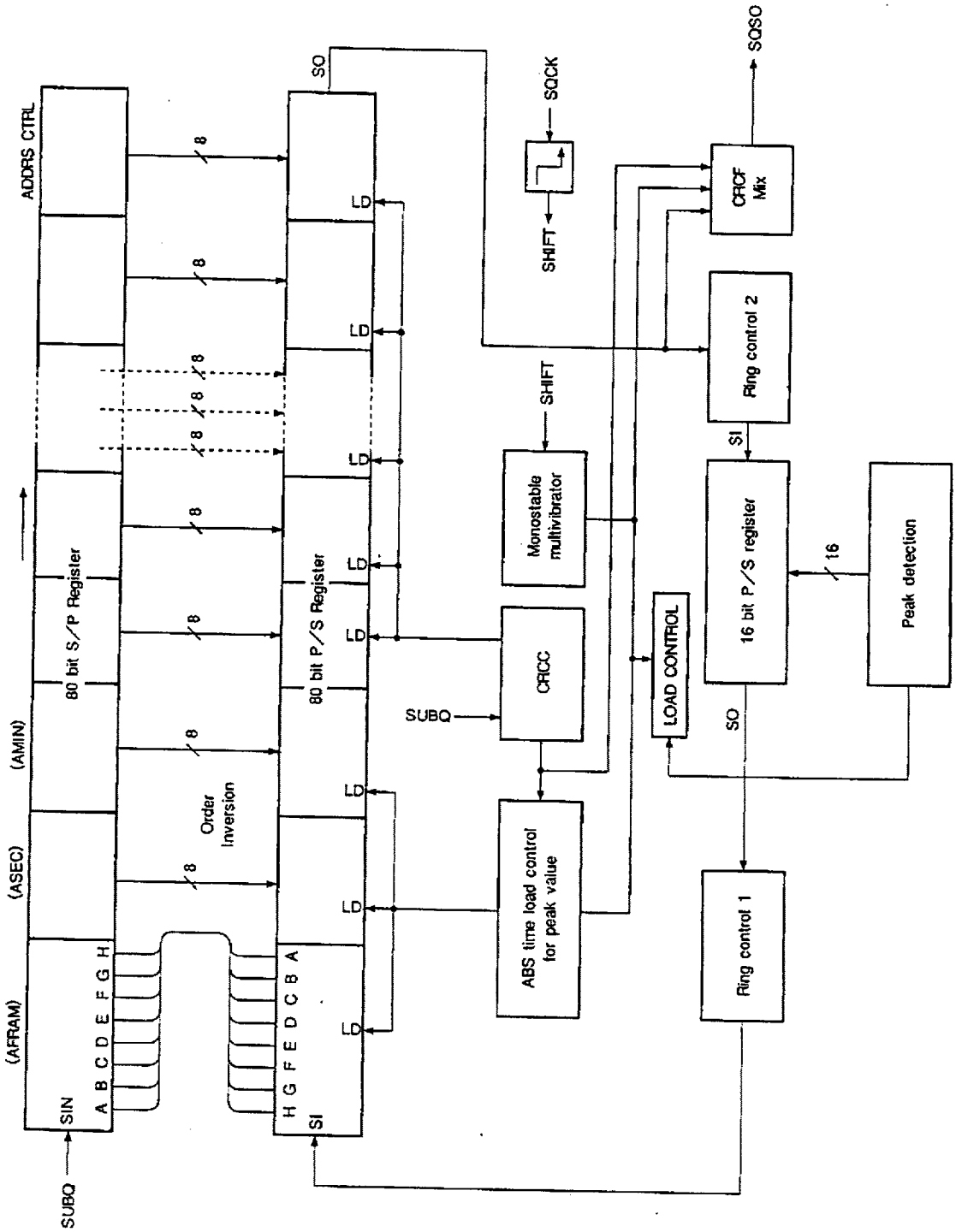
- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, SQSO pin outputs high meaning CRCF = 1. In addition, the 80 bits are loaded into the parallel/serial register.
  Therefore the CPU determines that new data (which passed the CRC check) has been loaded, if SQSO pin goes high after SCOR is output.
- In the CXD2540Q, when 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, the bits within the bytes are now ordered LSB first, the sequence of bytes is same though.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read. In this LSI, the SQCK input is detected, and the retriggerable monostable multivibrator for low is reset.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the S/P register is not loaded into the P/S register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others.
- In this LSI, the previously mentioned peak detection register can be connected to the shift-in of the 80-bit P/S register.
  Input and output for ring control 1 are shorted in peak meter or level meter mode.
  Those for ring control 2 are shorted in peak meter mode.
  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
  As a result, the 96-bit clock must be input in peak meter mode.
- The absolute time after peak is generated is stored in the memory in peak meter mode. (See the Timing Chart 2-3.)
- The high and low intervals for SQCK should be between 750ns and 120µs.

Timing Chart 2-1

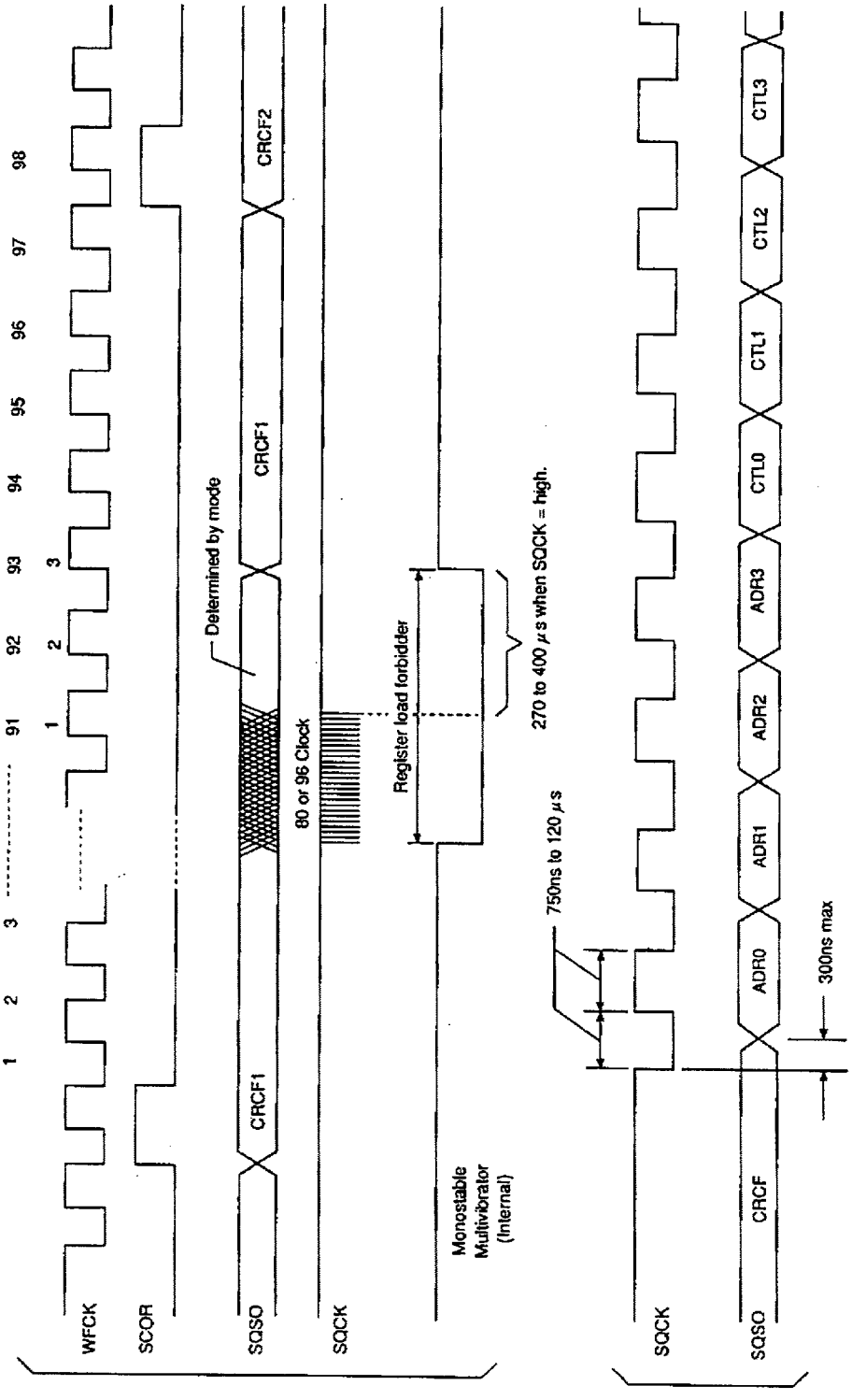


Subcode P.Q.R.S.T.U.V.W Read Timing

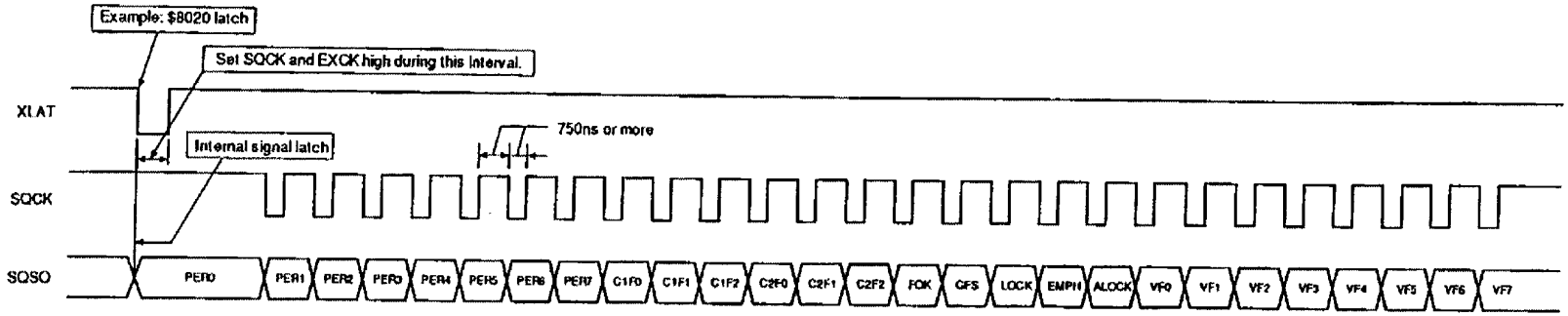
Block Diagram 2-2



Timing Chart 2-3



Timing Chart 2-4

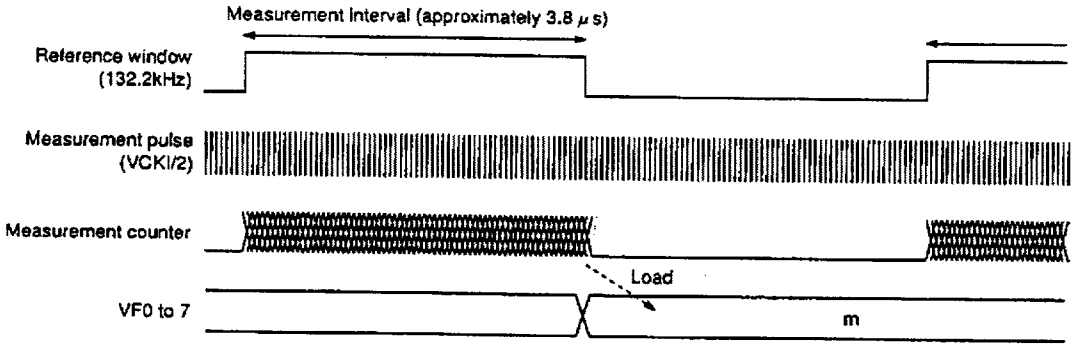


Signal	Explanation
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	High, when sampled value of GFS at 460Hz is high. Low, when sampled value of GFS at 460Hz is low by 8 times successively.
EMPH	Outputs a high signal when the playback disc has emphasis.
ALOCK	High, when sampled value of GFS at 460Hz is high by 8 times successively. Low, when sampled value of GFS at 460Hz is low by 8 times successively.
VF0 to 7	Used in CAV-W mode. The result obtained by measuring the rotational velocity of the disc. (See the Timing Chart 2-5.) VF0 = LSB, VF7 = MSB.

C1F2	C1F1	C1F0	Description
0	0	0	No C1 errors ; C1 pointer reset
0	0	1	One C1 error corrected ; C1 pointer reset
0	1	0	—
0	1	1	—
1	0	0	No C1 errors ; C1 pointer set
1	0	1	One C1 error corrected ; C1 pointer set
1	1	0	Two C1 errors corrected ; C1 pointer set
1	1	1	C1 correction impossible ; C1 pointer set

C2F2	C2F1	C2F0	Description
0	0	0	No C2 errors ; C2 pointer set
0	0	1	One C2 error corrected ; C2 pointer reset
0	1	0	Two C2 errors corrected ; C2 pointer reset
0	1	1	Three C2 errors corrected ; C2 pointer reset
1	0	0	Four C2 errors corrected ; C2 pointer reset
1	0	1	—
1	1	0	C2 correction impossible ; C1 pointer copy
1	1	1	C2 correction impossible ; C2 pointer set

Timing Chart 2-5



The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{m + 1}{32}$$ (R: Relative velocity, m: Measurement results)

VF0 to 7 is the result obtained by counting VCKI/2 pulses while the reference signal (132.2kHz) generated from crystal (384Fs) is high. This count is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

§3. Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

§3-1. CLV-N mode

This mode is compatible with the CXD2510Q, and operation is same as D2510Q and/or D2500 series (however, variable pitch cannot be used). Accordingly, the PLL capture range is ±150kHz.

§3-2. CLV-W mode

This is the wide capture range mode. This mode allows PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the CLV servo same as D2510Q and/or D2500 series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the VCKI pin.)

While starting to rotate a disc and/or speeding up to the lock range speed from the condition that a disc stops, CAV-W mode should be used. Because the lock range of CLV-W mode is too wide to do it. (much wider than that of D2510Q and/or D2500 series) Concretely saying, firstly send $E665 to set CAV-W mode and kick a disc, secondly send $E60C to set CLV-W mode if ALOCK is high, which can be read serially from SQSO pin. CLV-W mode is used for playback while ALOCK is high. The microcomputer monitors the serial data output, and must return to pull-in operation (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set to high, deceleration pulses are not output, thereby achieving low power consumption mode.

CLV-W mode supports control only by the ternary output of the MDP pin. Therefore, when using CLV-W mode, set DCLV PWM MD to low.

Note) The capture range for this mode is theoretically up to the signal processing limit.

§3-3. CAV-W mode

This is the CAV mode. In this mode, it is possible to control spindle to variable rotational velocity, the external crystal is fixed though. The rotational velocity is determined by the VP0 to 7 setting values or the external PWM. When controlling the spindle with VP0 to 7, setting the CAV-W mode with $E665 command and controlling VP0 to 7 with the $DX commands allows the rotational velocity to be varied from low speed to octuple-speed. (See $DX Commands.) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using V16M. And the reference for the velocity measurement is a signal of 132.2kHz obtained by 1/128 if crystal (384Fs). The velocity is obtained by counting V16M/2 pulses while the reference is high, and the result is output from the new CPU interface as 8 bits (VP0 to 7). These measurement results are 31 when the disc is rotating at normal speed or 127 when it is rotating at quadruple speed. These values match those of the 256-n for control with VP0 to 7. (See Table 2-5 and Fig. 2-6.)

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc (except for DATO, CLKO and XLTO).

Note) The capture range for this mode is theoretically up to the signal processing limit.
Note) Set FLFC is 1 when this mode is used.

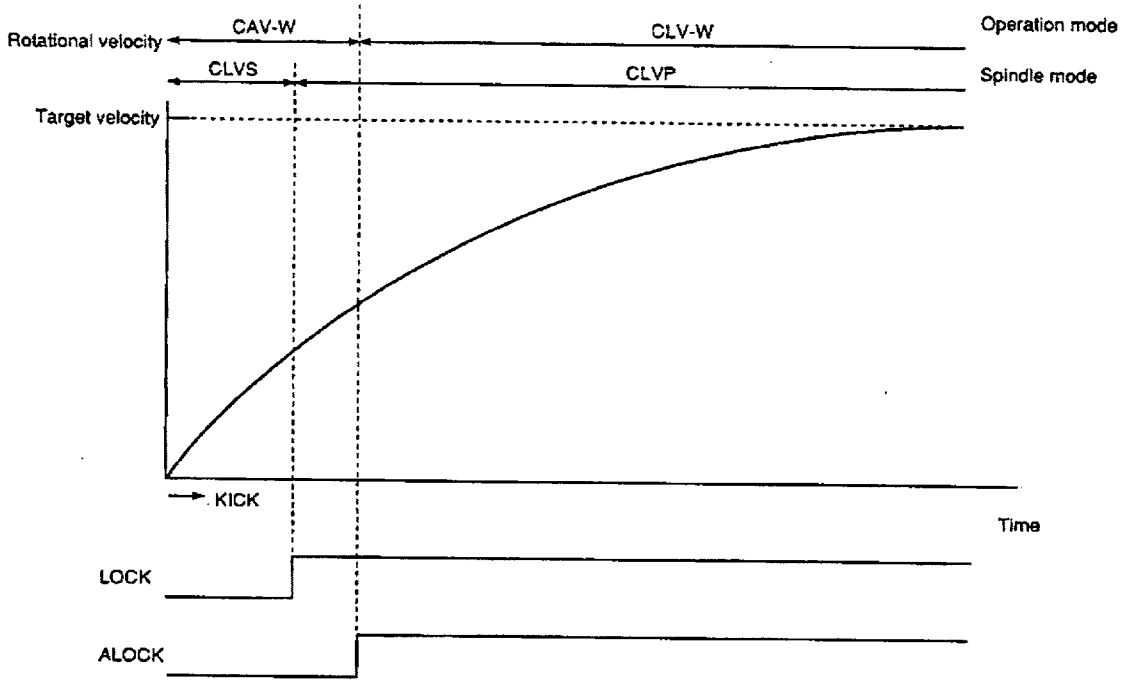


Fig.3-1. Disc Stop to Normal Condition in CLV-W Mode

CLV-W Mode

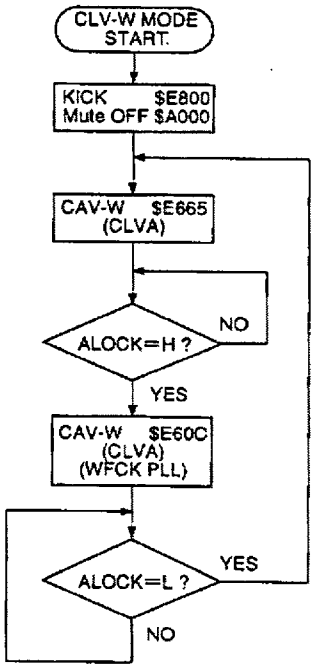


Fig. 3-2. CLV-W Mode Flow Chart

§4. Description of Other Functions

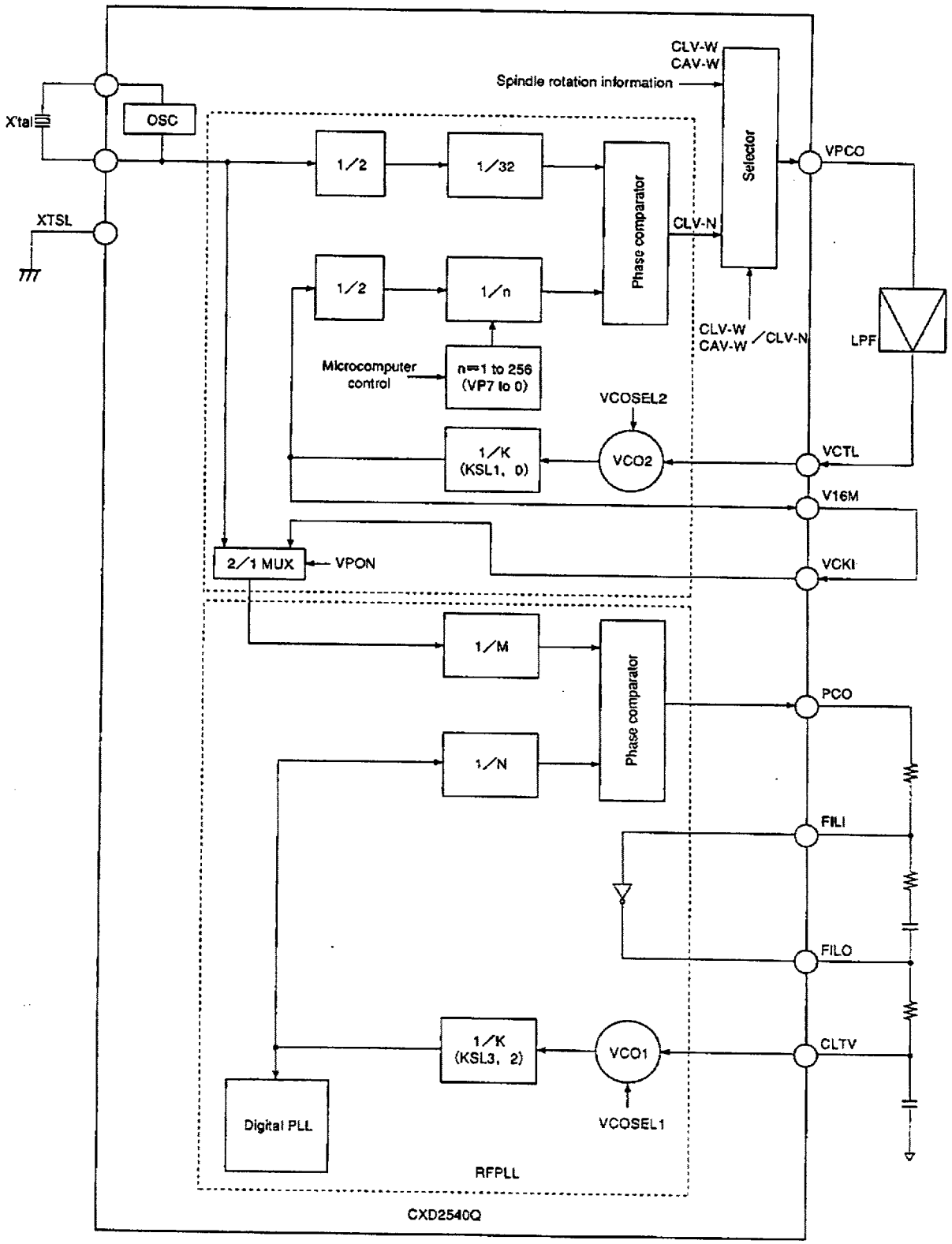
§4-1. Channel Clock Regeneration by the Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.
  Practically, PLL is necessary to regenerate the channel clock, because the EFM pulse width is altered by spindle rotation fluctuation.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD2540Q has a built-in three-stage PLL.

- The first-stage PLL is for the wide-band PLL. When the built-in VCO2 is used, LPF is required externally. When the built-in VCO2 is not used, LPF and VCO are required externally.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL generates a high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- The digital PLL in CLV-N mode has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off. High-frequency components such as 3T and 4T may contain deviations. In such a case, turning the secondary loop off yields better playability. However, in this case the capture range becomes 50kHz.
- The new digital PLL in CLV-W mode follows the rotational velocity of the disc, in addition to the conventional secondary loop.

Block Diagram 3-1



§4-2. Frame Sync Protection

- In a CD player operating at normal speed, a frame sync is recorded approximately every 136μs (7.35kHz). This signal is used as a reference to know which data is the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD2540Q, window protection and forward protection/backward protection have been adopted for frame sync protection. The adoption of these functions achieves very powerful frame sync protection. There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. In other words, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If frame sync cannot be detected for 13 frames or more, the window is released and the frame sync is resynchronized.
  In addition, immediately after the window is released and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window is released immediately.

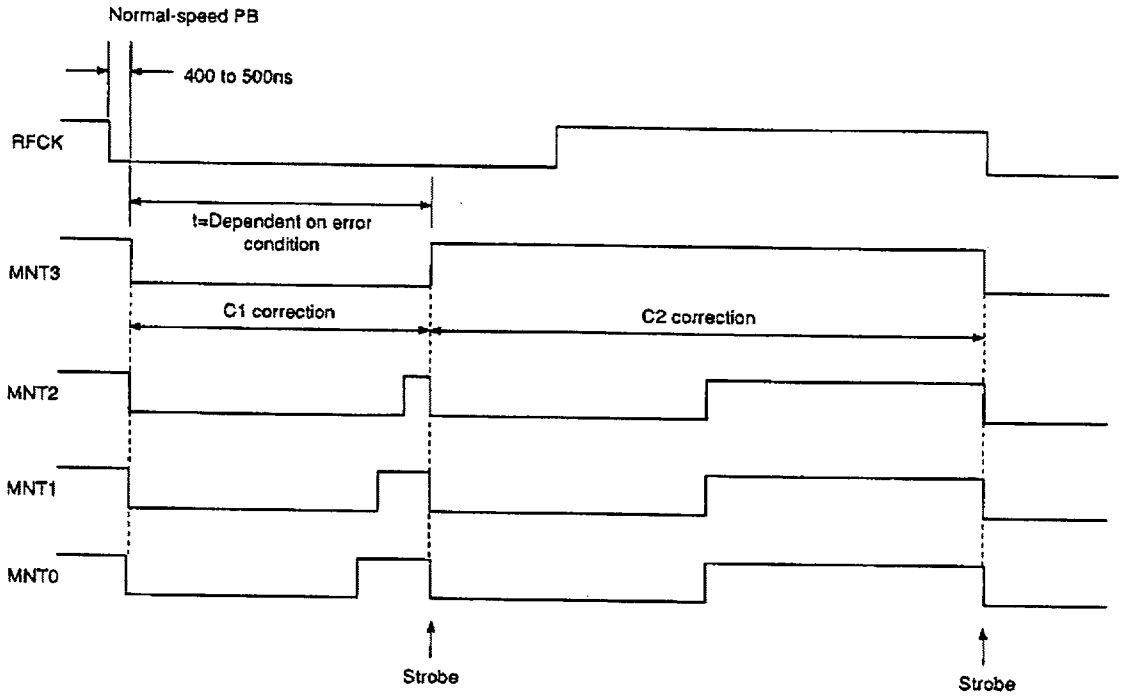
§4-3. Error correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD2540Q uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal, and the operating status of the player.
- The correction status can be monitored outside the LSI.
  See the Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description
0	0	0	0	No C1 errors ; C1 pointer reset
0	0	0	1	One C1 error corrected ; C1 pointer reset
0	0	1	0	—
0	0	1	1	—
0	1	0	0	No C1 errors ; C1 pointer set
0	1	0	1	One C1 error corrected ; C1 pointer set
0	1	1	0	Two C1 errors corrected ; C1 pointer set
0	1	1	1	C1 correction impossible ; C1 pointer set
1	0	0	0	No C2 errors ; C2 pointer reset
1	0	0	1	One C2 error corrected ; C2 pointer reset
1	0	1	0	Two C2 errors corrected ; C2 pointer reset
1	0	1	1	Three C2 errors corrected ; C2 pointer reset
1	1	0	0	Four C2 errors corrected ; C2 pointer reset
1	1	0	1	—
1	1	1	0	C2 correction impossible ; C1 pointer copy
1	1	1	1	C2 correction impossible ; C2 pointer set

Table 4-2.

Timing Chart 4-3



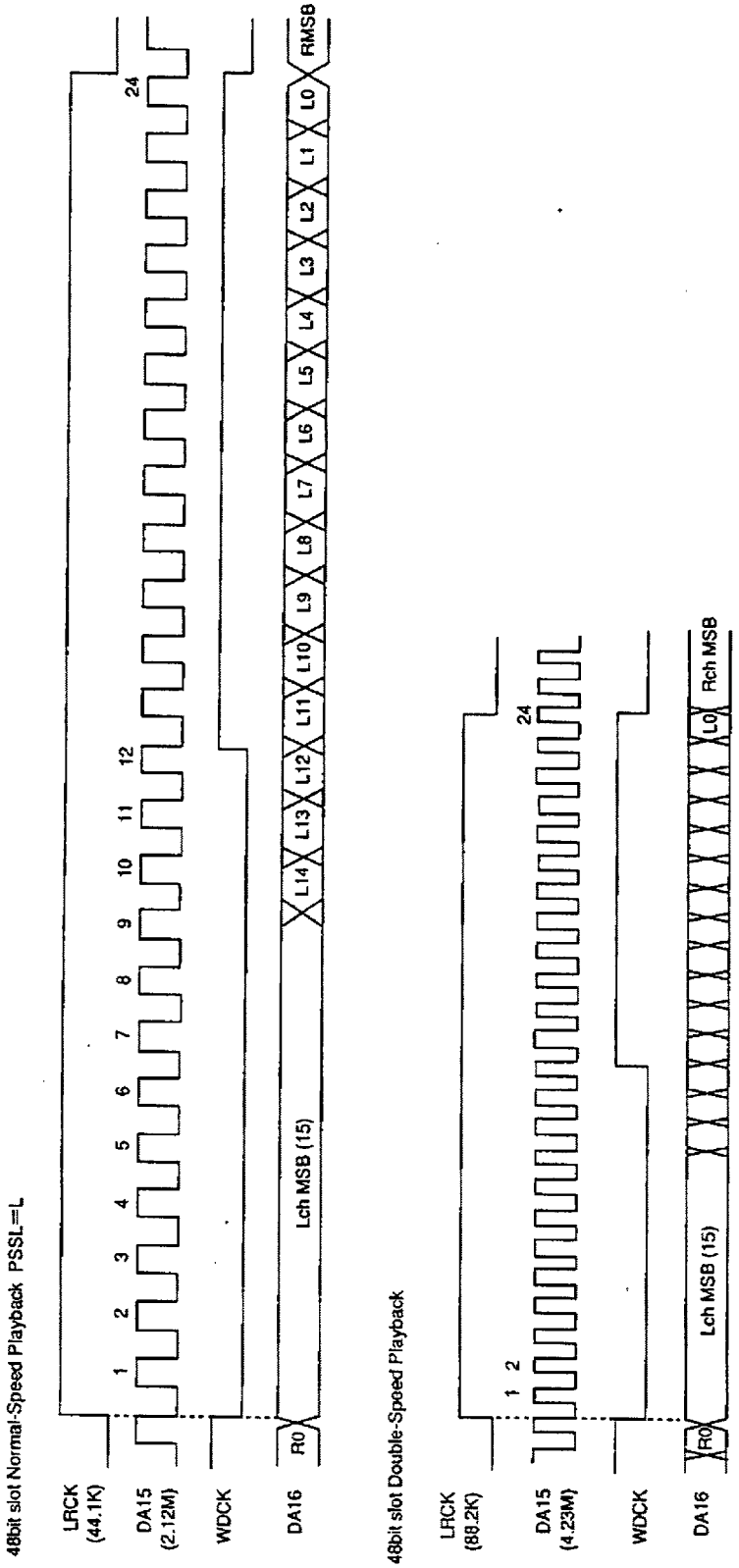
§4-4. DA Interface

- The CXD2540Q has two modes as DA interfaces.

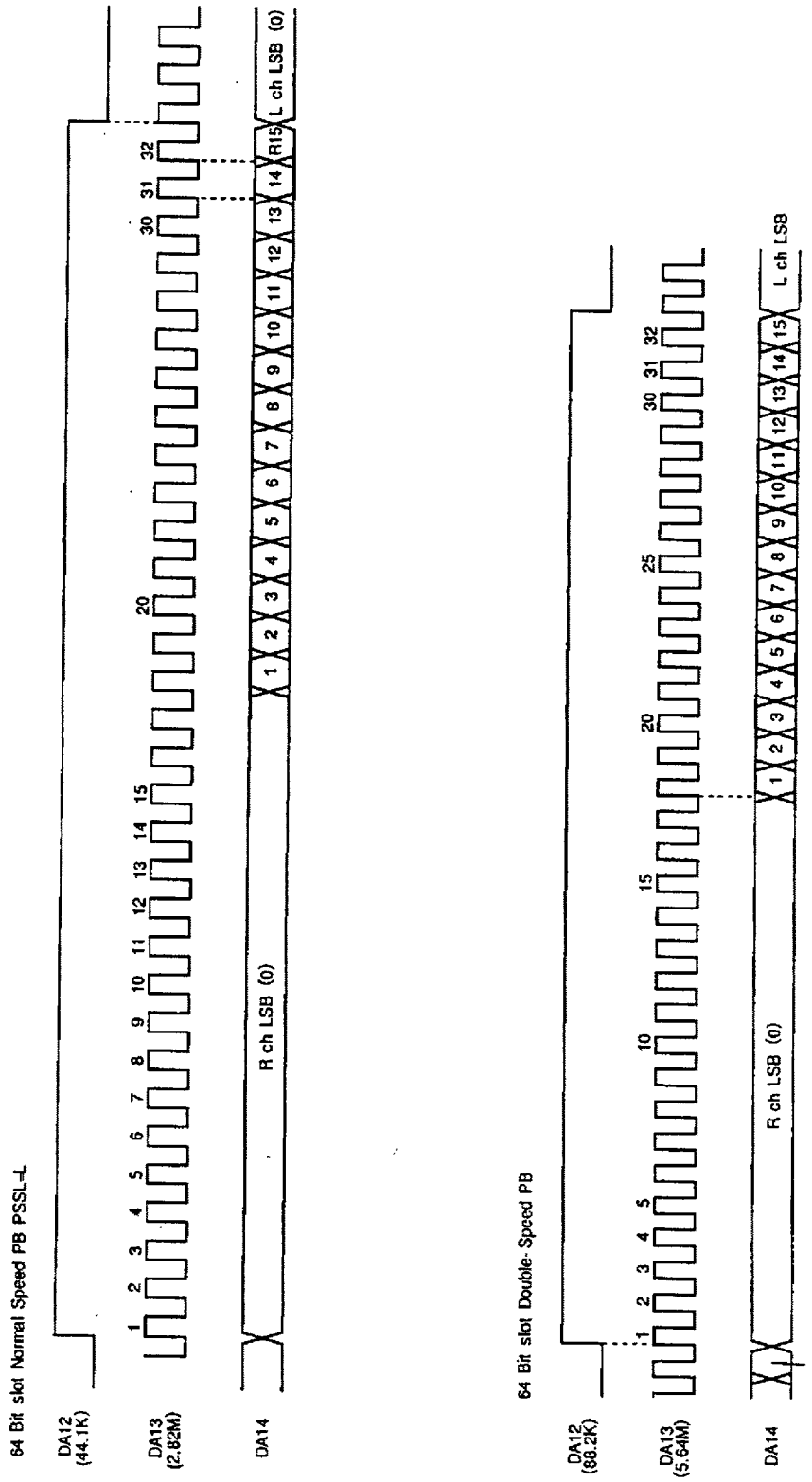
a) 48-bit slot interface
This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

b) 64-bit slot interface
This interface includes 64 cycles of the bit clock within one LRCK cycle, and is LSB first. When LRCK is low, the data is for the left channel.

Timing Chart 4-4



Timing Chart 4-5



§4-5. Digital Out

There are three digital out formats: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD2540Q supports type 2 form 1.

In addition, regarding the clock accuracy of the channel status, level III is set automatically when the crystal clock is used and level II is variable pitch. In addition, Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bit 0 to 3).

DOUT is output when the crystal is 34MHz, the variable pitch is reset, and DSPB = 1. Therefore, set MD2 to 0 and turn DOUT off.

bit 0 to 3 -Sub Q control bits that matched twice with CRCOK

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q →				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0 / 1	0	0
32																
48								0								
176																

bit0 to 3 —Sub Q control bits that matched twice with CRCOK

bit29 —Varipitch : 1 X'Tal : 0

Table 4-6.

§4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1 track jump, 2N track jumps, fine search, and M track move are executed automatically.

SSP (servo signal processor LSI) is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the SSP, but can be sent to the CXD2540Q.

In addition, when using the auto sequence, connect the CPU, RF and SSP as shown in Fig. 4-7, and turn the A.SEQ of register 9 on.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the SSP when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

In addition, a MAX timer is built in as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See §1, $4X commands concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.

Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus ($47)

Focus search up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-8. The auto focus is executed after focus search up, and the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. In other words, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

Connection diagram for using the auto sequencer (example)

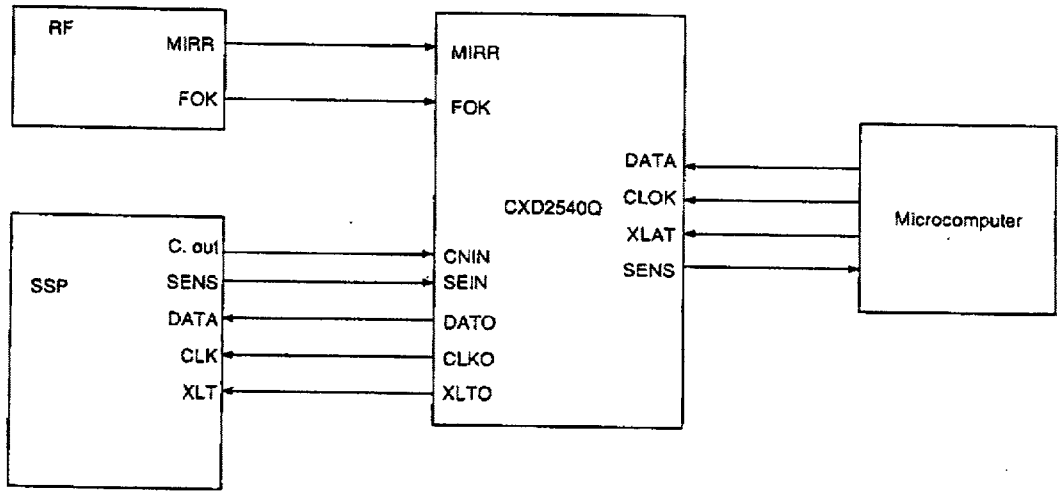


Fig. 4-7.

(b) Track jump

1, 10, and 2N-track jumps are performed respectively. Always use this when focus, tracking, and sled servo are on. Note that tracking gain-up and braking-on ($17) should be sent beforehand because they are not performed.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-9. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-10. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through CNIN, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the CNIN cycle becoming longer than the overflow C set in register 5), the tracking and sled servos are turned on.

- 2N-track jump

  When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-11. The track jump count "N" is set in register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. CNIN is used for counting the number of jumps when N is less than 16, and MIRR is used when N is 16 or higher.

  Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set in register 6.

- Fine search

  When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 4-12. The differences from a 2N-track jump are a higher precision jump achieved by controlling the traverse speed and a longer distance jump achieved by controlling the sled. The track jump count is set in register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F in register 6 and overflow G in register 5. And, the sled speed control for traversing can be turned off by raising COMP. In register B, the number of tracks for raising COMP is set. After N tracks have been counted through CNIN, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set in register 6. Then, the tracking and sled servos are turned on.

  Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.)

  For example, set the target track count N-α for the traverse monitor counter which is set in register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.

- M track move

  When $4E ($4F for REV) is received from the CPU, a FWD (REV) M track move is performed in accordance with Fig. 4-13. M can be set to 2^{16} tracks. CNIN is used for counting the number of moves when M is less than 16, and MIRR is used when M is 16 or higher. The M track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks. In addition, the track and sled servo are turned off after M tracks have been counted through CNIN or MIRR unlike for the other jumps. Transfer $25 after the actuator is stabled.

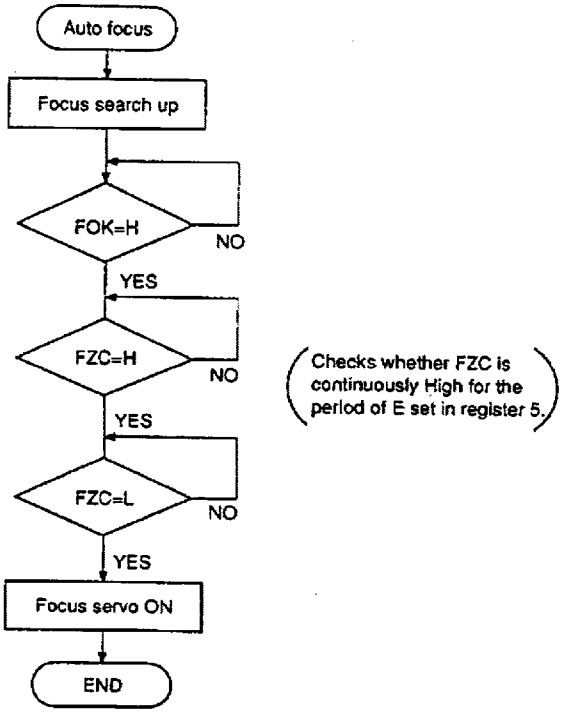


Fig. 4-8 (a). Auto focus flow chart

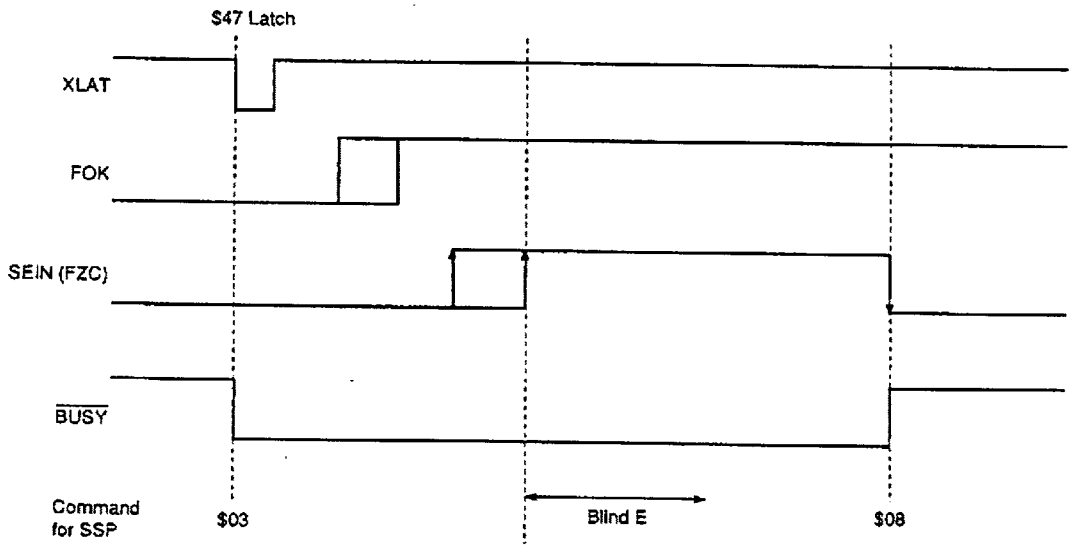


Fig. 4-8 (b). Auto focus timing chart

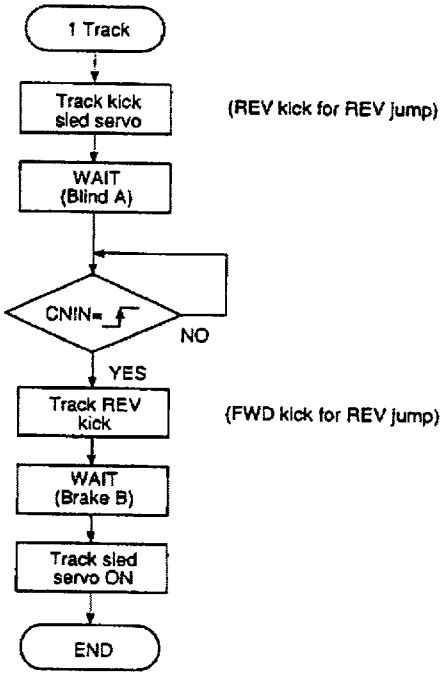


Fig. 4-9 (a). 1-Track Jump Flow Chart

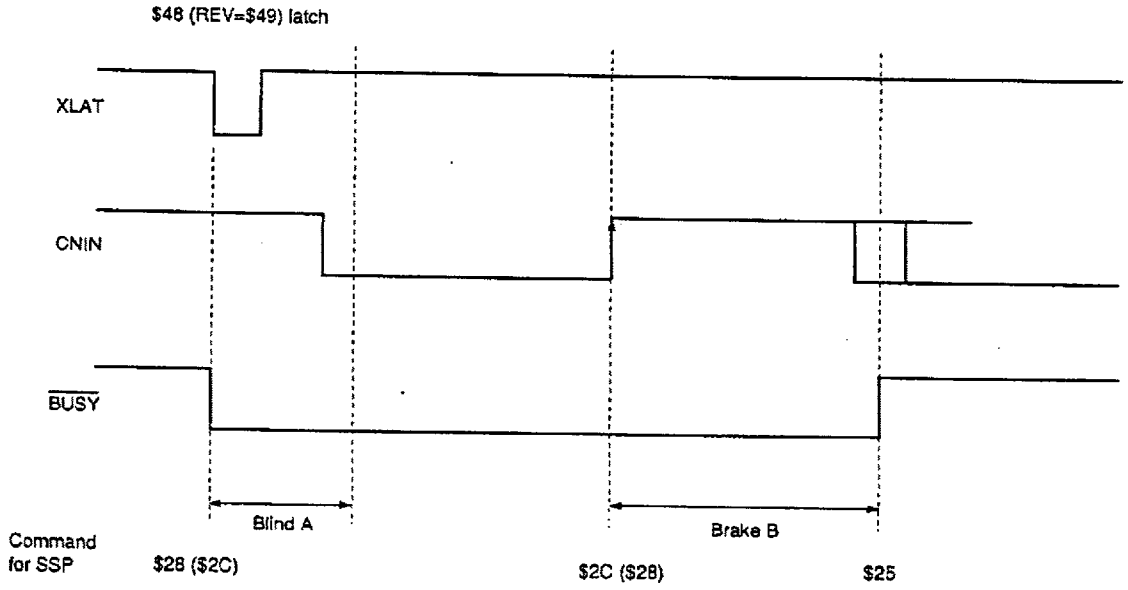


Fig. 4-9 (b). 1-Track Jump Timing Chart

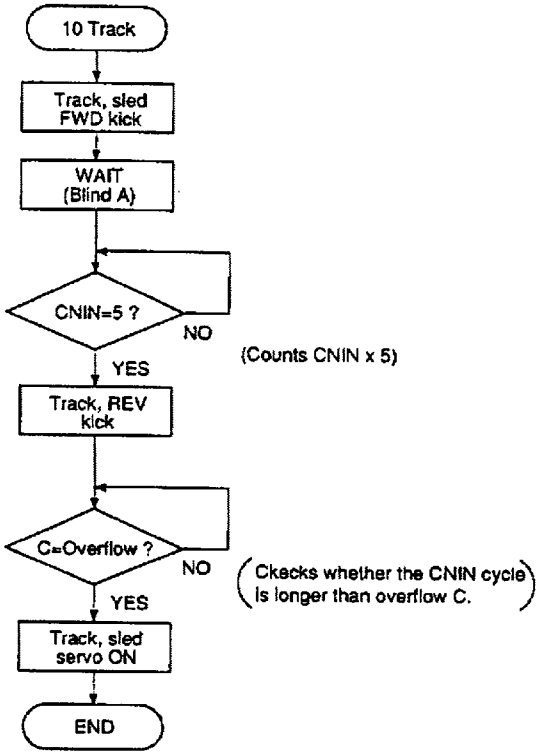


Fig. 4-10 (a). 10-Track Jump Flow Chart

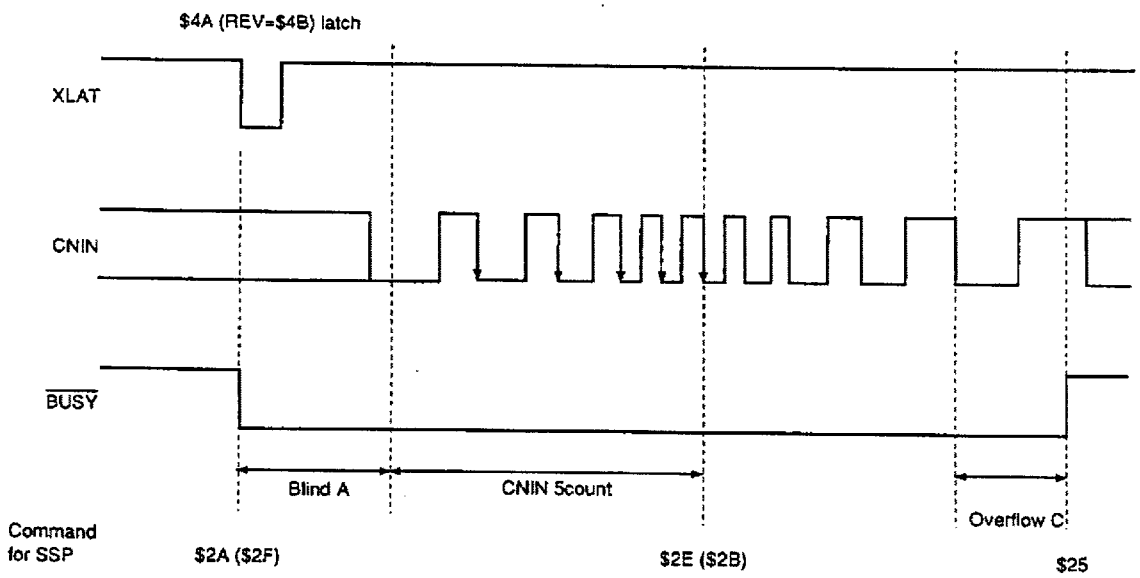


Fig. 4-10 (b). 10-Track Jump Timing Chart

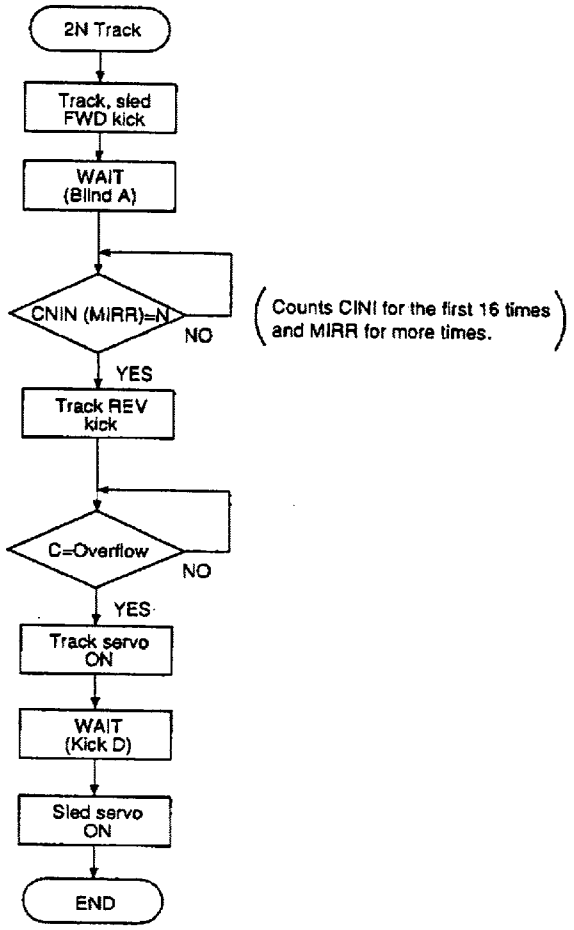


Fig. 4-11 (a). 2N-Track Jump Flow Chart

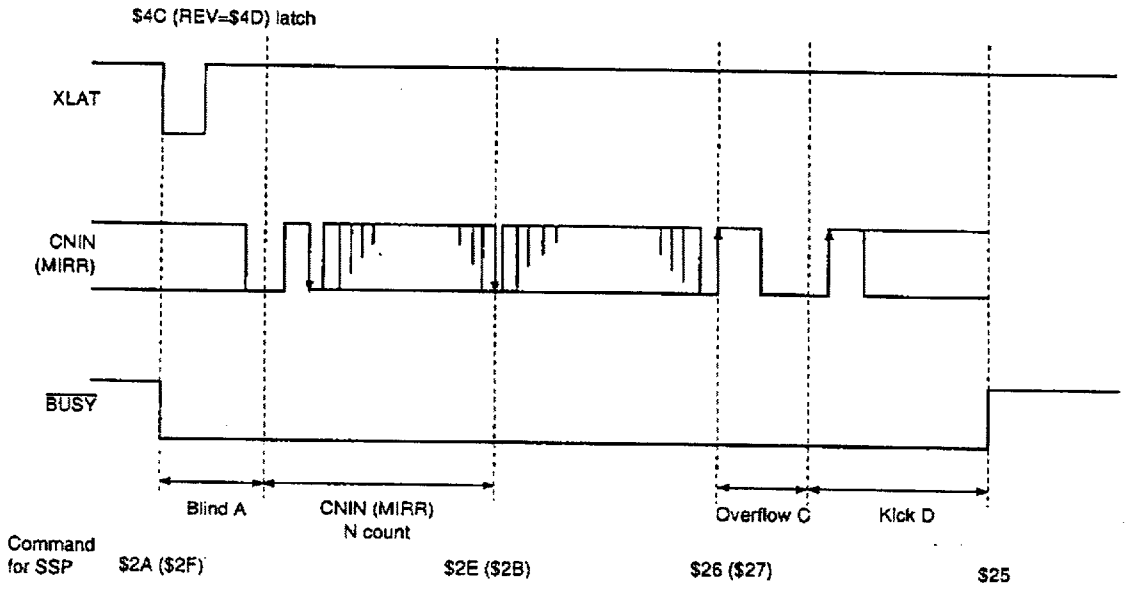


Fig. 4-11 (b). 2N-Track Jump Timing Chart

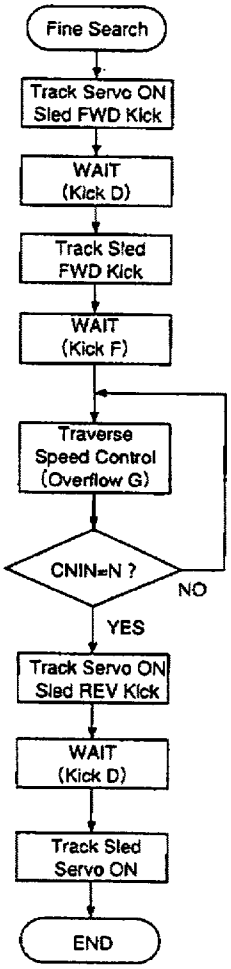


Fig. 4-12 (a). Fine Search Flow Chart

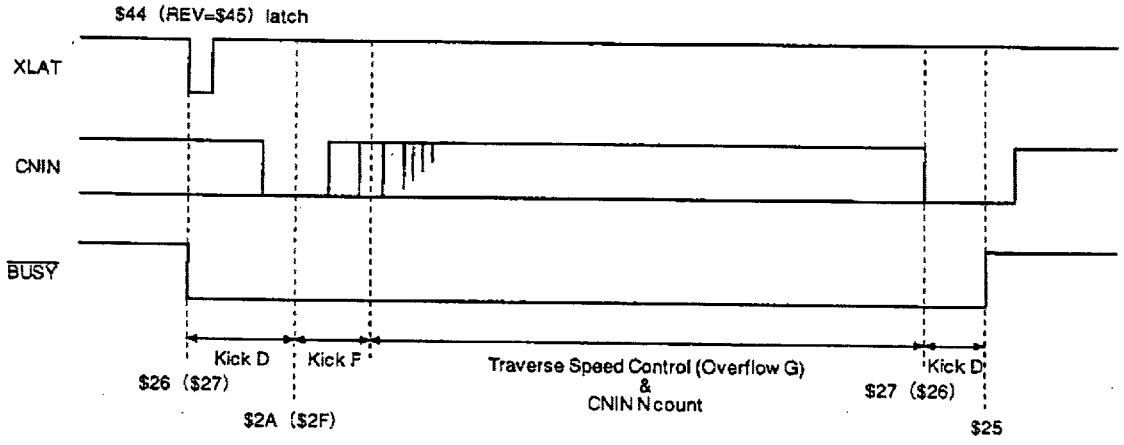


Fig. 4-12 (b). Fine Search Timing Chart

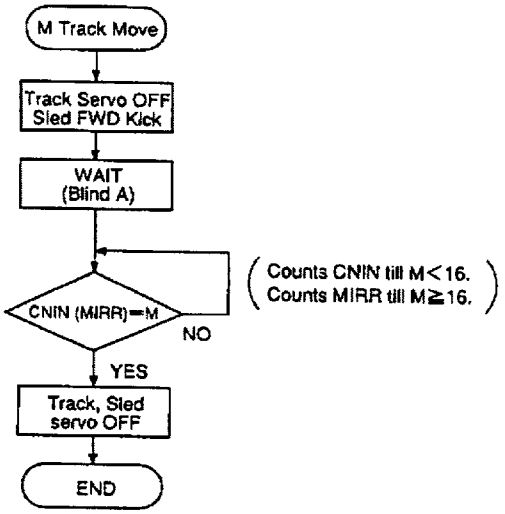


Fig. 4-13 (a). M-track Move Flow Chart

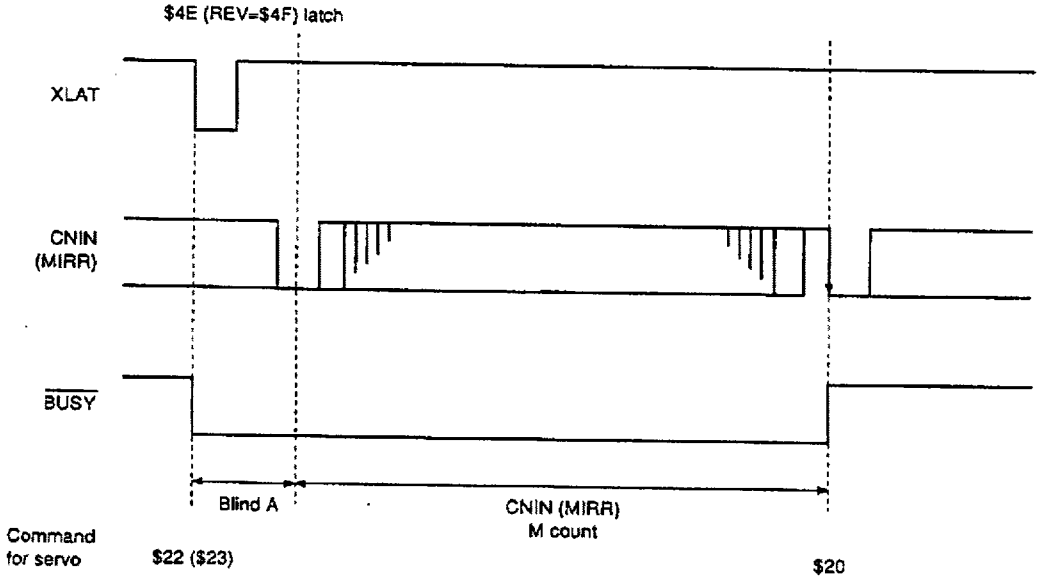
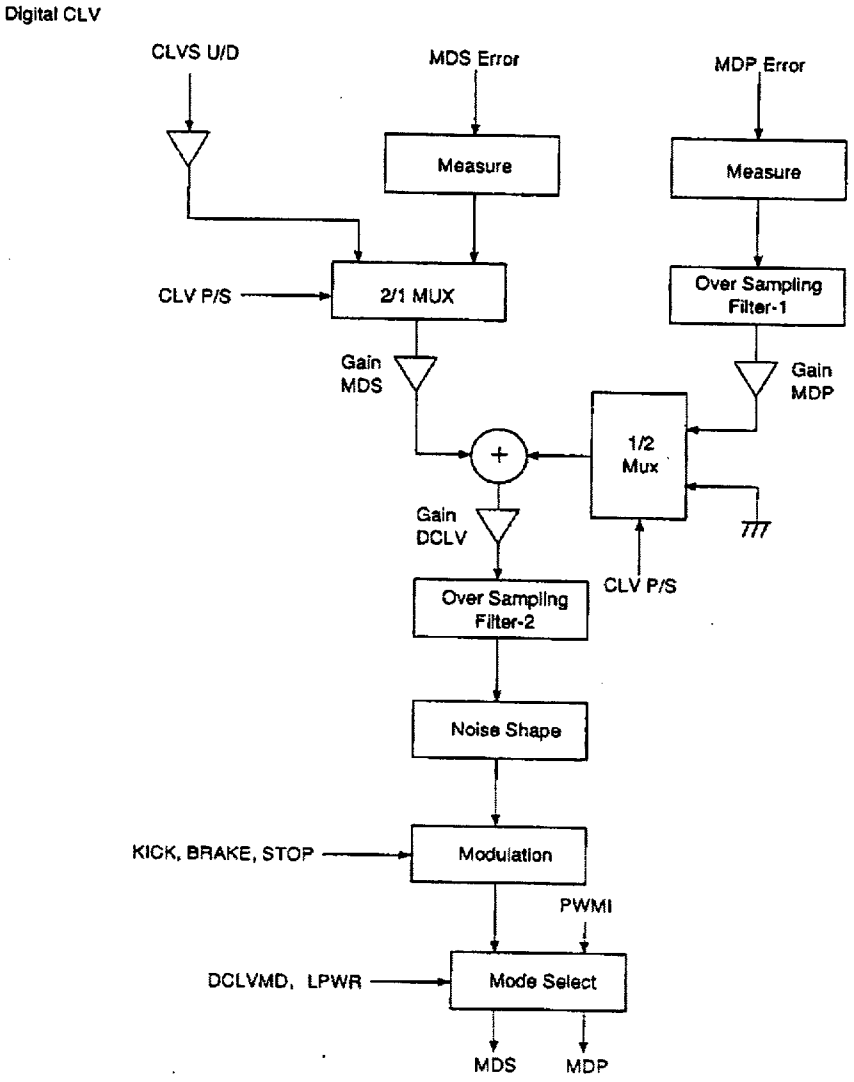


Fig. 4-13 (b). M-Track Move Timing Chart

§4-7. Digital CLV

Fig. 4-14 shows the block diagram. Digital CLV outputs MDS error and MDP error with PWM, and can increase the sampling frequency of it up to 130Hz during normal-speed playback, in CLVS, CLVP, and other mode.

In addition, the digital spindle servo can set the gain.



CLVS U/D: Up/down signal from the CLVS servo.
MDS error: Frequency error for CLVP servo.
MDP error: Phase error for CLVP servo.
PWMI: Spindle drive signal from the microcomputer.

Fig. 4-14. Block Diagram

§4-8. Asymmetry Compensation

Fig. 4-15 shows the block diagram and circuit example.

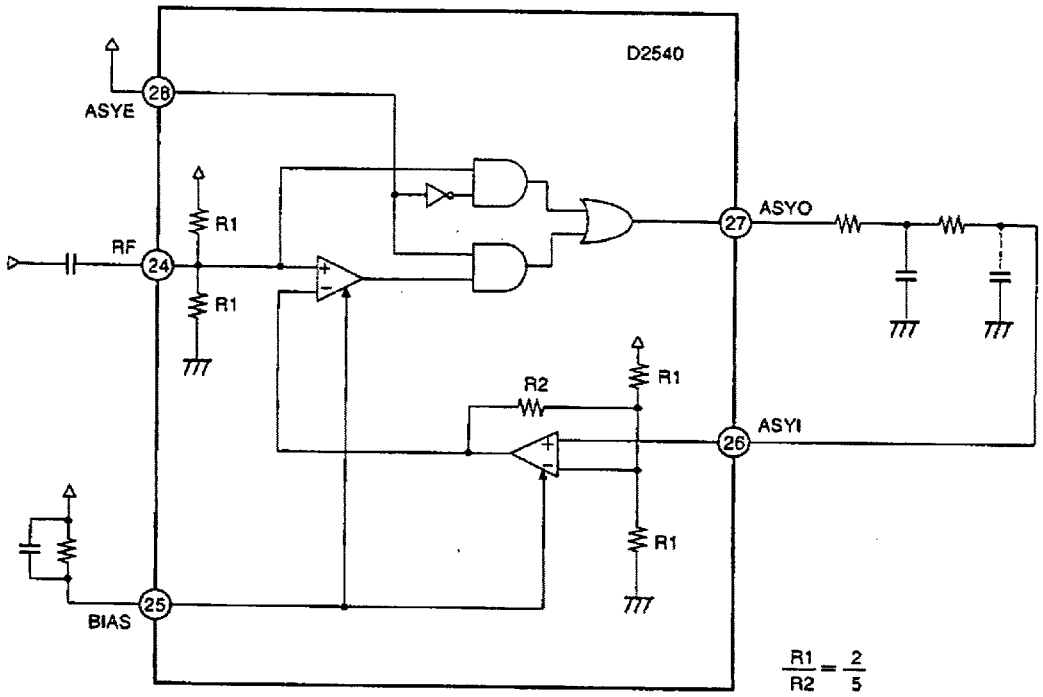


Fig. 4-15. Example of an Asymmetry Compensation Application Circuit

§4-9. Playback Speed

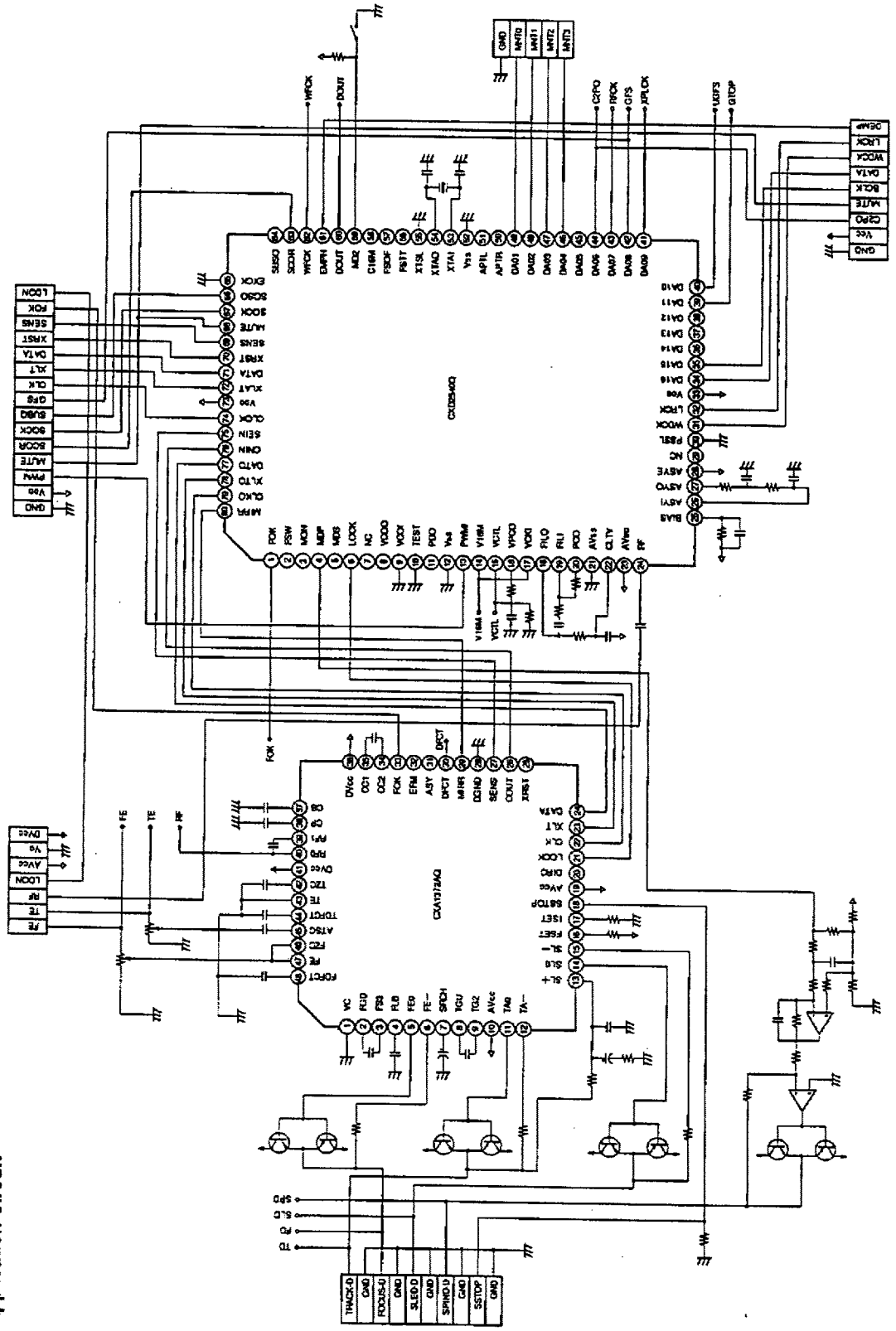
In the CXD2540Q-2, the following playback modes can be selected through different combinations of the crystal, XTSL pin, double-speed command (DSPB), VCO1 selection command (VCOSEL1), VCO1 frequency dividing command (KSL3, KSL2) and command transfer rate selector (ASHS). Also, the minimum operating voltage changes according to the playback mode. (See the Recommended Operating Conditions.)

Mode	X'tal	XTSL	DSPB	VCOSEL1*1	ASHS	Playback speed	Error correction
1	768Fs	1	0	0/1	0	x 1	C1: double; C2: quadruple
2	768Fs	1	1	0/1	0	x 2	C1: double; C2: double
3	768Fs	0	0	1	1	x 2	C1: double; C2: quadruple
4	768Fs	0	1	1	1	x 4	C1: double; C2: double
5	384Fs	0	0	0/1	0	x 1	C1: double; C2: quadruple
6	384Fs	0	1	0/1	0	x 2	C1: double; C2: double
7	384Fs	1	1	0/1	0	x 1	C1: double; C2: double

*1 Actually, use the optimal value by combining with the KSL3 and KSL2.

The playback speed can be varied by setting VP0 to 7 in CAV-W mode. See "§3. Description of Modes" for details.

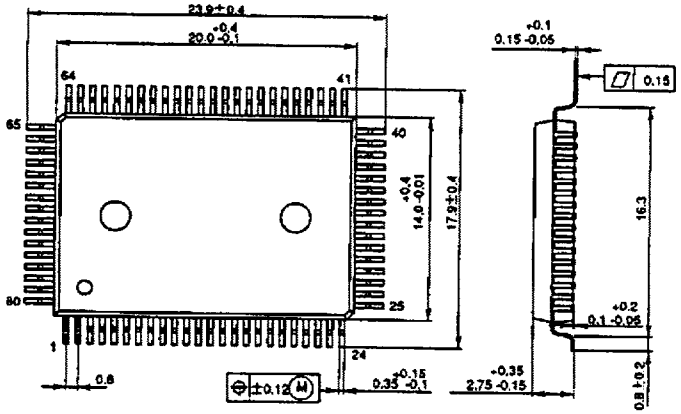
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

80PIN QFP(PLASTIC)

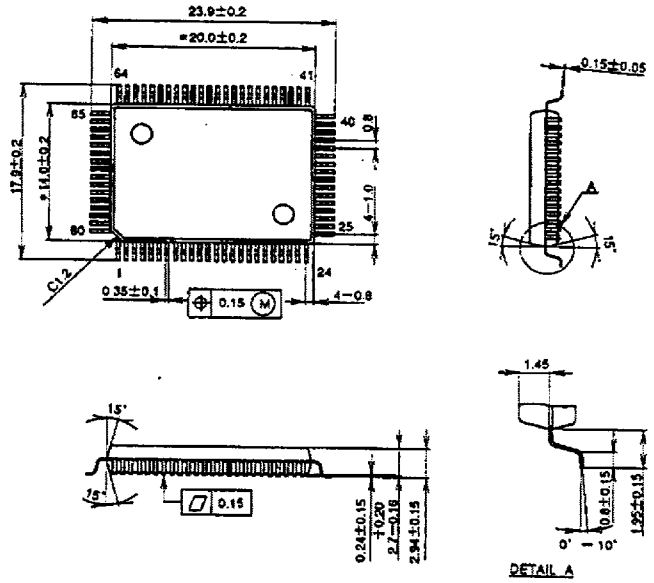


PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.8g

QFP 80PIN (PLASTIC)



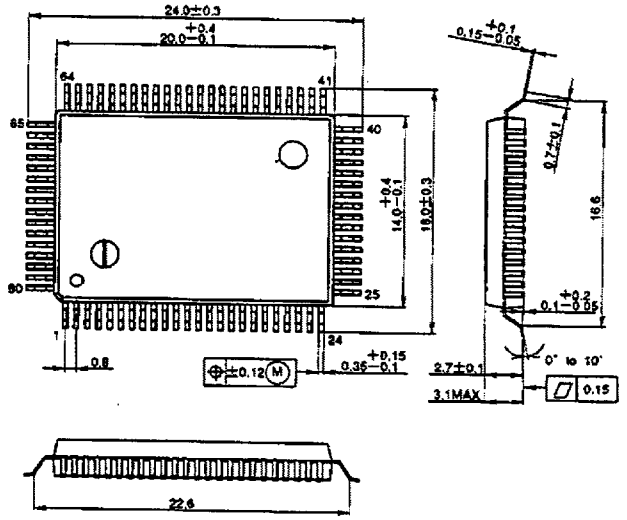
NOTE>Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L051
EIAJ CODE	*QFP080-P-1420-AH
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.6g

80PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L121
EIAJ CODE	*QFP080-P-1420-AX
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.6g