SONY

CXB1455R

VGA/SVGA/XGA 24-bit Transmitter

Description

The CXB1455R is the IC which transmits the 24-bit VGA/SVGA/XGA definition moving picture based on the GVIF (Gigabit Video Interface) technology.

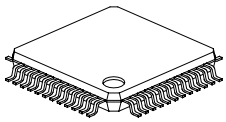
Features

- 1 chip transmitter for serial transmission of 24-bit color VGA/SVGA/XGA picture
- On-chip PLL synthesizer
- On-chip differential cable driver
- TTL/CMOS compatible interface
- Supports 1 pixel/shift clock mode with 1 chip and 2 pixel/shift clock mode with 2 chips
- Single 3.3V power supply
- Low power consumption
- 48-pin plastic QFP package (7mm × 7mm)

Application

Gigabit video interface

48 pin LQFP (Plastic)



Structure

Bi-CMOS IC

Absolute Maximum Ratings

• Power supply	V_{CC}	4.2	V
• Operating temperature	Topr	0 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	333	mW

Recommended Operating Condition

Supply voltage	3.3 ± 0.3	V

Block Diagram and Pin Configuration

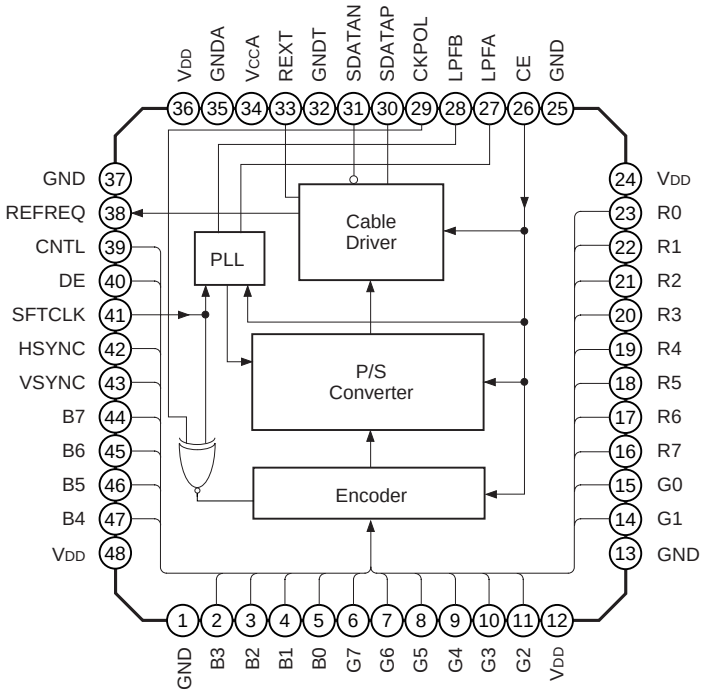


Fig. 1. Block Diagram and Pin Configuration

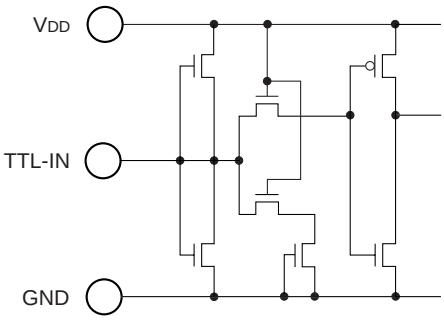
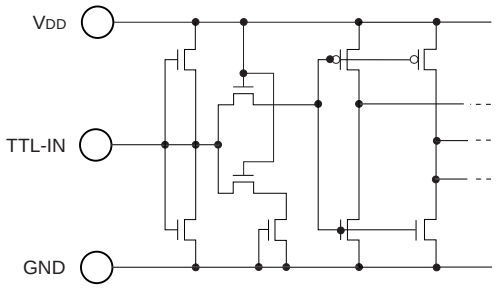
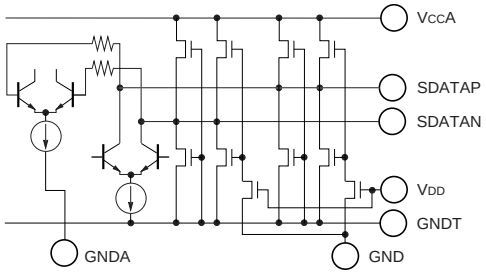
E98Y03A9X-PS

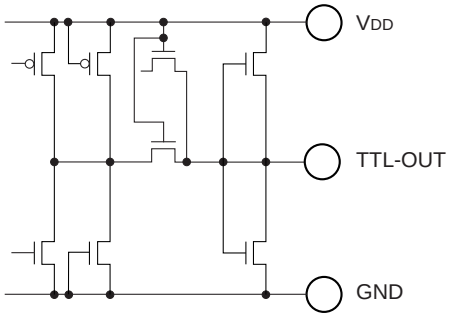
Pin Description

Power Supply/Ground

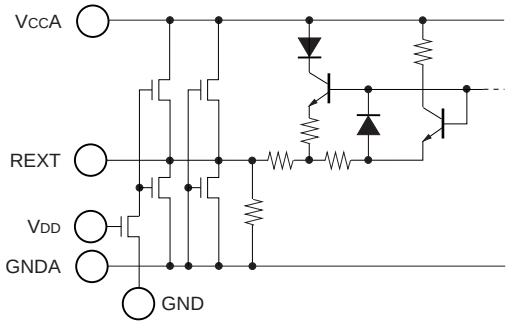
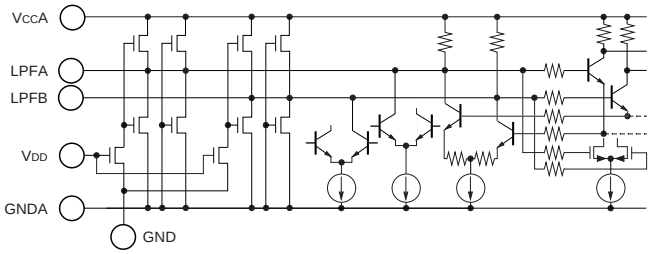
Symbol	Pin No.	Description
V_{DD}	12, 24, 36, 48	Logic power supply; connected to 3.3V ± 0.3V
GND	1, 13, 25, 37	Logic ground; connected to 0V
$V_{CC}A$	34	Analog power supply; connected to 3.3V ± 0.3V
GNDA	35	Analog ground; connected to 0V
GNDT	32	Transmission ground; connected to 0V

Digital Signal

Symbol	Pin No.	Type	Description	Equivalent Circuit
SFTCLK	41	TTL in 1	Shift clock, for the data fetch at rising or falling edge	
RED (7 to 0)	16, 17, 18, 19, 20, 21, 22, 23	TTL in 1	Pixel data. 1 pixel/shift clock input.	
GRN (7 to 0)	6, 7, 8, 9, 10, 11, 14, 15			
BLU (7 to 0)	44, 45, 46, 47, 2, 3, 4, 5			
HSYNC	42	TTL in 1	Hsync data	
VSYNC	43	TTL in 1	Vsync data	
CNTL	39	TTL in 1	Panel control data	
DE	40	TTL in 1	Data enable	
CE	26	TTL in 2	Chip enable	
CKPOL	29	TTL in 2	SFTCLK polarity	
SDATAP/N	30, 31	Tx	Serial output and Refclk request input	

Symbol	Pin No.	Type	Description	Equivalent Circuit
REFREQ	38	TTL out	Refclk request detection flag	

Special

Symbol	Pin No.	Description	Equivalent Circuit
REXT	33	SDATAP/N output current trimming. Connect to the external resistor.	
LPFA/B	27, 28	External loop filter	

Electrical Characteristics

Table 1. Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{CC}	–0.3		4.2	V	
TTL DC input voltage	V_I_T	–0.5		6.5	V	
TTL H level output current	I_{OH}_T	–20		0	mA	
TTL L level output current	I_{OL}_T	0		20	mA	
Serial output pin voltage	Vsdout	V_{CC}–1.2		V_{CC} + 0.5	V	
Ambient temperature	Ta	–55		120	°C	Under bias
Storage temperature	Tstg	–65		150	°C	

Table 2. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply voltage (Includes V_{DD} and VccA)	V_{CC}	3.0	3.3	3.6	V	
Ambient temperature	Ta	0		85	°C	

Table 3. DC Characteristics (Under the recommended operating conditions. See Table 2.)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL High level input voltage		V_{IH}_T	2		5.5	V	
TTL Low level input voltage		V_{IL}_T	0		0.8	V	
TTL High level input current		I_{IH}_T			1.0	µA	V_{IN} = V_{CC}
TTL Low level input current		I_{IL}_T	–1.0			µA	V_{IN} = 0
CE, CKPOL High level input voltage		V_{IH}_C	V_{CC} – 0.5		5.5	V	
CE, CKPOL Low level input voltage		V_{IL}_C	0		0.5	V	
CE, CKPOL High level input current		I_{IH}_C			1.0	µA	V_{IN} = V_{CC}
CE, CKPOL Low level input current		I_{IL}_C	–1.0			µA	V_{IN} = 0
TTL High level output voltage		V_{OH}_T	2.4			V	I_{OH} = –8mA
TTL Low level output voltage		V_{OL}_T			0.4	V	I_{OL} = 8mA
SDATA High level output current		I_{OH}_SD	–0.1	0	+0.5	mA	REXT = 4.7kΩ
SDATA Low level output current		I_{OL}_SD	14.5	15.7	17	mA	
SDATA High level output voltage		V_{IH}_SD	V_{CC} – 0.55			V	Common mode voltage
SDATA Low level output voltage		V_{IL}_SD			V_{CC} – 0.76	V	
Supply current	GRAYSCALE	I_{CC}	44.0	61.0	77.0	mA	@65MHz See Fig. 8
	WORSTCASE		50.0	71.0	92.0	mA	See Fig. 7

Table 4. AC Characteristics (Under the recommended operating conditions. See Table 2.)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL input rise time	Tir	0.7		5.0	ns	0.8 to 2.0V
TTL input fall time	Tif	0.7		5.0	ns	2.0 to 0.8V
Minimum SFTCLK frequency Maximum SFTCLK frequency	Fsftclk	 65.0		25.0	MHz MHz	
SFTCLK duty factor	Dsftclk	40		60	%	Vth = 1.4V
Pixel/Sync/Cntl setup time to SFTCLK	Tsetup	2.5			ns	
Pixel/Sync/Cntl hold time to SFTCLK	Thold	2.5			ns	
SDATA rise time	Tor		200		ps	20 to 80%, C_L = 2pF See Fig. 2.
SDATA fall time	Tof		200		ps	
Clock mode assert time	TAclk		50		ns	
Clock mode deassert time	TDclk		10		ns	
Idle mode assert time	TAidle		150		ns	
Idle mode deassert time	TDidle		100		ns	
PLL lock-in time	Tlockin		0.1		ms	

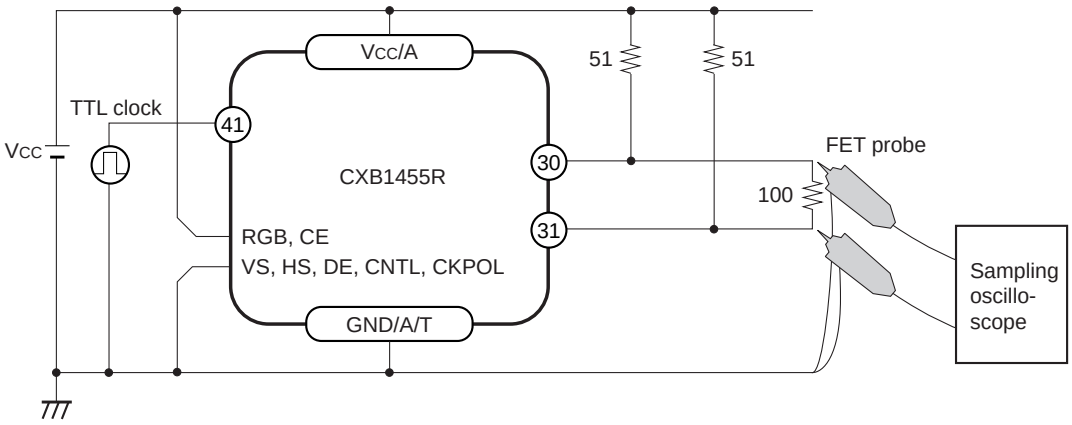
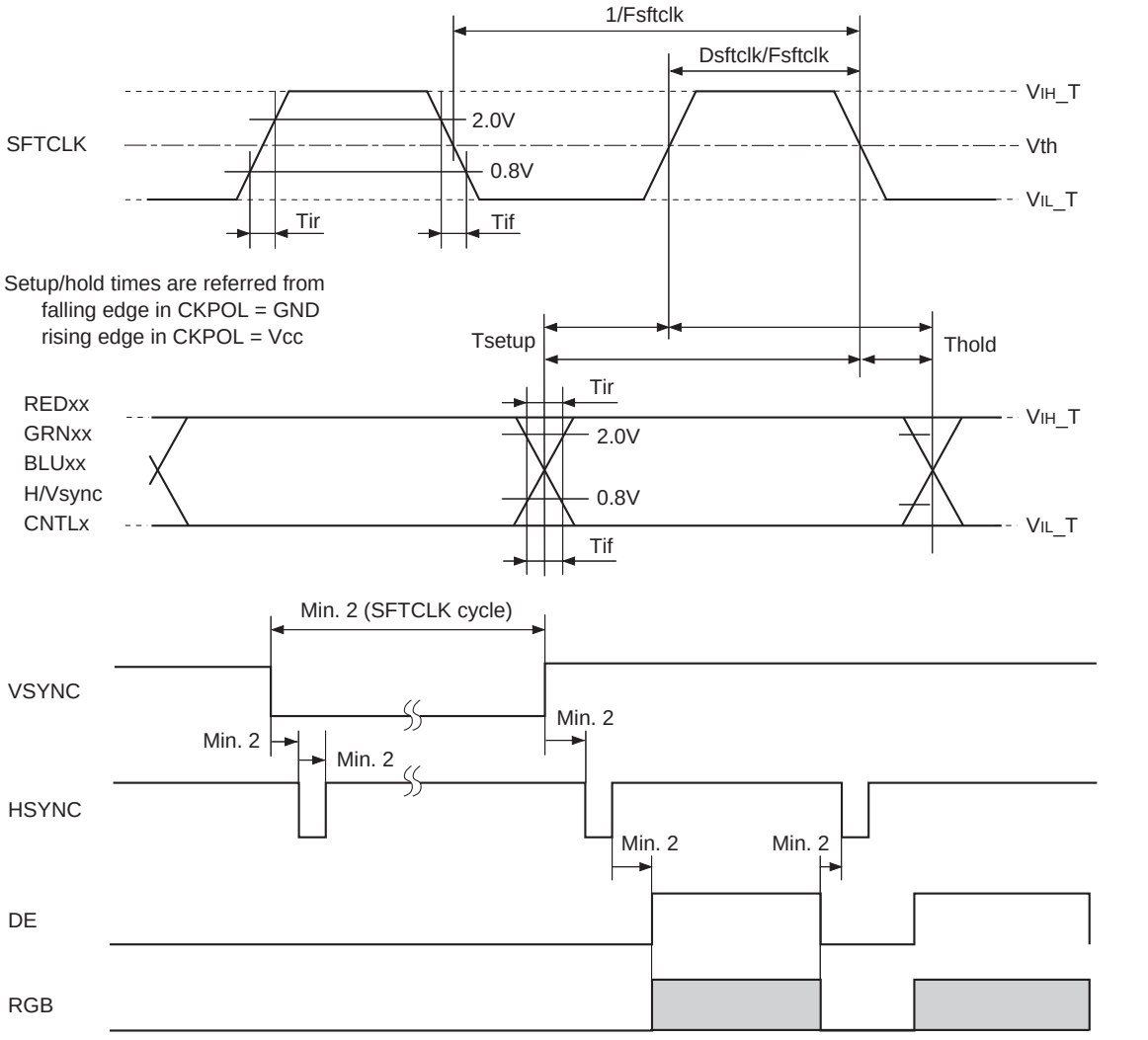


Fig. 2. SDATA waveform measurement

Timing Chart



CNTL There must be 2 SFTCLK cycles or more left between the CNTL edge and the HSYNC, VSYNC and DE edges.

Fig. 3. TTL input timing

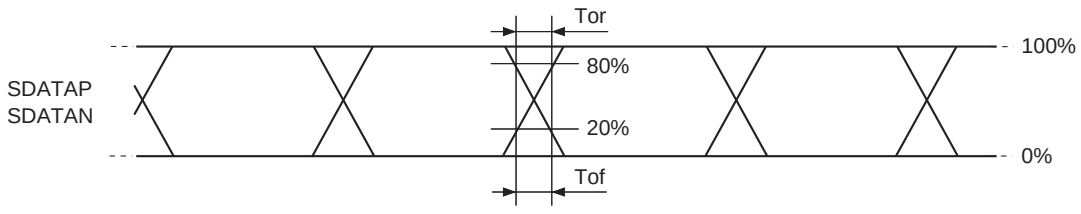


Fig. 4. Serial output timing

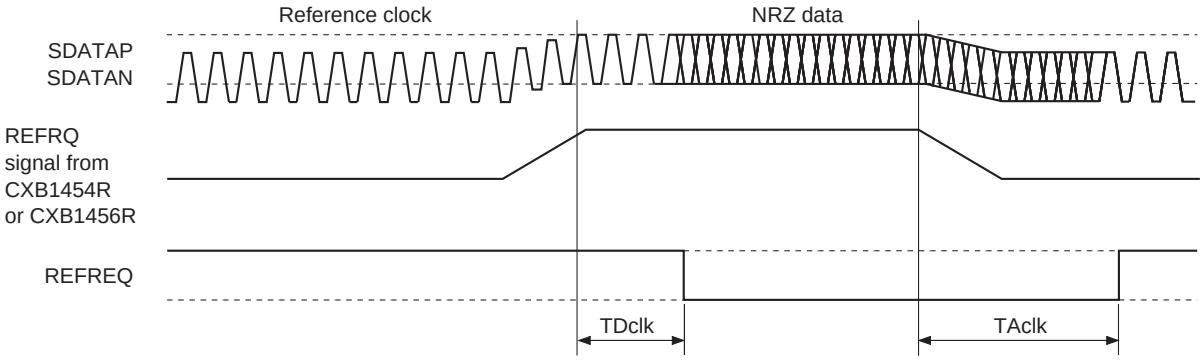


Fig. 5. Refclk request timing

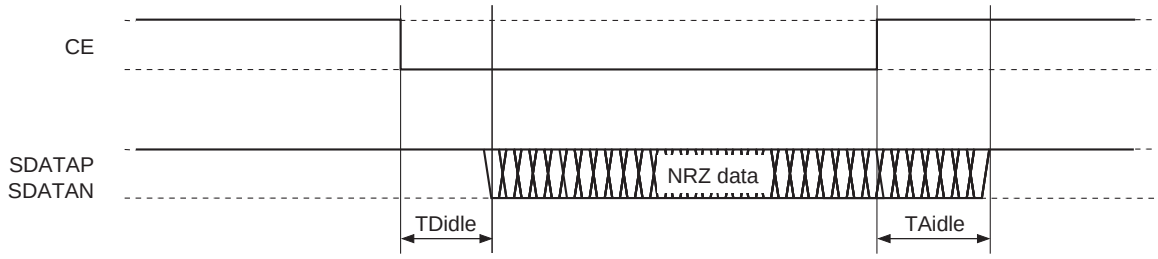


Fig. 6. Idle mode timing

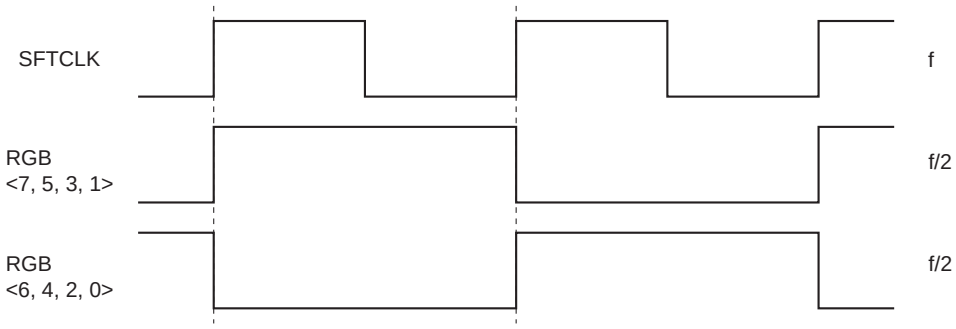


Fig. 7. Worst case test pattern

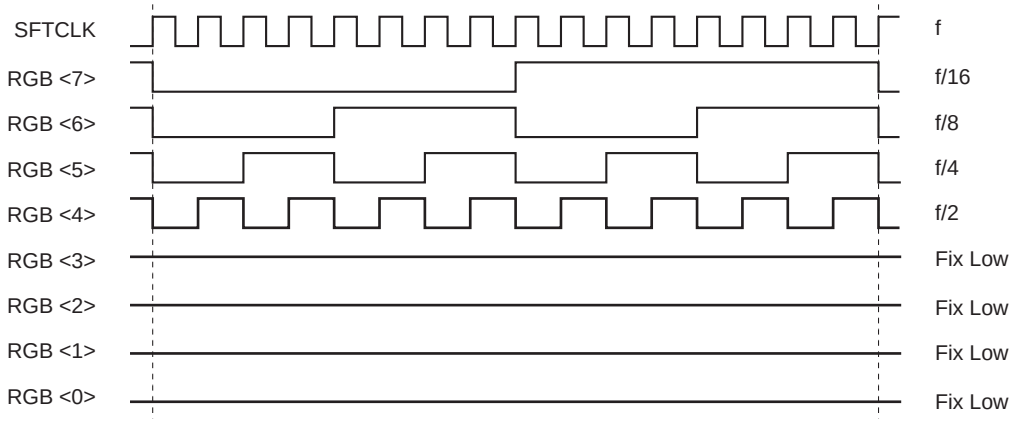


Fig. 8. 16 grayscale test pattern

CE Pin Control

The CE pin should be controlled as follows.
When the power is turned ON or SFTCLK stops, or when the SFTCLK input signal falls into the disorder while the SFTCLK frequency is varied, the CE pin should be set to Low level and the CE pin should be set to High level after the SFTCLK frequency stabilizes. (Figs. 9 and 10)

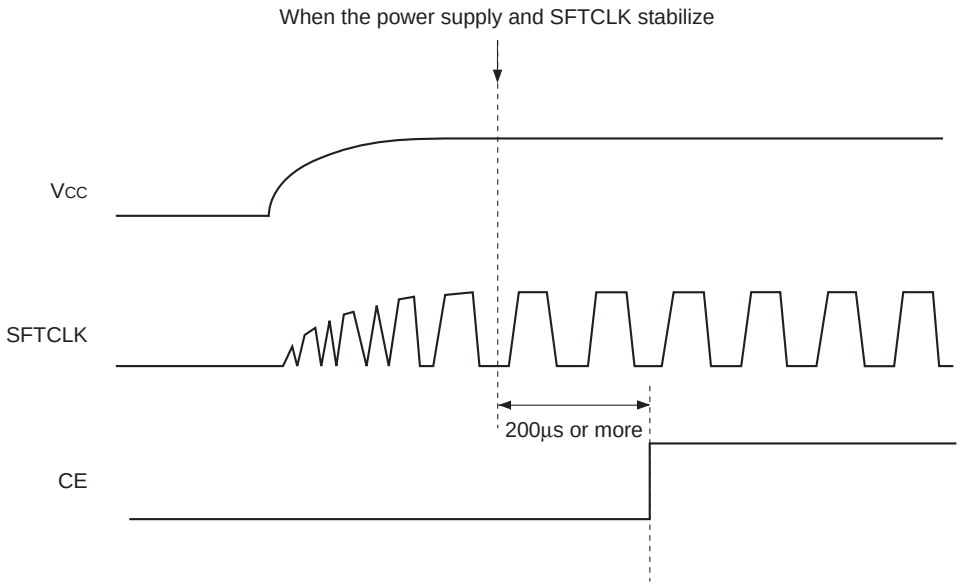
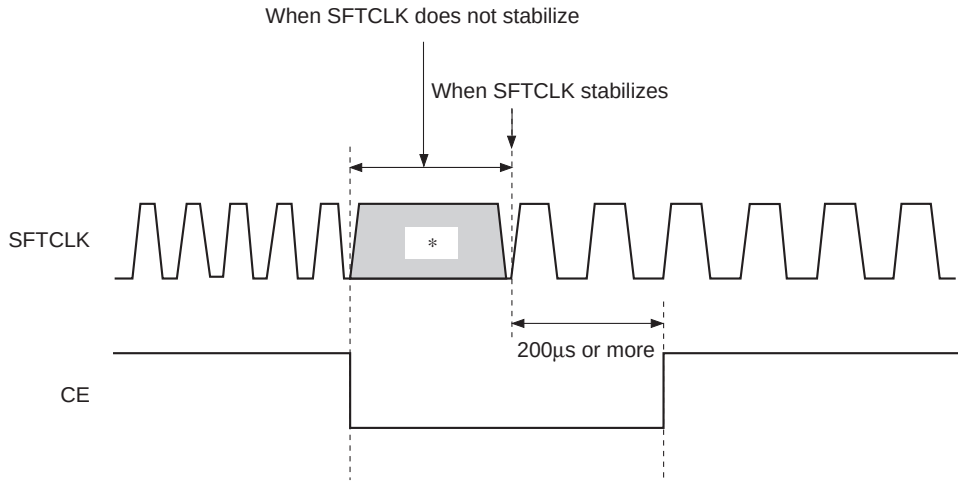


Fig. 9. CE timing when power supply is turned ON



* When SFTCLK stops or the frequencies of 15MHz or less and 75MHz or more are input.

Fig. 10. CE timing when SFTCLK input signal is not stabilized

CKPOL Pin Control

The CKPOL pin selects the SFTCLK data sampling trigger edge. (See Table 5)

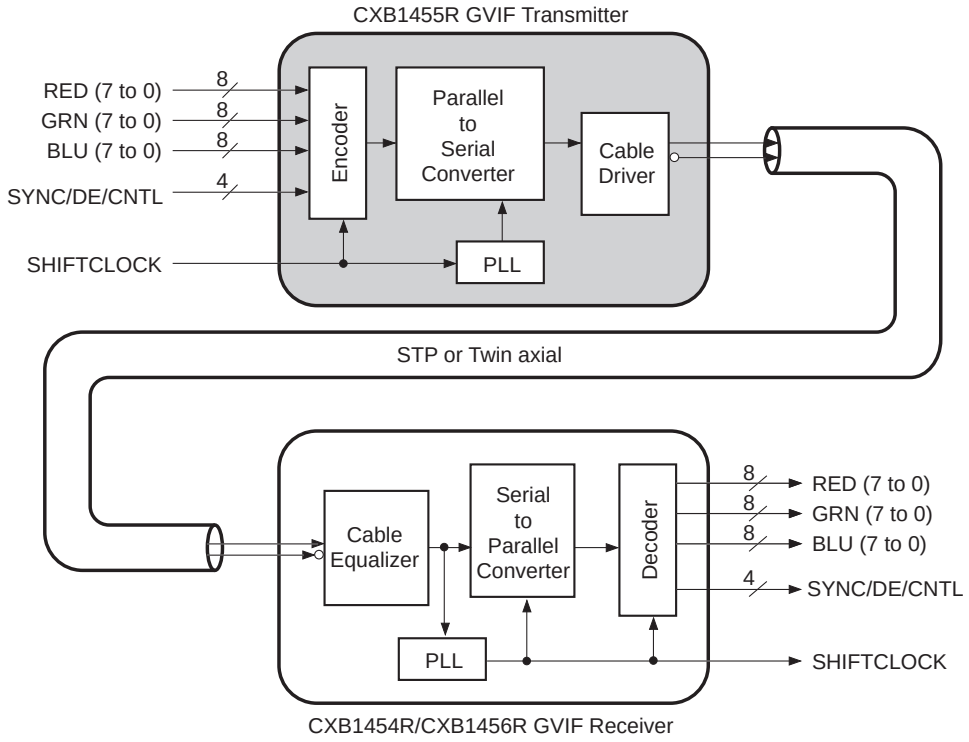
Table 5. SFTCLK polarity

CKPOL	SFTCLK data sampling trigger
L	Falling edge
H	Rising edge

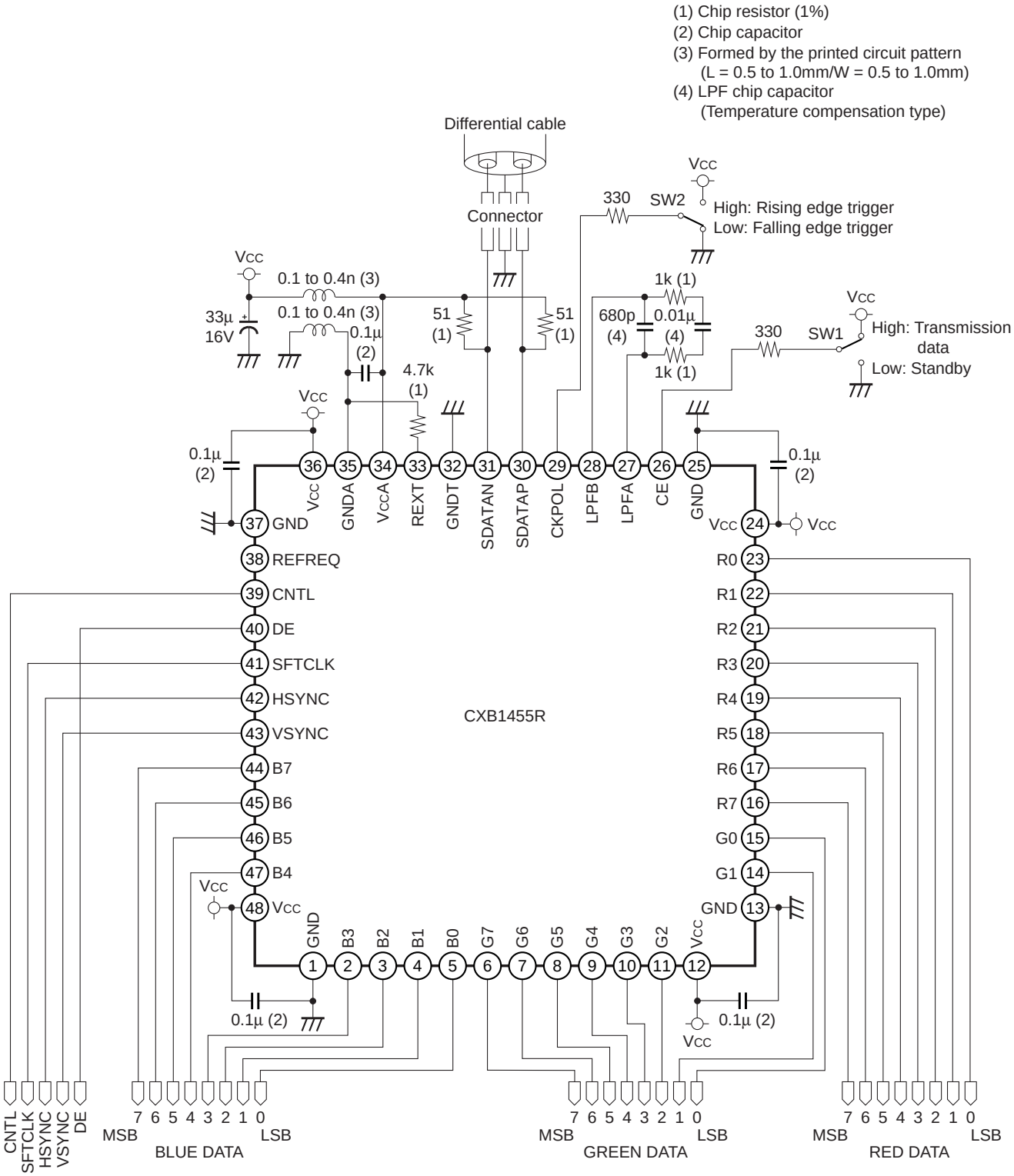
Applications

The CXB1455R GVIF transmitter is applied to the digital RGB signal transmission for
- P/C with LCD monitor
- Video-on-demand system
- Monitoring system
- Graphical controller
- Projector
- Digital TV monitor
- Automobile Navigation System

with GVIF receivers, CXB1454R/CXB1456R.

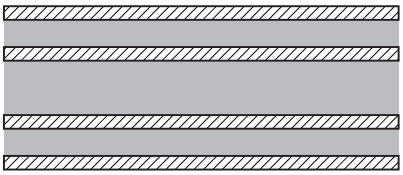


Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

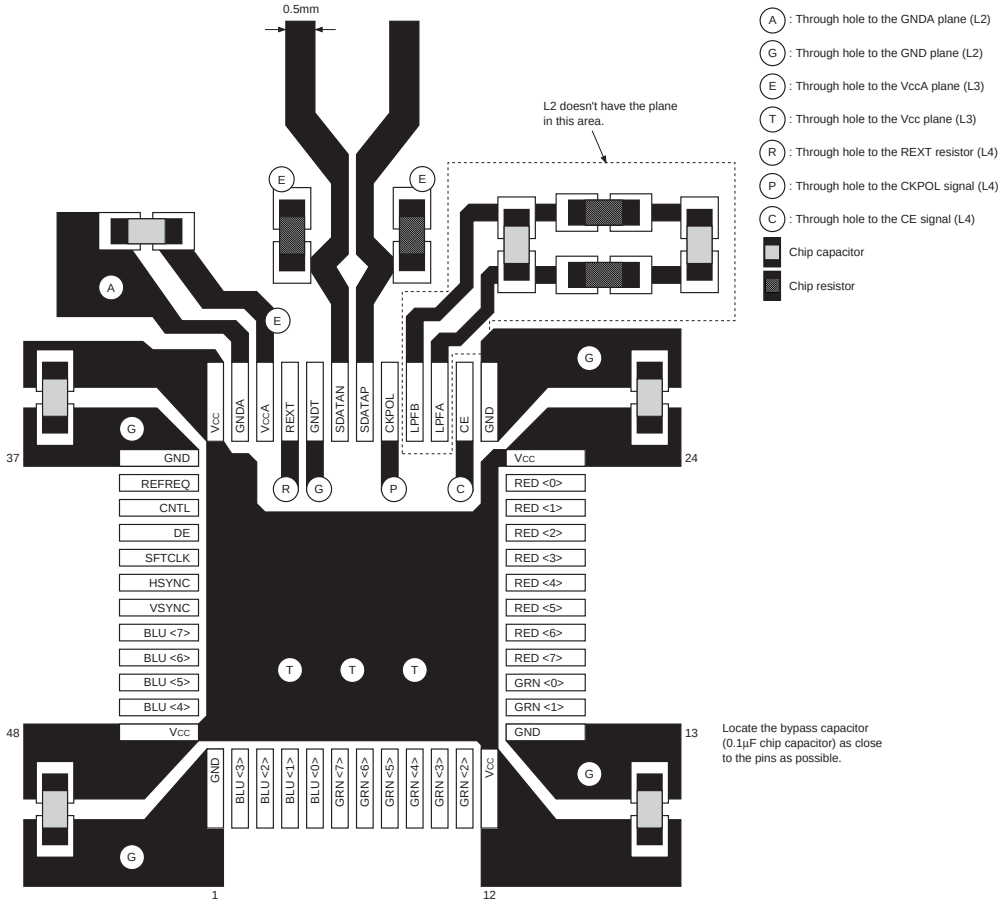
Recommended Printed Board Structure



L1: Cu plate (18µm) + solder coat
I1: Fiber-glass epoxy core (0.3mm)
L2: Cu plate (36µm)
I2: Fiber-glass epoxy core (0.8mm)
L3: Cu plate (36µm)
I3: Fiber-glass epoxy core (0.3mm)
L4: Cu plate (18µm) + solder coat

Recommended Printed Circuit Board Pattern

Example of power supply and special signal routing



Microstrip Line

The microstrip line with the characteristic impedance of 50Ω should be used to connect the LSI transmission signal pin SDATAP/N to the connector foot printer as GVIF transmits the high-speed digital signal with the maximum speed of 2Gb/s. The optimal line can be made by forming 0.5mm pattern on L1. (See the board structure shown below.) The line lengths should be the same and the through hole should be not used. Normally, L2 should be the mat GND.

Termination Elements

Locate the 51Ω termination resistors as close to the LSI as possible.

Filter Device and Reference Resistor

The capacitor and resistor connected to LPFA/B and REXT are the filter and the reference resistor. Locate them as close to the LSI as possible. Decrease the parasitic capacitance by removing the L2 GND plane under these elements and wiring.

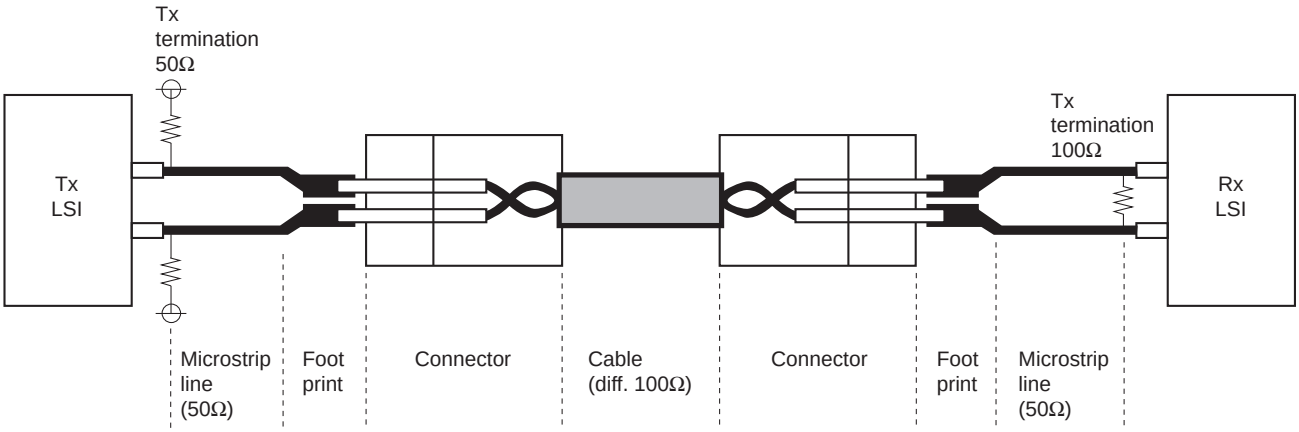
By-pass Capacitor

Locate a 0.1 µF chip capacitor as close to the pin as possible as shown in the Recommended Circuit Diagram.

Notes on Transmission System Configuration

The GVIF uses termination on both the transmitting and receiving ends, built-in equalizers, small amplitude differential signals, etc. in order to more easily resolve problems such as signal reflectance, signal attenuation and EMI which interfere with high-speed data transmission.

However, a number of cautions must be observed over the entire transmission system shown in the figure below in order to completely resolve these problems.



The transmission system has the following four requirements.

• Impedance matching shall be excellent. (Reflectance shall be low.)

A differential impedance that falls within the template shown on the following page is recommended.

• Attenuation shall be low and regular.

For the CXB1454R (built-in equalizer)

Attenuation of 15 dB (conforming to root f attenuation) @ 1 GHz or less is recommended.

See the following page.

For the CXB1456R (no equalizer)

Attenuation of 6 dB @ 1 GHz or less is recommended.

• Differential signal POS/NEG skew shall be small.

12% or less during the time for one bit is recommended.

160 ps @ VGA, 100 ps @ SVGA, 60 ps @ XGA

• EMI characteristics shall be excellent.

The following measures are effective for satisfying these requirements.

• Use a low attenuation, low skew differential cable with excellent impedance accuracy.

A cable with a two-core coaxial (shielded twisted pair) structure is recommended.

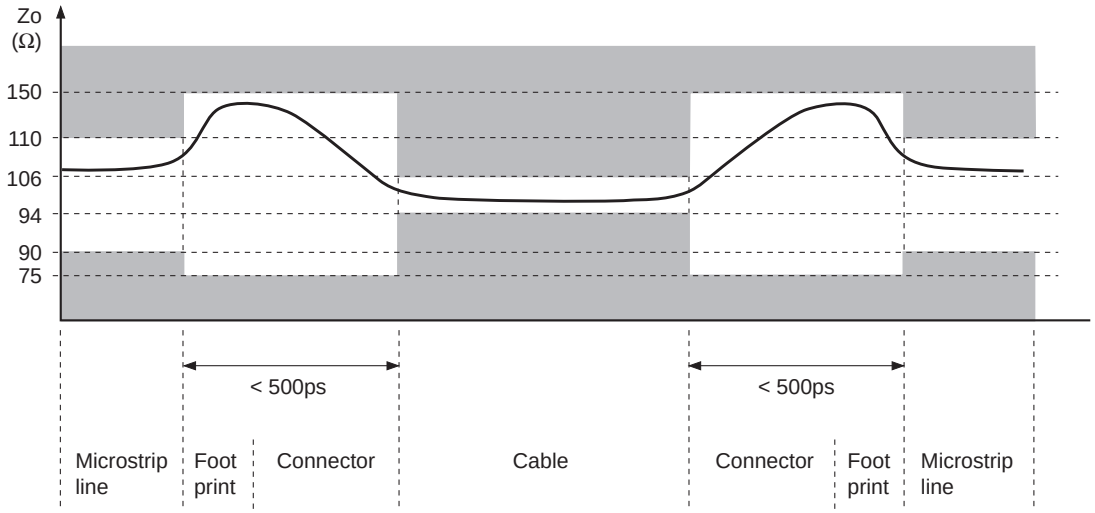
• Use low reflectance connectors.

• Take care for the connector pin assignment.

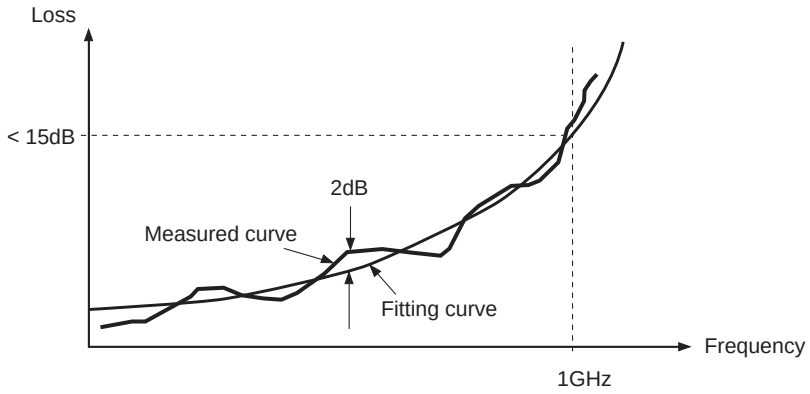
Select pins so that there is no interference with other signals and so that the positive and negative signal wiring are the same length on the board.

• Use a cable with a double shielded structure.

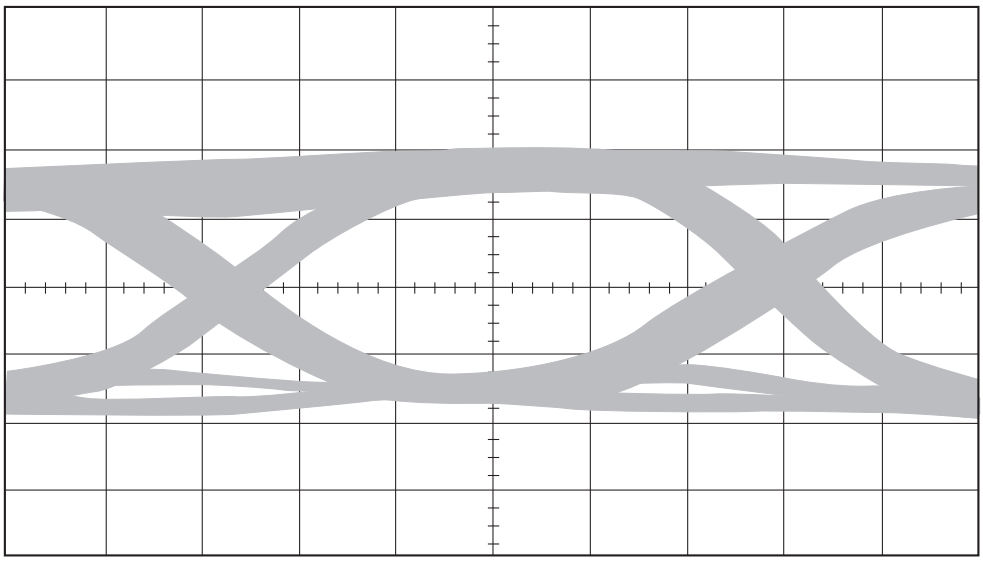
Recommended Transmission Path : Differential impedance template



Recommended Transmission Path : Attennation Characteristics

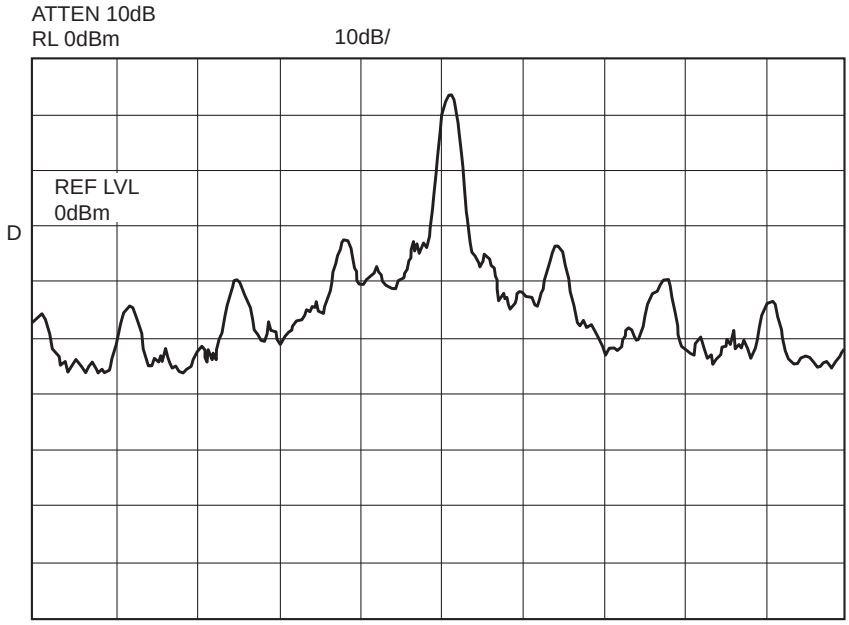


1.95Gbps SDATAP output waveform



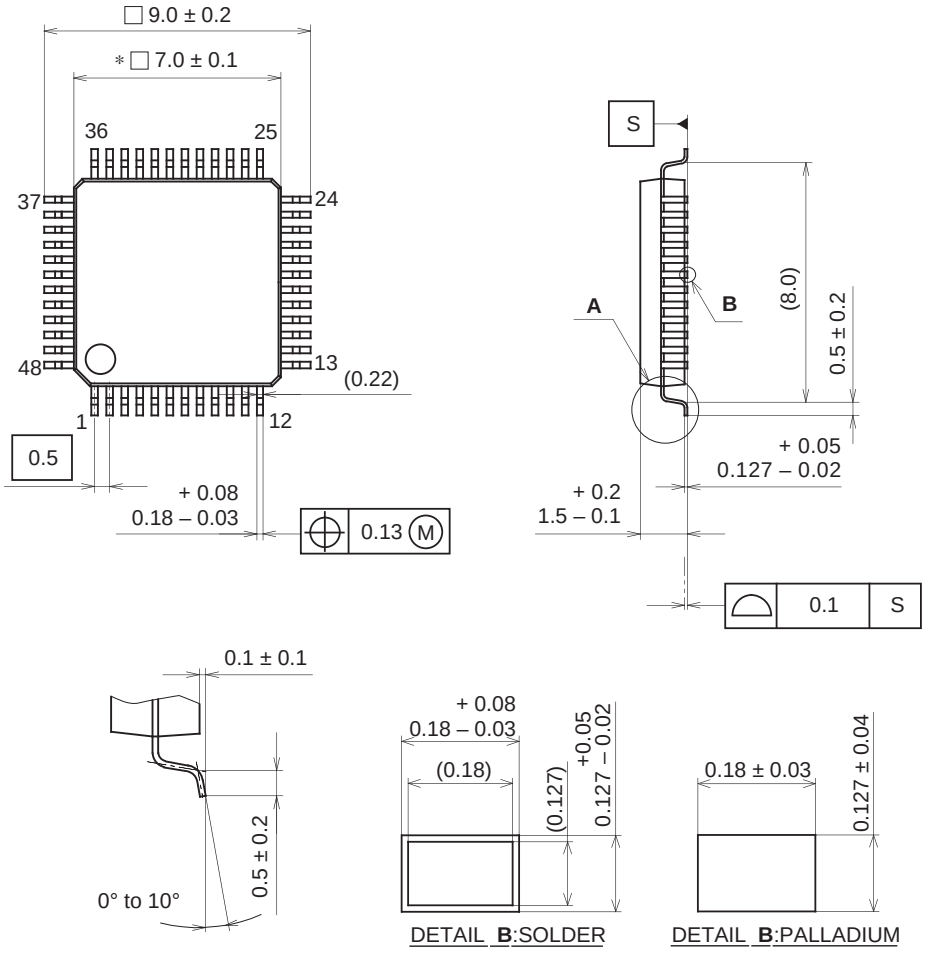
100mV/div
100ps/div

SFCLK jitter tolerance: Example of power spectrum which can be used for transmission



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**:SOLDER

DETAIL **B**:PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).