CS8182

Micropower 200 mA Low Dropout Tracking Regulator/Line Driver

The CS8182 is a monolithic integrated low dropout tracking regulator designed to provide adjustable buffered output voltage that closely tracks (±10 mV) the reference input. The output delivers up to 200 mA while being able to be configured higher, lower or equal to the reference voltages.

The output has been designed to operate over a wide range (2.8 V to 45 V) while still maintaining excellent DC characteristics. The CS8182 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45 V load dump transients and –50 V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The V_{REF}/ENABLE lead serves two purposes. It is used to provide the input voltage as a reference for the output and it also can be pulled low to place the device in sleep mode where it nominally draws less than 30 µA from the supply.

Features

- 200 mA Source Capability
- Output Tracks within ±10 mV Worst Case
- Low Dropout (0.35 V typ. @ 200 mA)
- Low Quiescent Current
- Thermal Shutdown
- Short Circuit Protection
- Wide Operating Range
- Internally Fused Leads in SO–8 Package

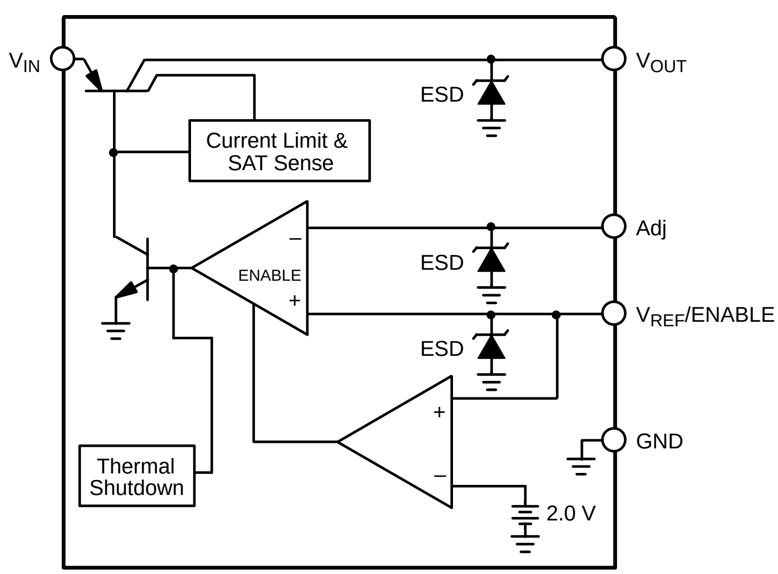
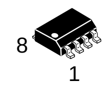


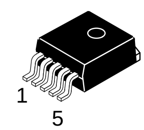
Figure 1. Block Diagram

ON Semiconductor™

http://onsemi.com

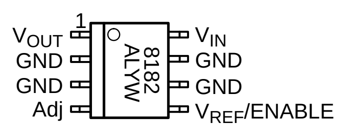


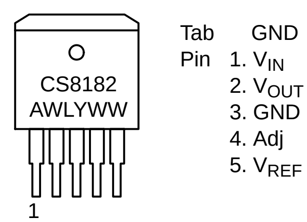
SO–8
DF SUFFIX
CASE 751



D²PAK 5–PIN
DPS SUFFIX
CASE 936A

PIN CONNECTIONS AND MARKING DIAGRAMS





A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION*

Device	Package	Shipping
CS8182YDF8	SO–8	95 Units/Rail
CS8182YDFR8	SO–8	2500 Tape & Reel
CS8182YDPS5	D²PAK 5–PIN	50 Units/Rail
CS8182YDPSR5	D²PAK 5–PIN	750 Tape & Reel

* Consult your local sales representative for SO–8 with exposed pads package option.

MAXIMUM RATINGS*

Rating		Value	Unit
Storage Temperature		–65 to 150	°C
Supply Voltage Range (continuous)		–15 to 45	V
Supply Voltage Range (normal, continuous)		3.4 to 45	V
Peak Transient Voltage (V_{IN} = 14 V, Load Dump Transient = 31 V)		45	V
Voltage Range (Adj, V_{OUT}, V_{REF}/ENABLE)		–10 to 45	V
Maximum Junction Temperature		150	°C
Package Thermal Resistance, SO–8: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 45 165	 °C/W °C/W
Package Thermal Resistance, D^2PAK, 5–Pin: Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$		 4.0 10–50**	 °C/W °C/W
ESD Capability (Human Body Model)		2.0	kV
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.
**Depending on thermal properties of substrate. $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V; V_{REF}/ENABLE > 2.75 V; –40°C < T_J < +125°C; C_{OUT} ≥ 10µF; 0.1 Ω < $C_{OUT-ESR}$ < 1.0 Ω @ 10 kHz, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Regular Output					
V_{REF} – V_{OUT} V_{OUT} Tracking Error	4.5 V ≤ V_{IN} ≤ 26 V, 100 µA ≤ I_{OUT} ≤ 200 mA, Note 2 V_{IN} = 12 V, I_{OUT} = 30 mA, V_{REF} = 5.0 V, Note 2	–10 –5.0	– –	10 5	mV mV
Dropout Voltage (V_{IN} – V_{OUT})	I_{OUT} = 100 µA I_{OUT} = 30 mA I_{OUT} = 200 mA	– – –	100 – 350	150 500 600	mV mV mV
Line Regulation	4.5 V ≤ V_{IN} ≤ 26 V, Note 2	–	–	10	mV
Load Regulation	100 µA ≤ I_{OUT} ≤ 200 mA, Note 2	–	–	10	mV
Adj Lead Current	Loop in Regulation	–	0.2	1.0	µA
Current Limit	V_{IN} = 14 V, V_{REF} = 5.0 V, V_{OUT} = 90% of V_{REF}, Note 2	225	–	700	mA
Quiescent Current (I_{IN} – I_{OUT})	V_{IN} = 12 V, I_{OUT} = 200 mA V_{IN} = 12 V, I_{OUT} = 100 µA V_{IN} = 12 V, V_{REF}/ENABLE = 0 V	– – –	15 75 30	25 150 55	mA µA µA
Reverse Current	V_{OUT} = 5.0 V, V_{IN} = 0 V	–	0.2	1.5	mA
Ripple Rejection	f = 120 Hz, I_{OUT} = 200 mA, 4.5 V ≤ V_{IN} ≤ 26 V	60	–	–	dB
Thermal Shutdown	GBD	150	180	210	°C
V_{REF}/ENABLE					
Enable Voltage	–	0.80	2.00	2.75	V
Input Bias Current	V_{REF}/ENABLE	–	0.2	1.0	µA

2. V_{OUT} connected to Adj lead.

PACKAGE PIN DESCRIPTION

Package Lead Number		Lead Symbol	Function
SO–8	D²PAK 5–PIN		
8	1	V_{IN}	Input voltage.
1	2	V_{OUT}	Regulated output.
2, 3, 6, 7	3	GND	Ground.
4	4	Adj	Adjust lead.
5	5	V_{REF}/ENABLE	Reference voltage and ENABLE input.

CIRCUIT DESCRIPTION

ENABLE Function

By pulling the V_{REF}/ENABLE lead below 2.0 V typically, (see Figure 5 or Figure 6), the IC is disabled and enters a sleep state where the device draws less than 55 μA from supply. When the V_{REF}/ENABLE lead is greater than 2.75 V, V_{OUT} tracks the V_{REF}/ENABLE lead normally.

Output Voltage

The output is capable of supplying 200 mA to the load while configured as a similiar (Figure 2), lower (Figure 4), or higher (Figure 3) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V_{REF} lead as the non–inverting.

The device can also be configured as a high–side driver as displayed in Figure 7.

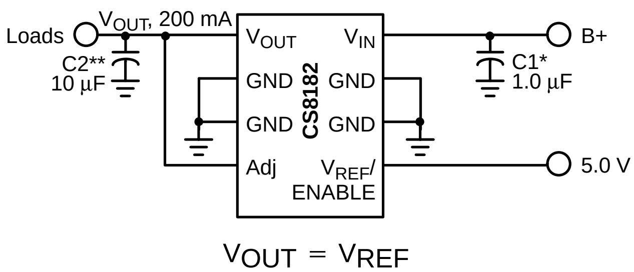


Figure 2. Tracking Regulator at the Same Voltage

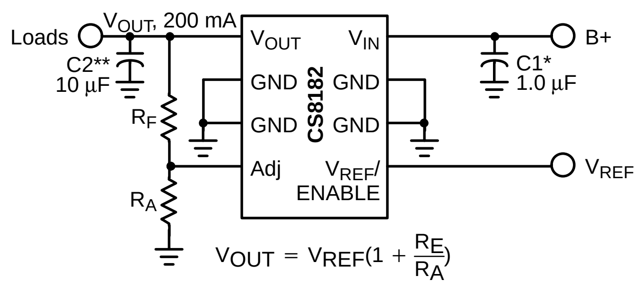


Figure 3. Tracking Regulator at Higher Voltages

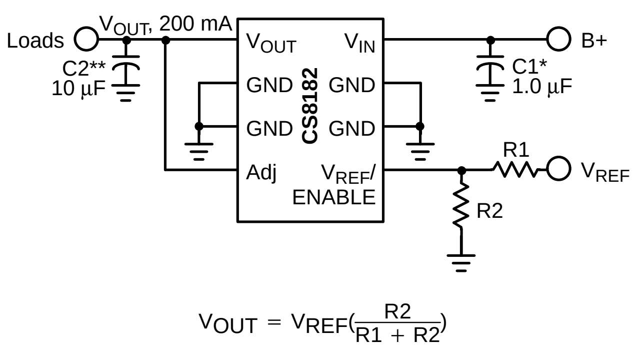


Figure 4. Tracking Regulator at Lower Voltages

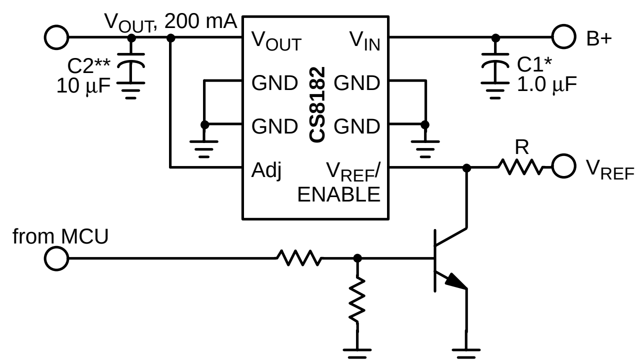


Figure 5. Tracking Regulator with ENABLE Circuit

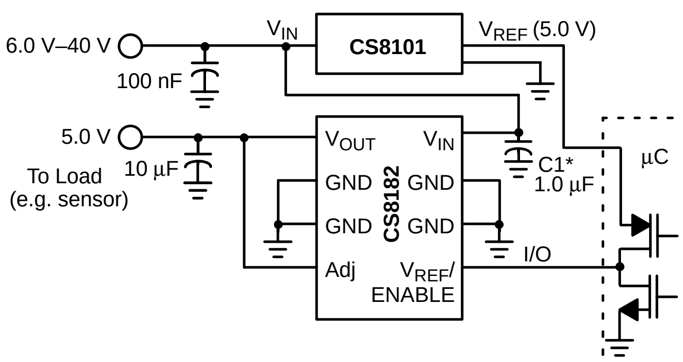


Figure 6. Alternative ENABLE Circuit

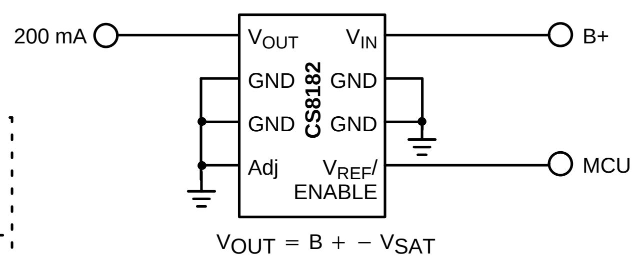


Figure 7. High–Side Driver

* C_1 is required if the regulator is far from the power source filter.
** C_2 is required for stability.

APPLICATION NOTES

Switched Application

The CS8182 has been designed for use in systems where the reference voltage on the V_{REF}/ENABLE pin is continuously on. Typically, the current into the V_{REF}/ENABLE pin will be less than 1.0 μA when the voltage on the V_{IN} pin (usually the ignition line) has been switched out (V_{IN} can be at high impedance or at ground.) Reference Figure 8.

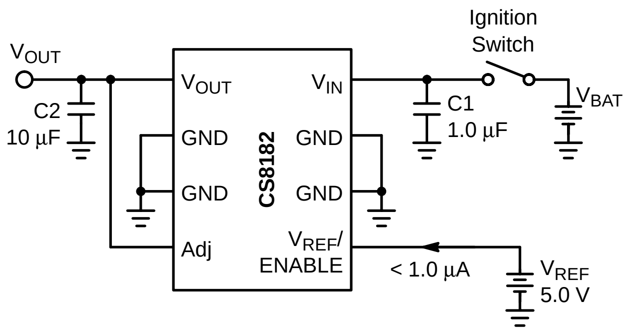


Figure 8.

External Capacitors

The output capacitor for the CS8182 is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst–case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to –40°C, a capacitor rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, “Compensation for Linear Regulators,” document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 9) is:

$$PD(max) = \{V_{IN}(max) - V_{OUT}(min)\} I_{OUT}(max) + V_{IN}(max) I_Q \qquad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current, for the application,and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of PD(max) is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^{\circ}C - T_A}{P_D} \qquad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$’s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

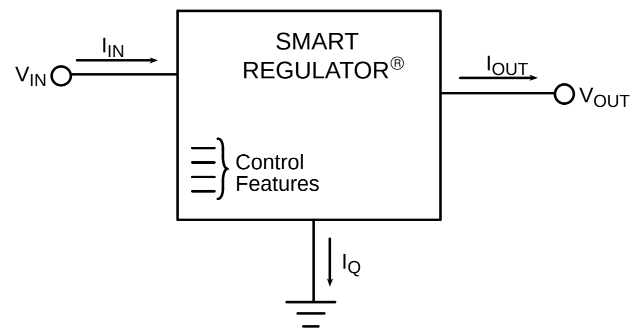


Figure 9. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \qquad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

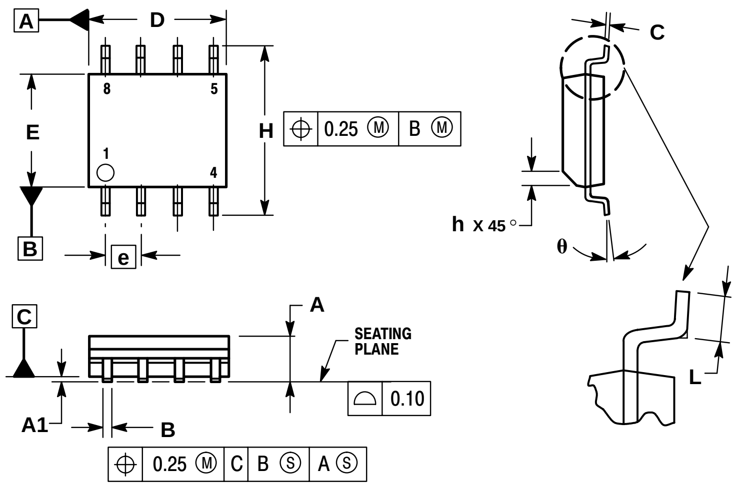
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE DIMENSIONS

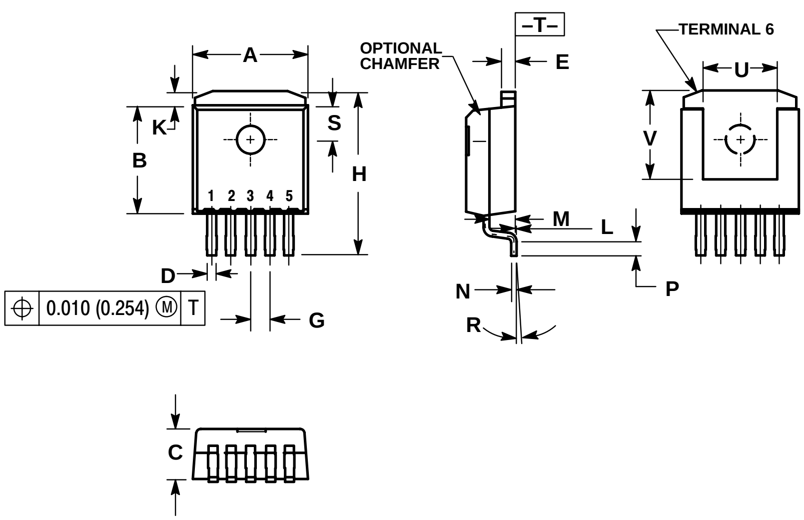
SO–8
DF SUFFIX
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

D^{2}PAK 5–PIN
D SUFFIX
CASE 936A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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