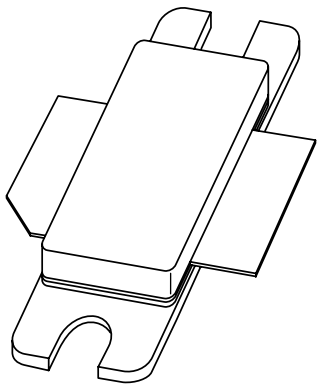


DATA SHEET



BLF2022-70 UHF power LDMOS transistor

Product specification
Supersedes data of 2002 Jul 04

2003 Feb 24

UHF power LDMOS transistor

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FEATURES

- Typical W-CDMA performance at a supply voltage of 28 V and I_{DQ} of 1 A:
 - Output power = 7.5 W (AV)
 - Gain = 12.5 dB
 - Efficiency = 20%
 - ACPR = -42 dBc at 3.84 MHz
 - $d_{im} = -36$ dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (2000 to 2200 MHz)
- Internally matched for ease of use.

APPLICATIONS

- RF power amplifiers for W-CDMA base stations and multicarrier applications in the 2000 to 2200 MHz frequency range.

DESCRIPTION

70 W LDMOS power transistor for base station applications at frequencies from 2000 to 2200 MHz.

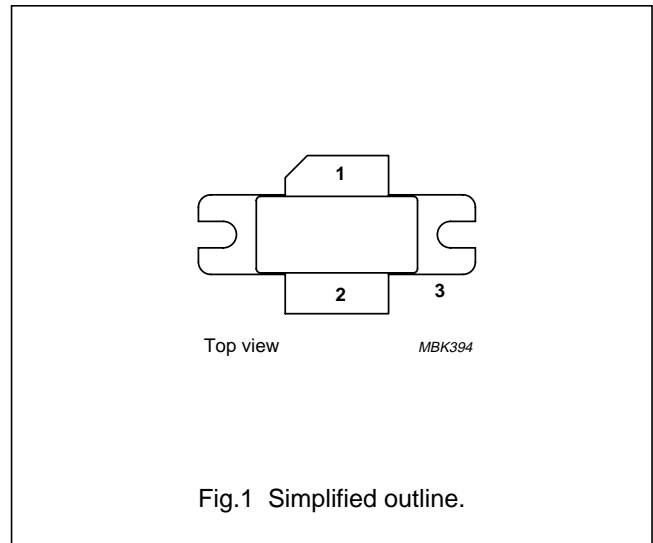
QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	$f_1 = 2170; f_2 = 2170.1$	28	65 (PEP)	>11	>30	≤ -25

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange



CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	9	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_h = 25\text{ °C}$; note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions.

CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 1.4\text{ mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 140\text{ mA}$	4.4	–	5.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$	–	–	10	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	18	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0$	–	–	25	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 5\text{ A}$	–	4.2	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GSth} + 9\text{ V}$; $I_D = 5\text{ A}$	–	0.15	–	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$; $f = 1\text{ MHz}$	–	3.4	–	pF

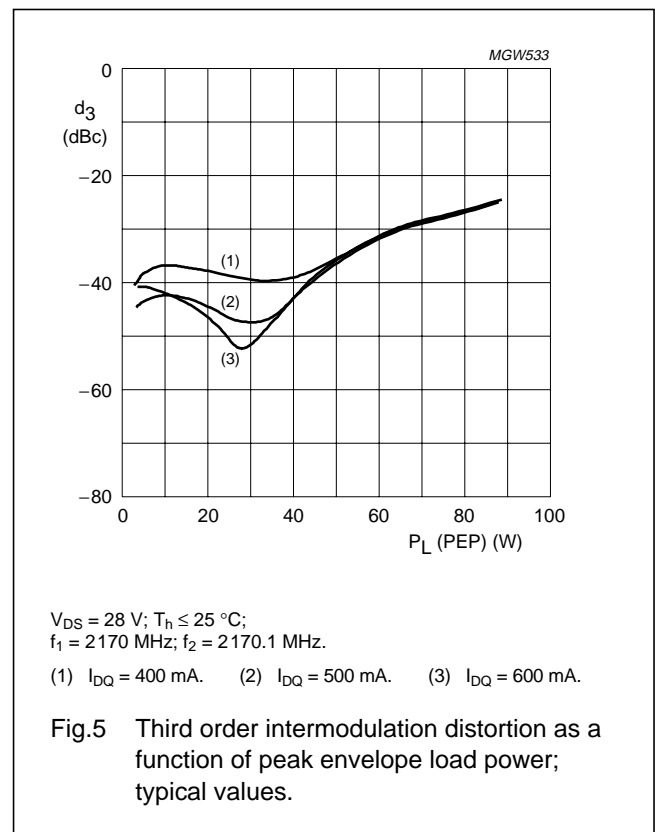
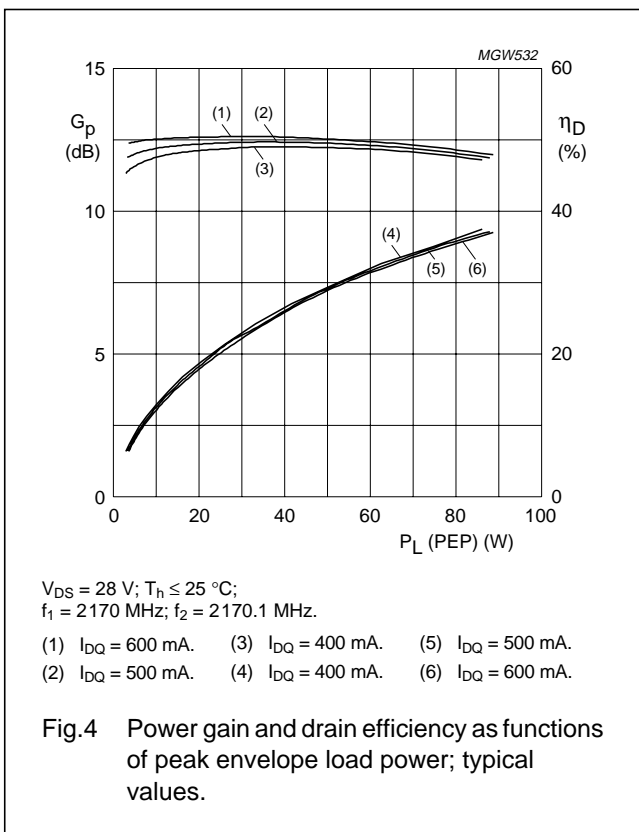
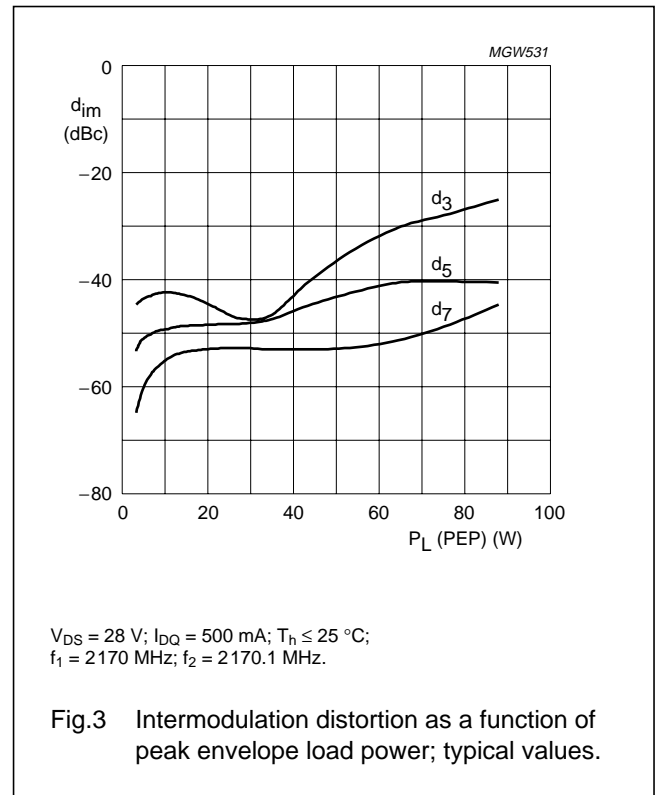
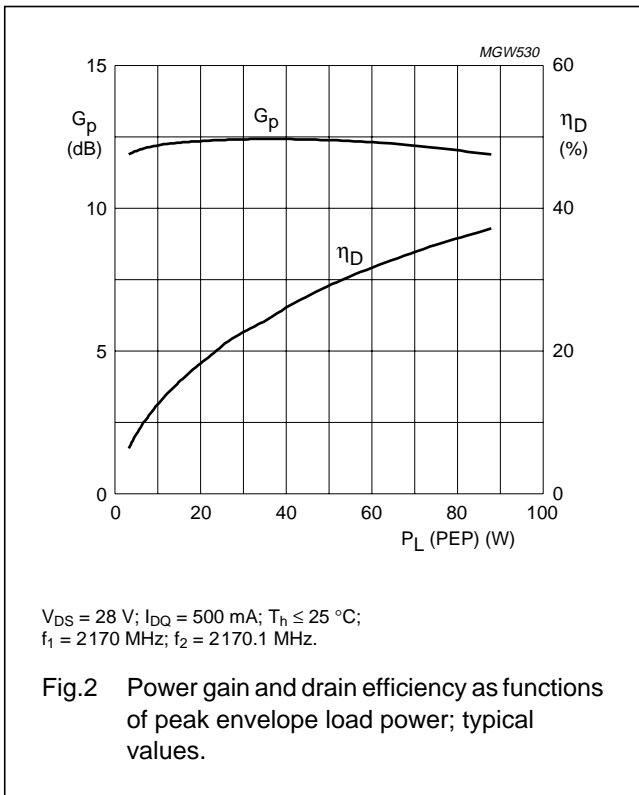
APPLICATION INFORMATIONRF performance in a common source class-AB circuit. $T_h = 25\text{ °C}$; $R_{th\ j-h} = 1.15\text{ K/W}$; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	$f_1 = 2170$; $f_2 = 2170.1$	28	500	65 (PEP)	>11	>30	≤–25

Ruggedness in class-AB operationThe BLF2022-70 is capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{DQ} = 500\text{ mA}$; $P_L = 65\text{ W (CW)}$; $f = 2170\text{ MHz}$.

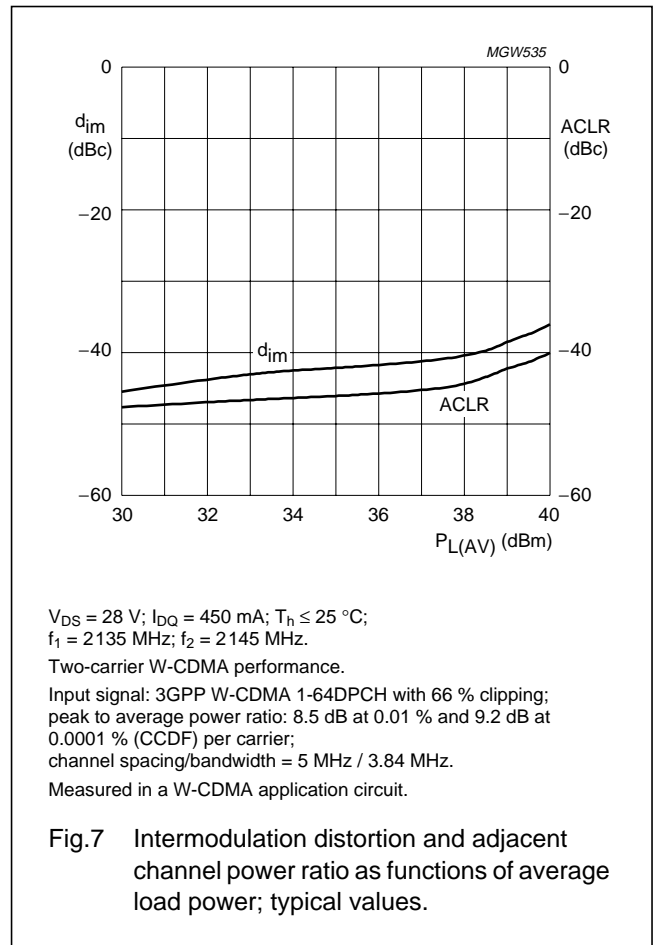
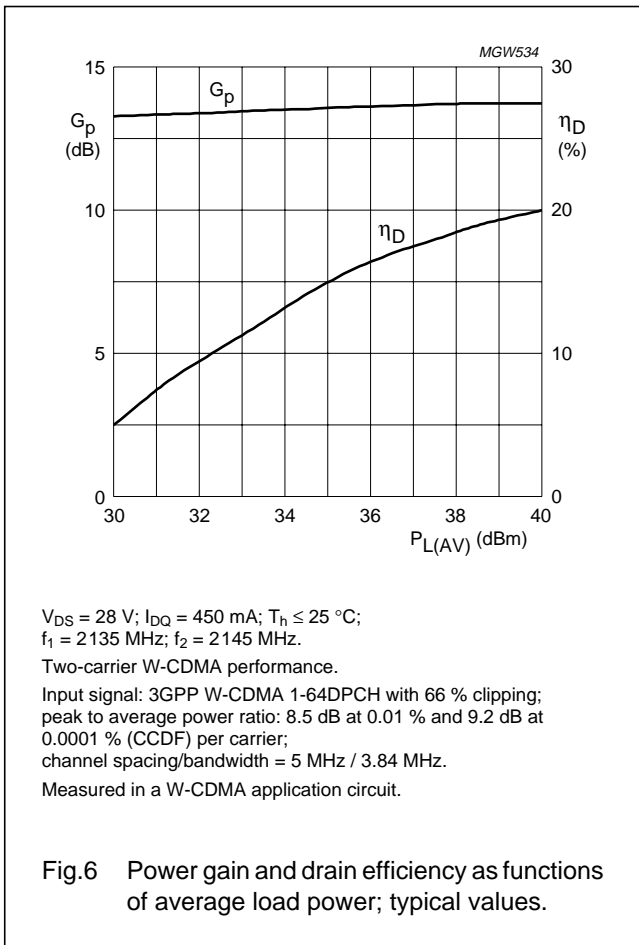
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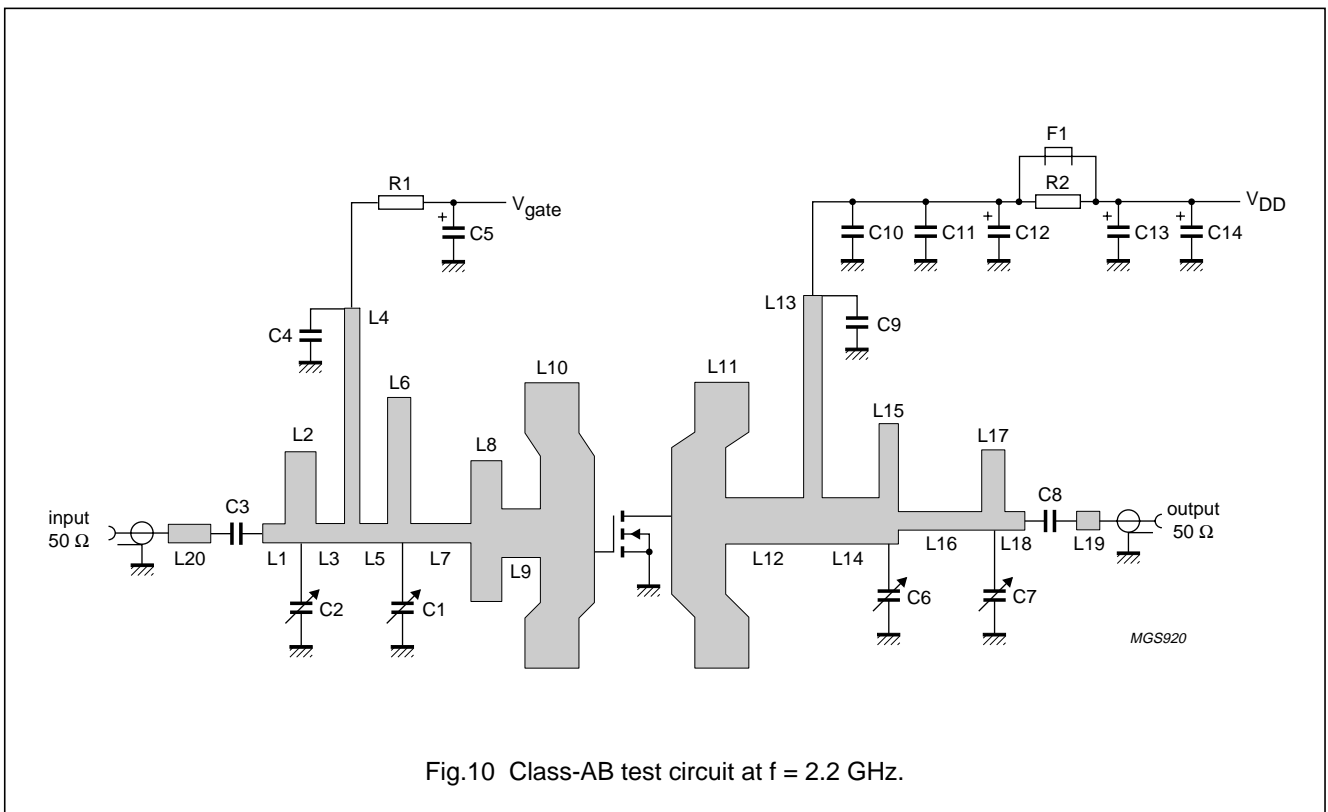
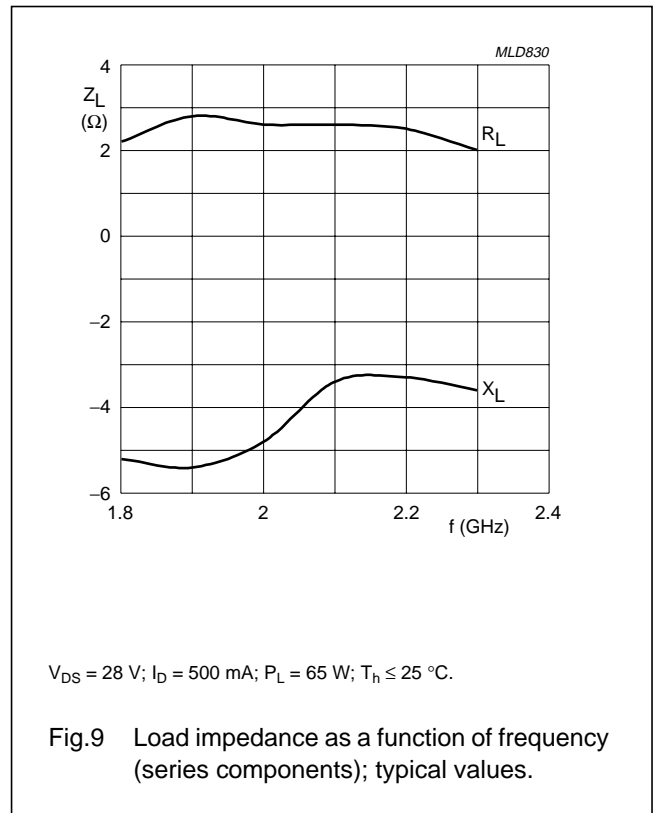
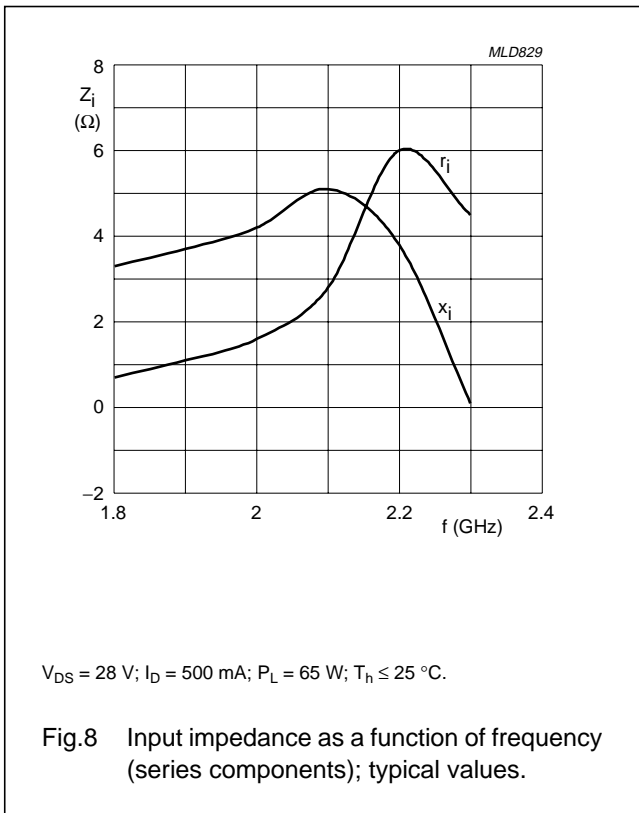
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List of components (See Figs 10 and 11)

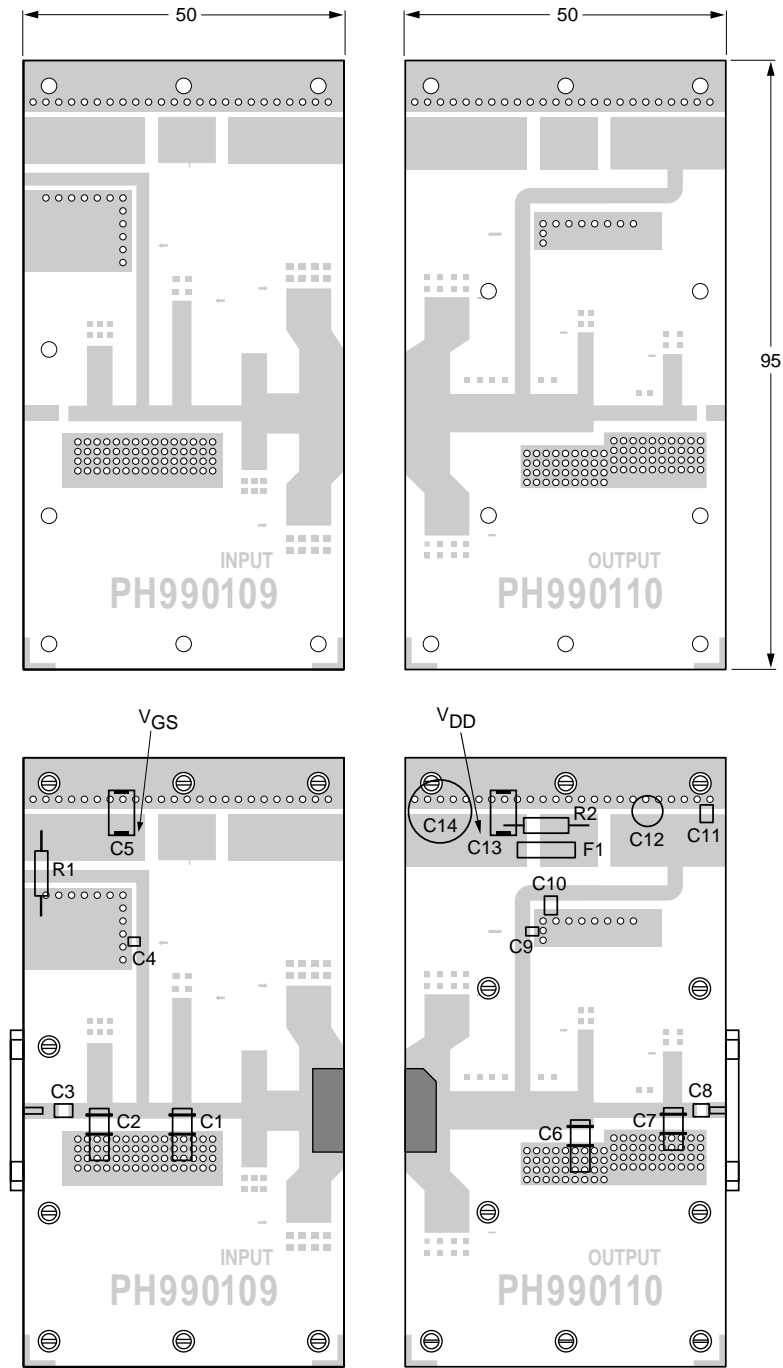
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C6, C7	Tekelec variable capacitor; type 37281	0.4 to 2.5 pF		
C3, C8	multilayer ceramic chip capacitor; note 1	12 pF		
C4, C9	multilayer ceramic chip capacitor; note 2	12 pF		
C5, C12	electrolytic capacitor	10 μ F; 100 V		2222 037 59109
C10	multilayer ceramic chip capacitor; note 1	1 nF		
C11	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C13	tantalum SMD capacitor	4.5 μ F; 50 V		
C14	electrolytic capacitor	100 μ F; 63 V		2222 037 58101
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	2.9 \times 2.4 mm	
L2	stripline; note 3	14.5 Ω	4 \times 11.7 mm	
L3	stripline; note 3	50 Ω	3.7 \times 2.4 mm	
L4	stripline; note 3	6 Ω	2 \times 30.8 mm	
L5	stripline; note 3	50 Ω	3.6 \times 2.4 mm	
L6	stripline; note 3	9.5 Ω	3 \times 18.8 mm	
L7	stripline; note 3	50 Ω	7.8 \times 2.4 mm	
L8	stripline; note 3	9.8 Ω	4 \times 18.3 mm	
L9	stripline; note 3	24.4 Ω	5 \times 6.3 mm	
L10, L11	stripline; note 3	5.1 Ω	7 \times 37 mm	
L12	stripline; note 3	25.4 Ω	10.1 \times 6 mm	
L13	stripline; note 3	5.7 Ω	2.4 \times 32.8 mm	
L14	stripline; note 3	25.4 Ω	7.4 \times 6 mm	
L15	stripline; note 3	11.3 Ω	2.5 \times 15.6 mm	
L16	stripline; note 3	50 Ω	10.8 \times 2.4 mm	
L17	stripline; note 3	16.1 Ω	3 \times 10.4 mm	
L18	stripline; note 3	50 Ω	2.3 \times 2.4 mm	
L19	stripline; note 3	50 Ω	3 \times 2.4 mm	
L20	stripline; note 3	50 Ω	5.5 \times 2.4 mm	
R1, R2	metal film resistor	10 Ω , 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$); thickness 0.79 mm.

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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.11 Component layout for 2.2 GHz class-AB test circuit.

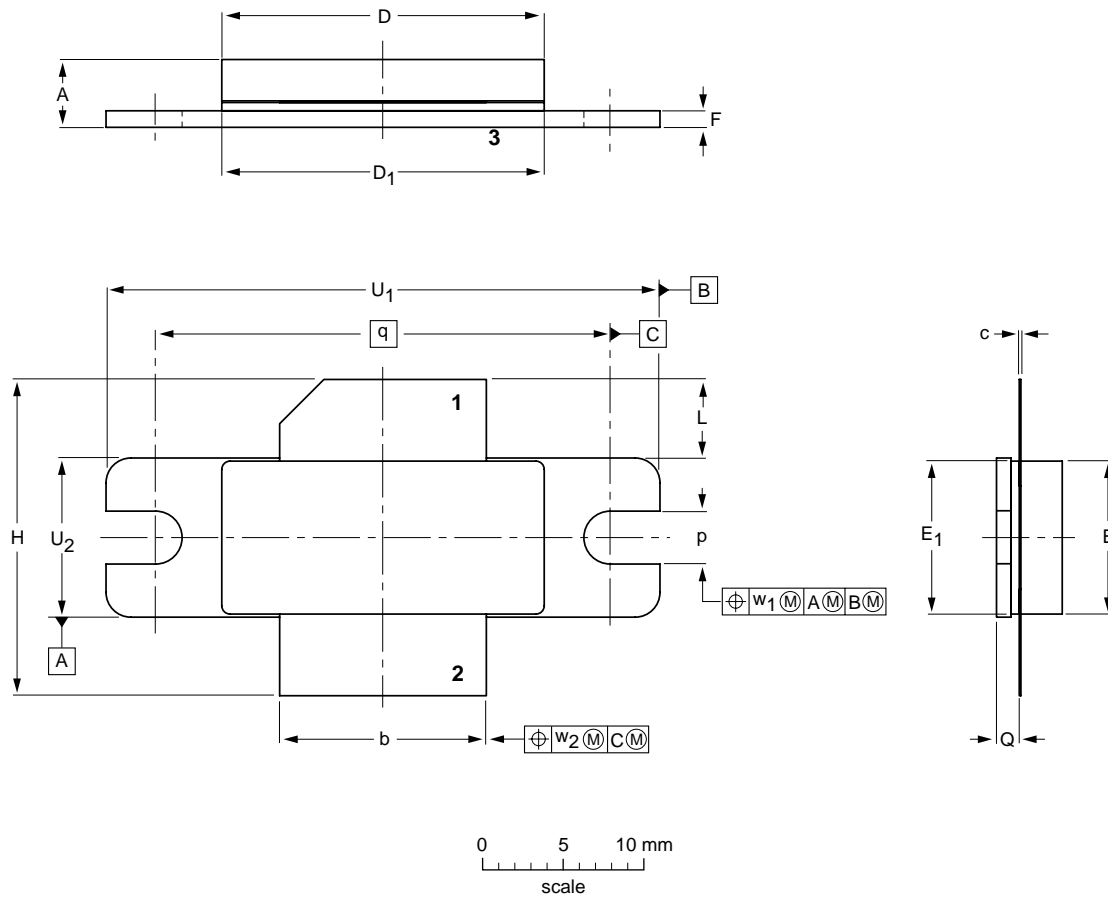
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						99-12-28 03-01-10

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DATA SHEET STATUS

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