High Speed ESD Protected Full-Duplex *i*Coupler® Isolated RS-485 Transceiver

Preliminary Technical Data

ADM2490E

FEATURES

Isolated Full Duplex RS-485/RS-422 transceiver
±8kV ESD protection on RS-485 I/O pins
16Mbps Data Rate
Complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482:1987(E)
Suitable for 5 V or 3 V operation (V_{DD1})
High common mode transient immunity: >25kV/ µs
Receiver open-circuit fail-safe design
Thermal shutdown protection
Safety and regulatory approvals pending
- **UL recognition: 2500 V rms for 1 minute per UL 1577**
- **CSA component acceptance notice #5A**
- **VDE certificate of conformity**
  - **DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01**
  - **DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000**
  - **V_{IORM} = 560 V peak**

Operating Temperature Range: -40° to 105°C
Wide body 16-lead SOIC package

APPLICATIONS

Isolated RS-485/RS-422 Interfaces
Industrial field networks
INTERBUS
Multipoint data transmission systems

FUNCTIONAL BLOCK DIAGRAM

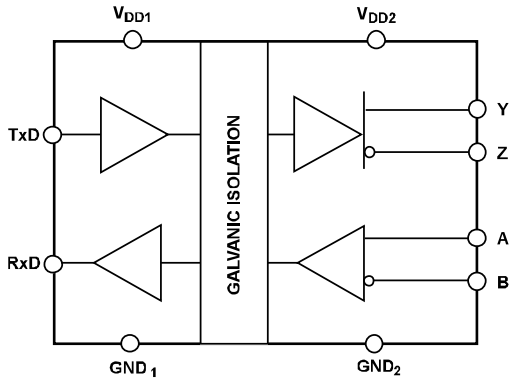

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADM2490E is an isolated data transceiver with ±8kV ESD protection suitable for high-speed full-duplex communication on multipoint transmission lines. It is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A and ISO 8482:1987(E). The device employs Analog Devices' iCoupler technology to combine a 2-channel isolator, a 3-state differential line driver and a differential input receiver into a single package.

The differential transmitter outputs and receiver inputs feature electrostatic discharge circuitry which provides protection to ±8kV using the Human Body Model (HBM). The logic side of the device can be powered with either a 5 V or a 3 V supply while an isolated 5V supply is required for the bus side.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation.

Rev. PrI

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ADM2490E—SPECIFICATIONS

Table 1. All voltages are relative to their respective ground; 2.7 ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All min/max specifications apply over the entire recommended operation range unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1}=V_{DD2}=5.0 V unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
Power Supply Current Logic Side						
TxD/RxD Data Rate < 2 Mbps	I_{DD1}			3.0	mA	2.7V≤V_{DD1}≤5.5V
Bus Side						
Power Supply Current Bus Side	I_{DD2}			4.0	mA	Unloaded
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.0		5.0	V	R=50Ω, (RS-422), Fig. 3
		1.5		5.0	V	R = 27 Ω (RS-485), Fig 3
	$\|V_{OD4}\|$	1.5		5.0	V	-7V≤V_{test1}≤12V, Fig. 4
Δ$\|V_{OD}\|$ for Complementary Output States	Δ$\|V_{OD}\|$			0.2	V	R_L=54Ω or 100Ω, Fig. 3
Common Mode Output Voltage	V_{OC}			3.0	V	R_L=54Ω or 100Ω, Fig. 3
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			0.2	V	R_L=54Ω or 100Ω, Fig. 3
Short Circuit Output Current	I_{OS}			200	mA	
Logic Inputs						
Input Threshold Low	V_{ILTxD}	0.25V_{DD1}			V	
Input Threshold High	V_{IHTRxD}			0.7V_{DD1}	V	
TxD Input Current	I_{TxD}	-10	0.01	10	µA	
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	-0.2		0.2	V	
Input Voltage Hysteresis	V_{HYS}		70		mV	V_{OC}=0V
Input Current (A, B)	I_I			1.0	mA	V_{OC}=12V
		-0.8			mA	V_{OC}=-7V
Line Input Resistance	R_{IN}	12			kΩ	
Logic Outputs						
Output Voltage Low	V_{OLRxD}		0.0	0.4	V	I_{ORxD}=4mA, V_A-V_B=-0.2V
Output Voltage High	V_{OHRxD}	V_{DD1} - 0.3	V_{DD1}-0.2		V	I_{ORxD}=-1.5 mA, V_A-V_B=0.2V

TIMING SPECIFICATIONS (T_A = -40°C to +85°C)

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		16			Mbps	
Propagation Delay	t_{PLH}, t_{PHL}		45	60	ns	R_L=54Ω, C_{L1}=C_{L2}=100pF, Fig. 5
Pulse Width Distortion, PWD=|t_{PYLH}-t_{PYHL}|, PWD=|t_{PZLH}-t_{PZHL}|	t_{PWD}, t_{PWD}			7	ns	R_L=54Ω, C_{L1}=C_{L2}=100pF, Fig. 5
Single Ended Output Rise/Fall Time	t_R, t_F			20	ns	R_L=54Ω, C_{L1}=C_{L2}=100pF, Fig. 5
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL},			60	ns	C_L=15pF, Fig. 6
Pulse Width Distortion, PWD=|t_{PLH}-t_{PHL}|,	t_{PWD},			10	ns	C_L=15pF, Fig. 6

TIMING SPECIFICATIONS (T_A = -40°C to +105°C)

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		10			Mbps	
Propagation Delay	t_{PYLH}, t_{PYHL}, t_{PZLH}, t_{PZHL}		45	60	ns	R_L=54Ω, C_{L1}=C_{L2}=100pF, Fig. 5
Pulse Width Distortion, PWD=|t_{PYLH}-t_{PYHL}|, PWD=|t_{PZLH}-t_{PZHL}|	t_{PWD}, t_{PWD}			9	ns	R_L=54Ω, C_{L1}=C_{L2}=100pF, Fig. 5
Single Ended Output Rise/Fall Time	t_R, t_F			35	ns	R_L=54Ω, C_{L1}=C_{L2}=100pF, Fig. 5
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL},			60	ns	C_L=15pF, Fig. 6
Pulse Width Distortion, PWD=|t_{PLH}-t_{PHL}|,	t_{PWD},			10	ns	C_L=15pF, Fig. 6

ABSOLUTE MAXIMUM RATINGS

Table 2. Ambient temperature = 25 °C unless otherwise noted. All voltages are relative to their respective ground.

Parameter	Rating
Storage temperature	-55°C to 150°C
Ambient operating temperature	-40°C to 105°C
V_{DD1}	−0.5 V to +7 V
V_{DD2}	−0.5 V to +6 V
Logic input voltages	-0.5V to V_{DD1} + 0.5V
Bus terminal voltages	-9V to 14V
Logic output voltages	-0.5V to V_{DD1} + 0.5V
Average output current, per pin	±35mA
ESD (human body model) on A,B,Y and Z pins	±8kV
θ_{JA} Thermal Impedance	73°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination.

ADM2490E CHARACTERISTICS

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	

[1] Device considered a two-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together, and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADM2490E is to be approved by the following organizations:

Table 4.

Organization	Approval Type	Notes
UL	To be recognized under 1577 component recognition program.	In accordance with UL1577, each ADM2490E is proof-tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).
CSA	To be approved under CSA Component Acceptance Notice #5A.	
VDE	To be certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01	In accordance with VDE 0884, each ADM2490E is proof-tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration.
Minimum External Air Gap (Clearance)	L(I01)	7.45 min	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance along body.
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89,).

VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on packages denotes VDE 0884 approval for 560 V peak working voltage.

Table 6.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110 for rated mains voltage			
≤150 V rms		I to IV	
≤300 V rms		I to III	
≤400 V rms		I to II	
Climatic classification		40/85/21	
Pollution degree (DIN VDE 0110, Table 1)		2	
Maximum working insulation voltage	V_{IORM}	560	V_{PEAK}
Input to output test voltage, Method b1	V_{PR}	1050	V_{PEAK}
$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC			
Input to output test voltage, Method a			
(After environmental tests, Subgroup 1)			
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		896	V_{PEAK}
(After input and/or safety test, Subgroup 2/3)			
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	V_{PEAK}
Highest allowable overvoltage			
(Transient overvoltage, t_{TR} = 10 sec)	V_{TR}	4000	V_{PEAK}
Safety-limiting values (maximum value allowed in the event of a failure. See thermal derating curve)			
Case temperature	TS	150	°C
Input current	$I_{S, INPUT}$	265	mA
Output current	$I_{S, OUTPUT}$	335	mA
Insulation resistance at Ts, V_{IO} = 500 V	Rs	$>10^9$	Ω

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

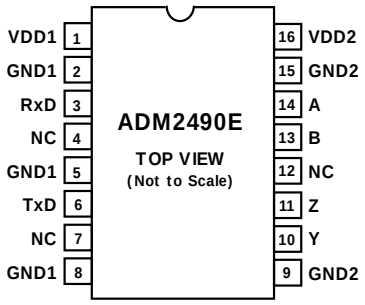

Figure 2. ADM2490E Pin Out

Table 7.Preliminary Pin Function Description

Pin(s)	Mnemonic	Function
1	V_{DD1}	Power supply, logic side. Decoupling capacitor to GND_1 required, capacitor value should be between 0.01 µF and 0.1 µF.
2,5,8	GND_1	Ground, logic side
3	RxD	Receiver output.
4,7,12	NC	No Connect, pins must be left floating
6	TxD	Transmit data
9,15	GND_2	Ground, bus side
16	V_{DD2}	Power supply, bus side. Decoupling capacitor to GND_2 required, capacitor value should be between 0.01 µF and 0.1 µF.
9, 15	GND_2	Ground, bus side
11	Z	Driver Inverting Output
10	Y	Driver Non-inverting Output
13	B	Receiver Inverting Input
14	A	Receiver Non-inverting Input

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TEST CIRCUITS

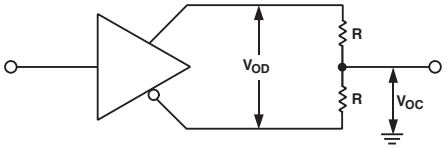

Figure 3. Driver Voltage Measurement

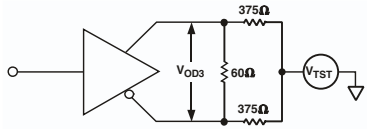

Figure 4. Driver Voltage Measurement

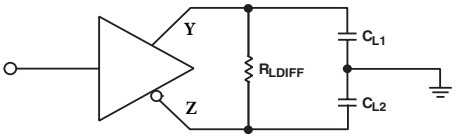

Figure 5. Driver Propagation Delay

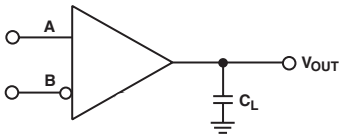

Figure 6. Receiver Propagation Delay

SWITCHING CHARACTERISTICS

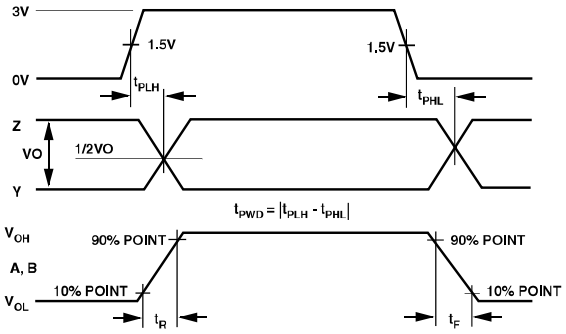

Figure 7. Driver Propagation Delay, Rise/Fall Timing

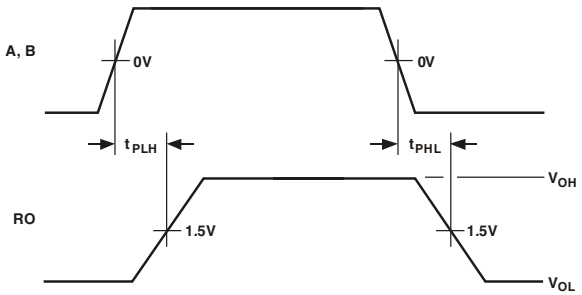

Figure 8. Receiver Propagation Delay

TYPICAL PERFORMANCE CHARACTERISTICS

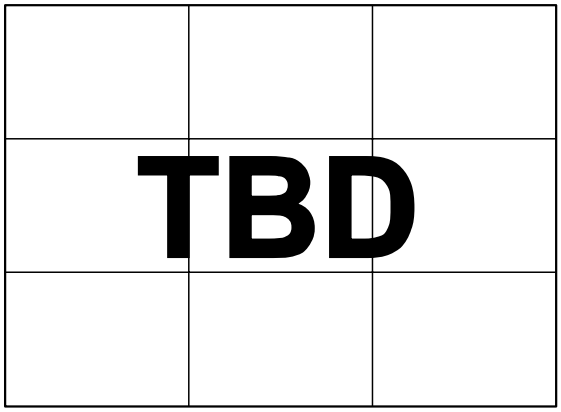

Figure 3. Unloaded Supply Current vs. Temperature

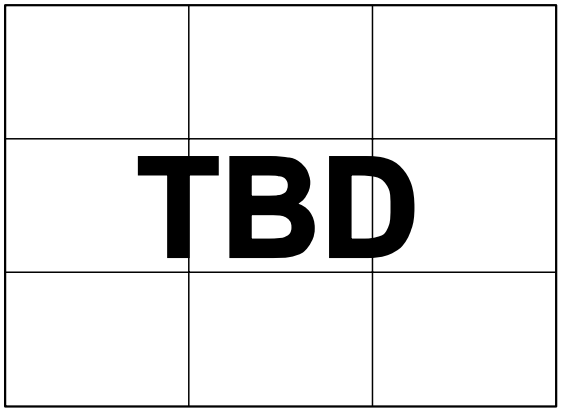

Figure 6. Driver/Receiver Propagation Delay, Low to High (R_{LDiff} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

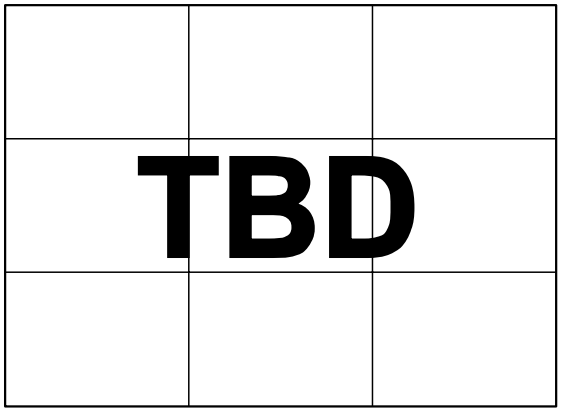

Figure 4. Driver Propagation Delay vs. Temperature

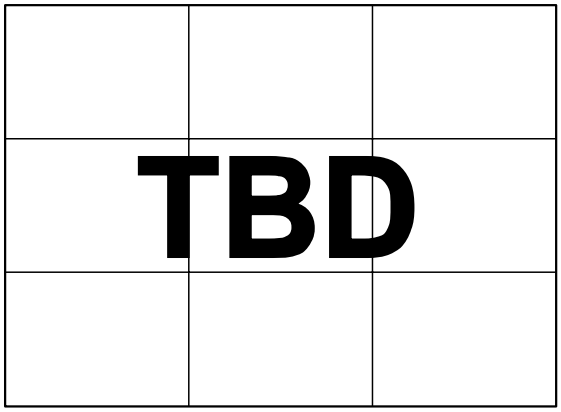

Figure 7. Driver/Receiver Propagation Delay, High to Low (R_{LDiff} = 54 Ω, C_{L1} = C_{L2} = 100 pF)

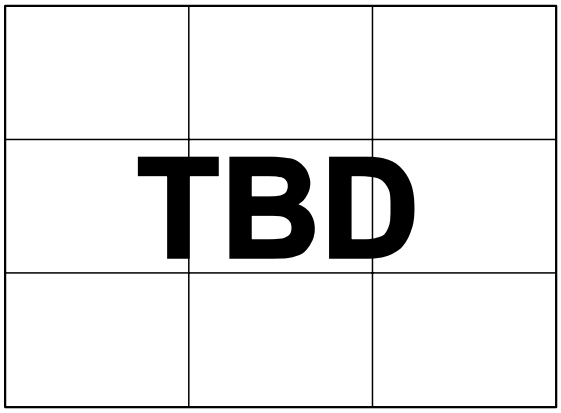

Figure 5. Receiver Propagation Delay vs. Temperature

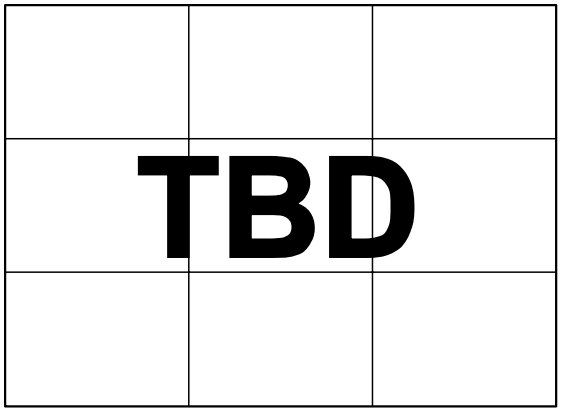

Figure 8. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

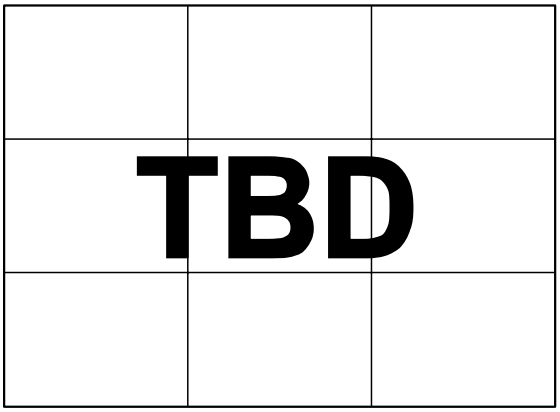

Figure 9. Output Current vs. Receiver Output High Voltage

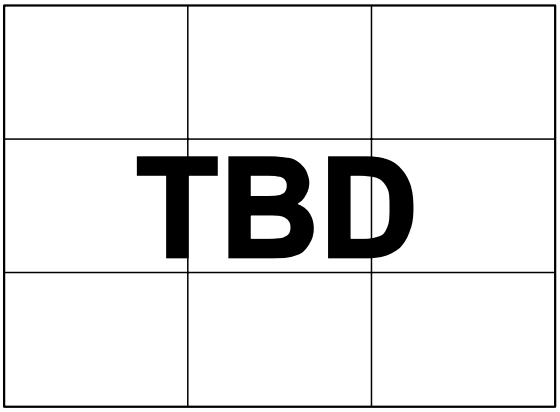

Figure 12. Receiver Output Low Voltage vs. Temperature
I_{RxD} = –4 mA

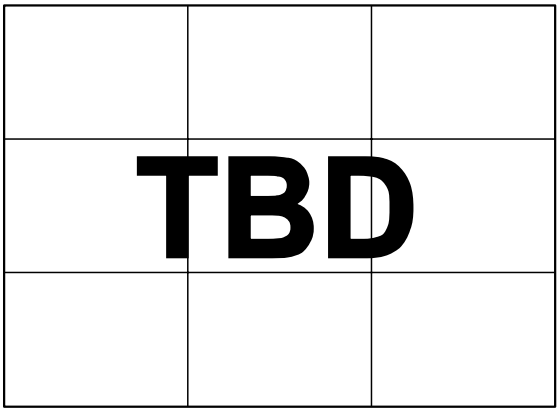

Figure 10. Output Current vs. Receiver Output Low Voltage

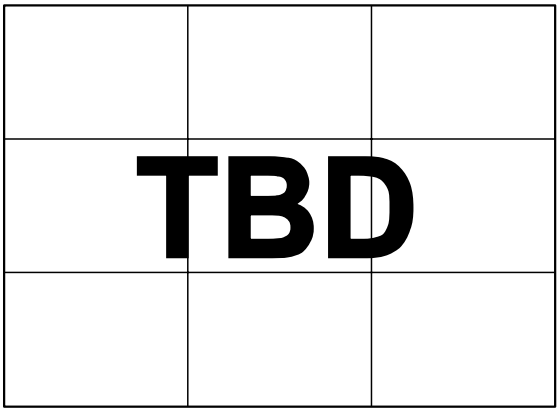

Figure 11. Receiver Output High Voltage vs. Temperature
I_{RxD} = –4 mA

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2490, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 9). Driver input signal, applied to the TxD pin, and referenced to logic ground (GND_1), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

iCoupler Technology

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

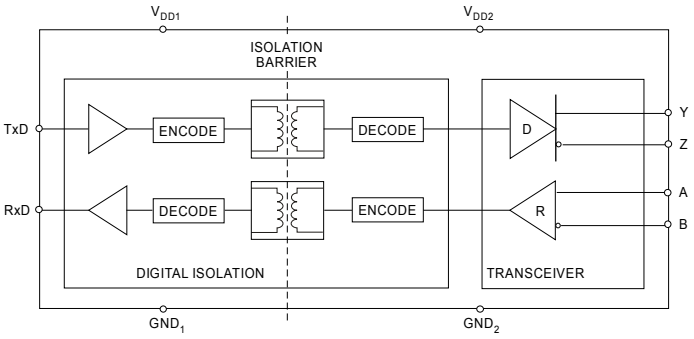

Figure 9. ADM2490E Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use these abbreviations:

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 8. Transmitting

Supply Status		Inputs	Output	
V_{DD1}	V_{DD2}	TxD	Y	Z
On	On	H	H	L
On	On	L	L	H

Table 9. Receiving

Supply Status		Inputs	Output
V_{DD1}	V_{DD2}	A–B (V)	RxD
On	On	>0.2	H
On	On	<–0.2	L
On	On	–0.2 < A – B < 0.2	I
On	On	Inputs open	H
On	Off	X	H
Off	On	X	H
Off	Off	X	L

THERMAL SHUTDOWN

The ADM2490E contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER FAIL-SAFE INPUTS

The receiver input includes a fail-safe feature that guarantees a logic high on the RxD pin when the A and B inputs are floating or open-circuited.

MAGNETIC FIELD IMMUNITY

Because *i*Couplers use a coreless technology, no magnetic components are present, and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The analysis below defines the conditions under which this may occur. The ADM2409E's 3 V operating condition is examined because it represents the most susceptible mode of operation. The limitation on the iCoupler's ac magnetic field immunity is set by the condition in which the induced error voltage in the receiving coil (the bottom coil in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2 \; ; \; n = 1, 2, \ldots, N$$

where, if the pulses at the transformer output are greater than 1.0 V in amplitude:

β = magnetic flux density (gauss)

N = number of turns in receiving coil

r_n = radius of nth turn in receiving coil (cm)

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 10.

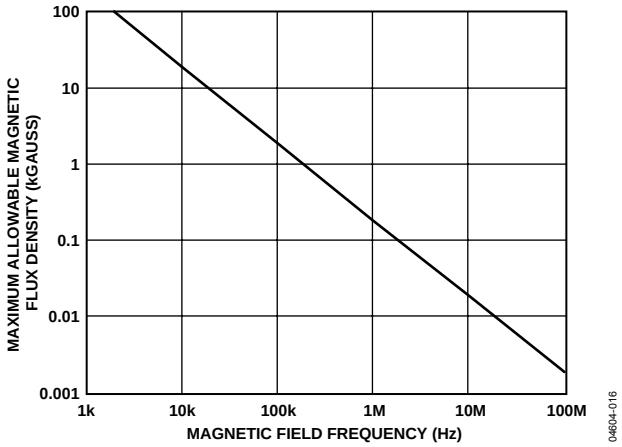

Figure10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

Figure 11 shows the magnetic flux density values in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2490E transformers.

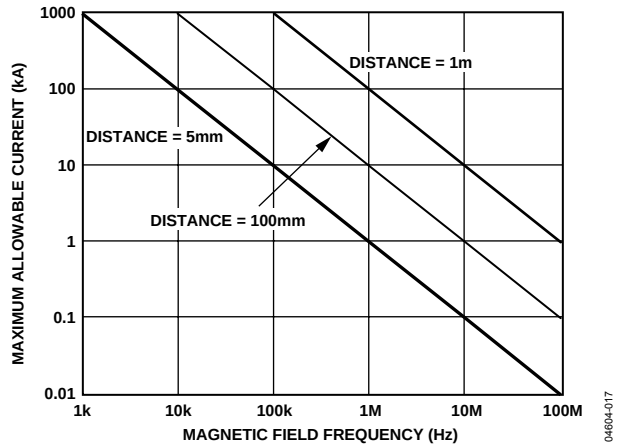

Figure11. Maximum Allowable Current for Various Current-to-ADM2490E Spacings

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

ISOLATED POWER SUPPLY CIRCUIT

The ADM2490E requires isolated power capable of 5 V at 100 mA to be supplied between the V_{DD2} and the GND_2 pins. A transformer driver circuit with a center-tapped transformer and LDO can be used to generate the isolated 5V supply as shown in figure 12 below. The center-tapped transformer provides electrical isolation of the 5V isolated power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated power supply to the ADM2490E's bus-side circuitry (VDD2).

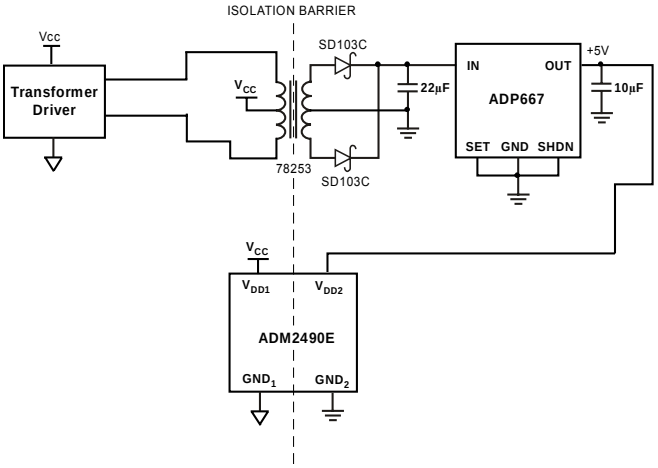

Figure 12. Isolated Power Supply Circuit

PC BOARD LAYOUT

The ADM2490E isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (Figure 13). Bypass capacitors are most conveniently connected between Pins 1 and 2 for V_{DD1} and between Pins 15 and 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypass-ing between Pins 1 and 8 and between Pins 9 and 16 should also be considered unless the ground pair on each package side is connected close to the package.

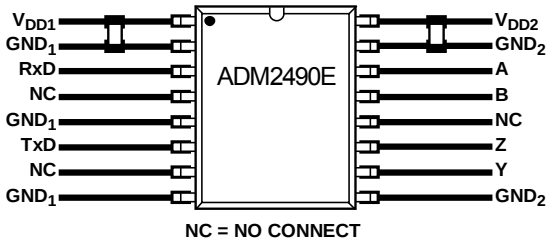

Figure13. *Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

OUTLINE DIMENSIONS

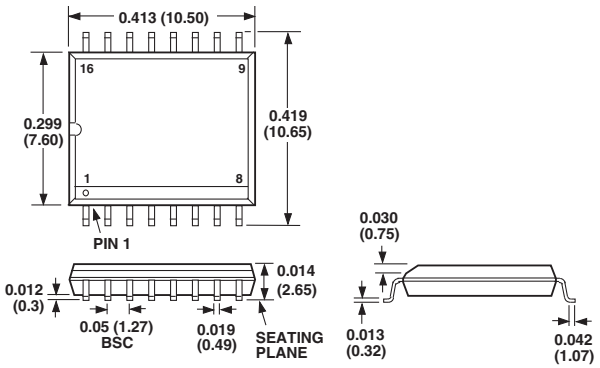

Figure 14. 16-Lead Wide-Body Small Outline Package [SOIC]

(RW-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM2490EWRWZ[1]	–40°C to +105°C	16-Lead Wide Body SOIC	RW-16
ADM2490EWRWZ–REEL7[1]	–40°C to +105°C	16-Lead Wide Body SOIC	RW-16

[1] Z = Pb-free part.