12-Bit, 170 MSPS/210 MSPS 3.3 V A/D Converter

AD9430

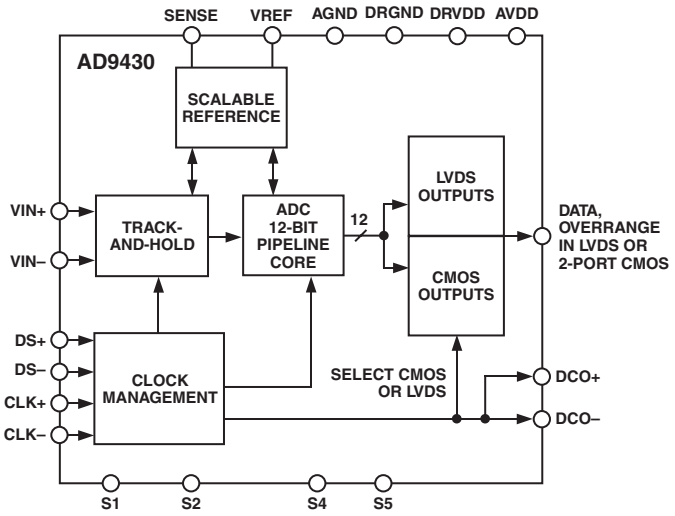
FEATURES

SNR = 65 dB @ f_{IN} up to 70 MHz @ 210 MSPS
ENOB of 10.6 @ f_{IN} up to 70 MHz @ 210 MSPS (–0.5 dBFS)
SFDR = 80 dBc @ f_{IN} up to 70 MHz @ 210 MSPS (–0.5 dBFS)
Excellent Linearity:
DNL = ±0.3 LSB (Typical)
INL = ±0.5 LSB (Typical)
2 Output Data Options:
Demultiplexed 3.3 V CMOS Outputs Each @ 105 MSPS
Interleaved or Parallel Data Output Option
LVDS at 210 MSPS
700 MHz Full Power Analog Bandwidth
On-Chip Reference and Track-and-Hold
Power Dissipation = 1.3 W Typical @ 210 MSPS
1.5 V Input Voltage Range
3.3 V Supply Operation
Output Data Format Option
Data Sync Input and Data Clock Output Provided
Clock Duty Cycle Stabilizer

APPLICATIONS

Wireless and Wired Broadband Communications
Cable Reverse Path
Communications Test Equipment
Radar and Satellite Subsystems
Power Amplifier Linearization

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9430 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates up to a 210 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution.

The ADC requires a 3.3 V power supply and a differential ENCODE clock for full performance operation. The digital outputs are TTL/CMOS or LVDS compatible and support either twos complement or offset binary format. Separate output power supply pins support interfacing with 3.3 V or 2.5 V CMOS logic.

Two output buses support demultiplexed data up to 105 MSPS rates in CMOS mode. A data sync input is supported for proper output data port alignment in CMOS mode and a data clock output is available for proper output data timing. In LVDS mode, the chip provides data at the ENCODE clock rate.

Fabricated on an advanced BiCMOS process, the AD9430 is available in a 100-lead surface-mount plastic package (100 e-PAD TQFP) specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 65 dB SNR @ 210 MSPS with a 65 MHz input.
2. Low Power—Consumes only 1.3 W @ 210 MSPS.
3. Ease of Use—LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample/hold provide flexibility in system design. Use of a single 3.3 V supply simplifies system power supply design.
4. Out of Range (OR)—The OR output bit indicates when the input signal is beyond the selected input range.

REV. A

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AD9430–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = –40°C, T_{MAX} = +85°C, f_{IN} = –0.5 dBFS, Internal Reference, Full Scale = 1.536 V, LVDS Output Mode, unless otherwise noted.)

Parameter	Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
RESOLUTION				12					Bits
ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Offset Error	25°C	I	–3		+3	–3		+3	mV
Gain Error	25°C	I	–5		+5	–5		+5	% FS
Differential Nonlinearity (DNL)	25°C	I	–1	±0.3	+1	–1	±0.3	+1	LSB
	Full	VI	–1	±0.3	+1.5	–1	±0.3	+1.5	LSB
Integral Nonlinearity (INL)	25°C	I	–1.5	±0.5	+1.5	–1.75	±0.3	+1.75	LSB
	Full	VI	–2.25	±0.5	+2.25	–2.5	±0.3	+2.5	LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		58			58		µV/°C
Gain Error	Full	V		0.02			0.02		%/°C
Reference Out (VREF)	Full	V		+0.12/–0.24			+0.12/–0.24		mV/°C
REFERENCE									
Reference Out (VREF)	25°C	I	1.15	1.235	1.3	1.15	1.235	1.3	V
Output Current[1]	25°C	IV			3.0			3.0	mA
I_{VREF} Input Current[2]	25°C	I			20			20	µA
I_{SENSE} Input Current[2]	25°C	I		1.6	5.0		1.6	5.0	mA
ANALOG INPUTS (VIN+, VIN–)[3]									
Differential Input Voltage Range (S5 = GND)	Full	V		1.536			1.536		V
Differential Input Voltage Range (S5 = AVDD)	Full	V		0.766			0.766		V
Input Common-Mode Voltage	Full	VI	2.65	2.8	2.9	2.65	2.8	2.9	V
Input Resistance	Full	VI	2.2	3	3.3	2.2	3	3.3	kΩ
Input Capacitance	25°C	V		5			5		pF
POWER SUPPLY (LVDS Mode)									
AVDD	Full	IV	3.1	3.3	3.6	3.2	3.3	3.6	V
DRVDD	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Currents									
I_{ANALOG} (AVDD = 3.3 V)[4]	Full	VI		335	372		390	450	mA
$I_{DIGITAL}$ (DRVDD = 3.3 V)[4]	Full	VI		55	62		55	62	mA
Power Dissipation[4]	Full	VI		1.29	1.43		1.5	1.7	W
Power Supply Rejection	25°C	V		–7.5			–7.5		mV/V
POWER SUPPLY (CMOS Mode)									
AVDD	Full	IV	3.1	3.3	3.6	3.2	3.3	3.6	V
DRVDD	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Currents									
I_{AVDD} (AVDD = 3.3 V)[5]	Full	IV		335	372		390	450	mA
I_{DRVDD} (DRVDD = 3.3 V)[5]	Full	IV		24	30		30	30	mA
Power Dissipation[5]	Full	IV		1.1			1.3		W
Power Supply Rejection	25°C	V		–7.5			–7.5		mV/V

NOTES

[1]Internal reference mode; SENSE = Floats.

[2]External reference mode; SENSE = DRVDD, VREF driven by external 1.23 V reference.

[3]S5 (Pin 1) = GND. See Analog Input section. S5 = GND in all dc, ac tests unless otherwise specified.

[4]I_{AVDD} and I_{DRVDD} are measured with an analog input of 10.3 MHz, –0.5 dBFS, sine wave, rated ENCODE rate, and in LVDS output mode. See Typical Performance Characteristics and Applications sections for I_{DRVDD}. Power consumption is measured with a dc input at rated ENCODE rate in LVDS output mode.

[5]I_{AVDD} and I_{DRVDD} are measured with an analog input of 10.3 MHz, –0.5 dBFS, sine wave, rated ENCODE rate, and in CMOS output mode. See Typical Performance Characteristics and Applications sections for I_{DRVDD}. Power consumption is measured with a dc input at rated ENCODE rate in CMOS output mode.

Specifications subject to change without notice.

AC SPECIFICATIONS[1] (AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = –40°C, T_{MAX} = +85°C, f_{IN} = –0.5 dBFS, Internal Reference, Full Scale = 1.536 V, LVDS Output Mode, unless otherwise noted.)

Parameter		Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
SNR										
Analog Input @ –0.5 dBFS	10 MHz	25°C	I	63.5	65		62.5	64.5		dB
	70 MHz	25°C	I	63	65		62.5	64.5		dB
	100 MHz	25°C	V		65			64.5		dB
	240 MHz	25°C	V		61			61		dB
SINAD										
Analog Input @ –0.5 dBFS	10 MHz	25°C	I	63.5	65		62.5	64.5		dB
	70 MHz	25°C	I	63	65		62.5	64.5		dB
	100 MHz	25°C	V		65			64.5		dB
	240 MHz	25°C	V		60			60		dB
EFFECTIVE NUMBER OF BITS (ENOB)										
	10 MHz	25°C	I	10.2	10.6		10.2	10.5		Bits
	70 MHz	25°C	I	10.2	10.6		10.2	10.5		Bits
	100 MHz	25°C	V		10.6			10.5		Bits
	240 MHz	25°C	V		9.8			9.8		Bits
WORST HARMONIC (2nd or 3rd)										
Analog Input @ –0.5 dBFS	10 MHz	25°C	I		–85	–75		–84	–74	dBc
	70 MHz	25°C	I		–85	–75		–84	–74	dBc
	100 MHz	25°C	V		–77			–77		dBc
	240 MHz	25°C	V		–63			–63		dBc
WORST HARMONIC (4th or Higher)										
Analog Input @ –0.5 dBFS	10 MHz	25°C	I		–87	–78		–87	–77	dBc
	70 MHz	25°C	I		–87	–78		–87	–77	dBc
	100 MHz	25°C	V		–77			–77		dBc
	240 MHz	25°C	V		–63			–63		dBc
TWO-TONE IMD[2]										
F1, F2 @ –7 dBFS		25°C	V		–75			–75		dBc
ANALOG INPUT BANDWIDTH		25°C	V		700			700		MHz

NOTES
[1]All ac specifications tested by driving CLK+ and CLK– differentially.
[2]F1 = 28.3 MHz, F2 = 29.3 MHz.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter	Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
ENCODE AND DS INPUTS (CLK+, CLK–, DS+, DS–)[1]									
Differential Input Voltage[2]	Full	IV	0.2			0.2			V
Common-Mode Voltage[3]	Full	VI	1.375	1.5	1.575	1.375	1.5	1.575	V
Input Resistance	Full	VI	3.2	5.5	6.5	3.2	5.5	6.5	kΩ
Input Capacitance	25°C	V		4			4		pF
LOGIC INPUTS (S1, S2, S4, S5)									
Logic "1" Voltage	Full	IV	2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8	V
Logic "1" Input Current	Full	VI			190			190	µA
Logic "0" Input Current	Full	VI			10			10	µA
Input Resistance	25°C	V		30			30		kΩ
Input Capacitance	25°C	V		4			4		pF
LOGIC OUTPUTS (CMOS Mode)									
Logic "1" Voltage[4]	Full	IV	DRVDD – 0.05			DRVDD – 0.05			V
Logic "0" Voltage[4]	Full	IV			0.05			0.05	V
LOGIC OUTPUTS (LVDS Mode)[4, 5]									
V_{OD} Differential Output Voltage	Full	VI	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	VI	1.125		1.375	1.125		1.375	V
Output Coding			Twos Complement or Binary			Twos Complement or Binary			

NOTES
[1]ENCODE and DS inputs identical on chip. See Equivalent Circuits section.
[2]All ac specifications tested by driving CLK+ and CLK– differentially, |(CLK+) – (CLK–)| > 200 mV.
[3]ENCODE inputs' common mode can be externally set, such that 0.9 V < ENC± < 2.6 V.
[4]Digital output logic levels: DRVDD = 3.3 V, C_{LOAD} = 5 pF.
[5]LVDS R_{TERM} = 100 Ω, LVDS output current set resistor = 3.74 kΩ (1% tolerance).
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter (Conditions)	Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
Maximum Conversion Rate[1]	Full	VI	170			210			MSPS
Minimum Conversion Rate[1]	Full	V			40			40	MSPS
CLK+ Pulsewidth High (t_{EH})[1]	Full	IV	2		12.5	2		12.5	ns
CLK+ Pulsewidth Low (t_{EL})[1]	Full	IV	2		12.5	2		12.5	ns
DS Input Setup Time (t_{SDS})[2]	Full	IV	–0.5			–0.5			ns
DS Input Hold Time (t_{HDS})[2]	Full	IV	1.75			1.75			ns
OUTPUT (CMOS Mode)									
Valid Time (t_V)	Full	IV	2			2			ns
Propagation Delay (t_{PD})	Full	IV		3.8	5		3.8	5	ns
Rise Time (t_R) (20% to 80%)	25°C	V		1			1		ns
Fall Time (t_F) (20% to 80%)	25°C	V		1			1		ns
DCO Propagation Delay (t_{CPD})	Full	IV		3.8	5		3.8	5	ns
Data to DCO Skew ($t_{PD} – t_{CPD}$)	Full	IV	–0.5	0	+0.5	–0.5	0	+0.5	ns
Interleaved Mode (A, B Latency)	Full	IV		14, 14			14, 14		Cycles
Parallel Mode (A, B Latency)	Full	IV		15, 14			15, 14		Cycles
OUTPUT (LVDS Mode)									
Valid Time (t_V)	Full	VI	2.0			2.0			ns
Propagation Delay (t_{PD})	Full	VI		3.2	4.3		3.2	4.3	ns
Rise Time (t_R) (20% to 80%)	25°C	V		0.5			0.5		ns
Fall Time (t_F) (20% to 80%)	25°C	V		0.5			0.5		ns
DCO Propagation Delay (t_{CPD})	Full	VI	1.8	2.7	3.8	1.8	2.7	3.8	ns
Data to DCO Skew ($t_{PD} – t_{CPD}$)	Full	IV	0.2	0.5	0.8	0.2	0.5	0.8	ns
Latency	Full	IV		14			14		Cycles
Aperture Delay (t_A)	25°C	V		1.2			1.2		ns
Aperture Uncertainty (Jitter, t_J)	25°C	V		0.25			0.25		ps rms
Out of Range Recovery Time (CMOS and LVDS)	25°C	V			1			1	Cycles

NOTES
[1]All ac specifications tested by driving CLK+ and CLK– differentially.
[2]DS inputs used in CMOS mode only.
Specifications subject to change without notice.

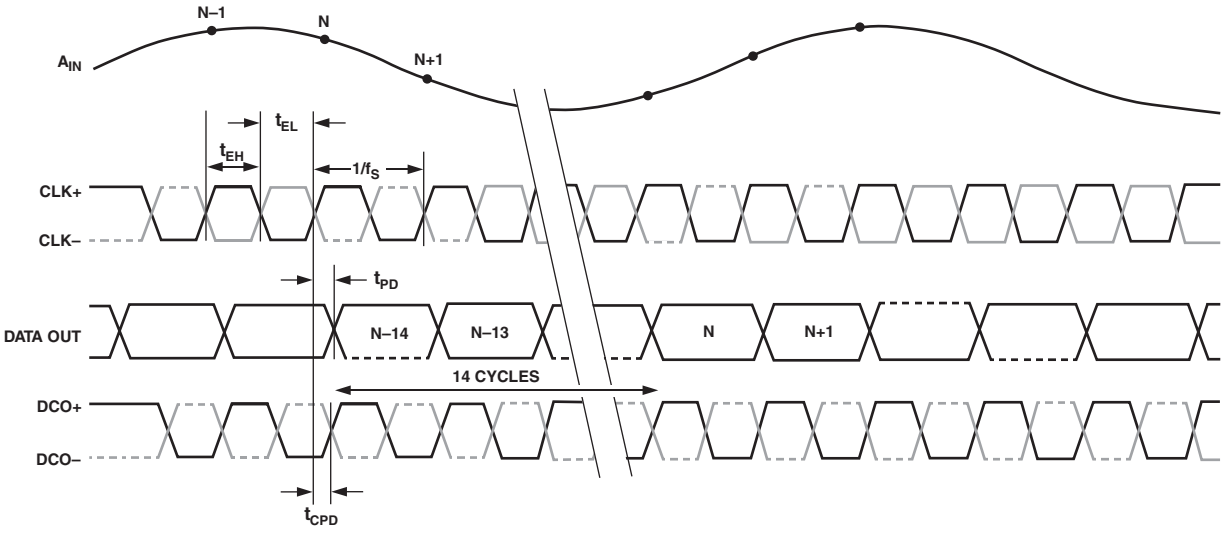


Figure 1. LVDS Timing Diagram

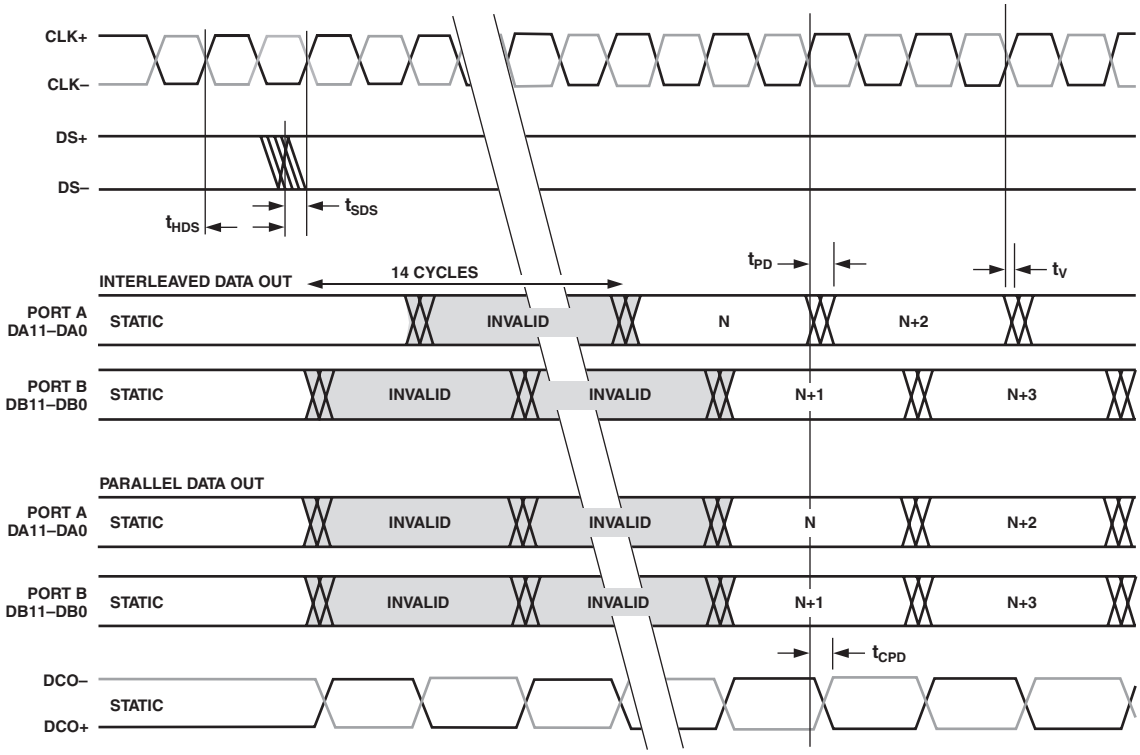


Figure 2. CMOS Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

AVDD, DRVDD	4 V
Analog Inputs	–0.5 V to AVDD + 0.5 V
Digital Inputs	–0.5 V to DRVDD + 0.5 V
REFIN Inputs	–0.5 V to AVDD + 0.5 V
Digital Output Current	20 mA
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C
θ_{JA}[2]	25°C/W, 32°C/W

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

[2]Typical θ_{JA} = 32°C/W (heat slug not soldered); typical θ_{JA} = 25°C/W (heat slug soldered), for multilayer board in still air with solid ground plane.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.
II. 100% production tested at 25°C and sample tested at specified temperatures.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.
VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9430BSV-170	–40°C to +85°C	e-PAD TQFP-100
AD9430BSV-210	–40°C to +85°C	e-PAD TQFP-100
AD9430/PCB-LVDS	25°C	Evaluation Board (LVDS Mode)
AD9430/PCB-CMOS	25°C	Evaluation Board (CMOS Mode)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9430 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS (CMOS Mode)

Pin Number	Mnemonic	Function
1	S5	Full-Scale Adjust Pin. AVDD sets f_S = 0.768 V p-p differential, GND sets f_S = 1.536 V p-p differential.
2, 7, 42, 43, 65, 66, 68	DNC	Do Not Connect
3	S4	Interleaved, Parallel Select Pin. High = interleaved.
4, 9, 12, 13, 16, 17, 20, 23, 25, 26, 30, 31, 35, 38, 41, 86, 87, 91, 92, 93, 96, 97, 100	AGND*	Analog Ground
5	S2	Output Mode Select. Low = dual-port CMOS, High = LVDS.
6	S1	Data Format Select. Low = binary, High = twos complement.
8, 14, 15, 18, 19, 24, 27, 28, 29, 34, 39, 40, 88, 89, 90, 94, 95, 98, 99	AVDD	3.3 V Analog Supply
10	SENSE	Reference Mode Select Pin, Float for Internal Reference Operation
11	VREF	1.235 Reference I/O – Function Dependent on SENSE
21	VIN+	Analog Input – True
22	VIN–	Analog Input – Complement
32	DS+	Data Sync (Input) – True. Tie low if not used. See Timing Diagram.
33	DS–	Data Sync (Input) – Complement. Tie high if not used.
36	CLK+	Clock Input – True
37	CLK–	Clock Input – Complement
44	DB0	B Port Output Data Bit (LSB)
45	DB1	B Port Output Data Bit
46	DB2	B Port Output Data Bit
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V)
48, 53, 61, 67, 74, 82	DRGND*	Digital Output Ground
49	DB3	B Port Output Data Bit
50	DB4	B Port Output Data Bit
51	DB5	B Port Output Data Bit
52	DB6	B Port Output Data Bit
55	DB7	B Port Output Data Bit
56	DB8	B Port Output Data Bit
57	DB9	B Port Output Data Bit
58	DB10	B Port Output Data Bit
59	DB11	B Port Output Data Bit (MSB)
60	OR_B	B Port Overrange
63	DCO–	Data Clock Output – Complement
64	DCO+	Data Clock Output – True
69	DA0	A Port Output Data Bit (LSB)
70	DA1	A Port Output Data Bit
71	DA2	A Port Output Data Bit
72	DA3	A Port Output Data Bit
73	DA4	A Port Output Data Bit
76	DA5	A Port Output Data Bit
77	DA6	A Port Output Data Bit
78	DA7	A Port Output Data Bit
79	DA8	A Port Output Data Bit
80	DA9	A Port Output Data Bit
81	DA10	A Port Output Data Bit
84	DA11	A Port Output Data Bit (MSB)
85	OR_A	A Port Overrange

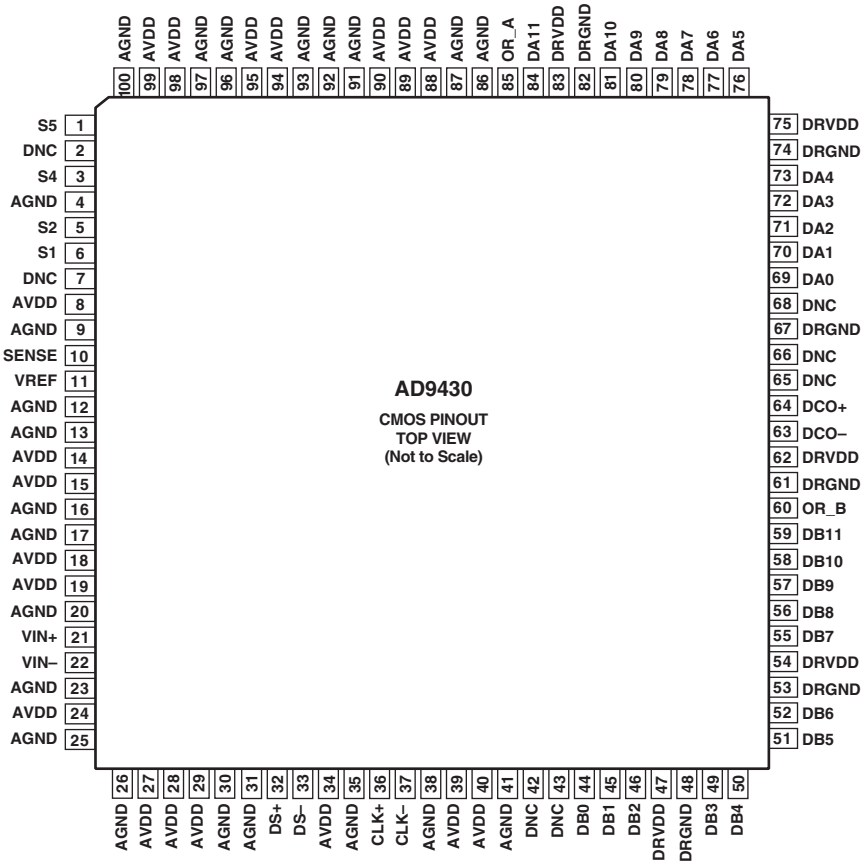
*AGND and DRGND should be tied together to a common ground plane.

PIN FUNCTION DESCRIPTIONS (LVDS Mode)

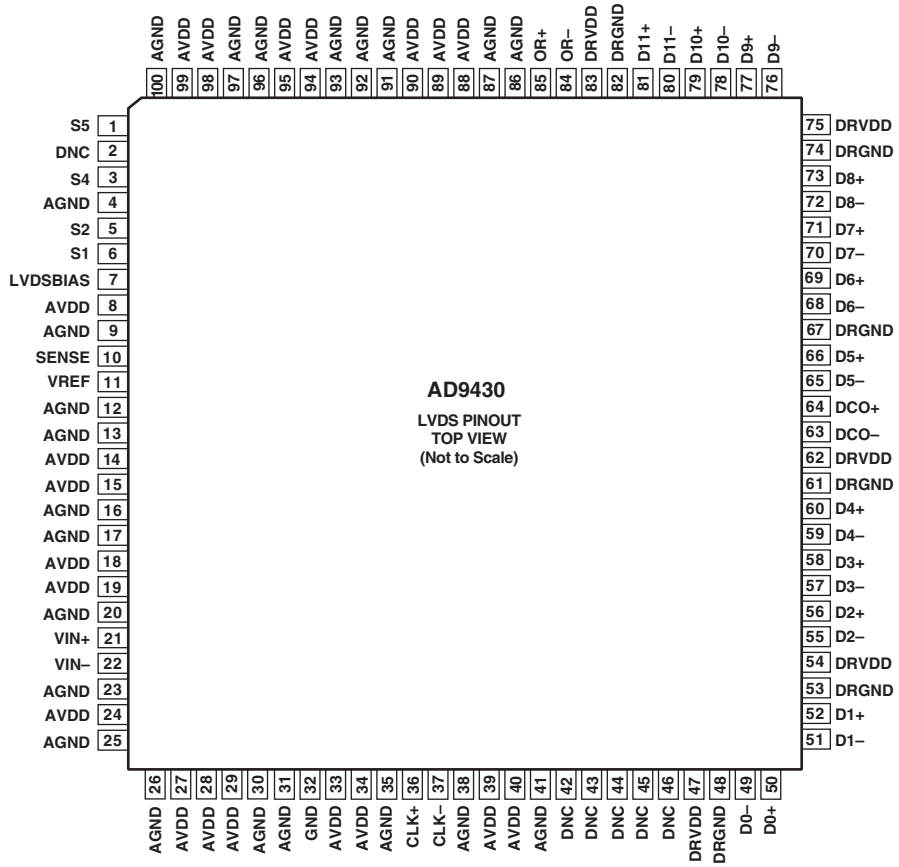
Pin Number	Mnemonic	Function
1	S5	Full-Scale Adjust Pin. AVDD sets f_S = 0.768 V p-p differential, GND sets f_S = 1.536 V p-p differential.
2, 42–46	DNC	Do Not Connect
3	S4	Control Pin for CMOS Mode. Tie low when operating in LVDS mode.
4, 9, 12, 13, 16, 17, 20, 23, 25, 26, 30, 31, 35, 38, 41, 86, 87, 91, 92, 93, 96, 97, 100	AGND*	Analog Ground
5	S2	Output Mode Select. GND = dual-port CMOS; AVDD = LVDS.
6	S1	Data Format Select. GND = binary, AVDD = twos complement.
7	LVDSBIAS	Set Pin for LVDS Output Current. Place 3.7 kΩ resistor terminated to ground.
8, 14, 15, 18, 19, 24, 27, 28, 29, 33, 34, 39, 40, 88, 89, 90, 94, 95, 98, 99	AVDD	3.3 V Analog Supply
10	SENSE	Reference Mode Select Pin, Float for Internal Reference Operation
11	VREF	1.235 Reference I/O – Function Dependent on SENSE
21	VIN+	Analog Input – True
22	VIN–	Analog Input – Complement
32	GND	Data Sync (Input) – Not Used in LVDS Mode. Tie to GND.
36	CLK+	Clock Input – True (LVPECL Levels)
37	CLK–	Clock Input – Complement (LVPECL Levels)
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V)
48, 53, 61, 67, 74, 82	DRGND*	Digital Output Ground
49	D0–	D0 Complement Output Bit (LSB)
50	D0+	D0 True Output Bit (LSB)
51	D1–	D1 Complement Output Bit
52	D1+	D1 True Output Bit
55	D2–	D2 Complement Output Bit
56	D2+	D2 True Output Bit
57	D3–	D3 Complement Output Bit
58	D3+	D3 True Output Bit
59	D4–	D4 Complement Output Bit
60	D4+	D4 True Output Bit
63	DCO–	Data Clock Output – Complement
64	DCO+	Data Clock Output – True
65	D5–	D5 Complement Output Bit
66	D5+	D5 True Output Bit
68	D6–	D6 Complement Output Bit
69	D6+	D6 True Output Bit
70	D7–	D7 Complement Output Bit
71	D7+	D7 True Output Bit
72	D8–	D8 Complement Output Bit
73	D8+	D8 True Output Bit
76	D9–	D9 Complement Output Bit
77	D9+	D9 True Output Bit
78	D10–	D10 Complement Output Bit
79	D10+	D10 True Output Bit
80	D11–	D11 Complement Output Bit
81	D11+	D11 True Output Bit
84	OR–	Overrange Complement Output Bit
85	OR+	Overrange True Output Bit

*AGND and DRGND should be tied together to a common ground plane.

PIN CONFIGURATIONS



CMOS Dual-Mode Pinout



LVDS Mode Pinout

DEFINITIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Crosstalk
Coupling onto one channel being driven by a low level (–40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input's phase 180° and again taking the peak measurement. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
Calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ dB}{6.02}$$

ENCODE Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time the ENCODE pulse should be left in logic 1 state to achieve rated performance; pulsewidth low is the minimum time the ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in the Application Notes, Encode Input section. At a given clock rate, these specifications define an acceptable ENCODE duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{FULLSCALE} = 10\log\left(\frac{\frac{V^2_{FULLSCALE_{RMS}}}{Z_{INPUT}}}{0.001}\right)$$

Gain Error
The difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The ENCODE rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The ENCODE rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of CLK+ and CLK– and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)
Calculated as follows:

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}$$

where *Z* is the input impedance, *FS* is the full scale of the device for the frequency in question, *SNR* is the value of the particular input level, and *Signal* is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Transient Response Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

EQUIVALENT CIRCUITS

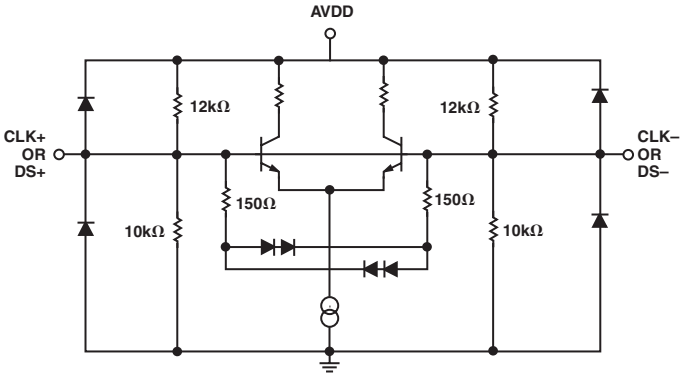


Figure 3. ENCODE and DS Inputs

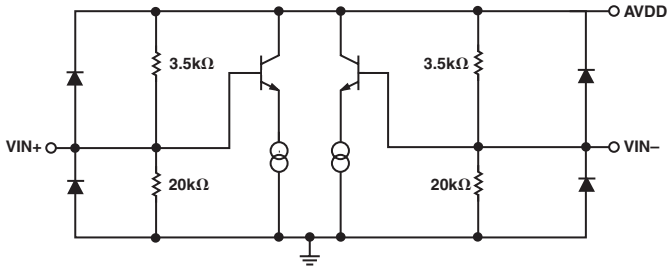


Figure 4. Analog Inputs

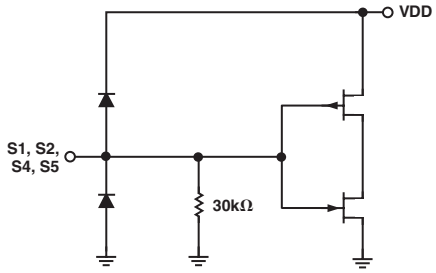


Figure 5. S1–S5 Inputs

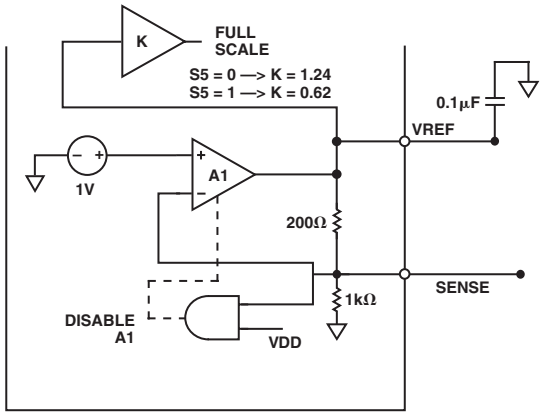


Figure 6. VREF, SENSE I/O

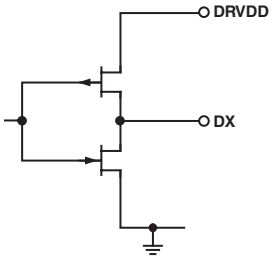


Figure 7. Data Outputs (CMOS Mode)

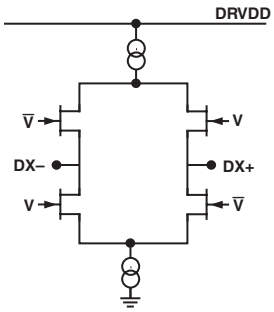
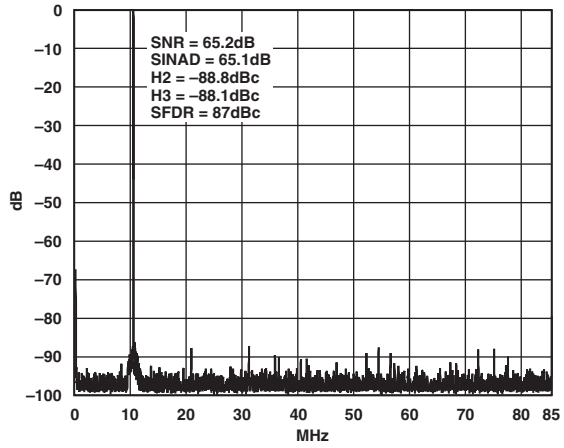
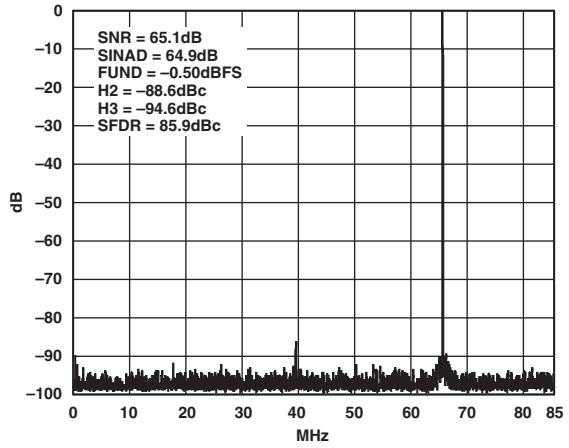


Figure 8. Data Outputs (LVDS Mode)

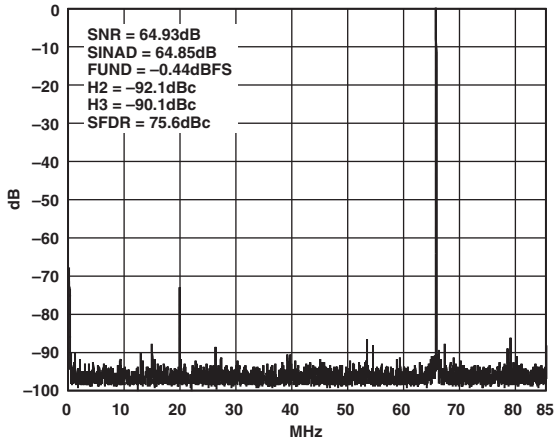
AD9430–Typical Performance Characteristics (Charts at 170 MSPS, 210 MSPS for -170, -210 grades, respectively.)



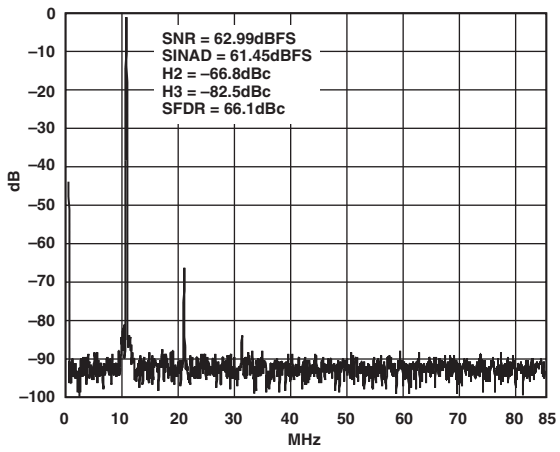
TPC 1. FFT: f_S = 170 MSPS, A_{IN} = 10.3 MHz @ –0.5 dBFS, LVDS Mode



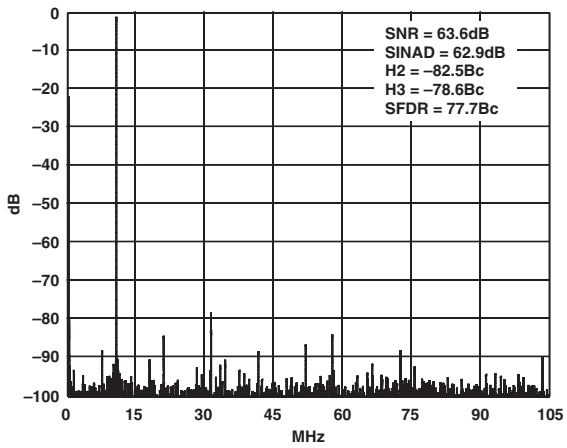
TPC 2. FFT: f_S = 170 MSPS, A_{IN} = 65 MHz @ –0.5 dBFS, LVDS Mode



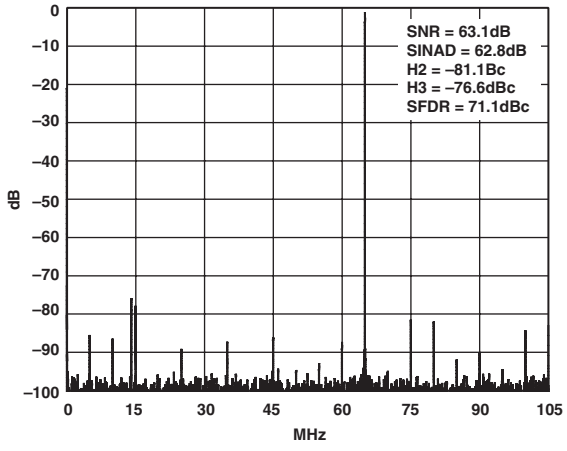
TPC 3. FFT: f_S = 170 MSPS, A_{IN} = 65 MHz @ –0.5 dBFS, Differential, 1.5 V p-p Input Range, CMOS Mode



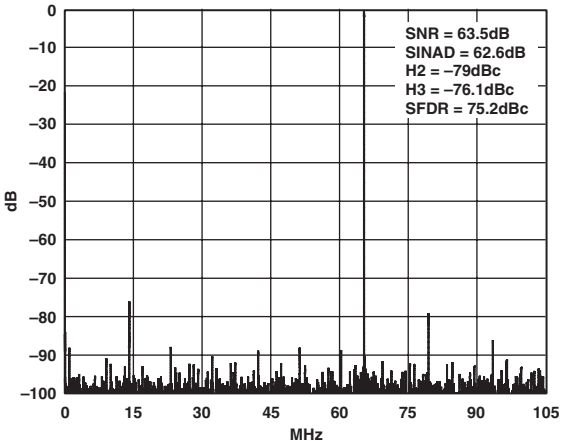
TPC 4. FFT: f_S = 170 MSPS, A_{IN} = 10.3 MHz @ –0.5 dBFS, Single-Ended Input, 0.76 V Input Range, LVDS Mode



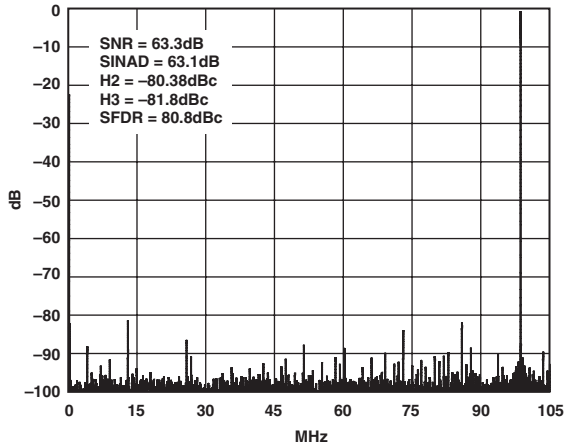
TPC 5. FFT: f_S = 210 MSPS, A_{IN} = 10.3 MHz @ –0.5 dBFS, LVDS Mode, Full Scale = 1.536 V



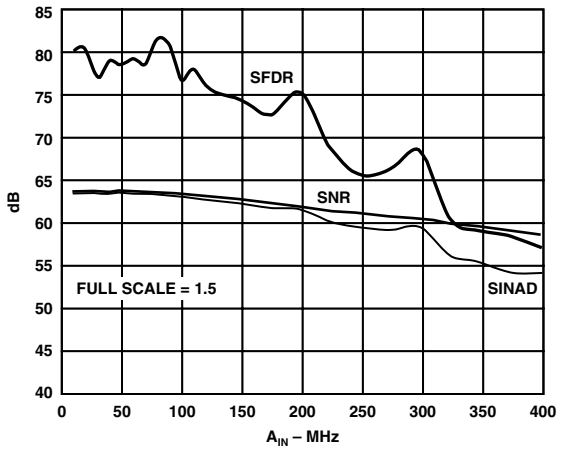
TPC 6. FFT: f_S = 210 MSPS, A_{IN} = 65 MHz @ –0.5 dBFS, CMOS Mode, Full Scale = 1.536 V



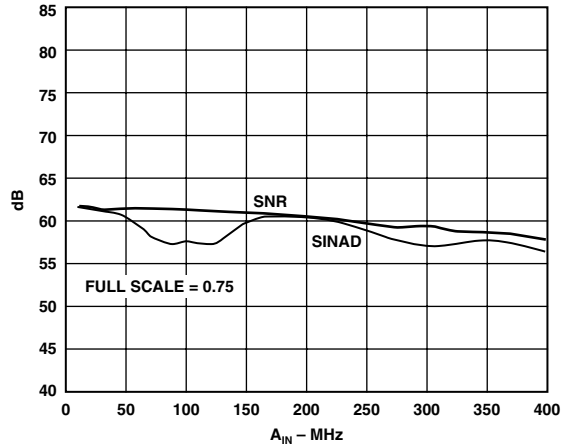
TPC 7. FFT: f_S = 210 MSPS, A_{IN} = 65 MHz @ –0.5 dBFS, LVDS Mode, Full Scale = 1.536 V



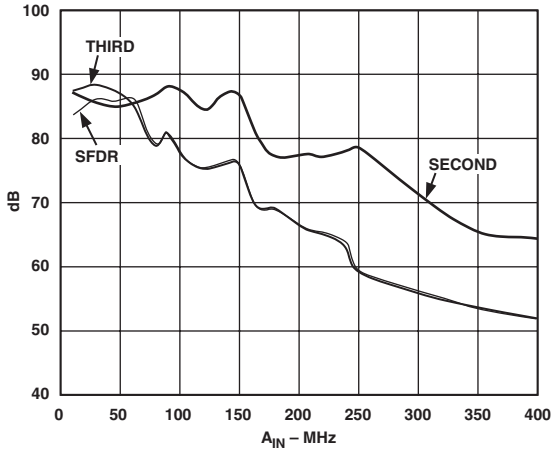
TPC 10. FFT: f_S = 213 MSPS, A_{IN} = 100 MHz @ –0.5 dBFS, LVDS Mode, Full Scale = 1.536 V



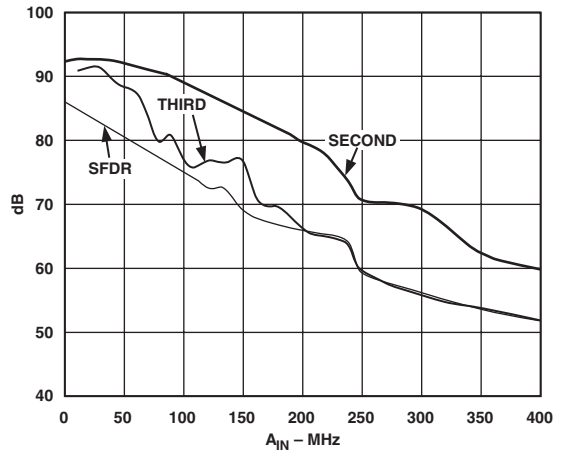
TPC 8. SNR, SINAD, and SFDR vs. A_{IN} Frequency; f_S = 210 MSPS, A_{IN} @ –0.5 dBFS, LVDS Mode, Full Scale = 1.536 V



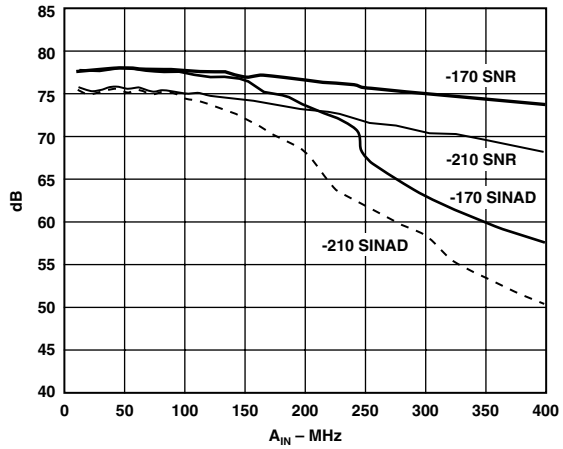
TPC 11. SNR, and SINAD vs. A_{IN} Frequency; f_S = 210 MSPS, A_{IN} @ –0.5 dBFS, LVDS Mode, Full Scale = 0.75 V



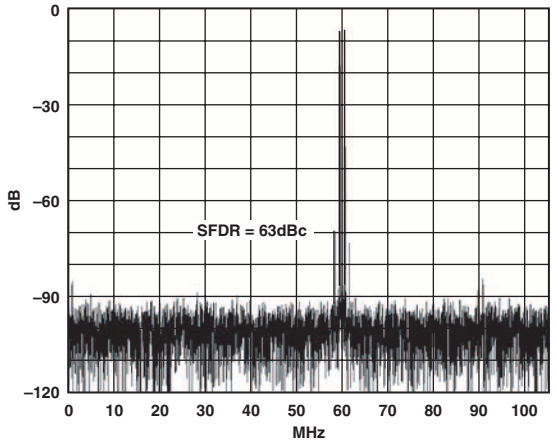
TPC 9. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency, f_S = 170 MSPS, LVDS Mode



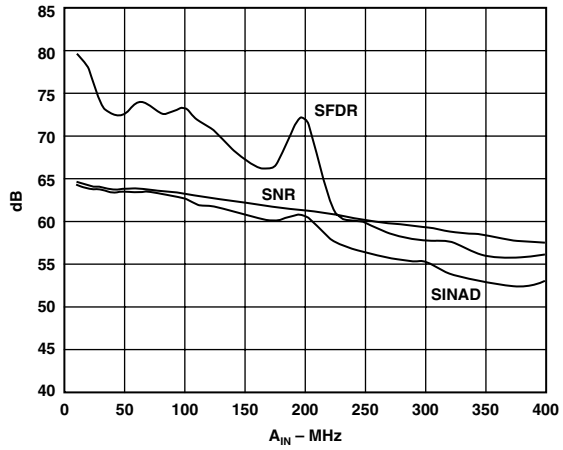
TPC 12. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency, f_S = 170 MSPS, CMOS Mode



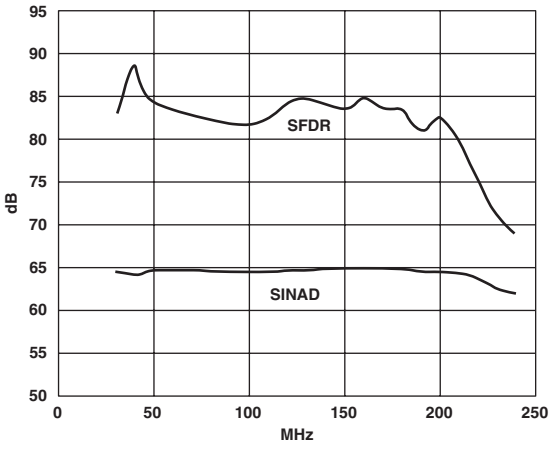
TPC 13. SNR, and SINAD vs. A_{IN} Frequency; f_S = 170, 210 MSPS, A_{IN} @ –0.5 dBFS, LVDS Mode, Full Scale = 1.536 V



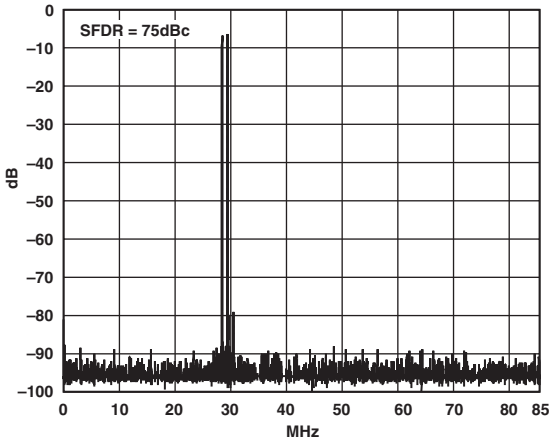
TPC 16. Two Tone Intermodulation Distortion (59 MHz and 60 MHz), LVDS Mode, Full Scale = 1.536 V, f_S = 210 MSPS



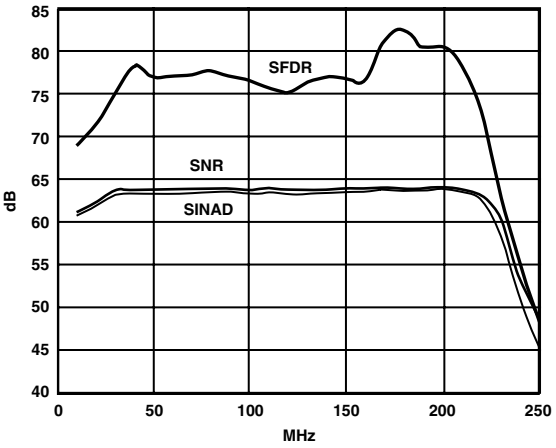
TPC 14. SNR, and SINAD, SFDR vs. A_{IN} Frequency; f_S = 210 MSPS, A_{IN} @ –0.5 dBFS, CMOS Mode, Full Scale = 1.536 V



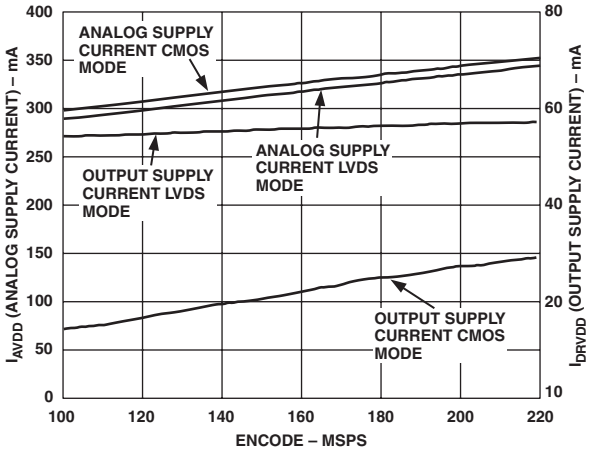
TPC 17. SINAD and SFDR vs. Clock Rate (A_{IN} = 10.3 MHz @ –0.5 dBFS, LVDS Mode), –170 Grade



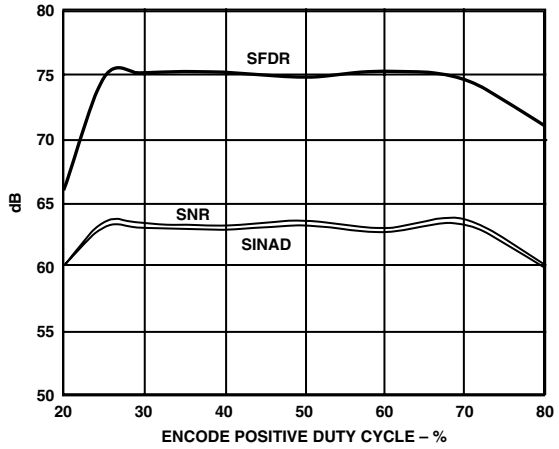
TPC 15. Two-Tone Intermodulation Distortion (28.3 MHz and 29.3 MHz; LVDS Mode, f_S = 170 MSPS)



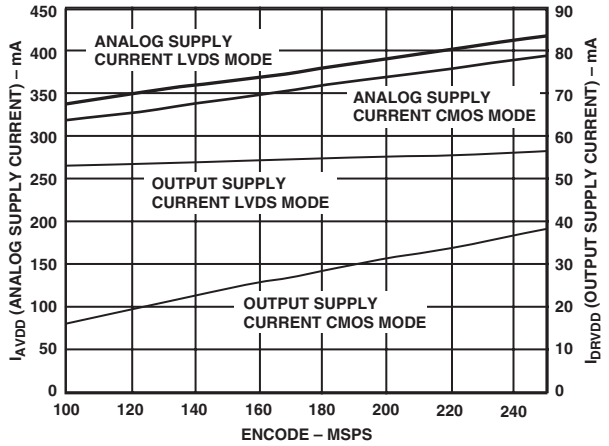
TPC 18. SNR, and SINAD, SFDR vs. Clock Rate; (A_{IN} = 10.3 MHz, @ –0.5 dBFS), LVDS Mode, Full Scale = 1.536 V, –210 Grade



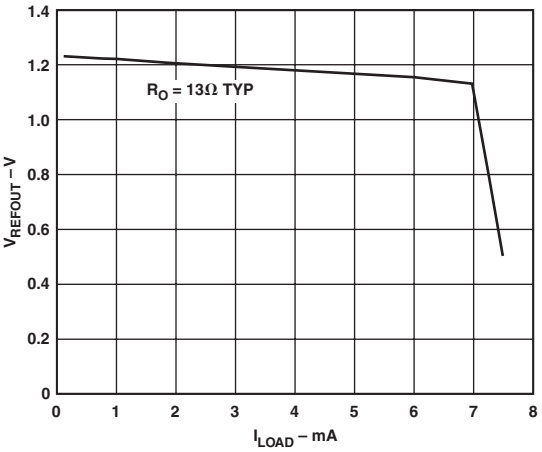
TPC 19. I_{AVDD} and I_{DRVDD} vs. Clock Rate (A_{IN} = 10.3 MHz @ –0.5 dBFS) 170 MSPS Grade, C_{LOAD} = 5 pF



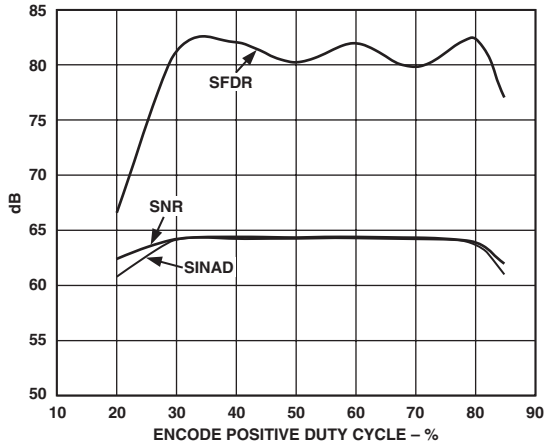
TPC 22. SNR, SINAD, and SFDR vs. ENCODE Pulsewidth High, (A_{IN} = 10.3 MHz @ –0.5 dBFS, 210 MSPS, LVDS)



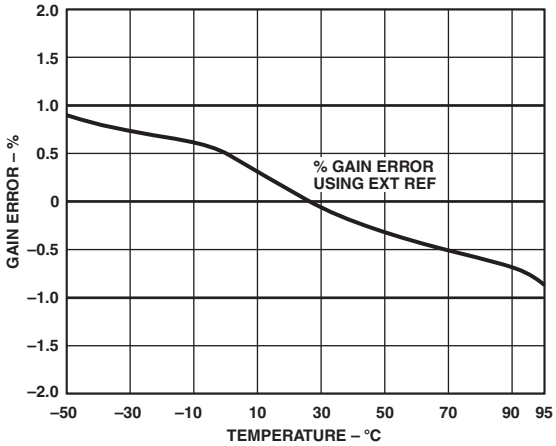
TPC 20. I_{AVDD} and I_{DRVDD} vs. Clock Rate (A_{IN} = 10.3 MHz @ –0.5 dBFS) 210 MSPS Grade, C_{LOAD} = 5 pF



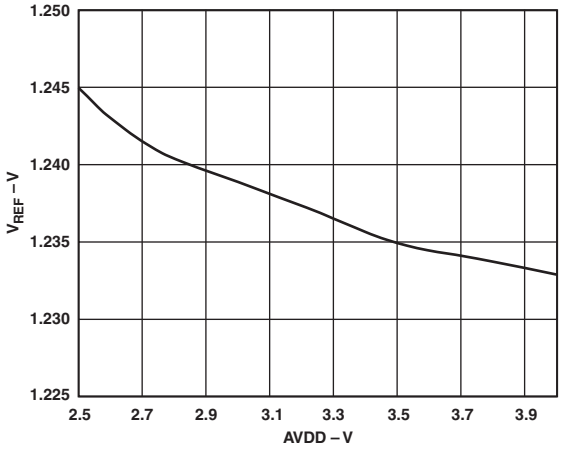
TPC 23. V_{REFOUT} vs. I_{LOAD}



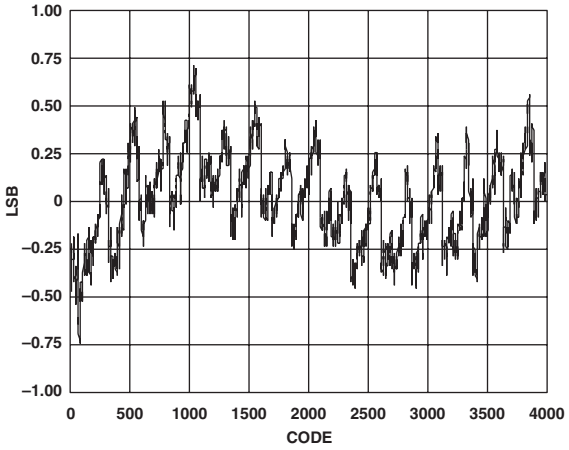
TPC 21. SINAD and SFDR vs. Clock Pulsewidth High (A_{IN} = 10.3 MHz @ –0.5 dBFS, 170 MSPS, LVDS)



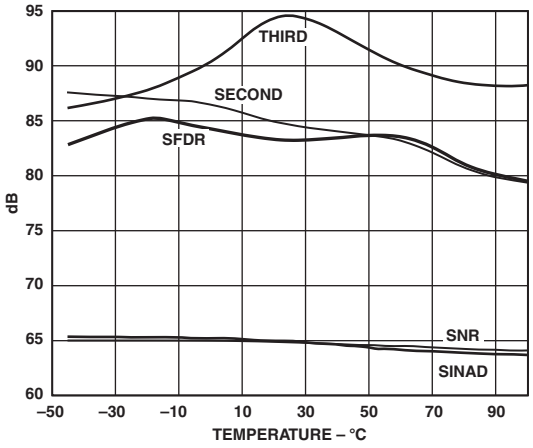
TPC 24. Full-Scale Gain Error vs. Temperature (A_{IN} = 10.3 MHz @ –0.5 dBFS, 170 MSPS/210 MSPS, LVDS)



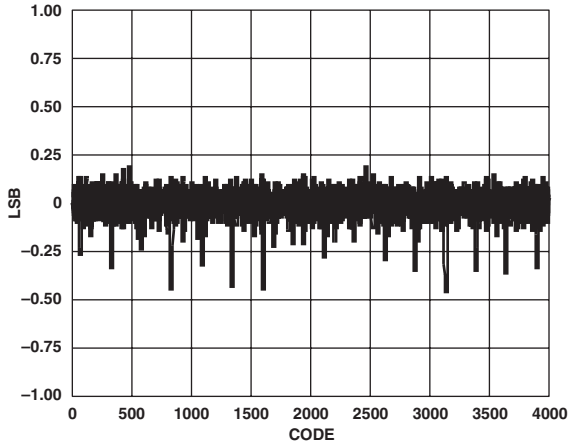
TPC 25. V_{REF} Output Voltage vs. AVDD



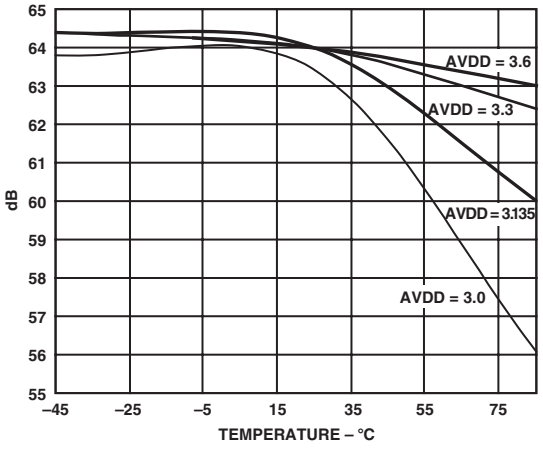
TPC 28. Typical INL Plot (A_{IN} = 10.3 MHz @ –0.5 dBFS, 170 MSPS, LVDS)



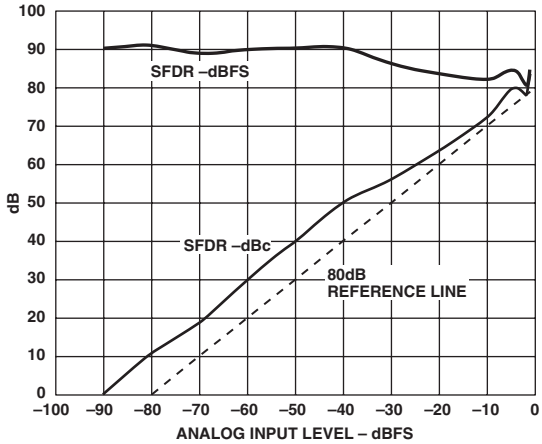
TPC 26. SNR, SINAD, SFDR vs. Temperature (A_{IN} = 10.3 MHz @ –0.5 dBFS, 170 MSPS)



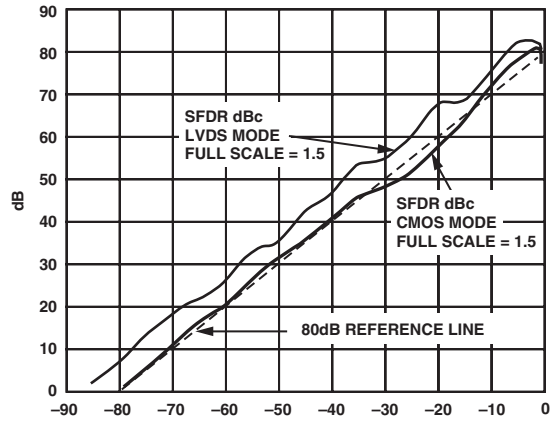
TPC 29. Typical DNL Plot (A_{IN} = 10.3 MHz @ –0.5 dBFS, 170 MSPS, LVDS)



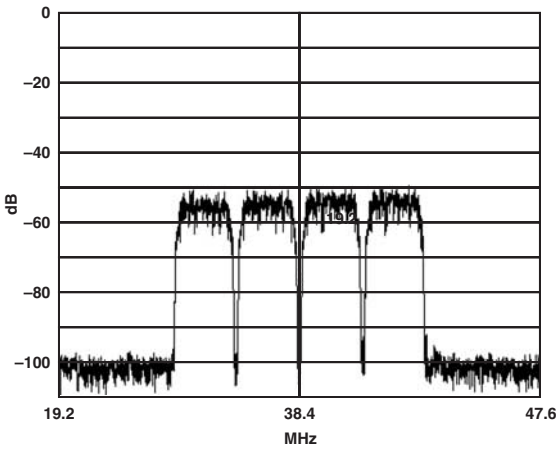
TPC 27. SINAD vs. Temperature, AVDD; (A_{IN} = 70 MHz @ –0.5 dB, 210 MSPS, LVDS Mode, Full Scale = 1.536 V)



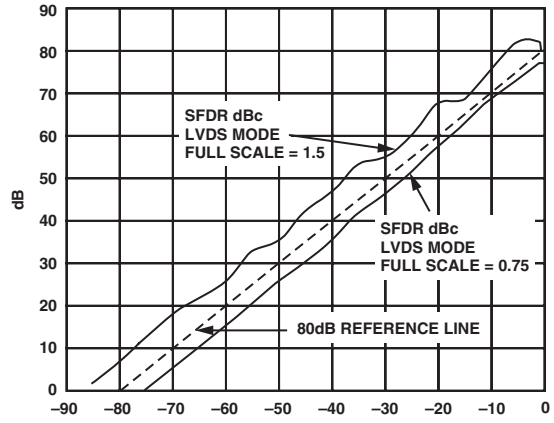
TPC 30. SFDR vs. A_{IN} Input Level 10.3 MHz, A_{IN} @ 170 MSPS, LVDS



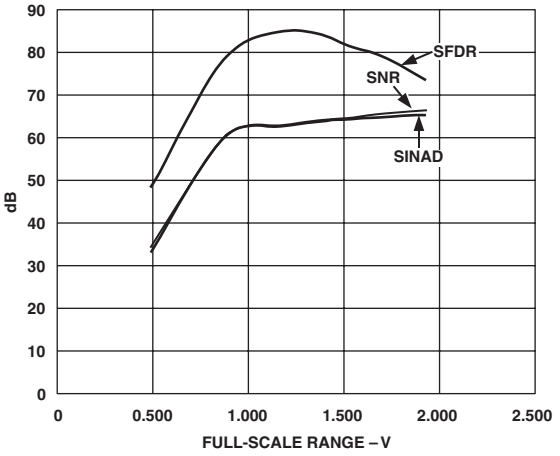
TPC 31. SFDR vs. A_{IN} Input Level @10.3 MHz, 210 MSPS, LVDS/CMOS, Full Scale = 1.536 V



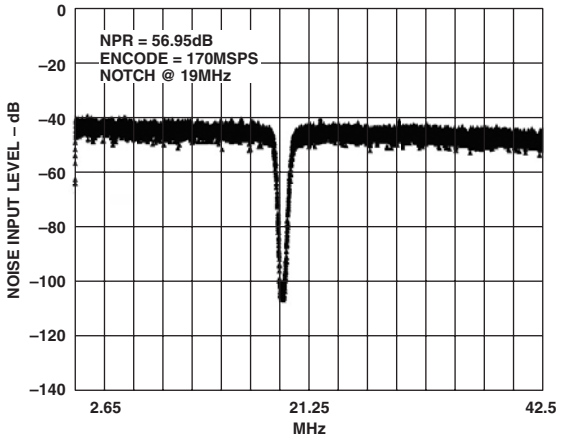
TPC 34. W-CDMA Four Channels Centered at 38.4 MHz, f_S = 153.6 MHz, LVDS, Full Scale = 1.536 V



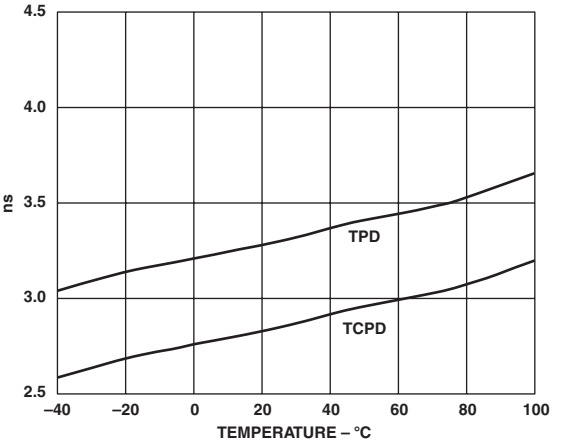
TPC 32. SFDR vs. A_{IN} Input Level @10.3 MHz, 210 MSPS, LVDS, Full Scale = 0.75 V/1.536 V



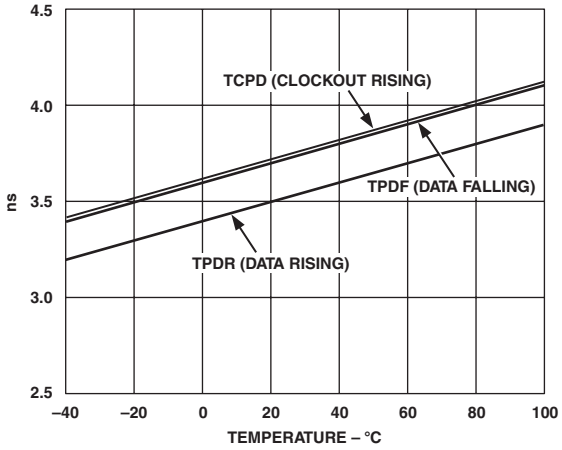
TPC 35. SNR, and SINAD, SFDR vs. Full-Scale Range, S5 = 0, Full-Scale Range Varied by Adjusting VREF, 170 MSPS



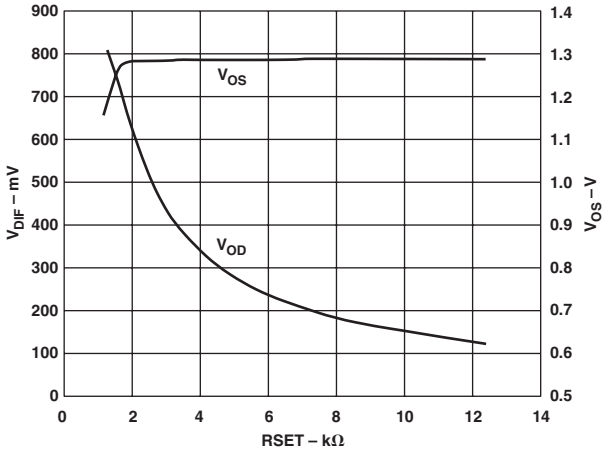
TPC 33. Noise Power Ratio Plot



TPC 36. Propagation Delay vs. Temperature, LVDS, 170 MSPS/210 MSPS



TPC 37. Propagation Delay vs. Temperature, CMOS, 170 MSPS/210 MSPS



TPC 38. LVDS Output Swing, Common-Mode Voltage vs. RSET, Placed at LVDSBIAS, 170 MSPS/210 MSPS

APPLICATION NOTES

THEORY OF OPERATION

The AD9430 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 12-bit core. For ease of use, the part includes an on-board reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output's logic levels are user selectable as standard 3 V CMOS or LVDS (ANSI-644 compatible) via Pin S2.

ENCODE INPUT

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the Clock inputs of the AD9430, and the user is advised to give careful thought to the clock source.

The AD9430 has an internal clock duty cycle stabilization circuit that locks to the rising edge of CLK+ and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 30 MHz nominally. The loop has a time constant associated with it that needs to be considered in applications where the clock rate can change dynamically, requiring a wait time of 1.5 μs to 5 μs after a dynamic clock frequency increase before valid data is available. This circuit is always on and cannot be disabled by the user.

The Clock inputs are internally biased to 1.5 V (nominal) and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. An MC100LVEL16 performs well in the circuit to drive the Clock inputs, as illustrated in Figure 9. Note that for this low voltage PECL device, the ac coupling is optional.

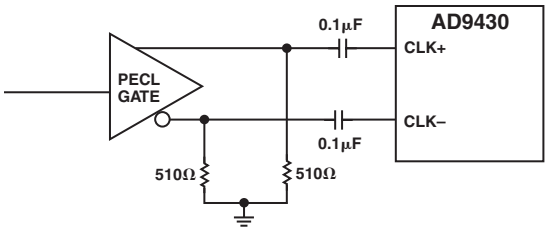


Figure 9. Driving Clock Inputs with LVEL16

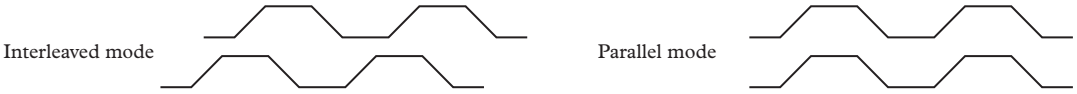
Table I. Output Select Coding

S1 (Data Format Select)	S2 (LVDS/CMOS Mode Select)[1]	S4 (I/P Select)	S5 (Full-Scale Select)[2]	Mode
1	X	X	X	Twos Complement
0	X	X	X	Offset Binary
X	0	1	X	Dual-Mode CMOS Interleaved
X	0	0	X	Dual-Mode CMOS Parallel
X	1	X	X	LVDS Mode
X	X	X	1	Full Scale = 0.768 V
X	X	X	0	Full Scale = 1.536 V

X = Don't Care

NOTES
[1]S4 used in CMOS mode only (S2 = 0). S1–S5 all have 30 kΩ resistive pull-downs on chip.
[2]S5 Full-Scale Adjust (see Analog Input section).

In interleaved mode, output data on Port A is offset from output data changes on Port B by one-half output clock cycle:



ANALOG INPUT

The analog input to the AD9430 is a differential buffer. For best dynamic performance, impedances at V_{IN+} and V_{IN-} should match. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance will degrade significantly if the analog input is driven with a single-ended signal. A wideband transformer, such as Minicircuits' ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 2.8 V (see the Equivalent Circuits section).

Special care was taken in the design of the analog input section of the AD9430 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.5 V_{DIFF} p-p. The nominal differential input range is 768 mV p-p × 2. Note that the best performance is achieved with S5 = 0 (full-scale = 1.5). See TPC 32.

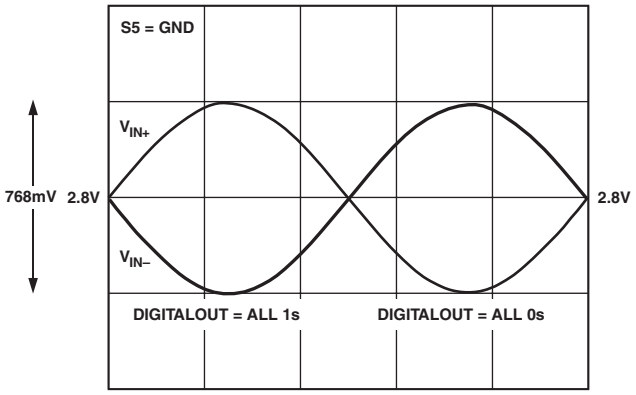


Figure 10. Differential Analog Input Range

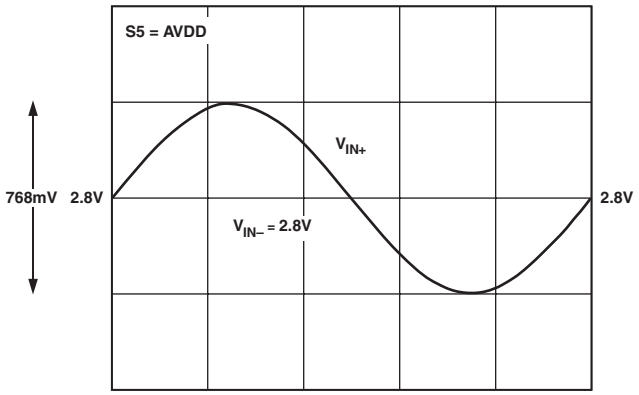


Figure 11. Single-Ended Analog Input Range

DS INPUTS (DS+, DS–)

In CMOS output mode, the Data Sync inputs (DS+, DS–) can be used in applications requiring that a given sample will appear at a specific output port (A or B) relative to a given external timing signal. The DS inputs can also be used to synchronize two or more ADCs in a system to maintain phasing between Ports A and B on separate ADCs (in effect, synchronizing multiple DCO outputs). When DS+ is held high (DS– low), the ADC data outputs and clock do not switch and are held static. Synchronization is accomplished by the assertion (falling edge) of DS+ within the timing constraints t_{SDS} and t_{HDS}, relative to a clock rising edge. (On initial synchronization, t_{HDS} is not relevant.) If DS+ falls within the required setup time (t_{SDS}) before a given clock rising edge N, the analog value at that point in time will be digitized and available at Port A, 14 cycles later in interleaved mode. The very next sample, N + 1, will be sampled by the next rising clock edge and available at Port B, 14 cycles after that clock edge. In dual parallel mode, Port A has a 15 cycle latency and Port B has a 14 cycle latency, but data is

available at the same time. Driving each ADC's DS inputs by the same sync signals will accomplish this. An easy way to accomplish synchronization is by a one time sync at power-on reset. Note that when running the AD9430 in LVDS mode, set DS+ to ground and DS– to 3.3 V, as the DS inputs are relevant only in CMOS output mode, simplifying the design for some applications as well as affording superior SNR/SINAD performance at higher encode/analog frequencies.

Digital Outputs

The off-chip drivers on the chip can be configured to provide CMOS or LVDS compatible output levels via Pin S2. The CMOS digital outputs (S2 = 0) are TTL/CMOS compatible for lower power consumption. The outputs are biased from a separate supply (DRVDD), allowing easy interface to external logic. The outputs are CMOS devices that will swing from ground to DRVDD (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (< 1 inch, for a total C_{LOAD} < 5 pF). When operating in CMOS mode, it is also recommended to place low value (20 Ω) series damping resistors on the data lines to reduce switching transient effects on performance.

LVDS Outputs

LVDS outputs are available when S2 = V_{DD} and a 3.7 Ω RSET resistor is placed at Pin 7 (LVDSBIAS) to ground. The RSET resistor current is ratioed on-chip, setting the output current at each output equal to a nominal 3.5 mA (11 3 IRSET). A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. LVDS mode facilitates interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor as close to the receiver as possible. It is recommended to keep the trace length 1–2 inches and to keep differential output trace lengths as equal as possible.

Clock Outputs (DCO+, DCO–)

The input ENCODE is divided by two (in CMOS mode) and available off-chip at DCO+ and DCO–. These clocks can facilitate latching off-chip, providing a low skew clocking solution (see timing diagram). The on-chip clock buffers should not drive more than 5 pF of capacitance to limit switching transient effects on performance. Note that the outputs clocks are CMOS levels when CMOS mode is selected (S2 = 0) and are LVDS levels when in LVDS mode (S2 = V_{DD}), (requiring a 100 Ω differential termination at receiver in LVDS mode). The output clock in LVDS mode switches at the ENCODE rate.

Voltage Reference

A stable and accurate 1.23 V voltage reference is built into the AD9430 (VREF). The analog input full-scale range is linearly proportional to the voltage at VREF. Note that an external reference can be used by connecting the SENSE pin to V_{DD} (disabling internal reference) and driving VREF with the external reference source. No appreciable degradation in performance occurs when VREF is adjusted ±5%. A 0.1 µF capacitor to ground is recommended at the VREF pin in internal and external reference applications. Float the SENSE pin for internal reference operation.

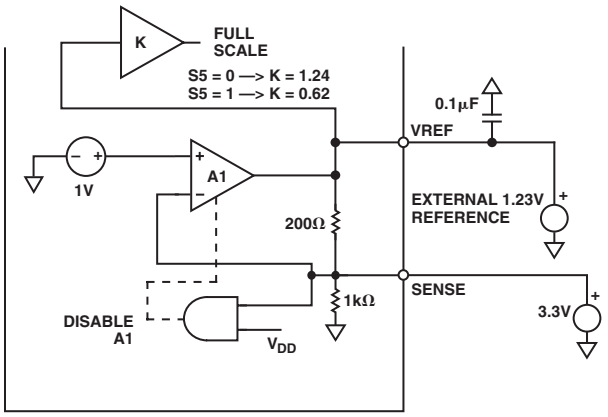


Figure 12. Using an External Reference

NPR Testing

Noise Power Ratio Testing is a test that is commonly used to characterize the return path of cable systems where the signals are typically QAM signals with a "noise-like" frequency spectrum. NPR performance of the AD9430 was characterized in the lab yielding an effective NPR = 56.9 dB at an analog input of 19 MHz. This agrees with a theoretical maximum NPR of 57.1 dB for an 11-bit ADC at 13.6 dB backoff. The rms noise power of the signal inside the notch is compared with the rms noise level outside the notch using an FFT. Sufficiently long record lengths to guarantee a sufficient number of samples inside the notch is a requirement, as well as a high order band-stop filter that provides the required notch depth for testing.

AD9430 EVALUATION BOARD

The AD9430 evaluation board offers an easy way to test the AD9430. It requires a clock source, an analog input signal, and a 3.3 V power supply. The clock source is buffered on the board to provide the clocks for the ADC, an on-board DAC, latches, and a data ready signal. The digital outputs and output clocks are available at two 40-pin connectors, P3 and P4. See Figure 18. The board has several different modes of operation and is shipped in the following configuration:

- Offset Binary
- Internal Voltage Reference
- CMOS Parallel Timing
- Full-Scale Adjust = Low

Power Connector

Power is supplied to the board via a detachable 12-lead power strip (three 4-pin blocks).

Table II. Power Connector

AVDD 3.3 V	Analog Supply for ADC (~ 350 mA)
DRVDD 3.3 V	Output Supply for ADC (~ 28 mA)
VDL 3.3 V	Supply for Support Logic and DAC (~ 350 mA)
EXT_VREF*	Optional External Reference Input
VCLK/V_XTAL	Supply for Clock Buffer/Optional XTAL
VAMP	Supply for Optional Amp

*LVEL16 clock buffer can be powered from AVDD or VCLK at E47 jumper (AVDD, DRVDD, and VDL are the minimum required power connections).

Analog Inputs

The evaluation board accepts a 1.3 V p-p analog input signal centered at ground at SMB connector J4. This signal is terminated to ground through 50 Ω by R16. The input can be alternatively terminated at transformer T1 secondary by R13 and R14. T1 is a wideband RF transformer providing the single-ended-to-differential conversion, allowing the ADC to be driven differentially, minimizing even order harmonics. An optional second transformer, T2, can be placed following T1 if desired. This would provide some performance advantage (~1–2 dB) for high analog input frequencies (>100 MHz). If T2 is placed, two shorting traces at the pads would need to be cut. The analog signal is low-pass filtered by R41, C12, and R42, C13 at the ADC input.

Gain

Full scale is set at E17–E19. Connecting E17 to E18 sets S5 low, full scale = 1.5 V differential; connecting E17 to E19 sets S5 high, full scale = 0.75 V differential.

ENCODE

The ENCODE clock is terminated to ground through 50 Ω at SMB connector J5. The input is ac-coupled to a high speed differential receiver (LVEL16) that provides the required low jitter, fast edge rates needed for optimum performance. J5 input should be > 0.5 V p-p. Power to the EL16 is set at jumper E47. Connecting E47 to E45 powers the buffer from AVDD, connecting E47 to E46 powers the buffer from VCLK/V_XTAL.

Voltage Reference

The AD9430 has an internal 1.23 V voltage reference. The ADC uses the internal reference as the default when jumpers E24–E27 and E25–E26 are left open. The full scale can be increased by placing optional resistor R3. The required value would vary with the process and needs to be tuned for the specific application. Full scale can similarly be reduced by placing R4; tuning would be required here as well. An external reference can be used by shorting the SENSE pin to 3.3 V (place jumper E26–E25). E27–E24 jumper connects the ADC VREF pin to EXT_VREF pin at the power connector.

Data Format Select

Data format select sets the output data format of the ADC. Setting DFS (E1 to E2) low sets the output format to be offset binary; setting DFS high (E1 to E3) sets the output to twos complement.

I/P

Output timing is set at E11–E13. E12 to E11 sets S4 low for parallel output timing mode. E11 to E13 sets S4 high for interleaved timing mode.

Timing Controls

Flexibility in latch clocking and output timing is accomplished by allowing for clock inversion at the timing controls section of the PCB. Each buffered clock is buffered by an XOR and can be inverted by moving the appropriate jumper for that clock.

Data Outputs

The ADC digital outputs are latched on the board by four LVT574s; the latch outputs are available at the two 40-pin connectors at Pins 11–33 on P23 (Channel A) and Pins 11–33 on P3 (Channel B). The latch output clocks (data ready) are available at Pin 37 on P23 (Channel A) and Pin 37 on P3 (Channel B). The data ready clocks can be inverted at the timing controls section if needed.

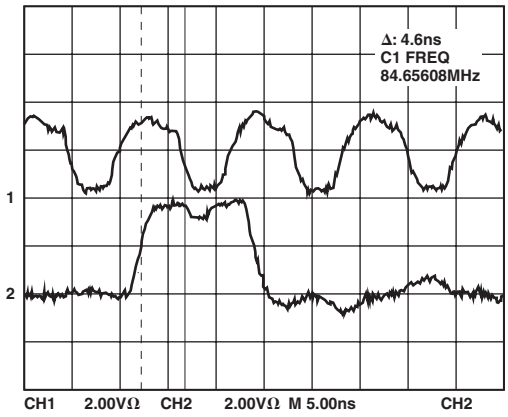


Figure 13. Data Output and Clock @ 80-Pin Connector

DAC Outputs

Each channel is reconstructed by an on-board dual-channel DAC, an AD9753. This DAC is intended to assist in debug—it should not be used to measure the performance of the ADC. It is a current output DAC with on-board 50 Ω termination resistors. The figure below is representative of the DAC output with a full-scale analog input. The scope setting is low bandwidth.

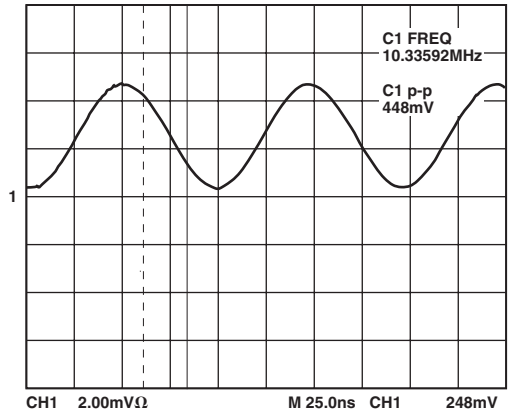


Figure 14. DAC Output

ENCODE XTAL

An optional XTAL oscillator can be placed on the board to serve as a clock source for the PCB. Power to the XTAL is through the VCLK/VXTAL pin at the power connector. If an oscillator is used, ensure proper termination for best results. The board has been tested with a Valpey Fisher VF561 and a Vectron JN00158-163.84. Test results for the VF561 are shown in Figure 15.

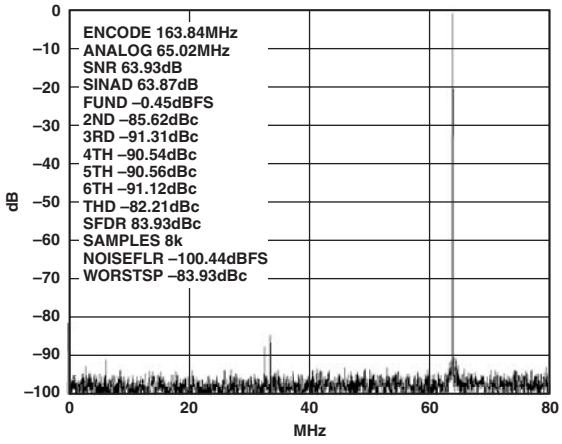


Figure 15. FFT—Using VF561 XTAL as Clock Source

Optional Amplifier

The footprint for transformer T2 can be modified to accept a wideband differential amplifier (AD8350) for low frequency applications where gain is required. Note that Pin 2 would need to be lifted and left floating for operation. Input transformer T1 would need to be modified to a 4:1 for impedance matching and ADC input filtering would enhance performance (see the AD8350 data sheet). SNR/SINAD performance of 61 dB/60 dB is possible and would start to degrade at about 30 MHz.

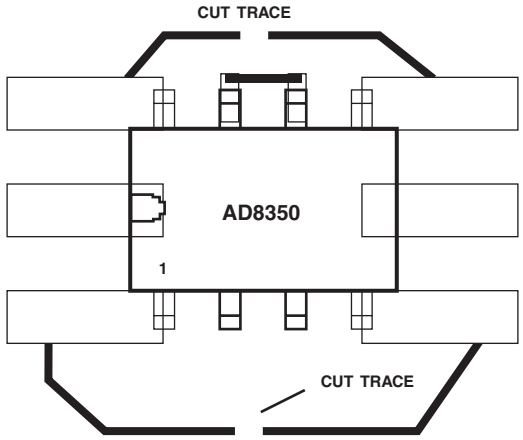


Figure 16. Using the AD8350 on the AD9430 PCB

Troubleshooting

If the board does not seem to be working correctly, try the following:

- Verify power at IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify VREF is at 1.23 V.
- Try running clock and analog inputs at low speeds (10 MSPS/1 MHz) and monitor latch, DAC, and ADC for toggling.

The AD9430 evaluation board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability, or fitness for a particular purpose.

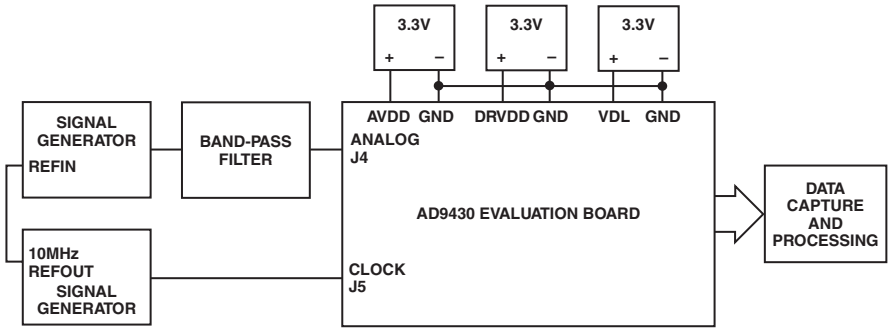


Figure 17. Evaluation Board Connections

Table III. Evaluation Board Bill of Materials

No.	Quantity	Reference Designator	Device	Package	Value	Comments
1	47	C1, C3–C11, C15–C17, C19–C29, C31–C48, C58–C62	Capacitor	0603	0.1 µF	C43, C47 Not Placed
2	1	C2	Capacitor	0603	10 pF	Not Placed
3	2	C12, C13	Capacitor	0603	20 pF	Not Placed
4	1	C14	Capacitor	0603	0.01 µF	
5	1	C18	Capacitor	0603	1 µF	
6	7	C30, C49, C63–C67	Capacitor	CAPL	10 µF	C30 Not Placed
7	9	E3–E1–E2	3-Pin Header/Jumper			
		E19–E17–E18	3-Pin Header/Jumper			
		E13–E11–E12	3-Pin Header/Jumper			
		E26–E25–E27–E24	4-Pin Header			
		E46–E47–E45	3-Pin Header/Jumper			
		E35–E33–E34	3-Pin Header/Jumper			
		E32–E30–E31	3-Pin Header/Jumper			
		E29–E23–E28	3-Pin Header/Jumper			
		E22–E16–E21	3-Pin Header/Jumper			
8	6	J1, J2, J3, J4, J5, J6	SMB	SMB		J2 Not Placed
9	2	P3, P23	40-Pin Header			
10	3	P4, P21, P22	4-Pin Power Connector	Post	Z5.531.3425.0	Wieland
				Detachable Connector	25.602.5453.0	Wieland
11	10	R1, R5, R13, R14, R16, R25, R27, R28, R41, R42	Resistor	0603	50 Ω	R1, R13, R14 Not Placed
12	3	R2, R3, R4	Resistor	0603	3.9 kΩ	R3, R4 Not Placed
13	14	R6–R8, R10, R15, R21–R24, R33–R36, R38	Resistor	0603	100 Ω	R15, R21–R24, Not Placed
14	5	R9, R11, R12, R30, R37	Resistor	0603	0 Ω	
15	4	R17, R18, R19, R20	Resistor	0603	510 Ω	
16	1	R26	Resistor	0603	2 kΩ	
17	1	R29	Resistor	0603	390 Ω	
18	7	R31, R32, R39, R40, R43, R44, R45	Resistor	0603	1 kΩ	
19	4	RZ1, RZ2, RZ3, RZ4	Resistor Pack 220 Ω	SO16RES	742C163221JTR	CTS
20	8	RZ5, RZ6, RZ7, RZ8, RZ9, RZ10, RZ11, RZ12	Resistor Pack 22 Ω	SO16RES	742C163220JTR	CTS
21	2	T1, T2	Transformer	CD542	Mini-Circuits ADT1–1WT	T2 Not Placed
22	1	U1	AD9430BSV	TQFP100	ADC	
23	1	U2	MC100LVEL16D	SO8NB	Clock Buffer	
24	1	U3	74LVC86	SO14NB	XOR	
25	4	U4, U5, U6, U7	74LVT574	SO20	Latch	
26	1	U9	AD9753AST	LQFP48	DAC	

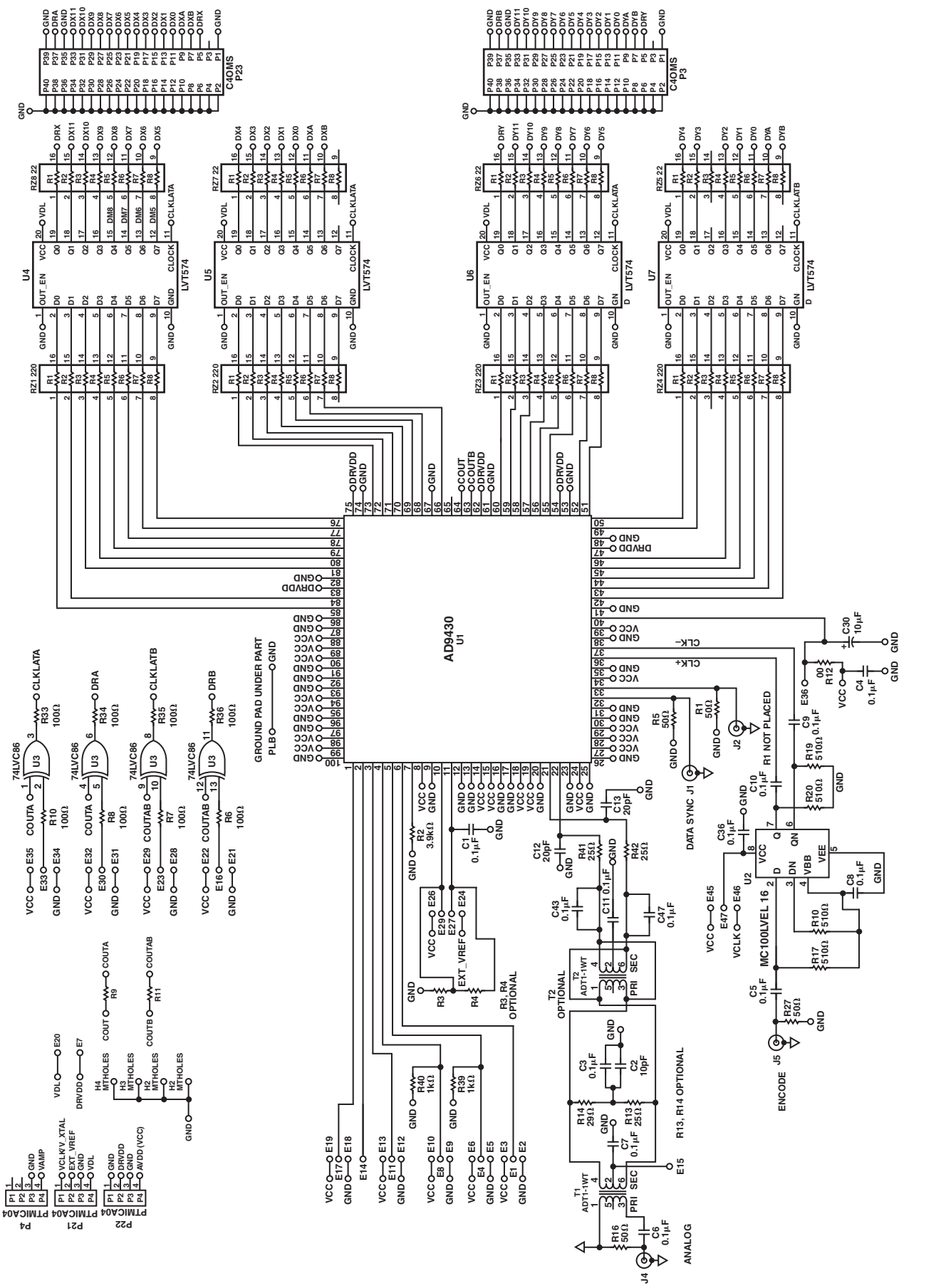


Figure 18a. Evaluation Board Schematic

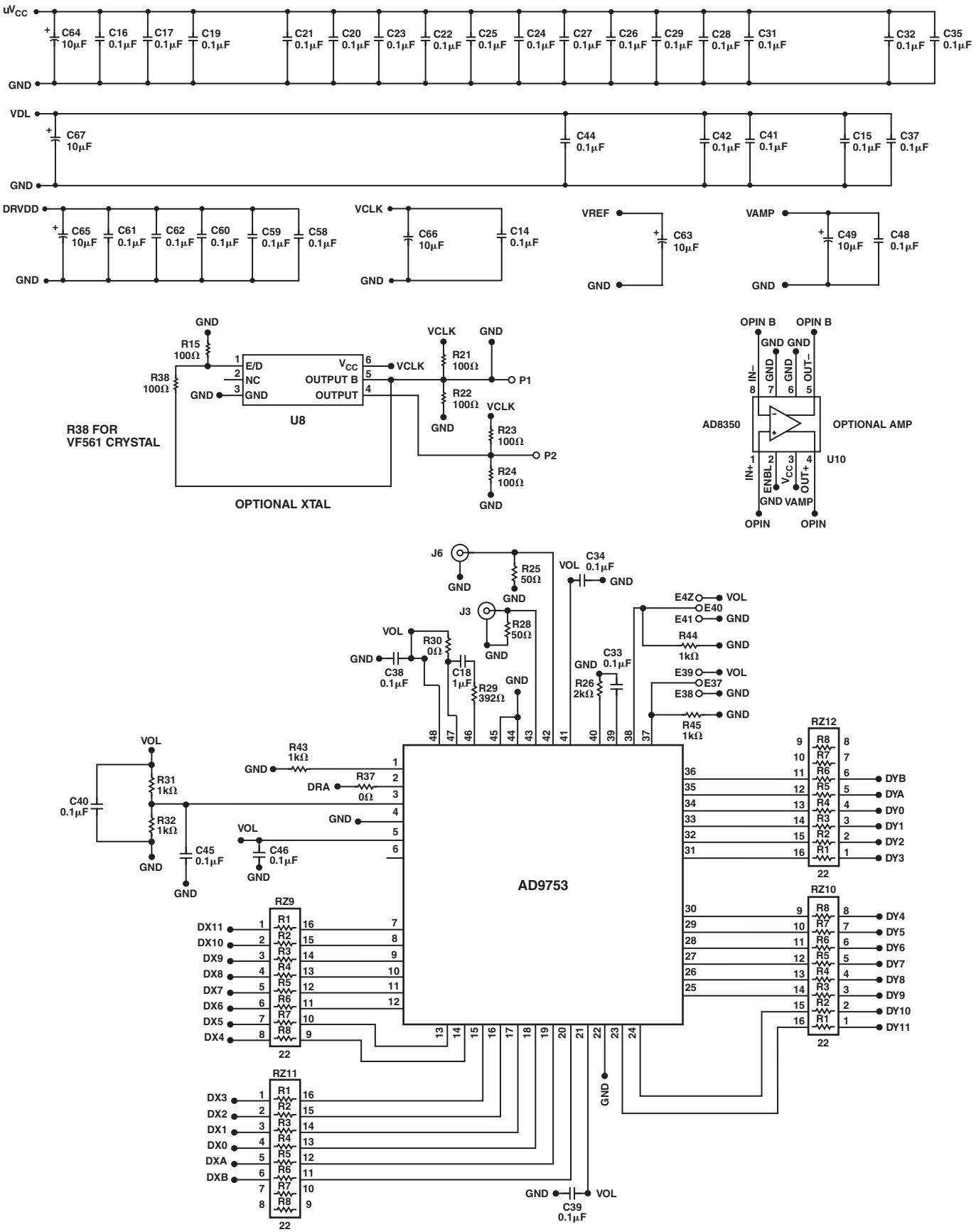


Figure 18b. Evaluation Board Schematic (continued)

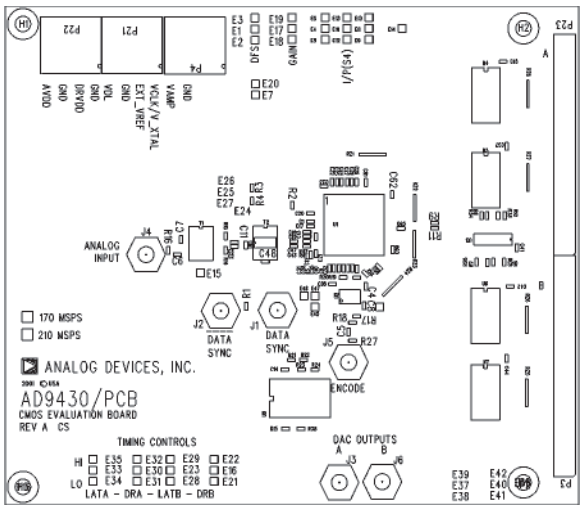


Figure 19. PCB Top Side Silkscreen

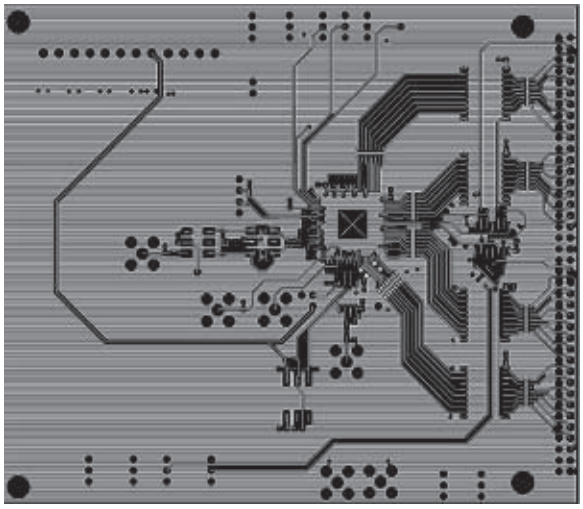


Figure 20. PCB Top Side Copper

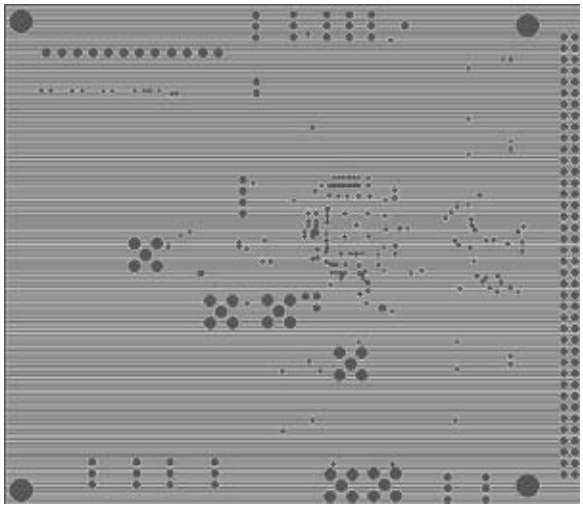


Figure 21. PCB Ground Layer

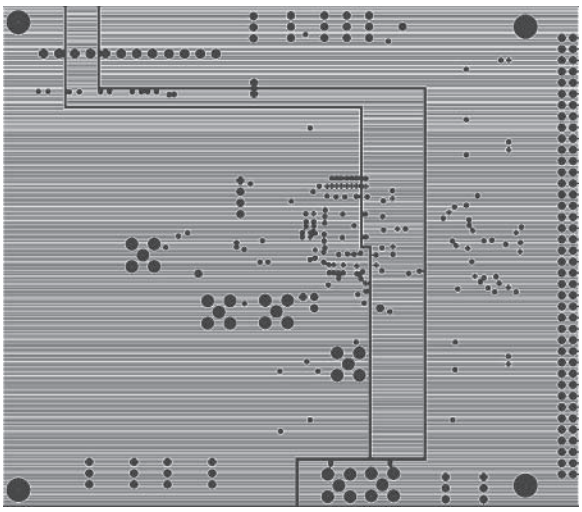


Figure 22. PCB Split Power Plane

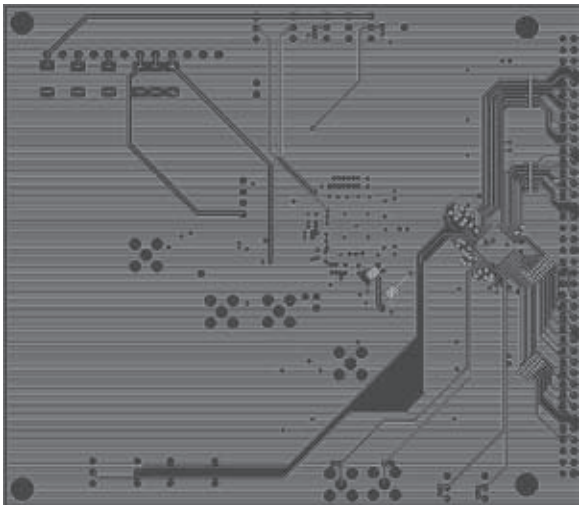


Figure 23. PCB Bottom Side Copper

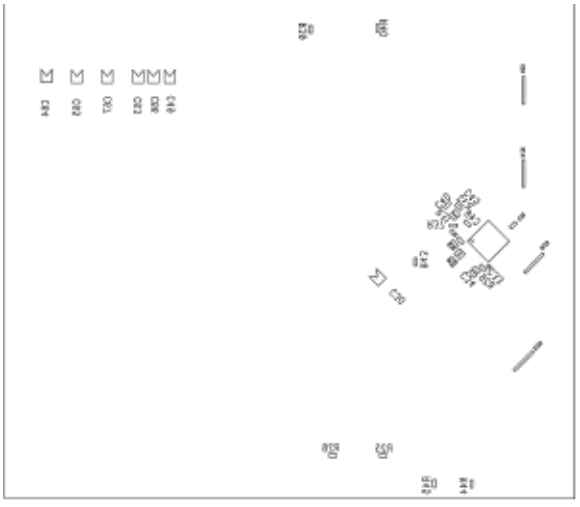
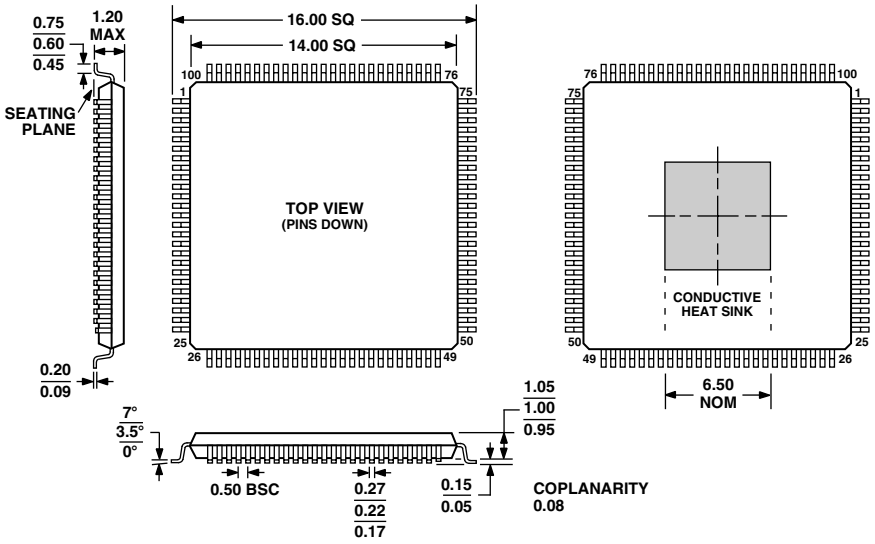


Figure 24. PCB Bottom Side Silkscreen

OUTLINE DIMENSIONS

100-Lead Thin Plastic Quad Flat Package, Exposed Pad [TQFP/EP]
(SV-100)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026AED-HD

NOTES

1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE AD9430 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

Revision History

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C02607–0–3/03(A)

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