NEC

MOS FIELD EFFECT TRANSISTOR
2SK3113

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3113 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

Part Number	Package
2SK3113	TO-251
2SK3113-Z	TO-252

FEATURES

- Low gate charge
  Q_G = 9 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 2.0 A)
- Gate voltage rating ±30 V
- Low On-state resistance
  $R_{DS(on)}$ = 4.4 Ω (MAX.) (V_{GS} = 10 V, I_D = 2.0 A)
- Avalanche capability ratings

ABSOLUTE MAXIMUM RATING (T_A = 25°C)

Drain to source voltage (V_{GS} = 0 V)	V_{DSS}	600	V
Gate to source voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain current (DC) (T_C = 25°C)	$I_{D(DC)}$	±2.0	A
Drain current (pulse) Note1	$I_{D(pulse)}$	±8.0	A
Total power dissipation (T_A = 25°C) Note2	P_{T1}	1.0	W
Total power dissipation (T_C = 25°C)	P_{T2}	20	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C
Single avalanche current Note3	I_{AS}	2.0	A
Single avalanche energy Note3	E_{AS}	2.7	mJ
Diode recovery dv/dt Note4	dv/dt	3.5	V/ns

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. On glass epoxy board with 40 x 40 x1.6 mm

3. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω , V_{GS} = 20 V→0 V

4. I_F ≤ 1.0 A, V_{clamp} = 600 V, di/dt ≤ 100 A/μs, T_A = 25°C

The information in this document is subject to change without notice.

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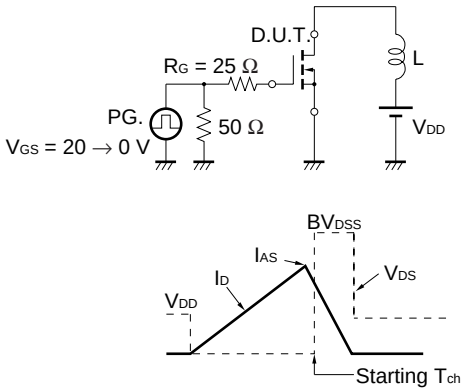
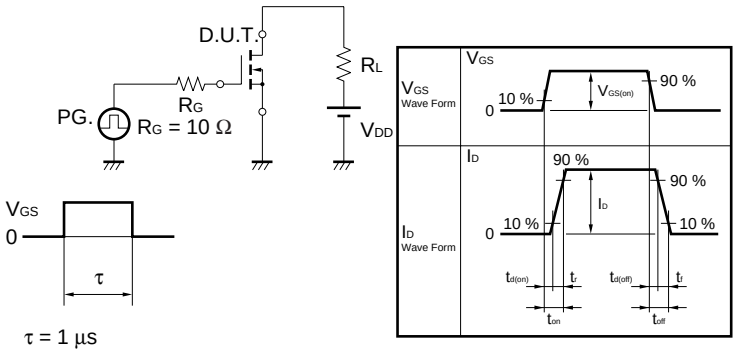
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 600 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	0.5			S	V_{DS} = 10 V, I_D = 1.0 A
Drain to Source On-state Resistance	$R_{DS(on)}$		3.3	4.4	Ω	V_{GS} = 10 V, I_D = 1.0 A
Input Capacitance	C_{iss}		290		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		60		pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss}		5		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		7		ns	V_{DD} = 150 V, I_D = 1.0 A
Rise Time	t_r		2		ns	$V_{GS(on)}$ = 10 V
Turn-off Delay Time	$t_{d(off)}$		22		ns	R_G = 10 Ω
Fall Time	t_f		9		ns	R_L = 10 Ω
Total Gate Charge	Q_G		9		nC	V_{DD} = 450 V
Gate to Source Charge	Q_{GS}		2.4		nC	V_{GS} = 10 V
Gate to Drain Charge	Q_{GD}		2		nC	I_D = 2.0 A
Diode Forward Voltage	$V_{F(S-D)}$		0.9		V	I_F = 2.0 A, V_{GS} = 0 V
Reverse Recovery Time	T_{rr}		0.9		μs	I_F = 2.0 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}		2.0		μC	di/dt = 50 A/μs

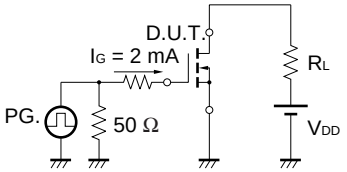
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

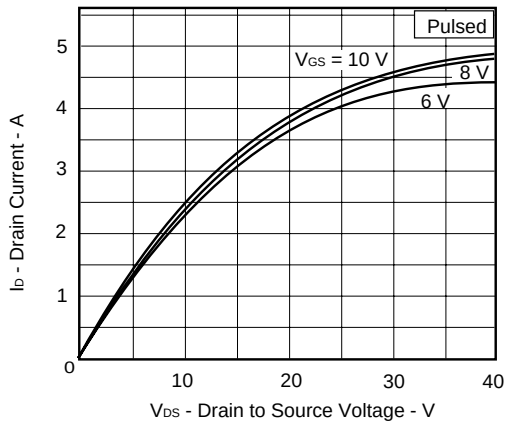


TEST CIRCUIT 3 GATE CHARGE

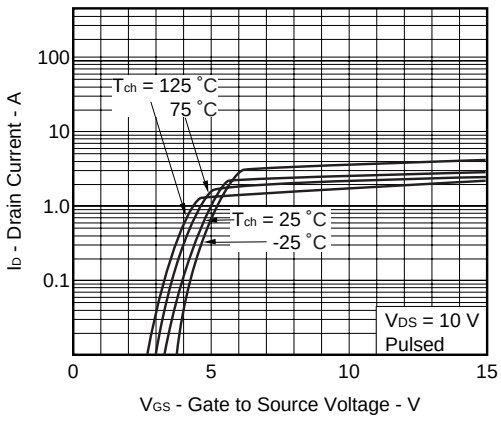


TYPICAL CHARACTERISTICS (T_A = 25°C)

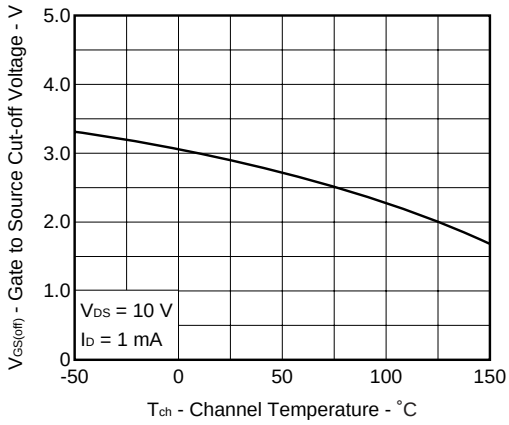
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



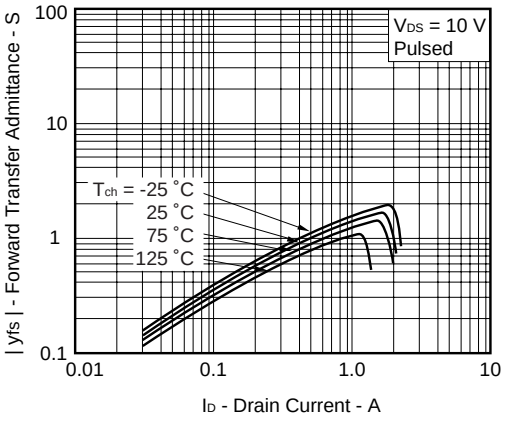
FORWARD TRANSFER CHARACTERISTICS



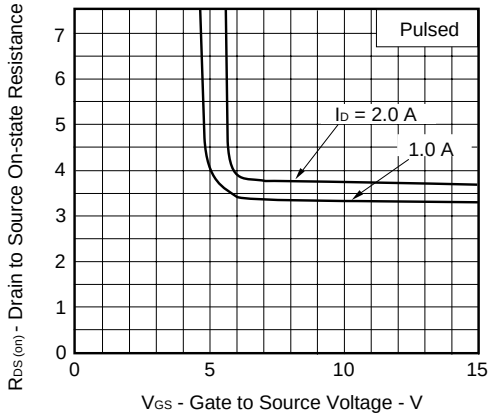
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



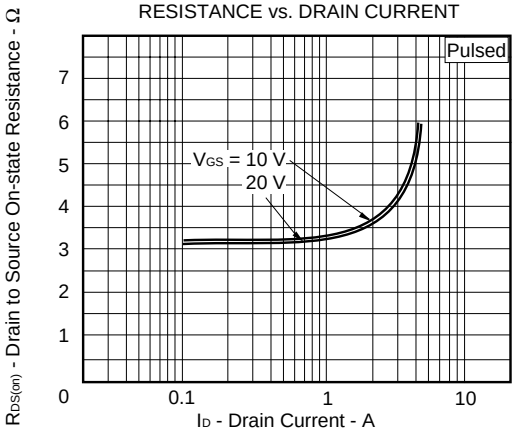
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



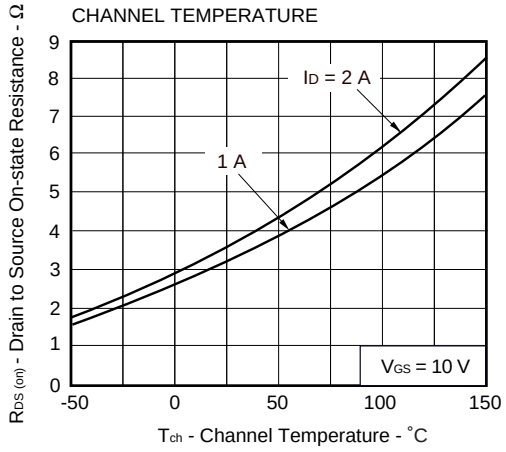
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



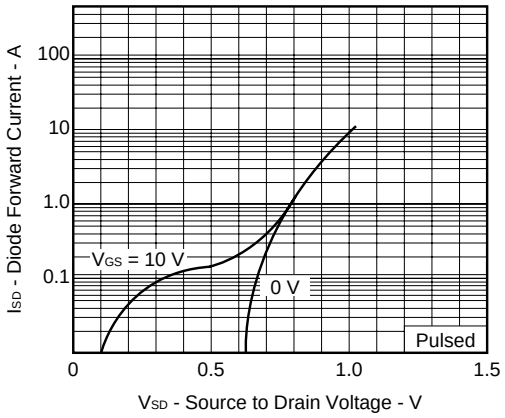
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



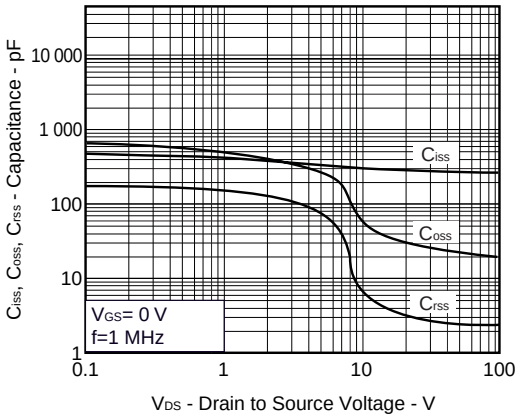
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



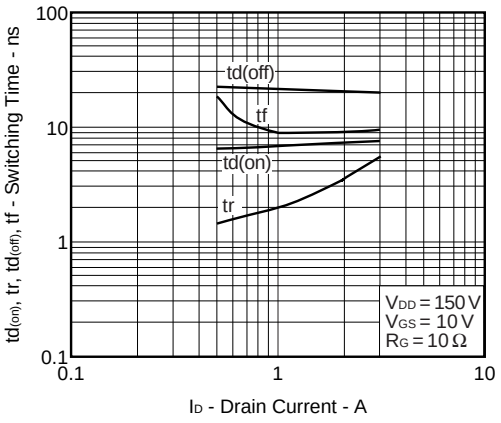
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



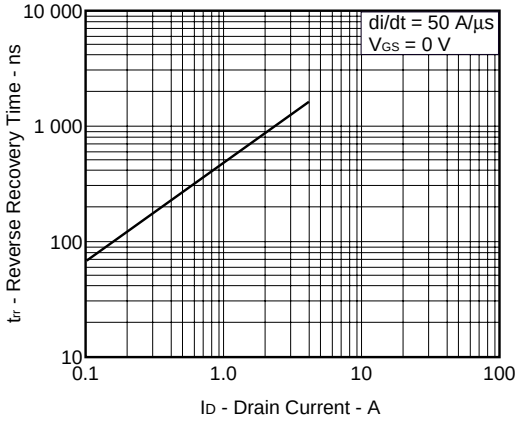
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



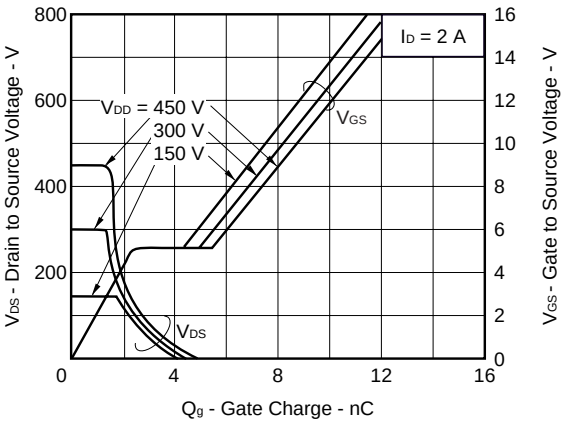
SWITCHING CHARACTERISTICS



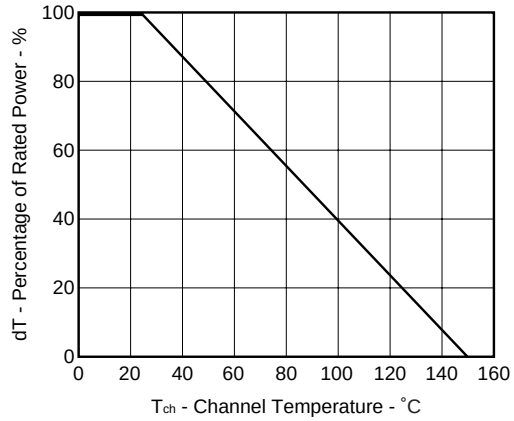
REVERSE RECOVERY TIME vs. DRAIN CURRENT



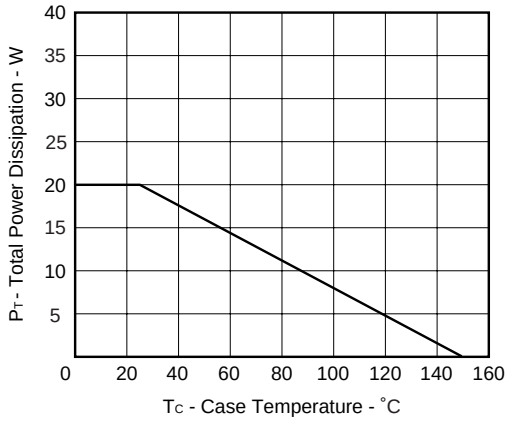
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



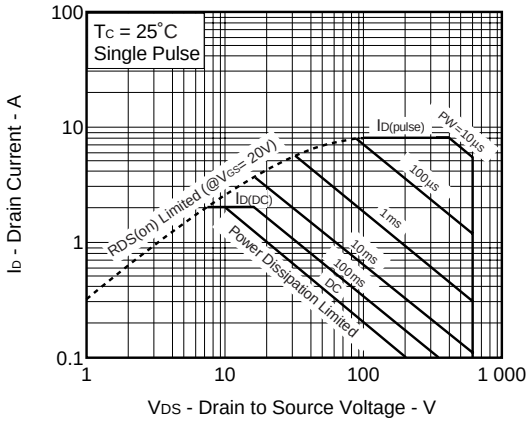
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



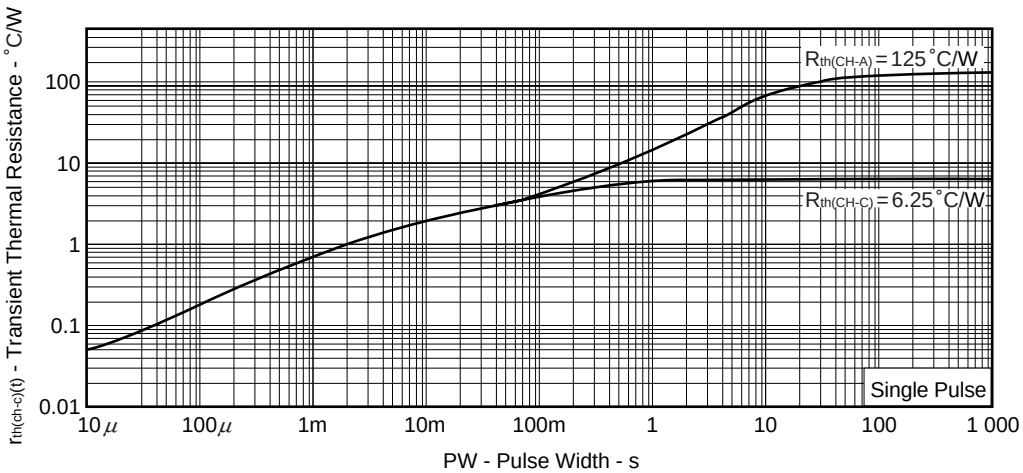
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



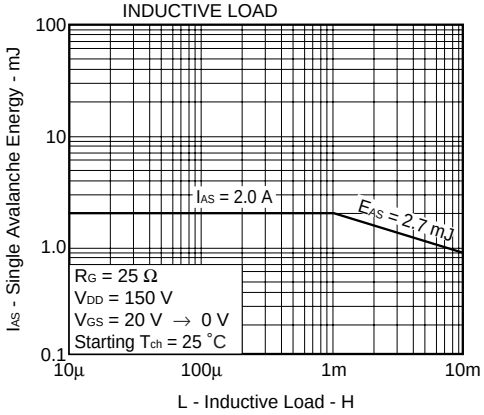
FORWARD BIAS SAFE OPERATING AREA



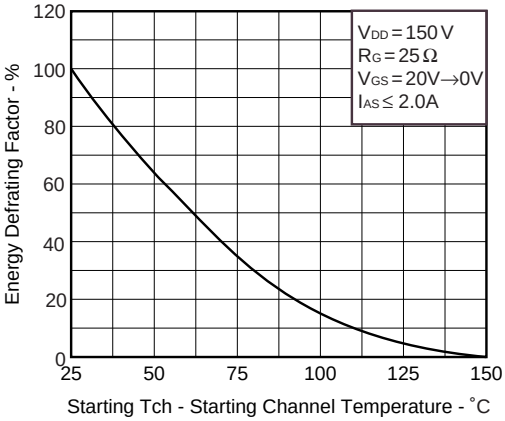
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE ENERGY vs.
INDUCTIVE LOAD

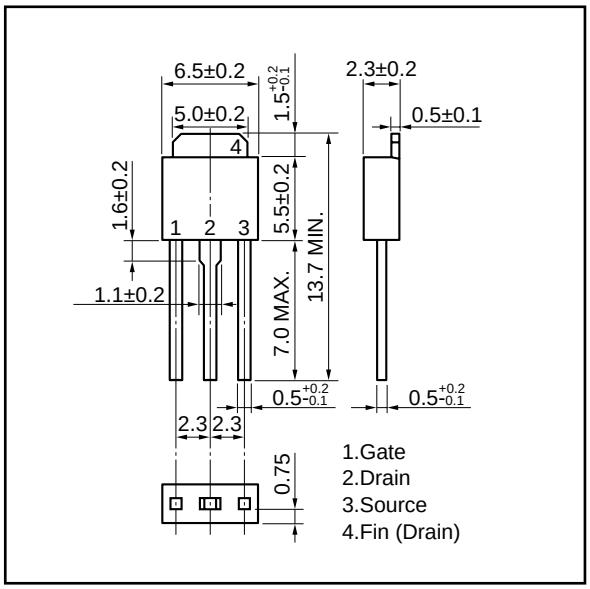


SINGLE AVALANCHE ENERGY
DERATING FACTOR

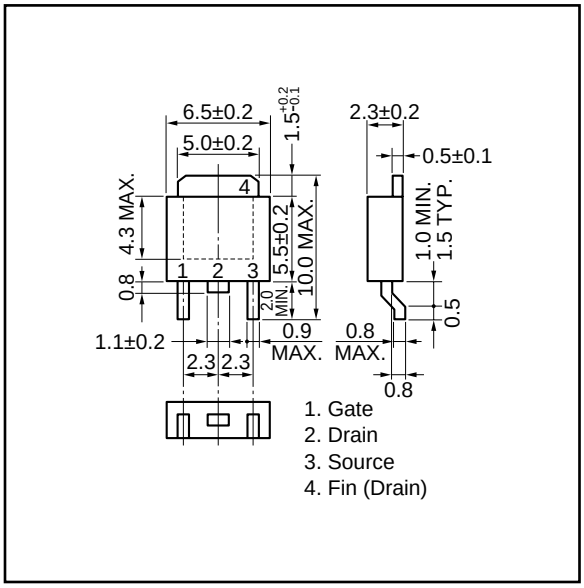


PACKAGE DRAWINGS (Unit : mm)

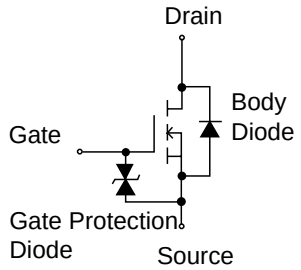
1)TO-251 (MP-3)



2)TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.