

2SA1344, 2SC3398



2018A

PNP/NPN Epitaxial Planar
Silicon Transistors

T-37-13
T-35-11

Switching Applications (with Bias Resistances $R_1=10k\Omega$, $R_2=10k\Omega$)

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Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit.

Features

- Built-in bias resistor ($R_1=10k\Omega$, $R_2=10k\Omega$).
- Small-sized package (CP).

(): 2SA1344

Absolute Maximum Ratings/ $T_a=25^\circ C$

			unit
Collector to Base Voltage	V_{CBO}	(-)50	V
Collector to Emitter Voltage	V_{CEO}	(-)50	V
Emitter to Base Voltage	V_{EBO}	(-)10	V
Collector Current	I_C	(-)100	mA
Peak Collector Current	i_{cp}	(-)200	mA
Collector Dissipation	P_C	200	mW
Junction Temperature	T_j	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$

Electrical Characteristics/ $T_a=25^\circ C$

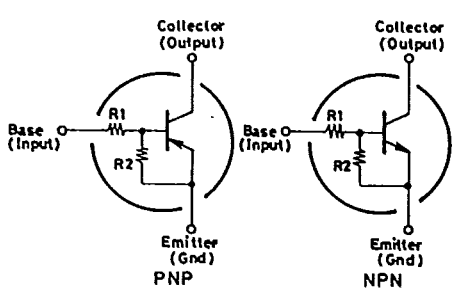
			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	$V_{CB}=(-)40V, I_E=0$			(-)0.1	μA
Collector Cutoff Current	I_{CEO}	$V_{CE}=(-)40V, I_B=0$			(-)0.5	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=(-)5V, I_C=0$	(-)170	(-)250	(-)330	μA
DC Current Gain	h_{FE}	$V_{CE}=(-)5V, I_C=(-)10mA$	50			
Gain Band-width product	f_T	$V_{CE}=(-)10V, I_C=(-)5mA$		250		MHz
				(200)		
Output Capacitance	c_{ob}	$V_{CB}=(-)10V, f=1MHz$		3.5		pF
				(5.3)		
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)10mA, I_B=(-)0.5mA$	(-)0.1	(-)0.3		V

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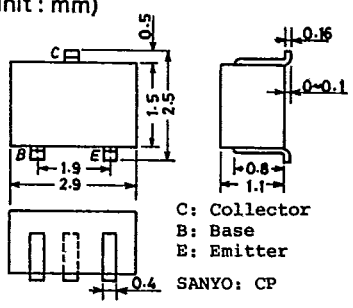
Marking

2SA1344: EL, 2SC3398: EY

Electrical Connection



Case Outline 2018A (unit : mm)



2SA1344/2SC3398

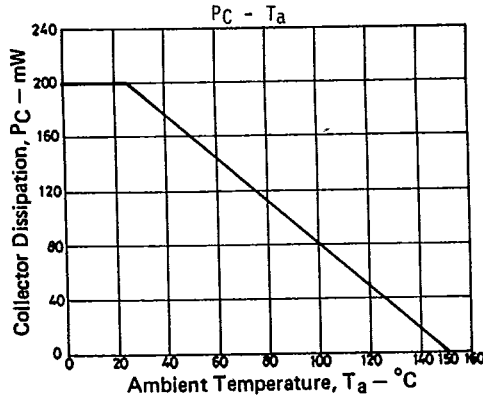
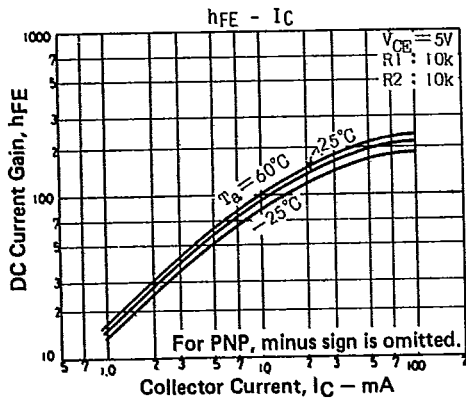
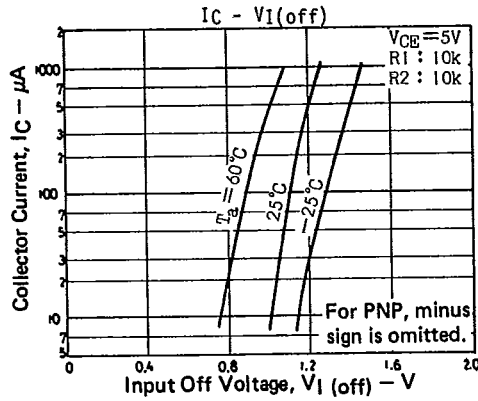
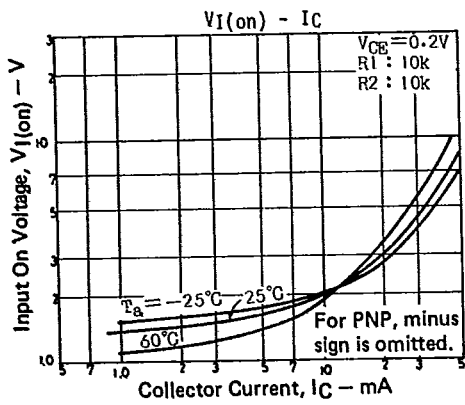
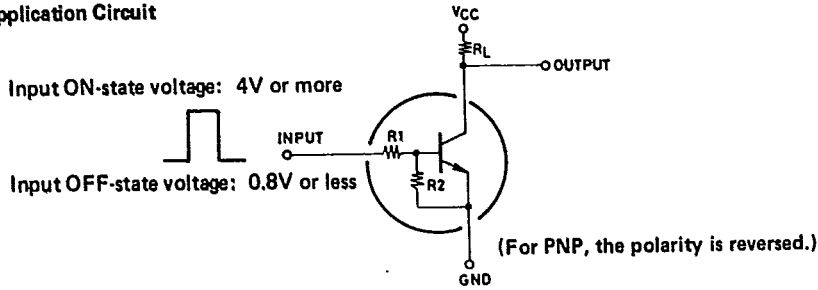
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			min	typ	max	unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu A, I_E=0$	(-)50			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)100\mu A, R_{BE}=\infty$	(-)50			V
Input Off Voltage	$V_{I(off)}$	$V_{CE}=(-)5V, I_C=(-)100\mu A$	(-)0.8	(-)1.1	(-)1.5	V
Input On Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2V, I_C=(-)10mA$	(-)1.0	(-)2.0	(-)4.0	V
Input Resistance	R_1		7.0	10	13	k Ω
Input Resistance Ratio	R_1/R_2		0.9	1.0	1.1	-

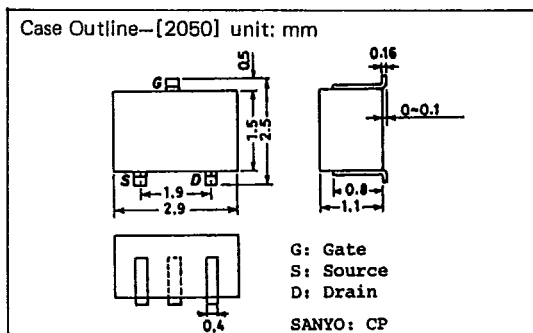
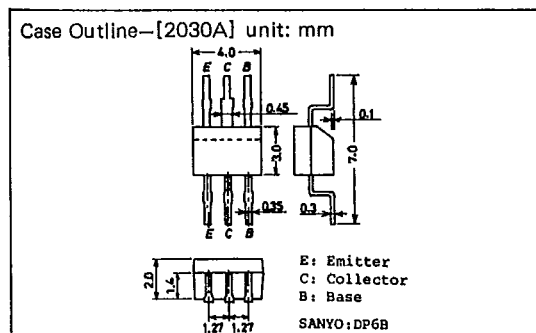
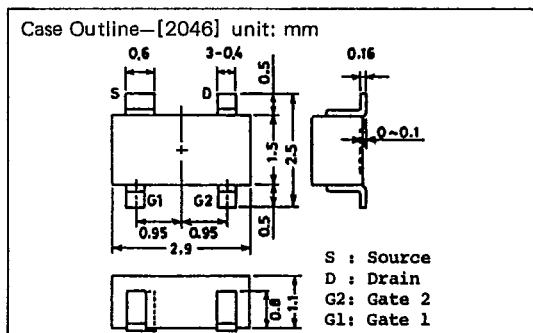
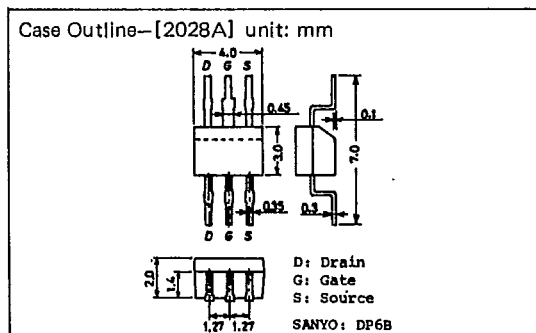
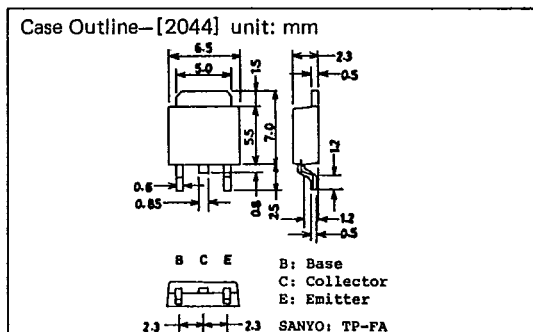
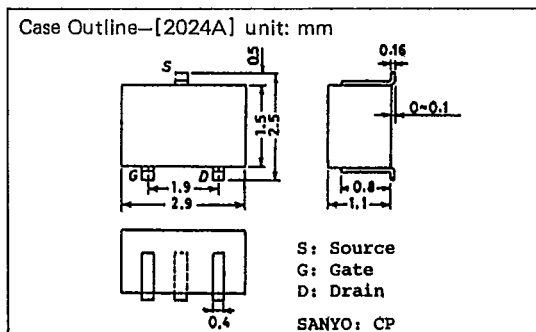
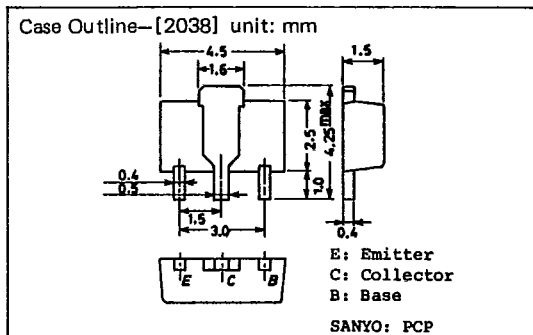
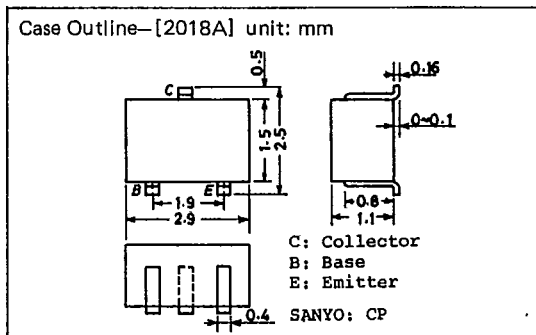
■ Sample Application Circuit



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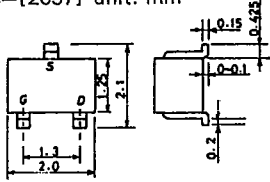
CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



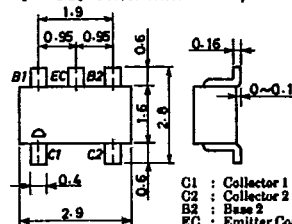
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Case Outline—[2057] unit: mm



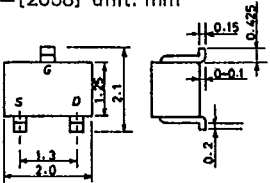
S: Source
G: Gate
D: Drain
SANYO: MCP

Case Outline—[2066] unit: mm



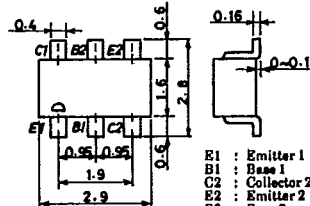
C1 : Collector 1
C2 : Collector 2
B2 : Base 2
EC : Emitter Common
B1 : Base 1
SANYO : CP6

Case Outline—[2058] unit: mm



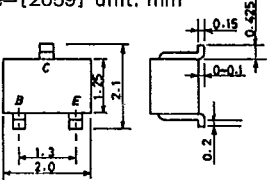
G: Gate
S: Source
D: Drain
SANYO: MCP

Case Outline—[2067] unit: mm



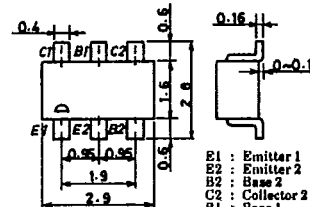
E1 : Emitter 1
B1 : Base 1
C2 : Collector 2
E2 : Emitter 2
B2 : Base 2
C1 : Collector 1
SANYO : CP6

Case Outline—[2059] unit: mm



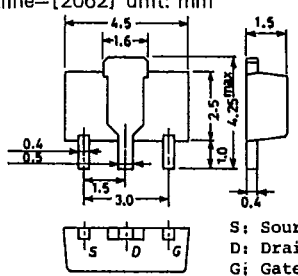
B: Base
C: Collector
E: Emitter
SANYO: MCP

Case Outline—[2068] unit: mm



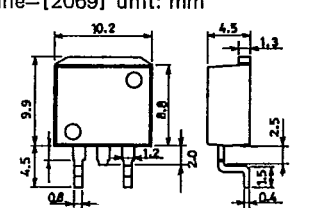
E1 : Emitter 1
E2 : Emitter 2
B2 : Base 2
C2 : Collector 2
B1 : Base 1
C1 : Collector 1
SANYO : CP6

Case Outline—[2062] unit: mm



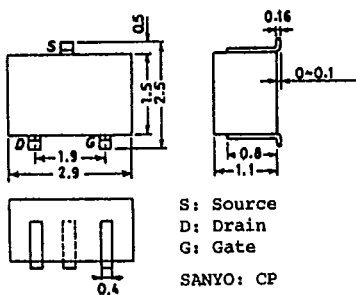
S: Source
D: Drain
G: Gate
SANYO: PCP

Case Outline—[2069] unit: mm



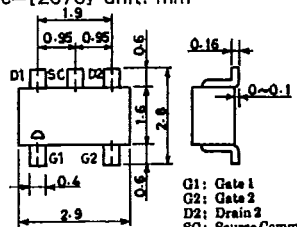
B: Base
C: Collector
E: Emitter
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source
D: Drain
G: Gate
SANYO: CP

Case Outline—[2070] unit: mm



G1 : Gate 1
G2 : Gate 2
D2 : Drain 2
SC : Source Common
D1 : Drain 1
SANYO : CP6

T-9120

