PM7380

FREEDM™-32P672

DEVELOPMENT KIT BOARD

DESIGN DOCUMENT

ISSUE 1: DECEMBER 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
Issue 1	December 2000	Document created

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1 ACRONYMS

DS-1:	Digital Signal Level 1, 1.544 Mbit/s.
T1:	Transmission at DS-1, 1.544 Mbit/s.
DS-3:	Digital Signal Level 3, 44.736 Mbit/s.
E1:	European Digital Signal Level 1, 2.048 Mbit/s.
PCI:	Peripheral Component Interconnect
HDLC:	High Level Data Link Control
BERT:	Bit Error Rate Test
FREEDM™-32P672:	Frame Engine and Data Link Manager
H-MVIP:	High Speed Multi-Vendor Integration Protocol. A synchronous TDM bus of N X 64 Kbit/s constant bit rate data streams.

2 OVERVIEW

2.1 Scope

This document describes the FREEDM™-32P672 Development Kit Board.

3 FUNCTIONAL DESCRIPTION

3.1 Overview

The FREEDM™-32P672 chip is a multichannel HDLC controller, with a 33-MHz/66-MHz, 32-bit PCI 2.1 compliant bus for configuration, monitoring, and packet data transfer. It supports up to 672 bidirectional HDLC channels. The following channel assignments are possible:

- 672 HDLC channels assigned to a maximum of 32 channelized T1/E1 links.
- 672 HDLC channels assigned to a maximum of 32 H-MVIP links (at 2.048 Mbps per link) or 8 H-MVIP links (at 8.192 Mbps per link).
- 32 HDLC channels assigned to arbitrary rate links, subject to a maximum aggregate link clock rate of 64 MHz.
- Channels assigned to links 0 to 2 that support a clock rate of up to 52 MHz. Channels assigned to links 3 to 31 that support a clock rate of up to 10 MHz.

The FREEDM™-32P672 development kit consists of a PCI Universal card that contains the FREEDM™-32P672 chip. Clock generation and distribution on the board enables the FREEDM™-32P672 chip to operate in various supported modes. The 2.5 V and 3.3 V voltage regulators used on the board provide a regulated supply for the FREEDM™-32P672 chip. External loopback on a per link basis is provided at the line interface of the chip. The PHY layer functionality is not implemented on the board. A provision is made for connecting the clock, data, and frame pulse signals from an external source. The development kit board provides a platform to implement and test software for the FREEDM™-32P672 chip.

3.2 Features and Benefits

The Development Kit board supports up to 32 data links, which you can configure to operate in the following modes:

- 2.048 Mbit/s H-MVIP
- 8.192 Mbit/s H-MVIP
- Non-HMVIP

- Mixed

3.2.1 2.048 Mbit/s H-MVIP Mode

You can configure the FREEDM™-32P672 to interface with the H-MVIP digital telephony buses at 2.048 Mbps. For 2.048 Mbps H-MVIP links, TD[31..0] and RD[31..0] are the transmit and receive links respectively. For the 2.048 Mbps H-MVIP operation, the links are grouped into four logical groups of eight links each. A common clock is shared among the links in each logical group. The four logical groups include links 0 through 7, 8 through 15, 16 through 23, and 24 through 31. The shared transmit clocks of these groups are respectively TMVCK[0], TMVCK[1], TMVCK[2], and TMVCK[3]. The shared receive clocks of these groups are respectively RMVCK[0], RMVCK[1], RMVCK[2], and RMVCK[3]. Both RMVCK[n] and TMVCK[n] have 4.096MHz clock frequency.

For channelized operations, frame pulse signals must be generated from an external source.

3.2.2 8.192 Mbit/s H-MVIP Mode

You can configure the FREEDM™-32P672 to interface with the H-MVIP digital telephony buses at 8.192 Mbps. For 8.192 Mbps H-MVIP operation, the FREEDM™-32P672 partitions the 32 physical links into eight logical groups of four links. In each logical group, only the first link, which must be located at physical links numbered 4m (m = 0,1,…,7), can be configured for 8.192 Mbps operation. The remaining three physical links in the logical group (numbered 4m+1, 4m+2 and 4m+3) are unused. All links configured for 8.192 Mbps H-MVIP operation share a common data clock. TMV8DC and RMV8DC are respectively the transmit and receive data clocks for this configuration.

Operation in this mode requires frame pulse signals. These signals are not generated on the board. Hence this mode can be operated only with clock and frame pulse signals supplied from an external source. Headers are provided for making the external connections.

3.2.3 Non-HMVIP Mode

The board supports 32 unchannelized T1/E1 links, with the following clock options:

- All 32 links driven by one reference clock (T1/E1)
- Links 0 to 15 driven by one reference clock (T1/E1), and links 16 to 31 driven of another reference clock (T1/E1).
- Links 0 to 2 also driven by another reference clock (52 MHz/T3)

Gapping of the clock is not done on the board. For channelized operations, an external source must obtain the gapped clocks.

3.2.4 Mixed Mode

The board supports mixing of up to 32 unchannelized T1/E1 and H-MVIP links. The total number of channels in each direction is limited to 32. The aggregate instantaneous clock rate, over all 32 possible links, is limited to 64 MHz.

3.3 Block Diagram

The detailed operations of the line interface, the PCI interface, and the BERT Unit are provided in the next section.

Figure 1: Block Diagram of the Development Kit

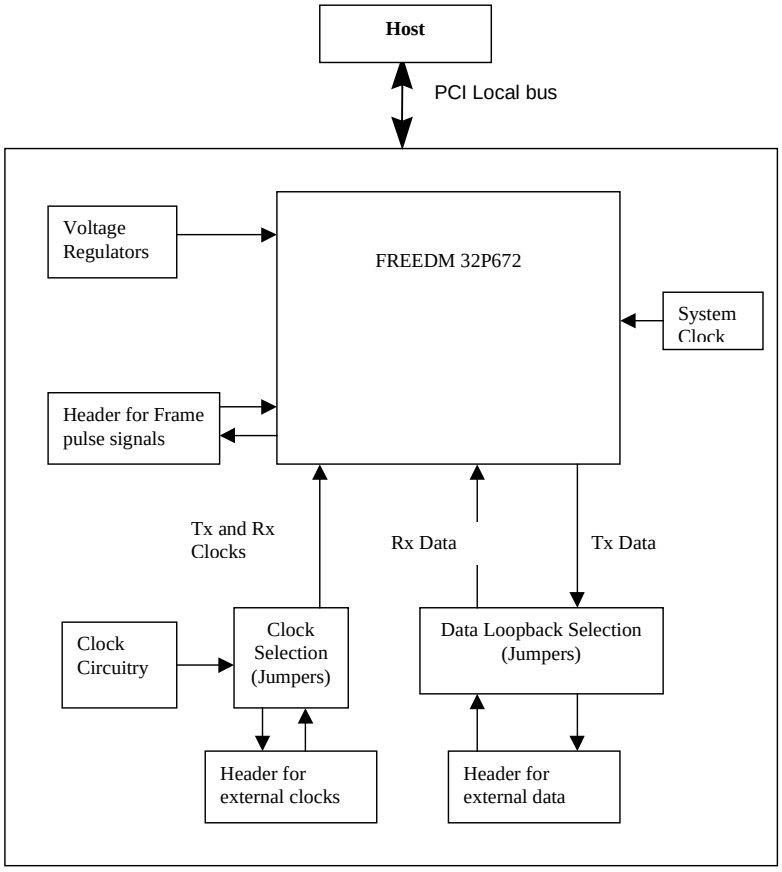


Figure 1 shows the basic components on the board. Voltage regulators provide the necessary 2.5 V and 3.3 V for the FREEDM™-32P672 chip. Clock selection

is done using shorting jumpers. All resistors and ceramic capacitors on board are 0603 in size. Surface mount devices are used wherever possible.

4 DETAILED DESCRIPTION

4.1 Detailed Interface Definitions

The development kit has three interfaces: the physical interface, the BERT interface, and the PCI interface. Each interface is defined in the following sections.

4.1.1 Physical Interface

The physical interface comprises the receive and transmit data links and the associated clocks. The physical interface is provided through headers. Wire to board connectors can be used to interface the external source with the development kit. The signals in this interface include RD[31..0], TD[31..0], RCLK[31..0], TCLK[31..0], RMVCK[3..0], TMVCK[3..0], RMV8DC, and TMV8DC. Traces from the headers are routed to the corresponding pins on the FREEDM™-32P672 chip.

The frame pulse signal and the frame pulse clock for the H-MVIP mode of operation has to be provided by an external source. For 2.048 Mbit/s, RFPB[3..0] and TFPB[3..0] are each provided by an external source by three-row, 12-position headers (P8 and P1, respectively) on the PCB. Header P9 provides the frame pulse signals, RFP8B and TFP8B. TMV8FPC and RMV8FPC are connected through header P4. Traces from these header pins are routed to the corresponding pins on the FREEDM™-32P672 chip (refer to the development kit Users Manual for information regarding header configuration). All the frame pulse signals can be pulled low when unused. For unchannelized operations in the HMVIP mode, the frame pulse signals must be pulled high. Table 1 shows the jumper settings for the provision of frame pulse signals.

Table 1: Configuration for the Provision of Frame Pulse Signals

Pins Shorted	Configuration Achieved
Pins b0 to b3 shorted respectively to pins a0 to a3 of header P8 and P1. Wire to board connector plugged into header P9	Provision of frame pulse signals for 8.192 Mbit/s mode.
Pins b0 to b1 shorted respectively to pins a0 to a1 of header P9. Wire to board connectors plugged into headers P8 and P1.	Provision of frame pulse signals for 4.096 Mbit/s mode.
Pins b0 to b3 shorted respectively to pins c0 to c3 of headers P8 and P1.	Unchannelized HMVIP operations

Pins b0 to b1 shorted respectively to pins c0 to c1 of header P9.	
Pins b0 to b3 shorted respectively to pins a0 to a3 of headers P8 and P1. Pins b0 to b1 shorted respectively to pins a0 to a1 of header P9.	No provision for frame pulse signals (non-HMVIP mode)

4.1.2 BERT Interface

The BERT signals are RBD, RBCLK, TBD, and TBCLK.These signals are connected to on board headers P15 (RBD and TBD) and P7 (RBCLK and TBCLK). The FREEDM™-32P672 chip can perform BERT emulation, by shorting the RD[2] and RBD pins, and also the TD[2] and TBD pins on header P15. At the same time, RBCLK should be connected to RCLK[2] and TBCLK should be connected to TCLK[2] on header P7. To accomplish BERT emulation, configure the FREEDM™-32P672 chip to transmit TBD on any one of the 31 links (not on TD[2]), and also to overwrite any one of the 31 links (not RD[2]) with RBD. Also, a test packet should be transmitted on link 2. RBCLK and TBCLK outputs are used as inputs to TCLK[2] and RCLK[2].

Table 2 shows the configuration for provision of BERT data and BERT clock.

Table 2: Configuration for Provision of BERT Data and BERT Clock

Pins Shorted on Headers J7 and J8	Configuration Achieved.
RBD shorted to RD[2] in P15 TBD shorted to TD[2] in P15	BERT Emulation.
RBCLK shorted to RCLK[2] in P7 TBCLK shorted to TCLK[2] in P7	

4.1.3 PCI Interface

The PCI Local Bus is a high performance 32-bit, 33/66-MHz bus with multiplexed address and data lines. The bus is used to connect the FREEDM™-32P672 development kit board to the host. The FREEDM™-32P672 chip provides a glueless interface to the PCI.

Table 3 shows the signals on the PCI connector with the pins on the FREEDM™-32P672 device to which they are routed.

Table 3: Regular PCI Pins and the Corresponding FREEDM™-32P672 Device Pins

PCI Pin	FREEDM™-32P672 Device Pin
AD[31..0]	AD[31..0]
C/BE[3..0]#	C/BEB[3..0]
PAR	PAR
FRAME#	FRAMEB
TRDY#	TRDYB
IRDY#	IRDYB
STOP#	STOPB
DEVSEL#	DEVSELB
IDSEL	IDSEL
PERR#	PERRB
SERR#	SERRB
REQ#	REQB
GNT#	GNTB
M66EN	M66EN
CLK	PCICLK
RST#	RSTB (through an AND gate)

Table 4 shows the optional PCI signals that are used on the development kit.

Table 4: Optional PCI Pins and the Corresponding FREEDM™-32P672 Device Pins

PCI Pin	Corresponding FREEDM™-32P672 Device Pin
LOCK#	LOCKB

INTA#	PCIINTB
TDI	TDI
TDO	TDO
TCK	TCK
TMS	TMS
TRST#	TRSTB (through an AND gate)

NOTE:
The pound sign (#) that follows the signal name indicates that the signal is active low. PRSNT1# is kept open, whereas PRSNT2 is grounded on the board. (Power requirement is < 15 W.)

Whenever PCI RST is asserted, the JTAG circuitry of the FREEDM™-32P672 chip must obtain a reset (through TRSTB). To obtain the JTAG reset (TRSTB) of the FREEDM™-32P672 chip, PCI TRST is ANDed with PCI RST. For more information about JTAG, see *JTAG Signals*.

To prevent the PCI RST signal from being connected to two loads, the signal is passed through an AND gate with the other input being pulled high. The output of this AND gate is connected to the FREEDM™-32P672 RSTB signal and is also used for generating the TRSTB signal.

The FREEDM™-32P672 chip has only one interrupt pin, PCIINTB. This chip is not a multifunction device, meaning that several independent functions are not integrated into a single device. Since there is only one interrupt pin, it is routed to INTA. The other three interrupt lines, INTB, INTC and INTD, remain unconnected.

4.2 Description of Functional Blocks

4.2.1 Clock Generation

The development kit supports several modes of operation, resulting in the use of oscillators of specific frequencies. Table 5 shows the use of oscillators on the board and its corresponding frequency.

Table 5: Frequencies of Oscillators for Board Use

Clock Frequency	Purpose of Use
1.544 MHz	Needed for T1 mode of operation (clock fed to TCLK and RCLK).
2.048 MHz	Needed for E1 mode of operation (clock fed to TCLK and RCLK).
4.096 MHz	Needed for 2.048 Mbps H-MVIP mode (clock fed to TMVCK and RMVCK).
44.736 MHz	Needed for DS-3 mode (clock fed only to TCLK[2..0] and RCLK[2..0]).
52.000 MHz	Needed for Unchannelised mode (clock fed only to TCLK[2..0] and RCLK[2..0]).
40 MHz	Needed in case PCICLKO is not used as SYSCLK.

The oscillator supplying a 16.384 MHz signal for the 8 Mbps HMVIP clock is not provided on the board. This mode of operation is possible only with frame pulse signals, which must be provided from an external source. The clock must also be provided by the external source.

The oscillators have a stability of 25 ppm and can drive 10 TTL loads. They are all 14-pin DIP-type oscillators and fit in standard sockets. All the sockets used on the board are manufactured by ARIES Electronics (part no. 1107741, reference **[9]**). Table 6 provides the oscillators that can be used in these sockets. Test points are provided for testing the line clocks and the external clocks.

Table 6: Sockets for the Various Oscillators

Socket Number	Oscillator Placed in the Socket
OSC 1	1.544/2.048 MHz (links 0 through 15)
OSC 2	4.096 MHz
OSC 3	52/44.736
OSC 4	1.544/2.048 MHz (links 16 through 31
OSC 5	40 MHz

The following different configurations are possible:

- All 32 links are driven by the same reference clock.
- Links 0 to 15 are driven by one reference clock, and links 16 to 31 are driven of a different reference clock.
- Links 0 to 2 are driven by another reference clock of high frequency, up to 52 MHz.

All the oscillators are socketed. The oscillator in socket OSC1 drives RCLK[15..0] and TCLK[15..0]. The oscillator in socket OSC4 drives RCLK[31..16] and TCLK[31..16], ensuring that just changing the oscillator can provide different frequencies. Table 7 shows you how to place the oscillators in sockets to achieve the above-mentioned configurations.

Table 7: Possible configurations of RCLK and TCLK

OSC1	OSC4	Configuration Achieved
1.544 MHz	1.544 MHz	All transmit and receive links at 1.544 MHz
2.048 MHz	2.048 MHz	All transmit and receive links at 2.048 MHz
1.544 MHz	2.048 MHz	TCLK[15..0] at 1.544 MHz, TCLK[31..16] at 2.048 MHz RCLK[15..0] at 1.544 MHz, RCLK[31..16] at 2.048 MHz
2.048 MHz	1.544 MHz	TCLK[15..0] at 2.048 MHz, TCLK[31..16] at 1.544 MHz RCLK[15..0] at 2.048 MHz, RCLK[31..16] at 1.544 MHz

4.2.2 Clock Distribution

In the development kit, clock frequencies as high as 52 MHz are used on the board. Clock generation circuits (oscillators) only generate the various clock frequencies. It is the task of the clock distribution network to distribute the clock to the various pins of the FREEDM™-32P672 chip. Clock drivers are used in preference to line drivers on the board to prevent excessive fan-out of the oscillators.

The TCLK and RCLK signals from the clock driver outputs are routed to the various pins by using traces of equal lengths. One to eight clock drivers are used since the links in most of the cases are grouped in multiples of eight. Each

output of the clock driver is connected to only one clock pin of the FREEDM™-32P672 chip.

Series termination is used for each clock line driven out of the clock driver.

RMVCK, TMVCK, RMV8DC, and TMV8DC are grounded when the development kit is configured to operate in unchannelized T1/E1 mode.

RCLK, TCLK, RMV8DC, and TMV8DC are grounded when the development kit is configured to operate in 2.048 Mbit/s H-MVIP mode.

RCLK, TCLK, RMVCK, and TMVCK are grounded when the development kit is configured to operate in 8.192 Mbit/s H-MVIP mode.

4.2.3 RMV8DC and TMV8DC Provision

RMV8DC and TMV8DC, as mentioned earlier, are respectively the receive and transmit clocks for 8.192 Mbps H-MVIP operation. The clocks are not generated on the board. Header P4 is provided to allow for external connections.

Table 8 shows the jumper settings over header P4 for two different configurations.

Table 8: Configuration for RMV8DC and TMV8DC Provision

Pins Shorted (on header P4)	Configuration Achieved
c0 shorted to d0, c1 shorted to d1	TMV8DC and RMV8DC are grounded
Wire to board connector plugged into pins c0, c1, d0, and d1	16.384 MHz provided to TMV8DC and RMV8DC

NOTE:
The RMV8DC and TMV8DC signals from the external source are made inputs to the FREEDM™-32P672 chip by plugging a wire to board connector onto pins c0, c1, d0, and d1 of header P4.

4.2.4 RCLK Distribution

RCLK is the receive data clock input to the FREEDM™-32P672 chip for unchannelised T1/E1 and DS-3/unchannelised (52 MHz) mode of operation. RCLK should be grounded when the development kit is not configured for either of these two modes of operation. On the board, RCLK and TCLK are obtained from the same oscillator to facilitate external loopback. However, a provision is

made for clocks from external sources, whereas RCLK and TCLK can be from different sources.

Clock signals applied to RCLK have the following frequencies, depending on the modes of operation.

- 1.544 MHz – for T1 configuration
- 2.048 MHz – for E1 configuration
- 44.736 MHz – for DS3 configuration
- 52 MHz – for unchannelized mode configuration

For unchannelized T1/E1 configuration, the distribution of the clock is such that an oscillator placed in socket OSC1 can drive each of the links (receive and transmit) from 0 through 15. Also, the oscillator placed in socket OSC4 can drive each of the remaining links (transmit and receive).

In the case of unchannelized 44.736/52 MHz configuration, all the receive links from 0 to 2 can be driven either at 44.736 MHz or at 52 MHz. The 44.736/52 MHz oscillator must be placed in socket OSC3. Links 3 to 31 are not used when all the links from 0 to 2 are driven at 52 MHz.

If links 0 to 2 are not all used for the 52/44.736 MHz operation, the oscillator in socket OSC1 can drive each of the receive (and transmit) links from 3 to 15. The oscillator placed in socket OSC4 can drive the receive (and transmit) links from 16 to 31.

However, in this configuration, the aggregate data rate over all links should not exceed 64 Mbit/s. The unused clock lines are grounded using jumpers.

Proper configuration of the above-mentioned modes can be done using jumpers. Figure 2 shows the clock distribution to RCLK. Two drivers are used for driving the 52 MHz/ DS3 clock for TCLK[2..0] and RCLK[2..0]. The driver can operate in the 40 MHz – to 80 MHz range, only if one bank of four outputs is being used.

Figure 2: Configuration for Distribution of RCLK

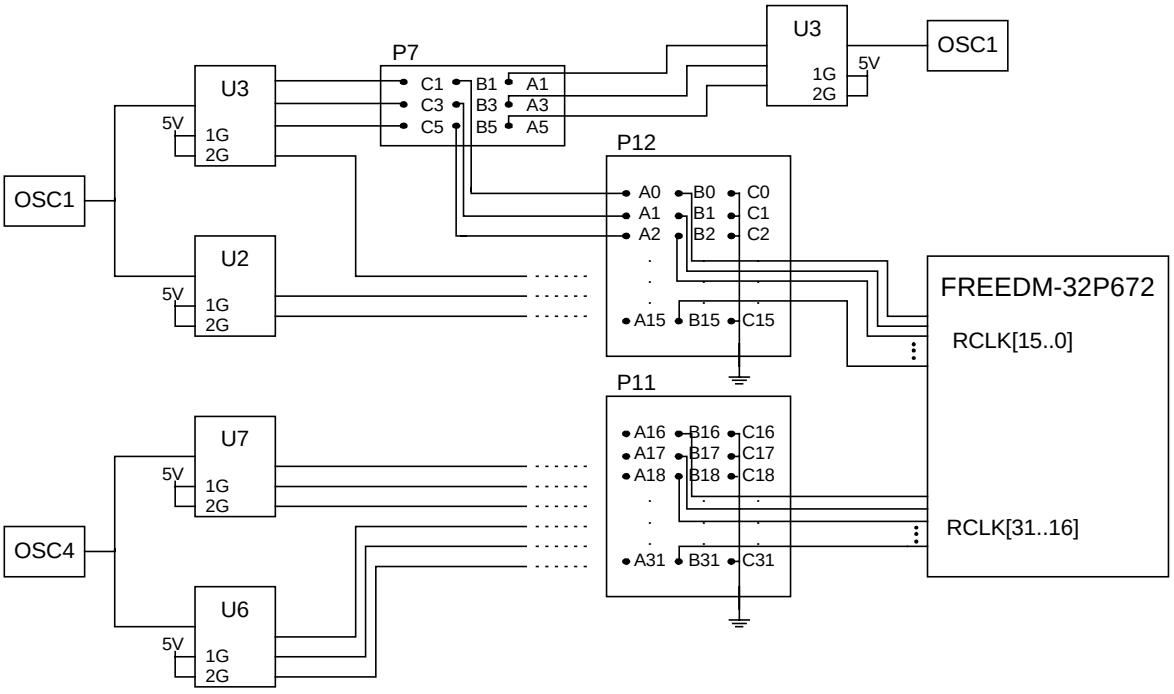


Table 9 shows how the different configurations for RCLK can be achieved.

Table 9: Configuration for RCLK Distribution

Jumper Settings at Header P7	Jumper Settings at Header P12, P11	Configuration Achieved
c1...c3 shorted to b1...b3	P12 b0...b15 shorted to a0...a15 P11 b16...b31 shorted to a16...a31	Unchannelized T1/E1
b1...b3 shorted to a1...a3	P12 b0...b2 shorted to a0…a2 P12 b3…b15 shorted to c3...c15 P11 b16…b31 shorted to c16…c31	Unchannelized DS3/52 MHz operation on links 1-3

	P12 b0…b15 shorted to c0...c15 P11 b16…b31 shorted to c16…c31	RCLK disabled for H-MVIP mode

Two pin-shorting jumpers are used to achieve the above-mentioned configurations. For mixed mode operation, only a few RCLK are used. The rest are grounded.

RCLK from an external source can be sourced to the FREEDM™-32P672 chip by plugging a wire to board connector into pins b1...b32, c1…c32 of headers P11 and P12. The grounded c1...c32 pins provide the necessary shielding to the external cable.

Sullins Electronics manufactures all the headers used on the board. Oupiin (part no. 2006A**[13]**) manufactures the jumpers used on the board.

All clock drivers used on the board are 1 to 8 clock drivers manufactured by Texas Instruments (part no. CDC341 **[10]**). To enable the outputs of the clock drivers, apply logic high (H) voltages to the enable pins of the driver IC. Table 10 shows the functionality of the clock driver.

Table 10: Function Table of 1-to-8 Clock Drivers

Function Table of 1 to 8 Clock Drivers				
Inputs			**Outputs**	
1G	**2G**	**A**	**1Y1-1Y4**	**2Y1-2Y4**
X	X	L	L	L
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	L	L	L
H	H	H	H	H

From Table 10, it is clear that pins 1G and 2G should both be at a high (H) logic level for driving the eight output lines. High logic level on pin 1G results in input A being driven onto output lines 1Y1-1Y4. Similarly, a high logic level on pin 2G results in input A being driven onto output lines 2Y1-2Y4.

Providing 5V to 1G and 2G pins permanently enables the outputs of all clock drivers on the board.

4.2.5 TCLK Distribution

TCLK is the transmit data clock input to the FREEDM™-32P672 chip, for unchannelized T1/E1 and DS-3/ 52 MHz modes of operation. TCLK should be grounded when the development kit is not configured for these two modes of operation. To facilitate external loopback, RCLK and TCLK are obtained from the same oscillator. However, a provision is made for clocks from external sources, whereas RCLK and TCLK can be from different sources.

Clock signals applied to TCLK have the following frequencies, depending on the mode of operation:

- 1.544 MHz – for T1 mode
- 2.048 MHz – for E1 mode
- 44.736 MHz – for DS3 mode
- 52 MHz – for unchannelized mode configuration

The distribution of the clock is such that each of the transmit links from 0 to 15 can be driven by an oscillator placed in socket OSC1. Each of the remaining transmit links can be driven by the oscillator placed in socket OSC4. TCLK[2..0] can also be driven at 44.736/52 MHz by the oscillator in socket OSC3.

Figure 3 shows the distribution of TCLK, which is similar to that of RCLK. Two drivers are used for driving 52 MHz/ DS3 clock for TCLK[2..0] and RCLK[2..0]. The driver can operate in the 40 MHz to 80 MHz range only if one bank of 4 outputs is being used.

Figure 3: Distribution of TCLK

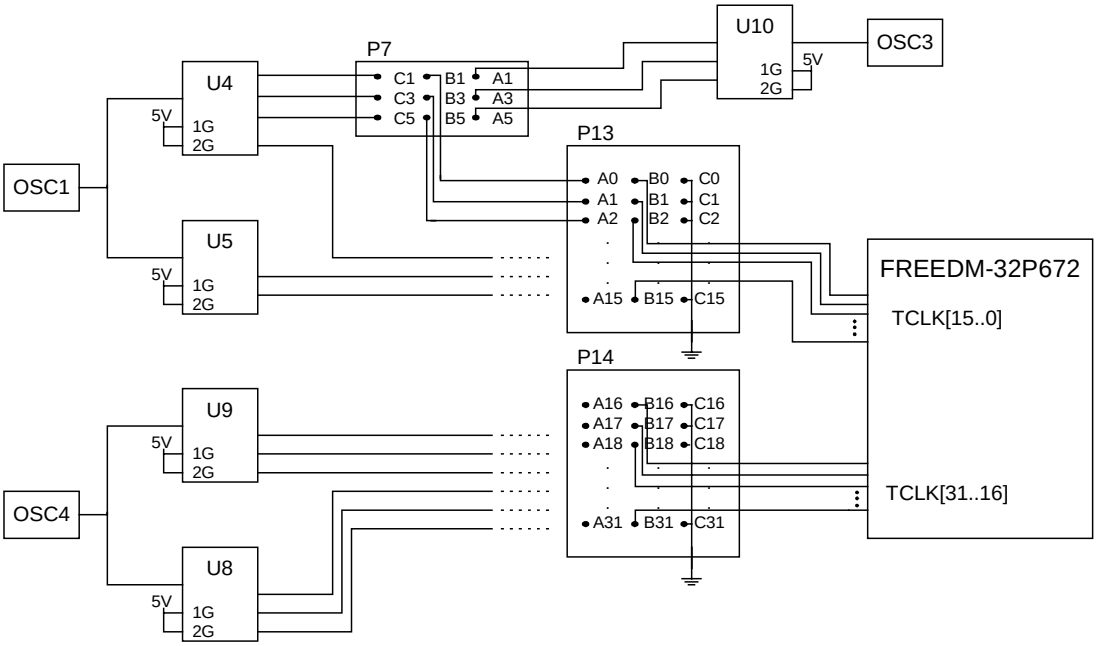


Table 11 shows how the different configurations for TCLK can be achieved

Table 11: Configuration for the Distribution of TCLK

Jumper Settings at Header P7	Jumper Settings at Header P13, P14	Configuration Achieved
a0…a2 shorted to b0…b2	P13, P14 b0...b31 shorted to a0…a31	Unchannelized T1/E1
b0…b2 shorted to c0…c2	P13 b0…b2 shorted to a0…a2 P13 b3...b15 shorted to c3...c15 P14 b16...b31 shorted to c16...c31	Unchannelized 44.736/52 MHz for links 1-3
	P13, P14 b0...b31 shorted to c0…c31	TCLK disabled for H-MVIP mode

Two pin-shorting jumpers are used to achieve the above-mentioned configurations. For mixed mode operation, only a few TCLK are used. The rest are grounded.

TCLK from an external source can be given to the FREEDM™-32P672 chip by plugging a wire to board connector onto pins b0...b31, c0…c31 of headers P13 and P14. The grounded c0…c31 pins provide the shielding for the external cable.

4.2.6 RMVCK and TMVCK Distribution

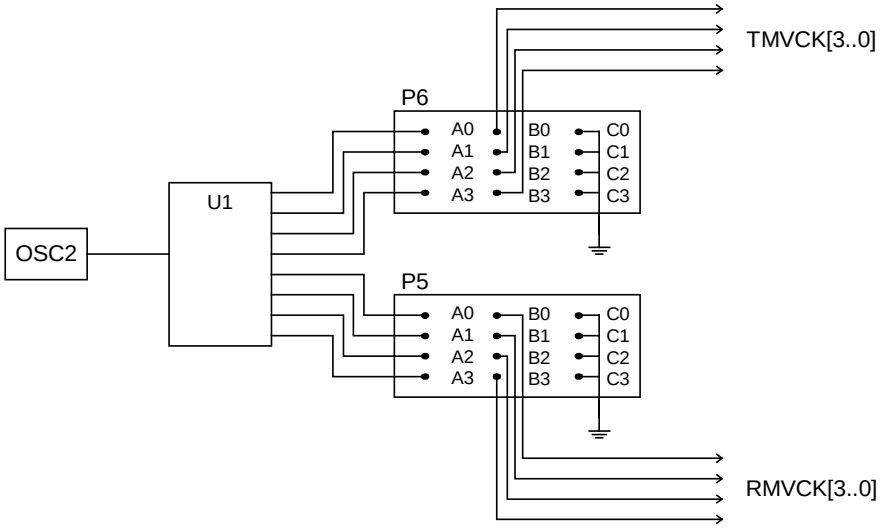
When the Development Kit is not configured for 2.048 Mbit/s H-MVIP operation, RMVCK[3..0] and TMVCK[3..0] are pulled down to ground. Figure 4 shows the distribution of RMVCK and TMVCK.

Table 12 shows the jumper settings over headers P5 and P6 for two different configurations.

Table 12: Configuration for RMVCK and TMVCK

Pins Shorted on Headers P5, P6	Configuration Achieved
b0…b3 shorted to a0...a3	TMVCK and RMVCK frequency = 4.096 MHz
b0...b3 shorted to c0...c3	TMVCK and RMVCK disabled for non-MVIP mode

Figure 4: RMVCK and TMVCK Distribution



TMVCK and RMVCK from an external source can be given to the FREEDM™-32P672 chip by plugging a wire to board connector into pins b0...b3, c0…c3 of headers P5 and P6. The grounded c0...c3 pins provide the shielding for the external cable.

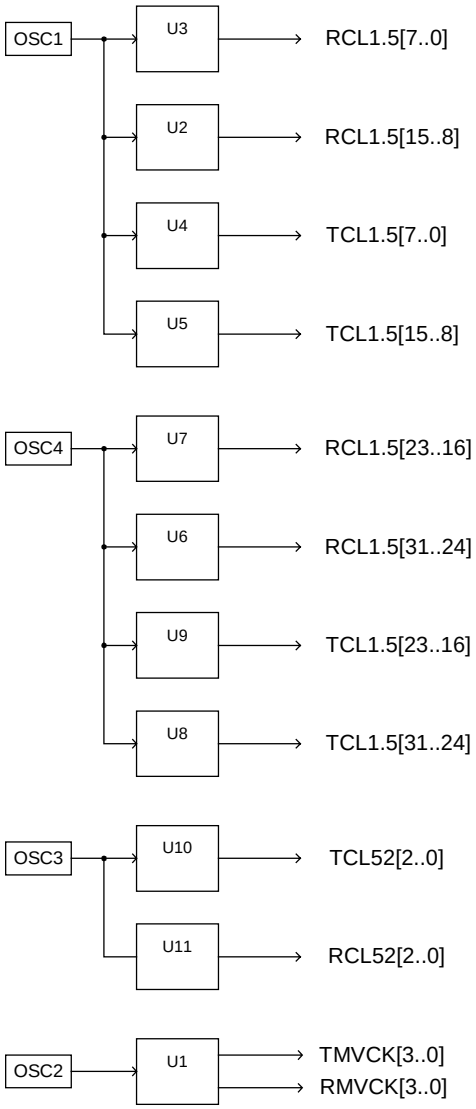
4.2.7 Clock Drivers

The total number of clock lines (not including those for H-MVIP mode) to be driven by the clock drivers is 70. This includes:

- 32 lines driven by oscillator in socket OSC1 (RCLK[15..0] and TCLK[15..0]).
- 32 lines driven by oscillator in socket OSC4 (RCLK[31..16] and TCLK[31..16]).
- 6 lines driven at 44.736 MHz/52 MHz (RCLK[2..0] and TCLK[2..0]).

Figure 5 shows the connections between the clock oscillators and the clock drivers. In total, 11 clock driver ICs (each one is a 1 to 8 clock driver) are used, including one for RMVCK and TMVCK.

Figure 5: Clock Drivers Used for Distribution of Line Clocks



NOTE:
U1 to U11 are 1 to 8 clock drivers (part no. CDC341 manufactured by Texas Instruments).

4.2.8 Provision for Loopback of Data

There is a provision on the board for performing either loopback of TD[31..0] or connecting TD[31..0] to an external system. RD[31..0] can be connected to either TD[31..0] (in case of loopback) or an external system.

Figure 6 shows the configuration of headers for performing loopback on a per link basis. P15 and P10 are dual row headers with 32 positions. Table 13 shows the jumper settings for loopback configuration.

Figure 6: Configuration for the Loopback of Data

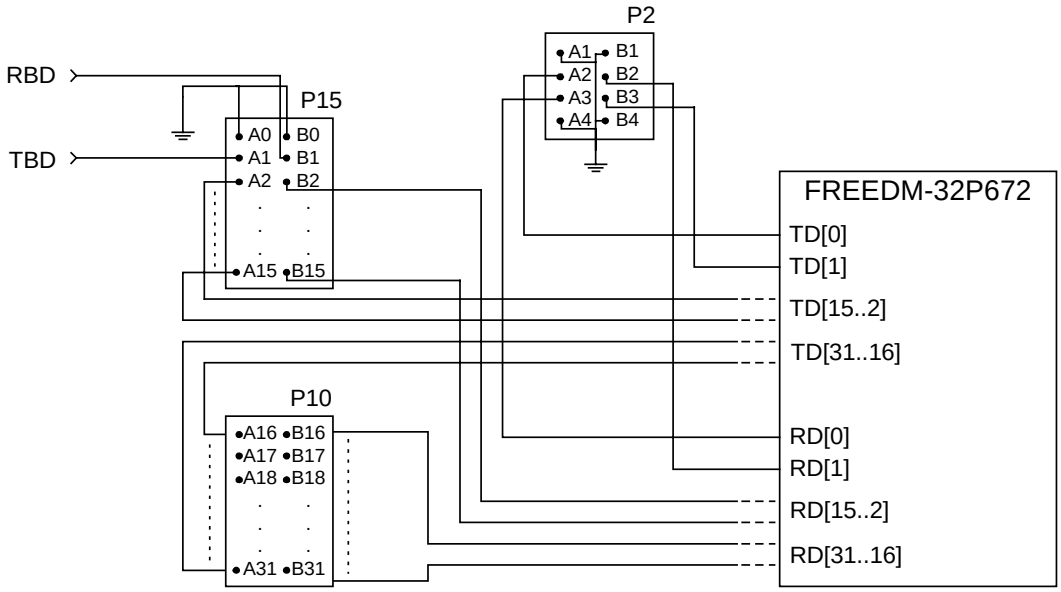


Table 13: Configuration for the Loopback of Data

Jumper Setting at Headers P15, P10	Jumper Setting at Header P2	Configuration Achieved
P15 a2…a15 shorted to b2...b15 P10 a16…a31 shorted to b16…b31	a2 shorted to b2, a3 shorted to b3	Simultaneous cross-connect on links 0 and 1, loopback in others.
P15 a2…a15 shorted to b2...b15 P10 a16…a31 shorted to b16…b31	a2 shorted to a3, b2 shorted to b3	Simultaneous loopback on links 0 to 31.

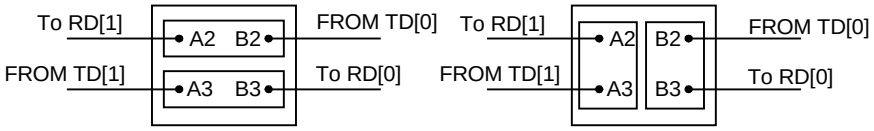
NOTE:
Loopback can be performed on a per link basis by using two pin-shorting jumpers over headers P15 and P10.

Pins a2...a15 of header P15, a16...a31 of header P10, and pins b3 and a2 of header P2 are used as the physical interface with the external source for TD. b2...b15 of header P15, b16...b31 of header P10, and pins b2 and a3 of header P2 are used as the physical interface with the external source for RD. Wire to

board connectors are used to interface the external source with FREEDM™-32P672 inputs TD and RD.

The following configurations can be performed for the loopback of data from TD[31..0] to RD[31..0].

Figure 7: Simultaneous Cross-Connect and Loopback of 52 Mbit/s Data Stream (P2).



4.2.9 Simultaneous Cross-Connect and Loopback of Two 52 Mbit/s Data Streams

You can accomplish a simultaneous cross-connect by placing shorting jumpers over (a2, b2) and (a3, b3), as shown in Figure 7. In this configuration, RD[0] gets data from TD[1], whereas RD[1] gets data from TD[0].

You can perform a simultaneous loopback by placing shorting jumpers over (a2, a3) and (b2, b3), as shown in Figure 7. In this configuration, RD[0] gets data from TD[0], whereas RD[1] gets data from TD[1].

4.2.10 Loopback of Unchannelised T1/E1 Data Streams

In Figure 6, the loopback of unchannelized T1/E1 data streams on links 2 to 31 can be performed by using shorting jumpers on headers P15 and P10. The remaining two links can also be used for unchannelized T1/E1 operation. In that case, loopback is achieved by using shorting jumpers over header P2.

4.2.11 Miscellaneous Signals

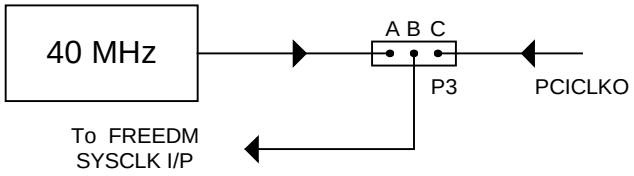
The FREEDM™-32P672 chip has several miscellaneous signals on pins such as SYSCLK, RSTB, M66EN, PMCTEST, TCK, TMS, TDI, TDO, and TRSTB.

4.2.12 SYSCLK Provision

With a frequency of 33 MHz/ 40MHz. SYSCLK can be provided in two different ways to the FREEDM™-32P672 chip. One is to use the PCICLKO clock output of the FREEDM™-32P672 device by feeding it back to the SYSCLK input. However, this will provide only a 33 MHz SYSCLK. When the PCI bus is operating at 66 MHz, to obtain a 40 MHz SYSCLK a 40 MHz oscillator needs to

be used. Figure 8 shows a jumper that enables configuration to any of the two frequencies. A single row 3 pin header (P3) is used for SYSCLK provision. The SYSCLK input can be fed the oscillator-generated clock by shorting pins a1 and b1 using a two-pin shorting jumper. PCICLKO clock output can be fed to the SYSCLK input by shorting pins b1 and c1 of header P3.

Figure 8: SYSCLK Provision



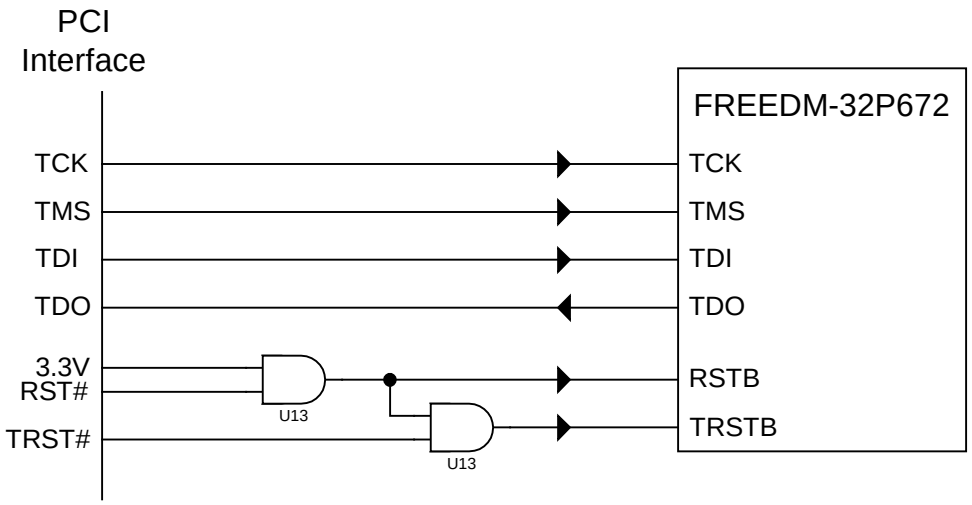
4.2.13 M66EN

The M66EN signal reflects the speed of operation of the PCI bus. M66EN is set high (by the system motherboard) for 66 MHz, and low for 33 MHz operation on the PCI bus. A trace from the M66EN pin of the PCI connector is routed to the M66EN pin of the FREEDM™-32P672 chip.

4.2.14 JTAG Signals

TCK, TMS, TDI, TDO, and TRSTB pins of the FREEDM™-32P672 carry the JTAG signals. Traces from the JTAG pins TCK, TMS, TDI, and TDO, of the PCI connector, are directly routed to the corresponding pins of the FREEDM™-32P672 chip. However, TRSTB is asserted low whenever RST# (of PCI connector) is asserted low. Figure 9 shows how this is done by using AND gates on the board. The 74LCX08 from Fairchild Semiconductor is used for this purpose. Its inputs are 5V tolerant.

Figure 9: JTAG Signals



4.2.15 Production Test Interface Signals

To enable normal operation of the FREEDM™-32P672 chip, PMCTEST is grounded.

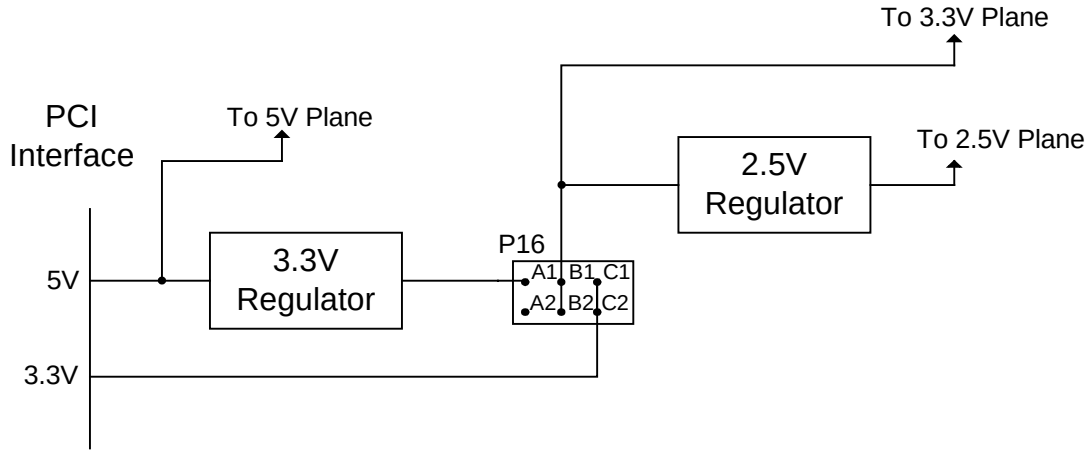
4.2.16 Power

The FREEDM™-32P672 development kit board consists of multiple planes. The ground plane has ground potential provided by the PCI connector. The power plane has islands of 5 V, 3.3 V, and 2.5 V. The PCI connector provides 5 V for the 5 V island. The 3.3 V island may be powered either by the 3.3 V supply from the PCI connector (as in the case of the 3.3 V signalling environment) or by a 3.3 V regulated supply on the PCB (as in the case of the 5 V signalling environment). The 2.5 V island on the power plane is connected to the 2.5V potential of the 2.5 Volt regulator.

NOTE:
The PCI connector is the only source of power for the development toolkit.

Figure 10 shows the provision of voltages to the power plane. In a 3.3 V signalling environment, header pins b1 and b2 should be shorted respectively to pins c1 and c2, by means of jumpers. In a 5 V signalling environment, header pins a1 and a2 should be shorted respectively to pins b1 and b2, by means of jumpers.

Figure 10: Provision of 2.5V, 3.3V and 5V to the Power Plane



4.2.17 Power Calculations

The maximum power allowed for the PCI board is 25 watts and represents the total power drawn from all of the power rails provided at the connector. In the worst case, all 25 watts could be drawn from either the +5V or +3.3V rail. The 5V rail powers the oscillators and the clock drivers. In the 3.3 V signaling environment, the 3.3 V rail powers the 2.5 V regulator, the AND gate, and the FREEDM™-32P672 chip. In a 5 V signaling environment, the 3.3 V rail is obtained from the 5 V rail itself. Table 14 and Table 15 show the tabulations for the maximum power consumption values for all devices on the board.

Table 14: Power Calculations (5 V Signaling Environment)

Device	**Consumed current (A)** **I = (no. of devices) x (I_{device})**	**Consumed power (W)** **P_5 = 5.5 x I**
1.544 MHz oscillator (2 nos.)	2 x 0.025	0.275
2.048 MHz oscillator (2 nos.)	2 x 0.025	0.275
4.096 MHz oscillator (1 no.)	1 x 0.025	0.1375
8.192 MHz oscillator (1 no.)	1 x 0.025	0.1375
52/44.736 MHz	1 x 0.060	0.33

oscillator (1 no.)		
40 MHz oscillator (1 no.)	1 x 0.040	0.22
CDC341 (11 nos.)	11 x 0.033	1.9965
LT1528CQ	x 1.0 (Current drawn by 3.3V and 2.5V power rail of FREEDM™-32P672)	5.5
Maximum power required		8.8715

Table 15: Power Calculations (3.3 V Signaling Environment)

Device	**Consumed current (A)** **I = (no. of devices) x (I_{device})**	**Consumed power (W)** **$P_{3.3}$ = 3.6 x I** **$P_{3.3}$ = 5.5 x I (for devices with 5 V supply)**
1.544 MHz oscillator (2 nos.)	2 x 0.025	0.275
2.048 MHz oscillator (2 nos.)	2 x 0.025	0.275
4.096 MHz oscillator (1 no.)	1 x 0.025	0.1375
8.192 MHz oscillator (1 no.)	1 x 0.025	0.1375
52/44.736 MHz oscillator (1 no.)	1 x 0.060	0.33
40 MHz oscillator (1 no.)	1 x 0.040	0.22
CDC341 (11 nos)	11 x 0.033	1.9965
AND gate	1 x 0.100	0.36
MIC39150 (1 no.)	1 x 0.700 (2.5 V power rail of FREEDM™-32P672)	2.52

FREEDM™-32P672 (1 no.)	1 x 0.200 (3.3V power rail of FREEDM™-32P672)	0.72
Maximum power required		6.9715

NOTE:
The current taken by the FREEDM™-32P672 chip from the 2.5 V rail is assumed to be 700 mA (maximum). The current taken by the FREEDM™-32P672 chip from the 3.3 V rail is assumed to be 200 mA (maximum).

4.2.18 Voltage Regulation

The FREEDM™-32P672 chip needs 3.3 V I/O pad power and 2.5 V core logic power. Voltage regulators are required for providing 2.5 V and 3.3 V to the FREEDM™-32P672 device. The various criteria for choosing a voltage regulator are:

- Stable output voltage with a good load regulation.
- Low dropout.
- Good thermal characteristics.
- Board space occupied by the regulators and their heat sinks.

The regulated 3.3 V (obtained from 5 V) would be used when the universal card is plugged into a 5V signaling environment. The 3.3 V from the PCI connector is used when the PCI card is plugged into a 3.3V signaling environment.

Power requirement on the 3.3 V rail of the FREEDM™-32P672 chip is about 227 mW. The corresponding current comes out to be around 68 mA. However, the 2.5 V regulator also sources current from the 3.3 V rail. This current is about 320 mA. Hence the current rating of the 3.3 V regulator should be the sum of these two currents. LT1528CQ, a 3.3 V regulator from Linear Technology **[6]** is used on the add-on card. Heat sink area calculations for this regulator are shown below.

Calculation of maximum power dissipation in the 3.3 V regulator:

For proper design, the worst case values for all the parameters are used. Worst case V_{in} is high supply; in this case, 5 V + 10% or 5.5 V. Worst case V_{out} for thermal conditions is minimum, or 3.3 V – 2%, or 3.234 V. Iout is taken at its

highest steady state value, that is, 1 A. The ground current value of 10 mA comes from the device's datasheet (reference), from the I_{gnd} vs. I_{out} plot.

P_d (max) = [(V_{in} – V_{out}) x (I_{out})] + [(V_{in}) x (I_{gnd})]
= [(5.5 – 3.234)x(1)] + [(5.5) x (.01)]
= 2.266 + 0.055
= 2.321 W

Calculation of Junction to Ambient Thermal Resistance (for 3.3 V):

$¢_{ja}$ = [(T_j – T_a) / P_d] – [$¢_{jc}$ + $¢_{cs}$]
= [(125 – 70) / 2.321]
$¢_{ja}$ = 23.7 $^oC/W$

From the device datasheets provided by Linear Technology (reference), 2500 square mm of copper area is required on both sides of the board for the 3.3 V regulator's heat sink.

The voltage regulator used to provide 2.5 V to the VDD2V5 pin of the FREEDM™-32P672 chip should have a current rating of at least 320 mA. MIC39150-2.5BU [5**],** manufactured by MICREL, comes in a TO-263 package and matches our requirements.

Proper voltage regulator design involves calculation of the thermal resistance, from which heat sink area can be computed. This section shows the calculations for MIC39150-2.5BU (used in the development kit).

Calculation of maximum power dissipation in the 2.5 V regulator:

For proper design, the worst case values for all the parameters are used. Worst case V_{in} is high supply; in this case, 3.3 V + 10% or 3.63 V. Worst case V_{out} for thermal conditions is minimum, or 2.5 V – 2%, or 2.45V. Iout is taken at its highest steady state value, that is,. 700 mA. The ground current value of 7.5 mA comes from the device's datasheet **[5]**, from the I_{gnd} vs I_{out} plot.

P_d (max) = [(V_{in} – V_{out}) x (I_{out})] + [(V_{in}) x (I_{gnd})]
= [(3.63 – 2.45)x(0.7)] + [(3.630) x (.0075)]
= 0.826 + 0.027225
= 0.853225 W

Calculation of Heat Sink Thermal Resistance (for 2.5 V regulator):

$¢_{sa}$ = [(T_j – T_a) / P_d] – [$¢_{jc}$ + $¢_{cs}$]
= [(125 – 70) /0.853225] – [2 + 2]
$¢_{sa}$ = 64.46 – 4
= 60.46 $^oC/W$

From the heat sink design curves provided by Micrel **[7]**, at least 500 square mm of copper area is required on the board for the 2.5 V regulator's heat sink.

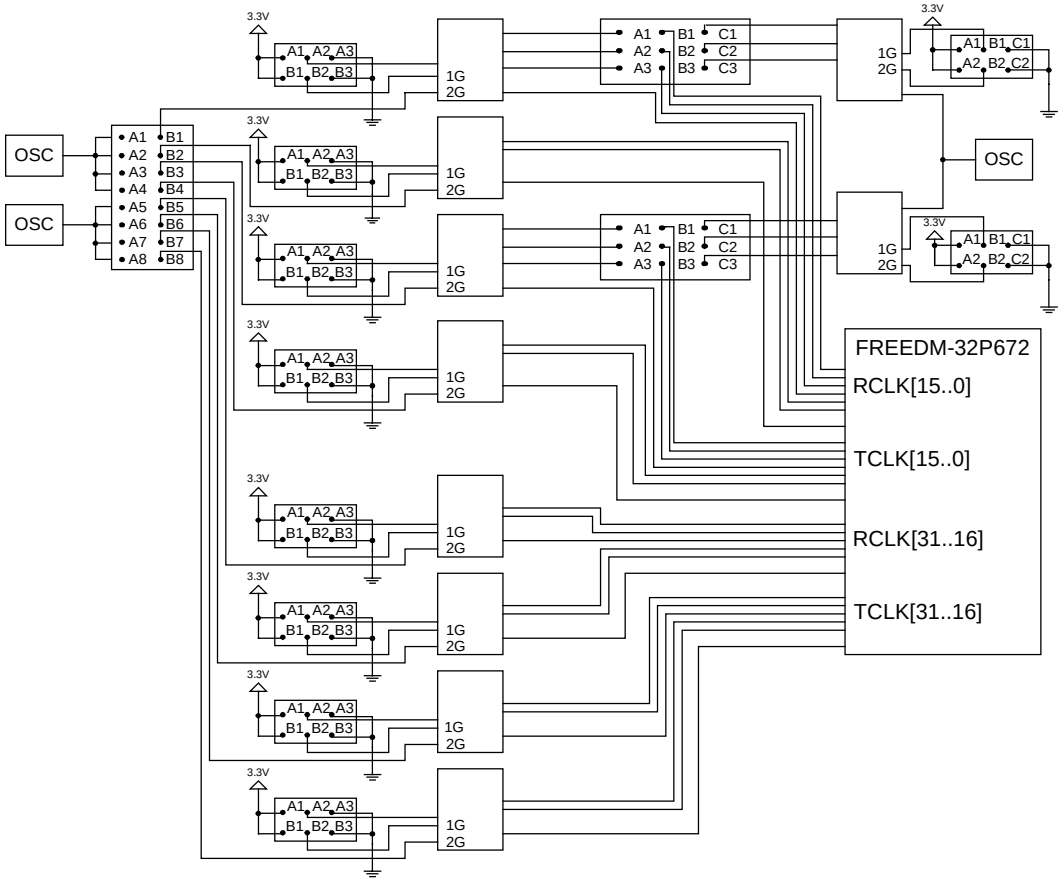
4.3 Design Alternatives

4.3.1 Using Enable Pins of Clock Drivers

The clock inputs to the FREEDM™-32P672 chip should not be kept hanging. If they are not used, they should be pulled down to ground. In the alternative design of the development kit, the enable pins of clock drivers are used to disable (pulled down to ground) the output of the clock drivers.

The alternative design occupies lesser board space, but reduces the flexibility of configuring the modes of operation. This is because the output lines of the clock drivers can be disabled or enabled, only in groups of four **[10]**. Figure 11 shows the alternative design.

Figure 11: Alternative Design for clock distribution in the Development Kit



As shown in this figure, headers for the external interface are not placed after the clock drivers. A dual row header with eight positions is used for the external interface. A wire to board connector can be plugged into pins b1 to b8, to provide the external clock to RCLK and TCLK inputs of the FREEDM™-32P672 chip. Dual row headers with three positions are associated with each clock driver. Pins 1G and 2G of each clock driver in the alternative design can be independently pulled high or low.

The drawback of the alternative design is the reduced flexibility in configuring for the different modes of operation of the development kit. This drawback occurs because the clock inputs to the FREEDM™-32P672 chip (that is, the outputs of the clock drivers) can be configured only in groups of four.

For example, it is not possible to drive RCLK[1..0] at one frequency and have no drive on RCLK[3..2] at all.

Table 16 lists the configurations that can be achieved by means of shorting jumpers.

Table 16: Jumper Configuration in the Alternative Design

Jumper Settings on the Headers (Figure 11)	Configuration Achieved
Wire to board connector plugged into pins b1 to b8 of header J1. Pins a1 to a3 shorted respectively to pins b1 to b3 on headers J10 and J11. Pins a1 and b1 shorted respectively to pins a2 and b2 on headers J2 through J9.	All RCLK and TCLK from an external source.
Pins a1 to a8 shorted respectively to pins b1 to b8 on header J1. Pins a1 to a3 shorted to pins b1 to b3 on headers J10 and J11. Pins a1 and b1 shorted respectively to pins a2 and b2 on headers J2 through J9.	RCLK[15..0] and TCLK[15..0] driven by the oscillator in socket S1. RCLK[31..16] and TCLK[31..16] driven by the oscillator in socket S2.
Pins a1 to a8 shorted respectively to pins b1 to b8 on header J1. Pins c1 to c3 shorted to pins b1 to b3 on	RCLK[15..3] and TCLK[15..3] driven by the oscillator in socket S1. RCLK[2..0] and TCLK[2..0] driven by the

headers J10 and J11. Pins a1 and b1 shorted respectively to pins a2 and b2 on headers J2 through J9.	oscillator in socket S0 (52/44.736 MHz). RCLK[31..16] and TCLK[31..16] driven by the oscillator in socket S2.

NOTE:
Except for those configurations mentioned in Table 16, several different configurations are possible. One such configuration is to have no drive on RCLK[31..16] and TCLK[31..16]. This is achieved by having pins a1 and b1 shorted to pins a2 and b2 respectively, on headers J6 to J9 (see Figure 11).

5 SOFTWARE INTERFACES

The software interfaces are described in reference [3].

6 MECHANICAL

6.1 Board size/outline

The Universal PCI short card will be used for the FREEDM™-32P672 Development Toolkit Design. Its dimensions (form factor) are 6.875 inches x 4.2 inches as per PCI 2.1. The PCI card has an end bracket.

All the oscillators on board are socketed. The first five boards also have the FREEDM™-32P672 chip socketed. Boards thereafter will have the FREEDM™-32P672 chip directly soldered to the board. The PMC-Sierra logo is present on all the boards.

6.2 Estimate of real estate

The approximate area occupied by each component on the board is as follows:

- FREEDM™-32P672 : 31 mm x 31 mm
- CDC341 (11 nos.) : 10.3 mm x 10.3 mm
- MIC39150 (1 no.) : 640 square mm approx[1]
- LT1528CQ (1 no.) : 5140 square mm approx[1]
- Socket 1107741(6 no : 17.78 mm x 10.16 mm
- Headers (total space) : 375 x 2.54 mm x 2.54 mm

[1] including copper area

The above-mentioned area sums up to approximately 11415 square mm. The area occupied by other passive components (resistors, capacitors and LEDs) has not been included in the real estate calculation, as they will be placed on the rear side of the board. The area of a universal PCI short card is 18628.995 square mm (i.e. 6.875 x 4.2 x $(2.54)^2$).

6.3 Cooling requirements

The ambient temperature should not exceed the maximum value of 70 degrees C. The heat sink has been designed considering a maximum ambient temperature value of 70 degrees Celsius.

7 LIMITATIONS

There is no on-board provision for the gapping of clock and frame pulse generation.

The PCI connector is the sole supplier of power to the development kit.

The development kit as a stand alone board does not support the channelized mode of operation.

It is assumed that all the clock signals from the external system are buffered. These clocks are not buffered by the drivers on the PCB.

8 REQUIREMENTS TRACEABILITY

Table 17: Traceability Matrix

Functionality Supported [4]	Section Number
H1	3.3, 6
H2	0
H3	4.2.1
H4	4.1.1, 4.2.8
H5	4.1.1
H6	4.2.18
H7	6.1
H8	6.1
H9	4.2.16, 4.2.1
H10	4.2.8, 4.2.9
H11	3.3
H12	6.1
H13	6.1

9 BILL OF MATERIALS

Table 18: Bill of Materials

Description	Part Number	Manufacturer	Quantity
2.5 V, 1A Low Dropout Voltage regulator (TO-263)	MIC39150-2.5BU	Micrel	1
3.3 V, 3A Low Dropout Voltage regulator	LT1528CQ	Linear Technology	1
Oscillator 1.544 MHz	S13R8R	Connor Winfield	2
Oscillator 2.048 MHz	S13R8R	Connor Winfield	2
Oscillator 4.096 MHz	S13R8R	Connor Winfield	1
Oscillator 52 MHz	S13R8R	Connor Winfield	1
Oscillator 44.736 MHz	S13R8R	Connor Winfield	1
Oscillator 40 MHz	S13R8R	Connor Winfield	1
Socket for Oscillator	1107741	Aries Electronics	5
FREEDM™-32P672 Device	PM7380	PMC-Sierra	1
1 to 8 clock driver	CDC341	Texas Instruments	11
AND gate	74LCX08	Fairchild Semiconductor	1
Dual Row Header (32 positions)	PZC32DAAN	Sullins Electronics	6
Single Row Header (32 positions)	PZC32SAAN	Sullins Electronics	4
Single position shunt	2006A	Oupiin	150

10 SCHEMATIC DIAGRAMS

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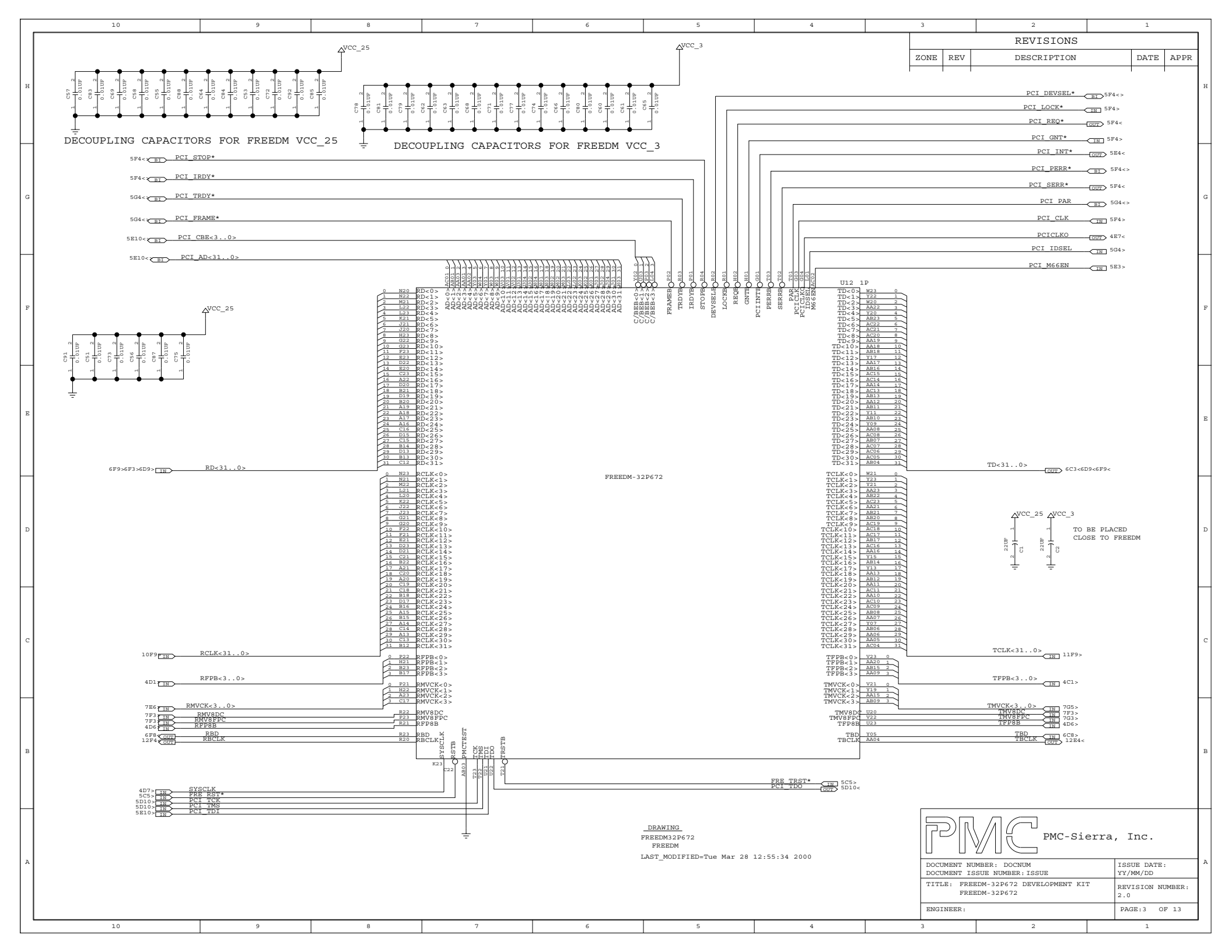
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DECOUPLING CAPACITORS FOR FREEDM VCC_3
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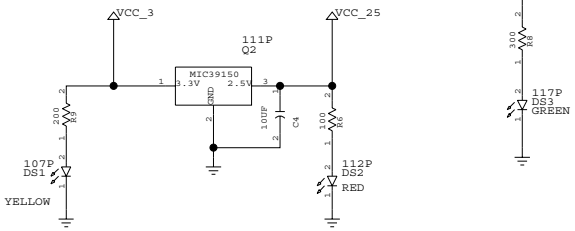
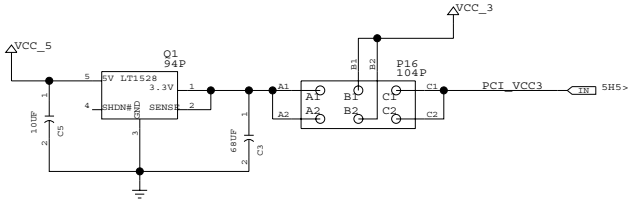
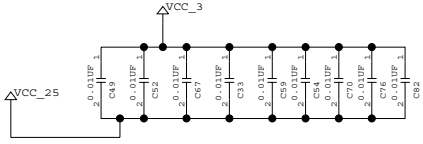


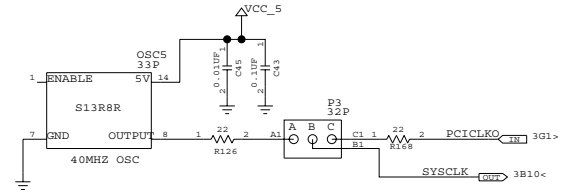
2.5 VOLTAGE REGULATOR



3.3V VOLTAGE REGULATOR



CAPACITORS FOR PLANE SPLITS



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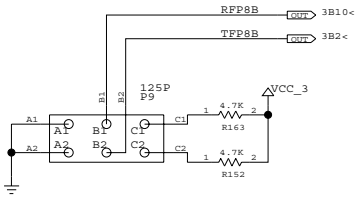
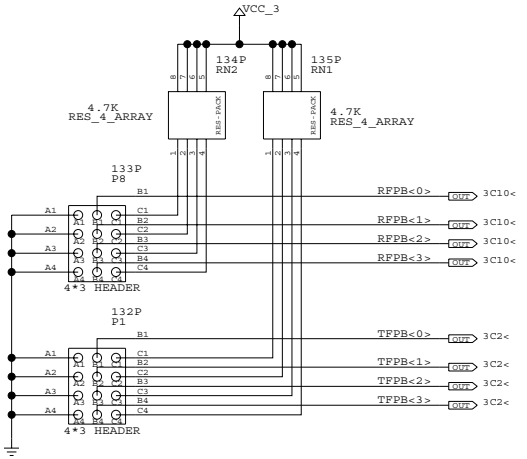


FRAME PULSE SIGNALS 2.048 MBPS HMVIP MODE



FRAME PULSE SIGNALS FOR 2.048HMVIP MODE

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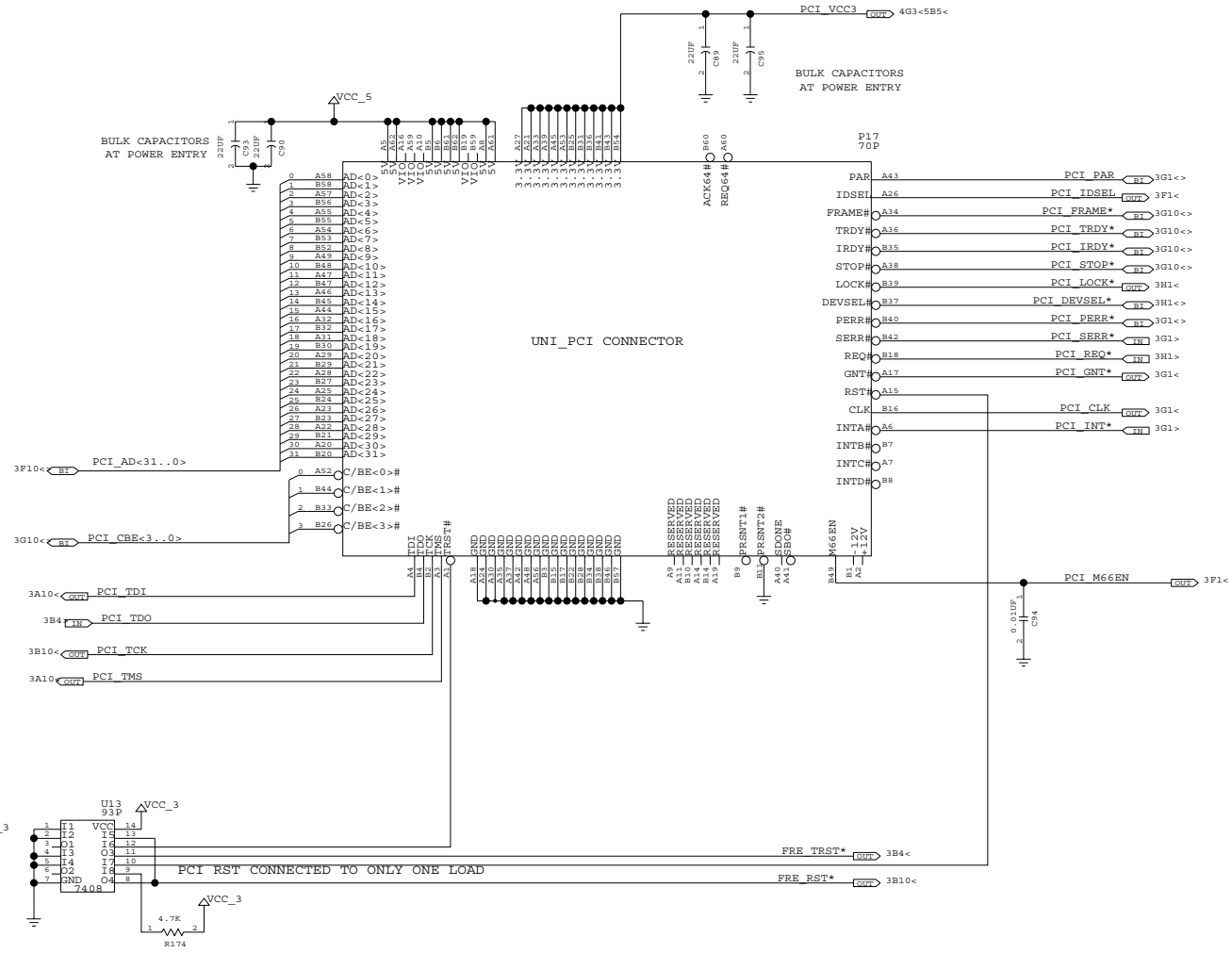

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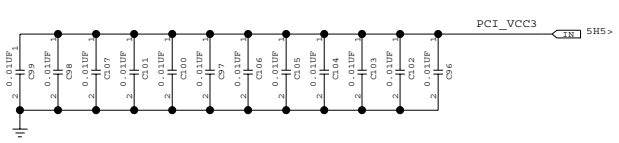

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LAST_MODIFIED=Tue Mar 28 12:55:38 2000

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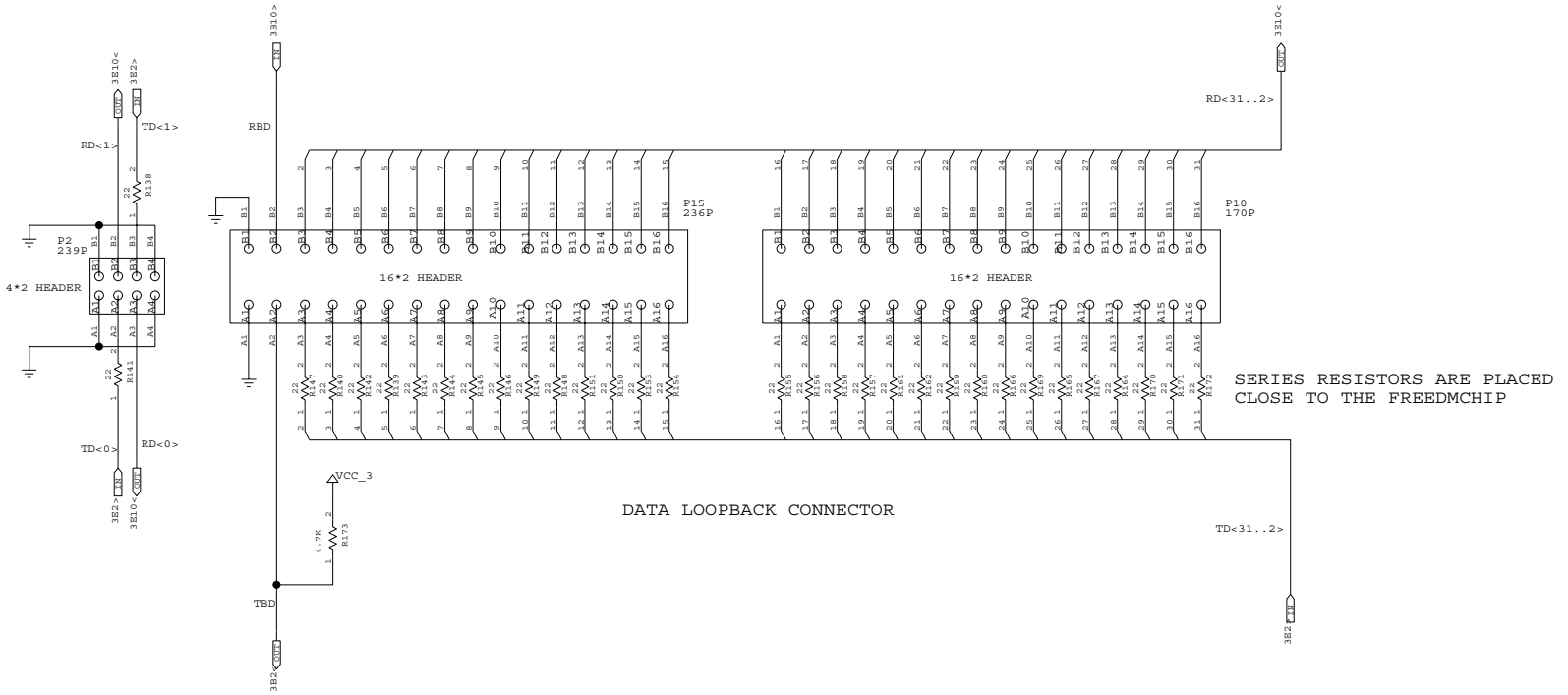
DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT PCI CONNECTOR	REVISION NUMBER: 2.0
ENGINEER:	PAGE:5 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

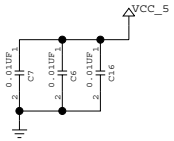
DATA_LOOPBACK
LOOPBACK

LAST_MODIFIED=Tue Mar 28 12:55:40 2000

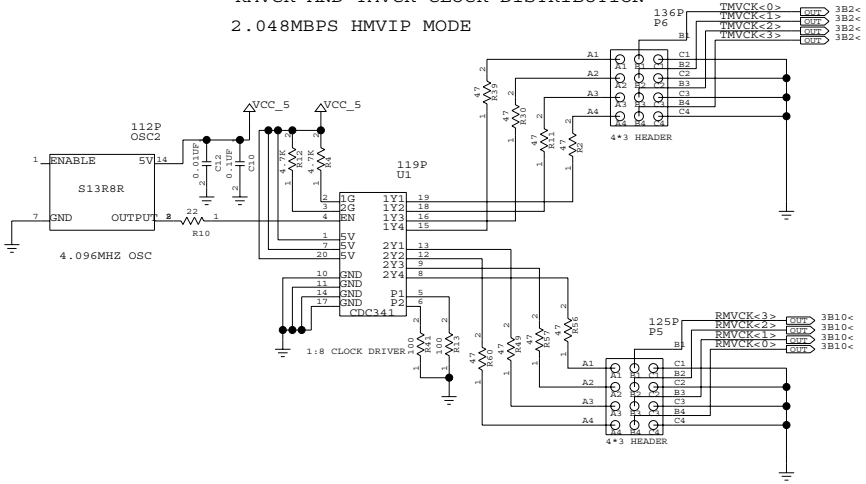
PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT DATA LOOPBACK	REVISION NUMBER: 2.0
ENGINEER:	PAGE:6 OF 13

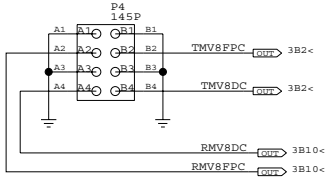
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

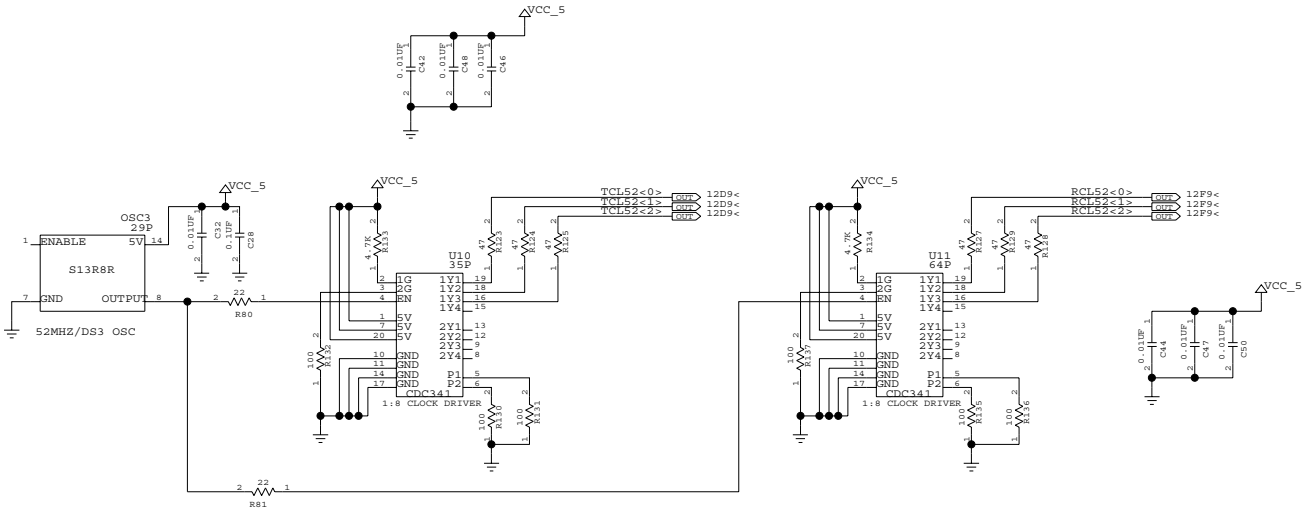


RMVCK AND TMVCK CLOCK DISTRIBUTION
2.048MBPS HMVIP MODE



HEADER FOR 8.192MBPS HMVIP CLOCKS





DISTRIBUTION OF TCLK<2..0> AND RCLK<2..0>
52 MHZ OR DS3

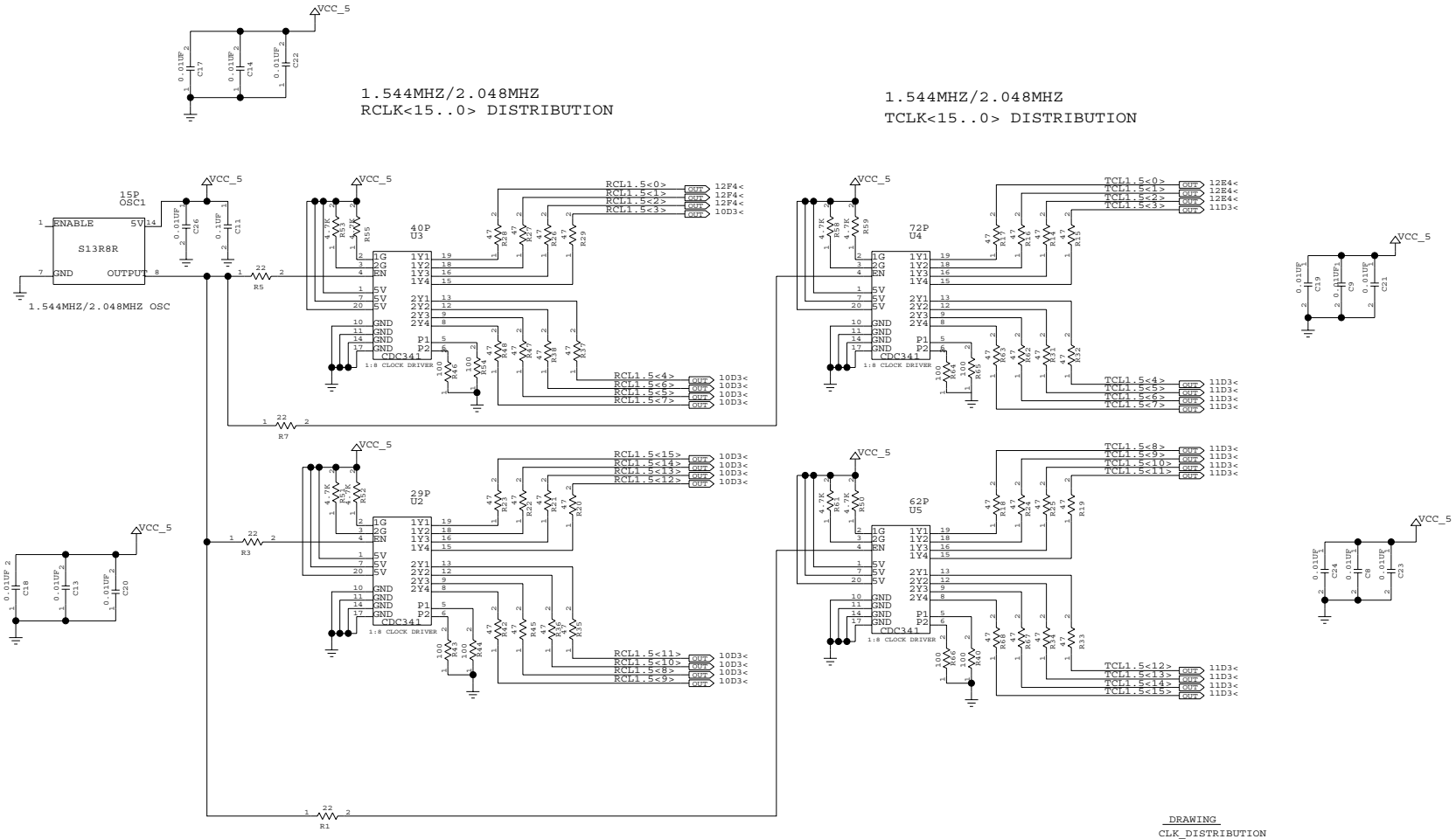
DRAWING
HMVIP_CLKS
HMVIP

LAST_MODIFIED=Tue Mar 28 12:55:42 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT HMVIP AND DS3 CLOCKS	REVISION NUMBER: 2.0
ENGINEER:	PAGE:7 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING
CLK_DISTRIBUTION
CLK

LAST_MODIFIED=Tue Mar 28 12:55:44 2000

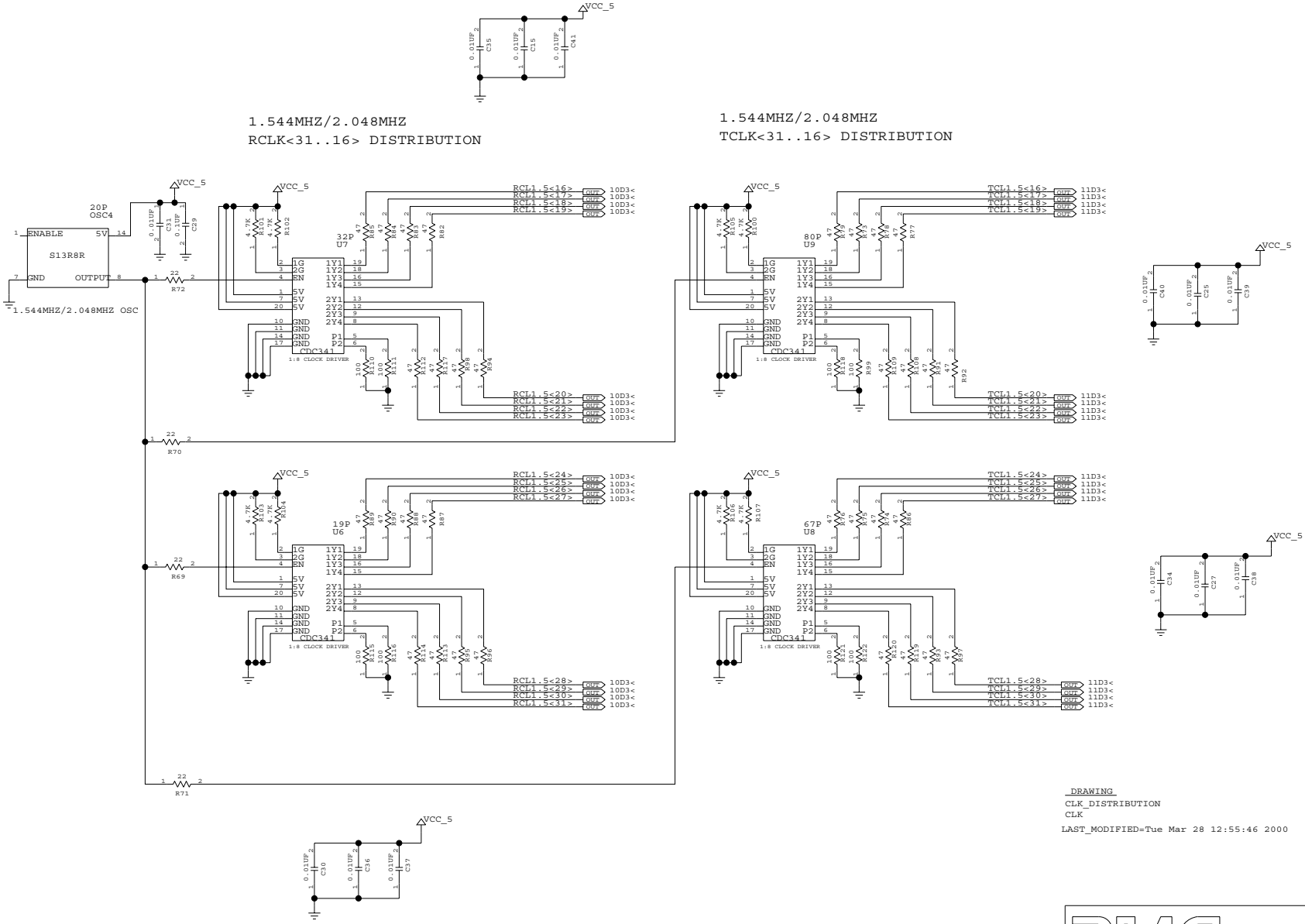
PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT RCLK<15..0> AND TCLK<15..0>	REVISION NUMBER: 2.0
ENGINEER:	PAGE: 8 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

1.544MHZ/2.048MHZ
RCLK<31..16> DISTRIBUTION

1.544MHZ/2.048MHZ
TCLK<31..16> DISTRIBUTION

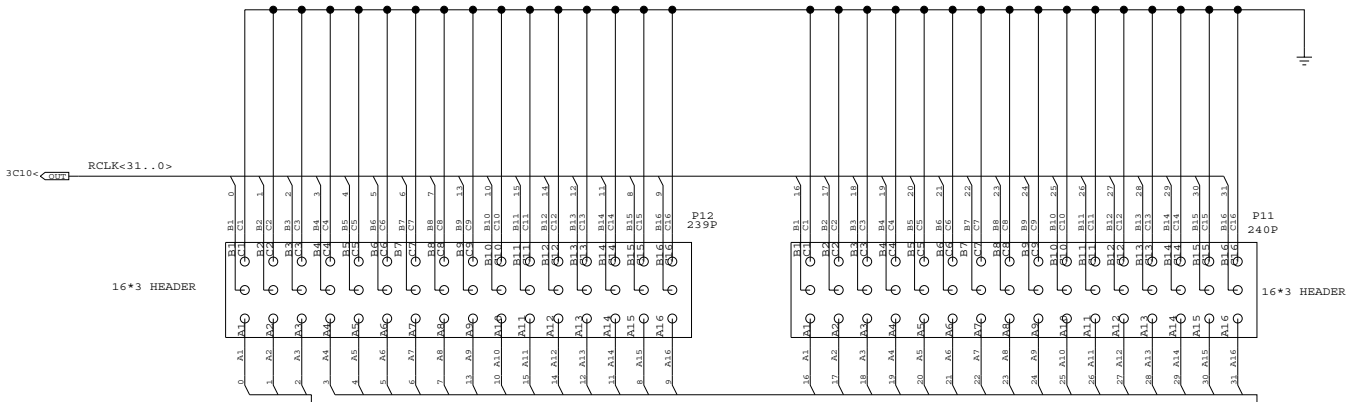


DRAWING
CLK_DISTRIBUTION
CLK
LAST_MODIFIED=Tue Mar 28 12:55:46 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT RCLK<31..16> AND TCLK<31..16>	REVISION NUMBER: 2.0
ENGINEER:	PAGE:9 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



SELECTION OF RCLK<31..0>

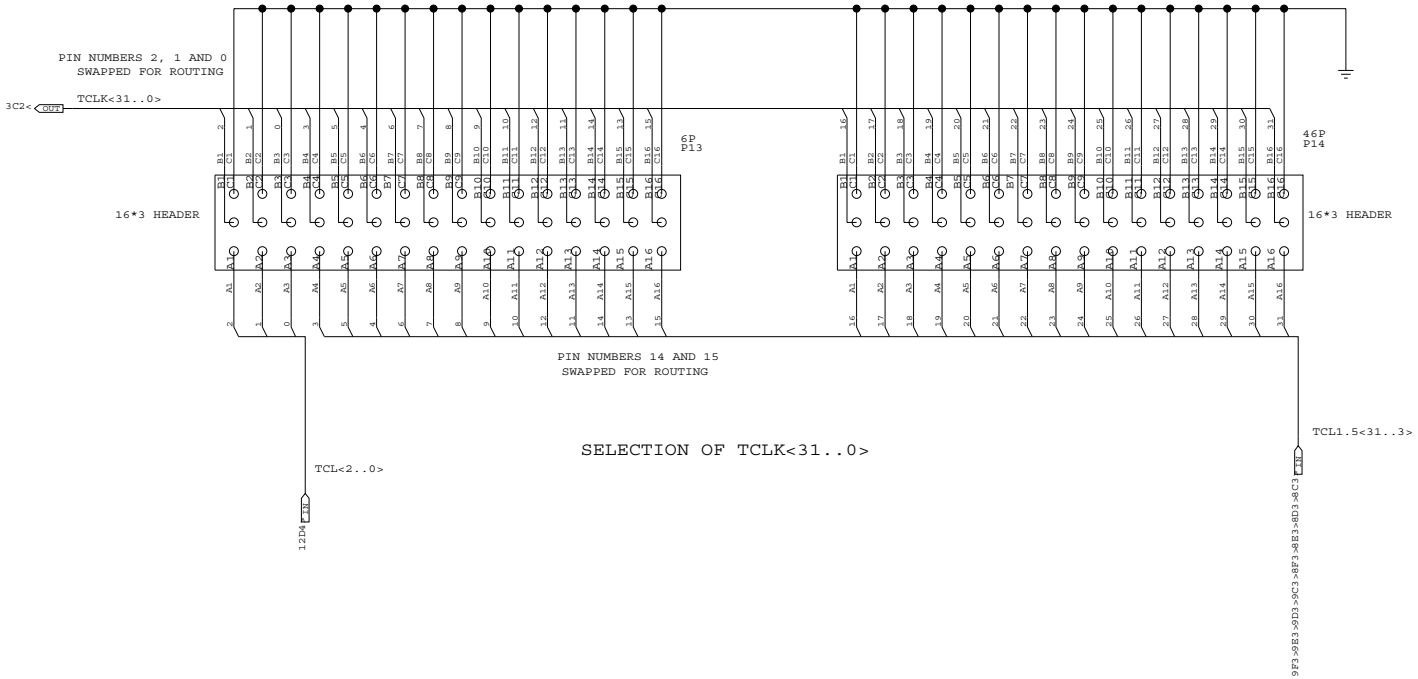
DRAWING
RCLK_SELECTION
RCLK

LAST_MODIFIED=Tue Mar 28 12:55:48 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT RCLK HEADERS	REVISION NUMBER: 2.0
ENGINEER:	PAGE:10 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



SELECTION OF TCLK<31..0>

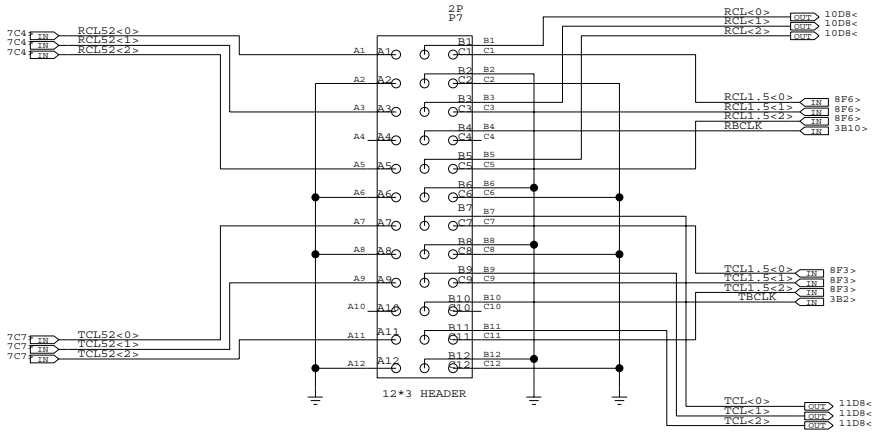
DRAWING
TCLK_SELECTION
TCLK

LAST_MODIFIED=Tue Mar 28 12:55:49 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT TCLK HEADERS	REVISION NUMBER: 2.0
ENGINEER:	PAGE:11 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



SELECTION OF TCLK<2..0> AND RCLK<2..0> FOR 1.544/2.048MHZ OR 52MHZ/DS3 CLOCK

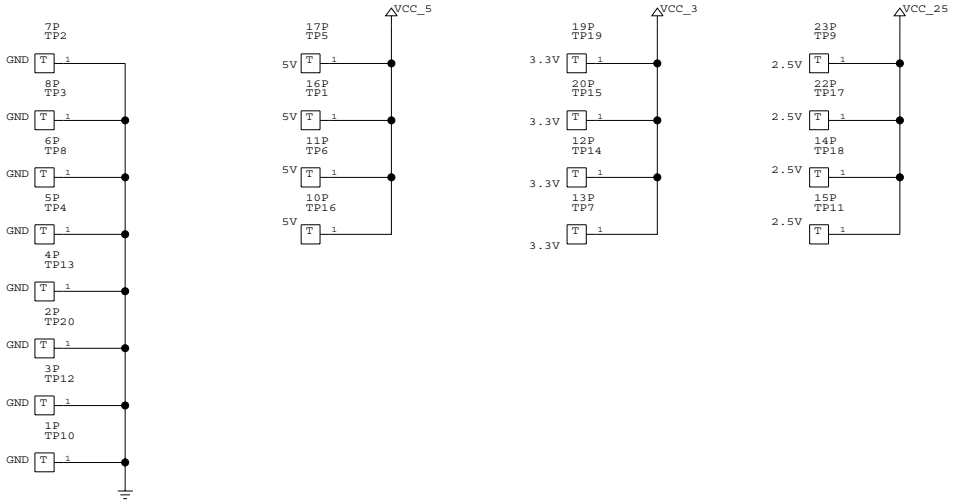
DRAWING
DS3_CLK_SELECTION
DS3_CLK
LAST_MODIFIED=Tue Mar 28 12:55:50 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT DS3 CLOCK HEADER	REVISION NUMBER: 2.0
ENGINEER:	PAGE:12 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

TEST POINT FOR GND,5V,3.3V AND 2.5V



DRAWING
TEST_POINTS
TEST_POINTS
LAST_MODIFIED=Tue Mar 28 12:55:51 2000

PMC-Sierra, Inc.

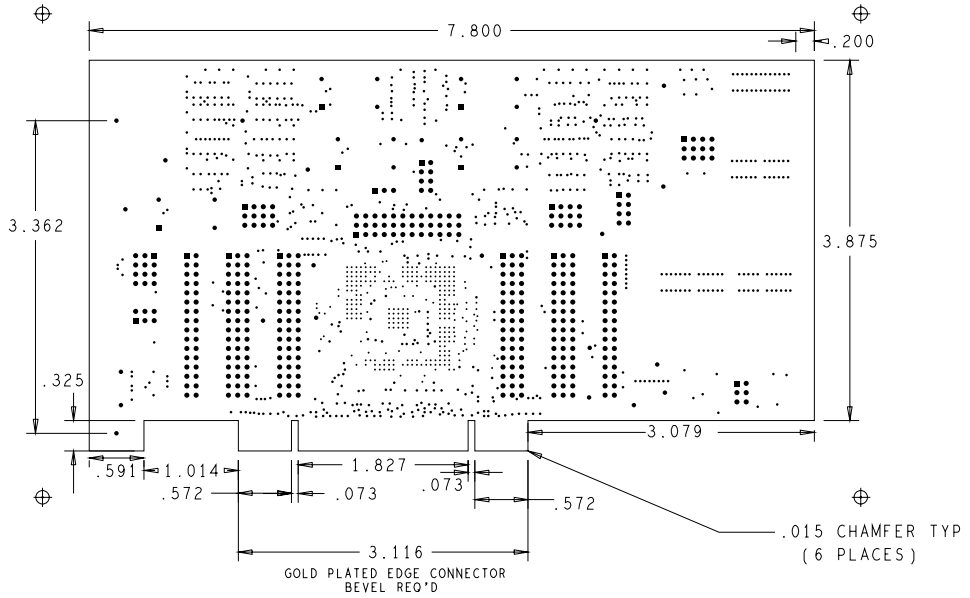
DOCUMENT NUMBER: DOCNUM DOCUMENT ISSUE NUMBER: ISSUE	ISSUE DATE: YY/MM/DD
TITLE: FREEDM-32P672 DEVELOPMENT KIT TEST POINTS	REVISION NUMBER: 2.0
ENGINEER:	PAGE:13 OF 13

11 LAYOUT

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED

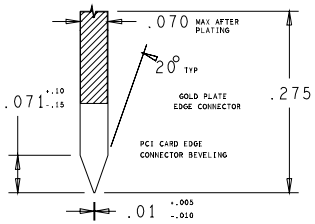
ARTWORK FILM
TOP_LAYER
GND_PLANE
SIG1
VCC_PLANE
GND2_PLANE
SIG2
VCC2_PLANE
BOTTOM_LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING

Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	6.4 mil	4.5
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	7.9 mil	4.5
COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	9.5 mil	4.5
COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC		-------	7.9 mil	4.5
COPPER	CONDUCTOR	GND2_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC		-------	9.5 mil	4.5
COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	7.9 mil	4.5
COPPER	CONDUCTOR	VCC2_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	6.4 mil	4.5
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------



PMC-SIERRA FREEDM-32P672 DEV. KIT REV.2.0 2000

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY



Notes:
1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers. All track width shown under Gerbr files are final trace width.
2. Total thickness of board shall be 62 mil +/- 7 mil. The stackup shown above is the final stackup of this board.
3. The outline dimension are specified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness. All holes size shown are final hole size.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON:	CHECKED			
2 PL DECIMALS ±	ENGRG			
3 PL DECIMALS ±	ISSUED			
ANGLES ±				
FRACTIONS ±				

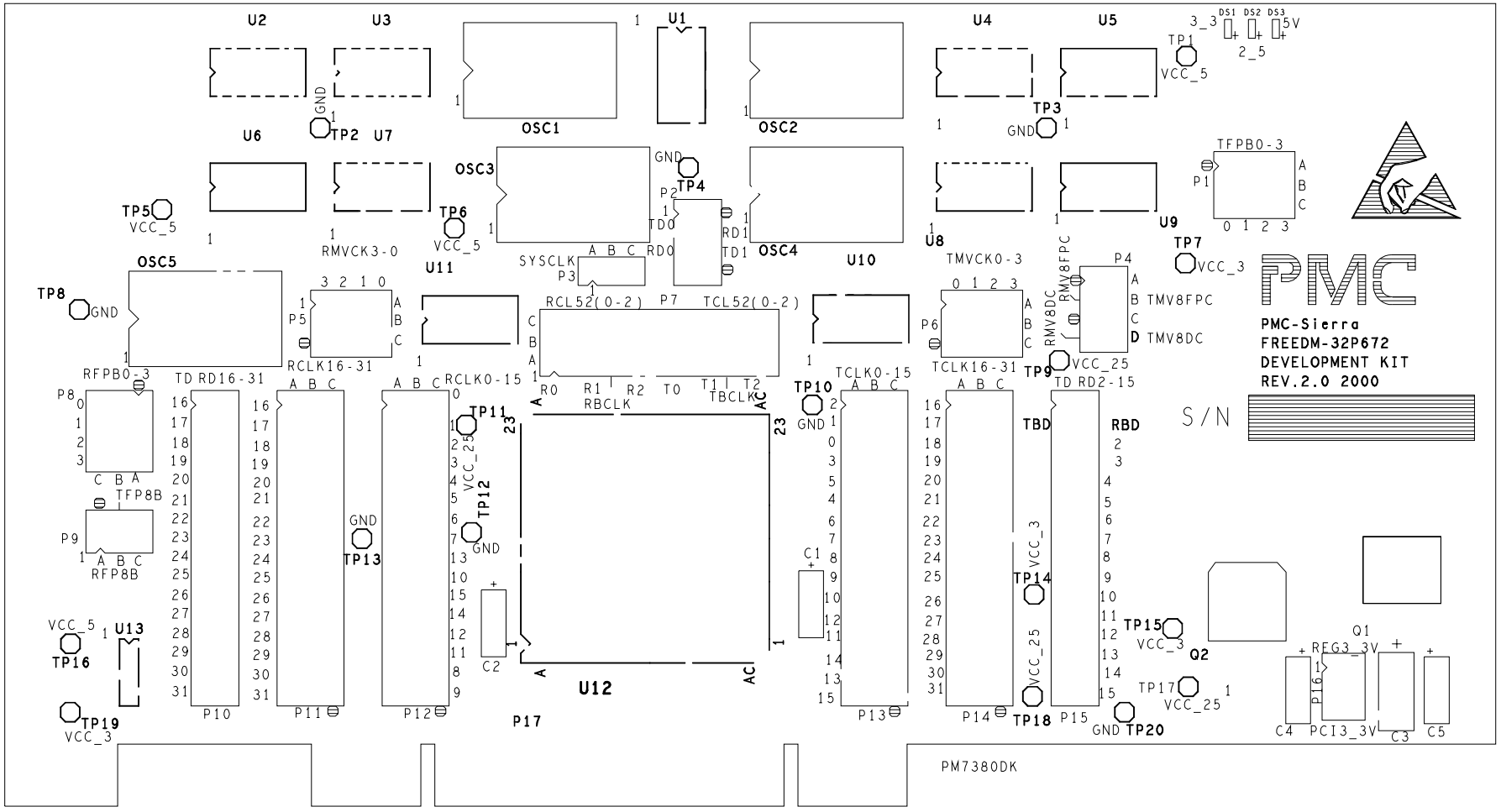
PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

Tel: 604 415-6000 Fax: 604 415-6200

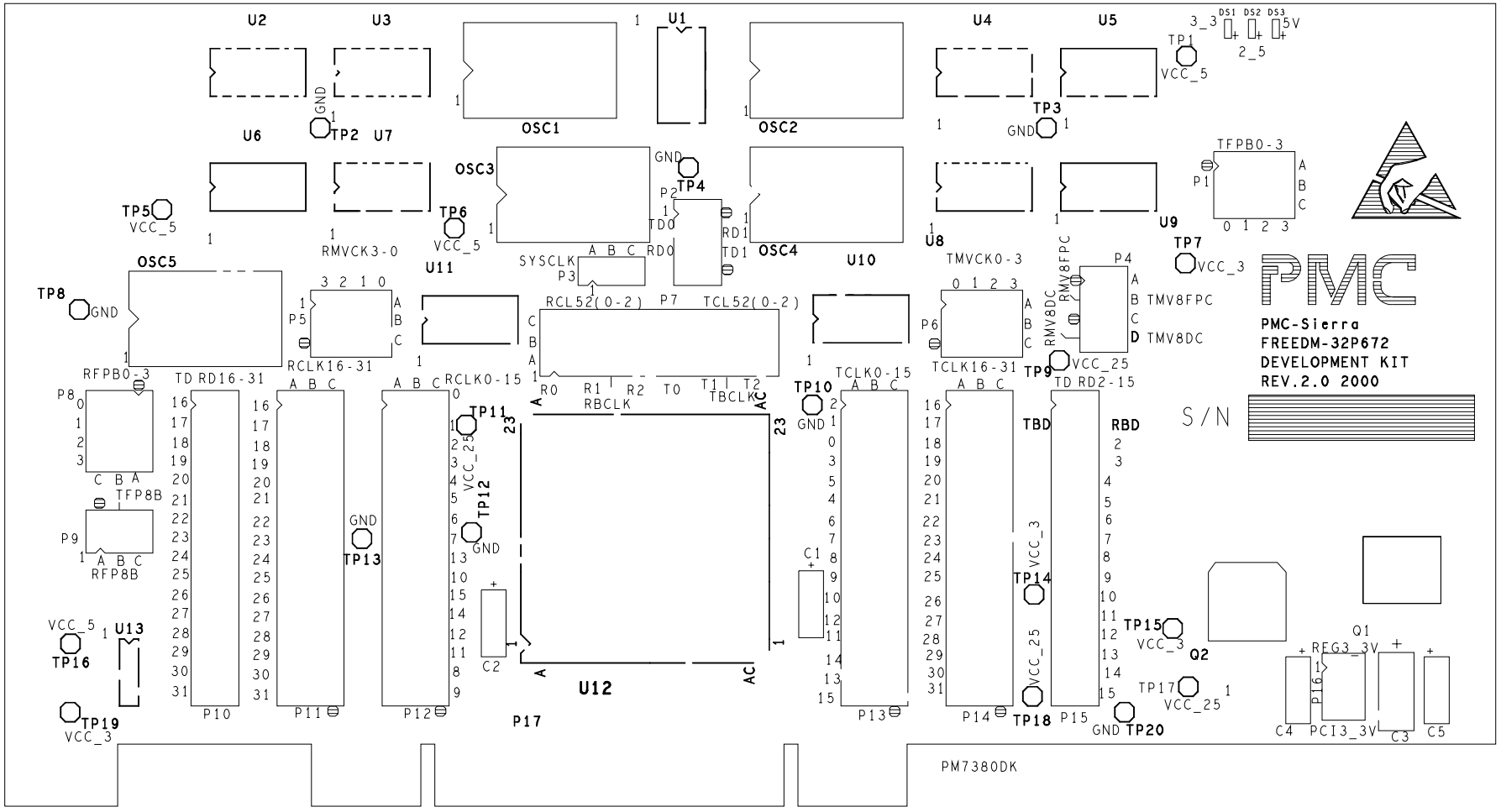
SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

SILK SCREEN TOP



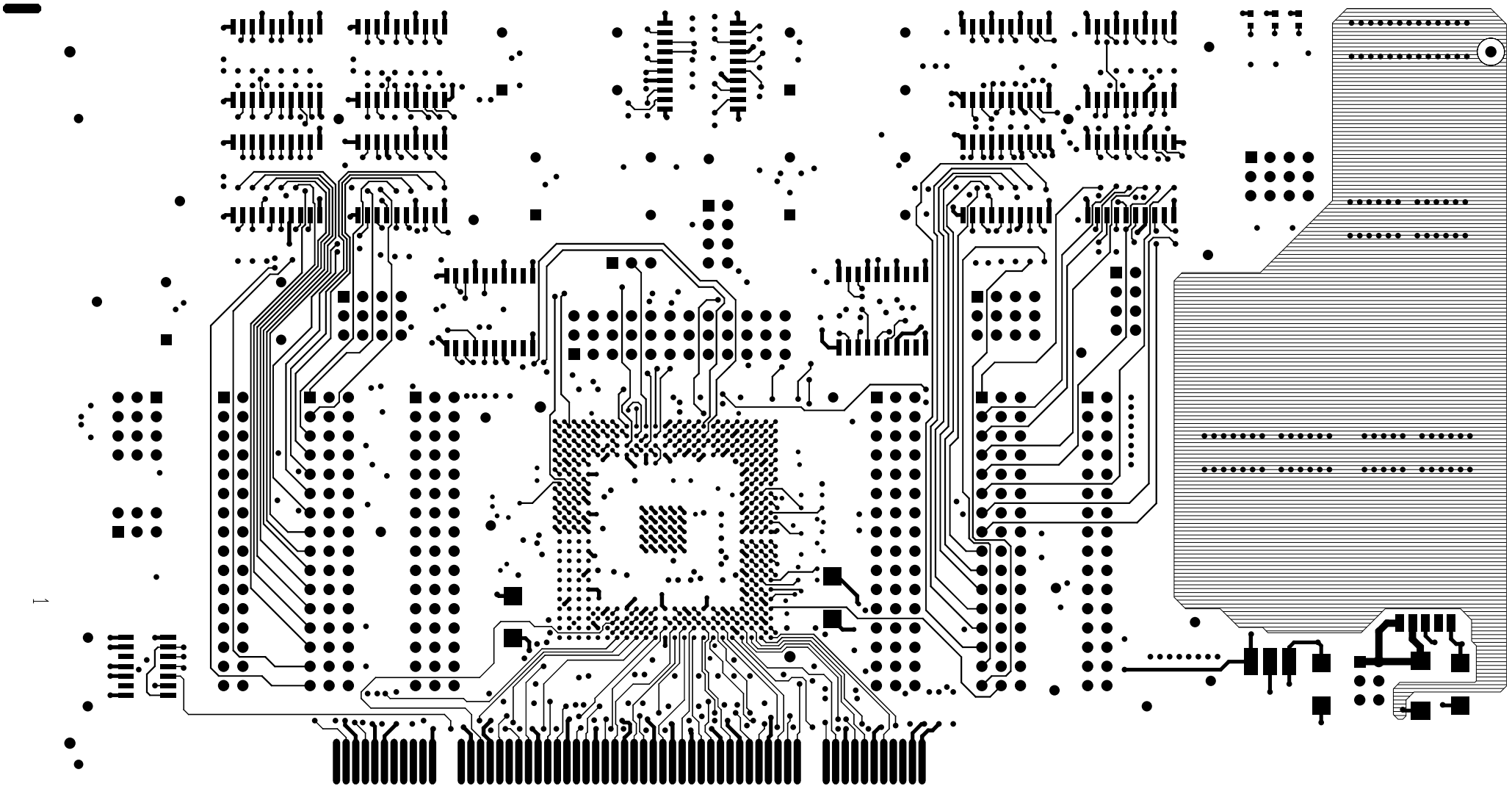
PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

SILK SCREEN TOP



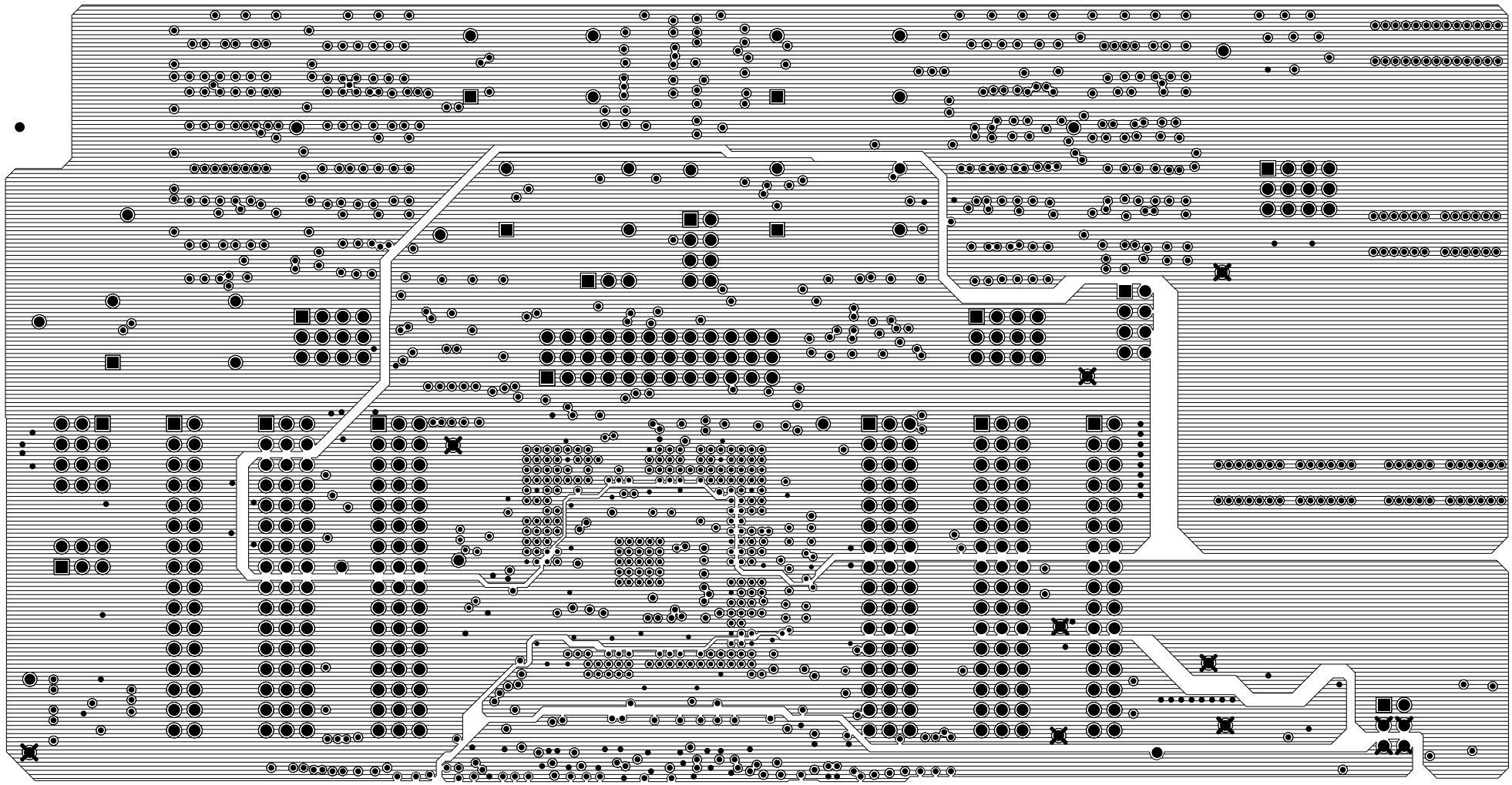
PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

TOP LAYER



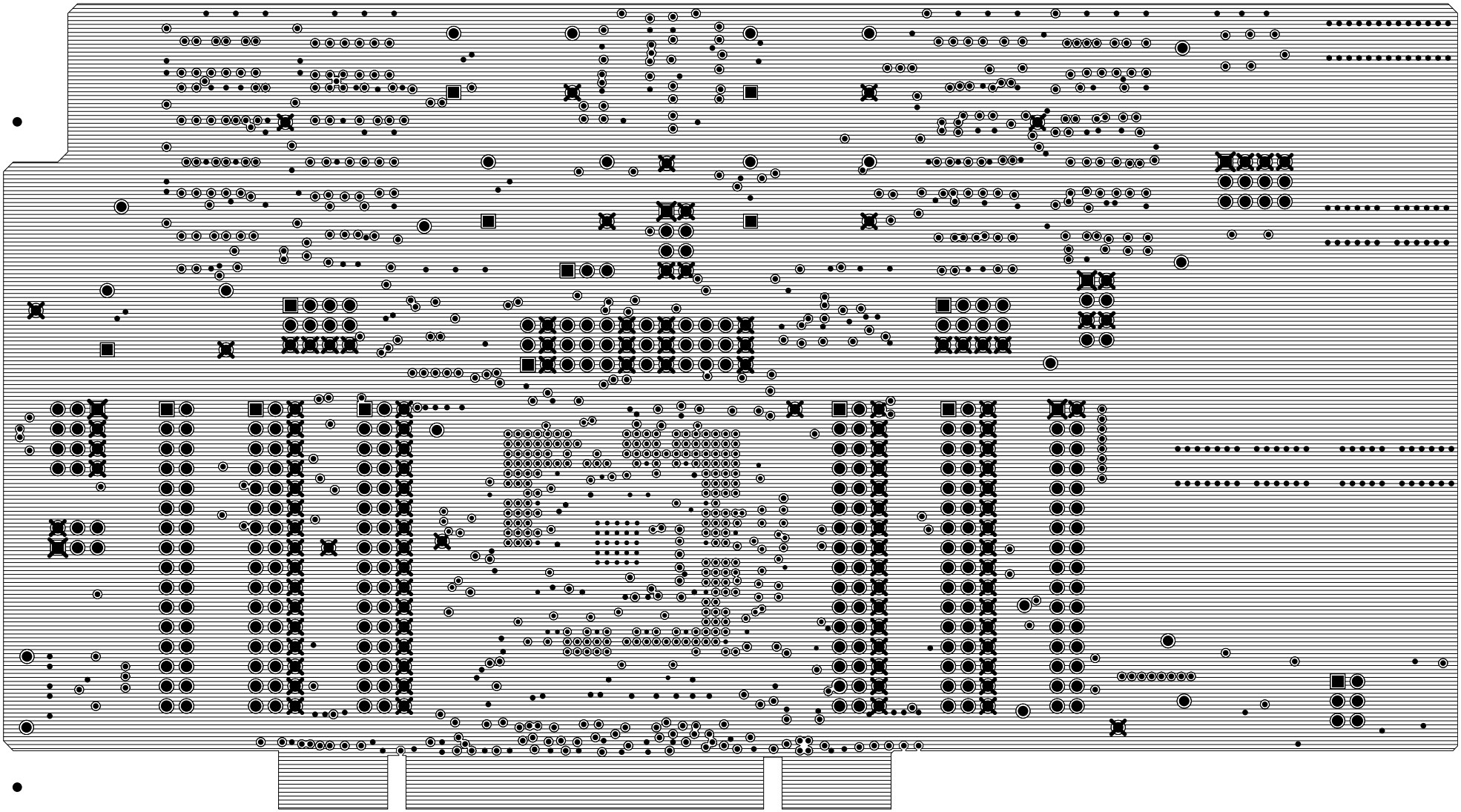
PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

VCC PLANE



4

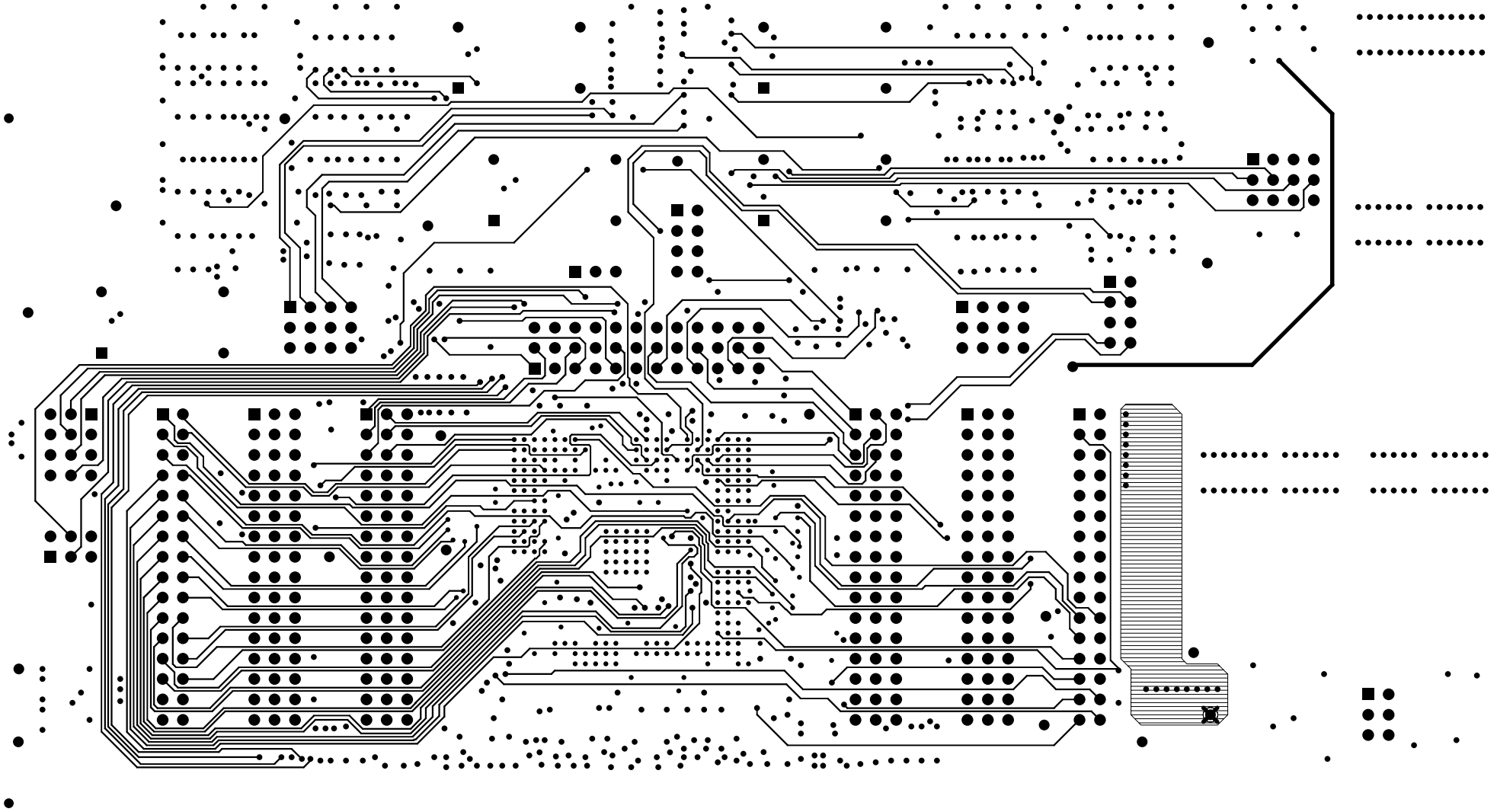
GND_PLANE



2

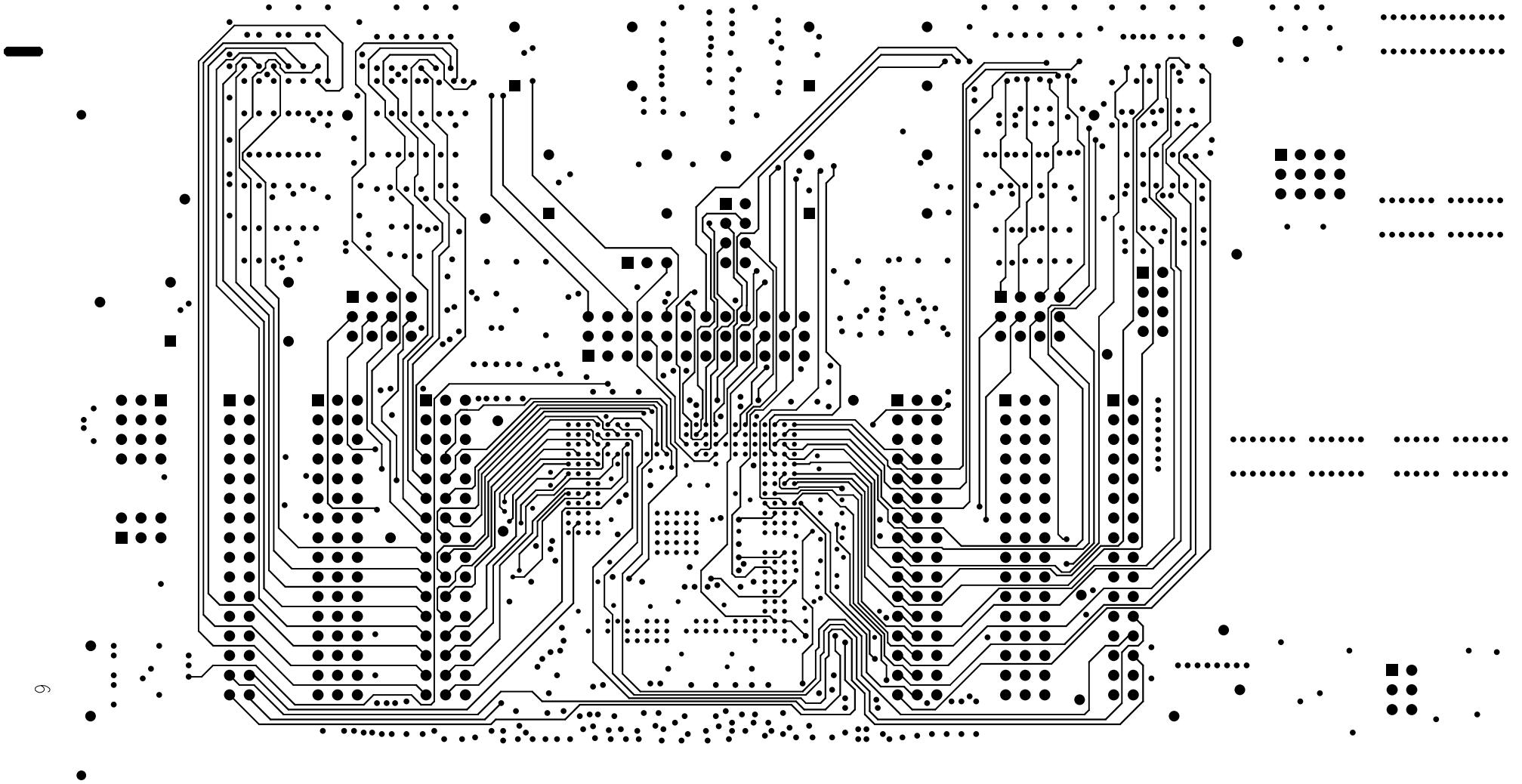
PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

SIG1 LAYER

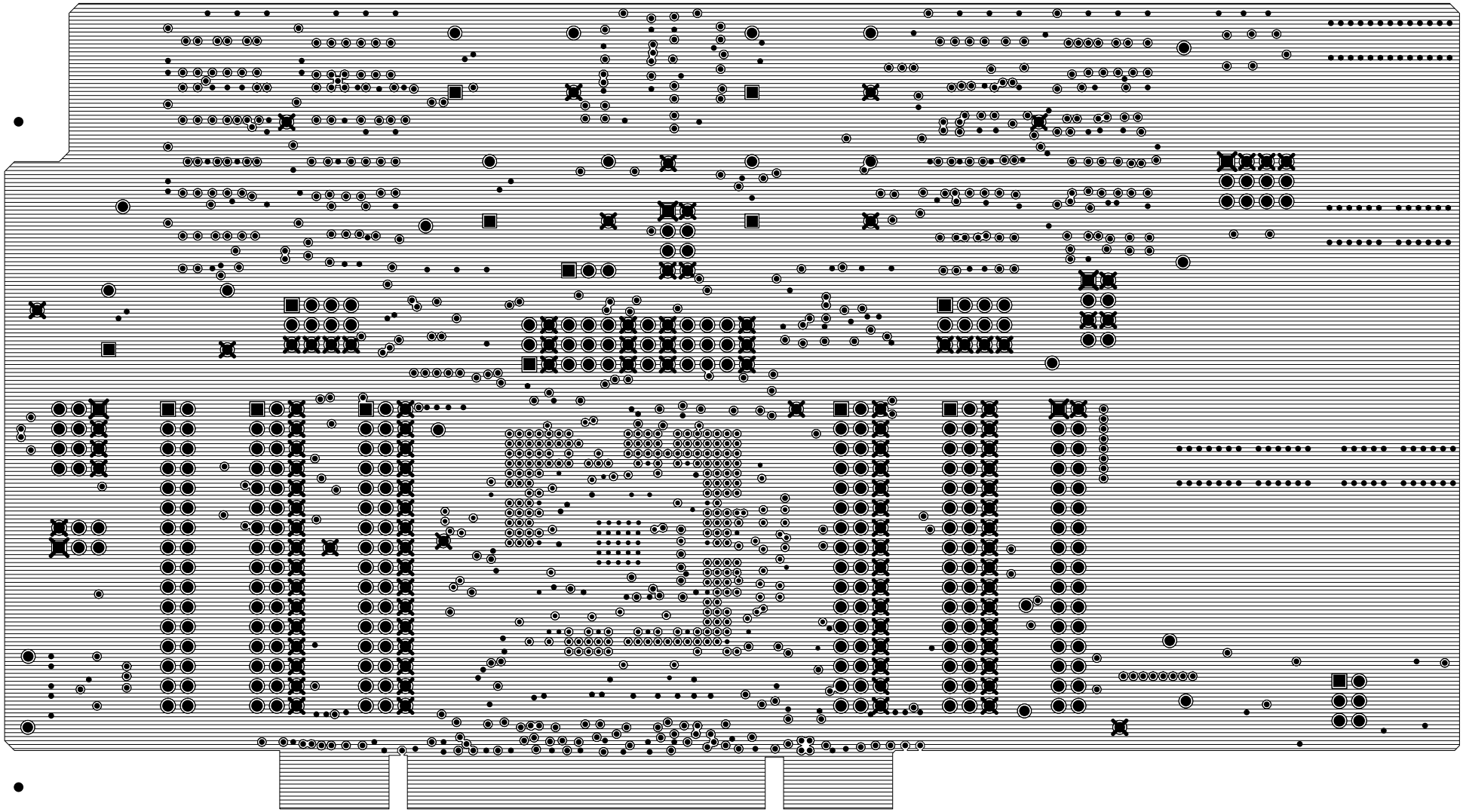


3

SIG2 LAYER

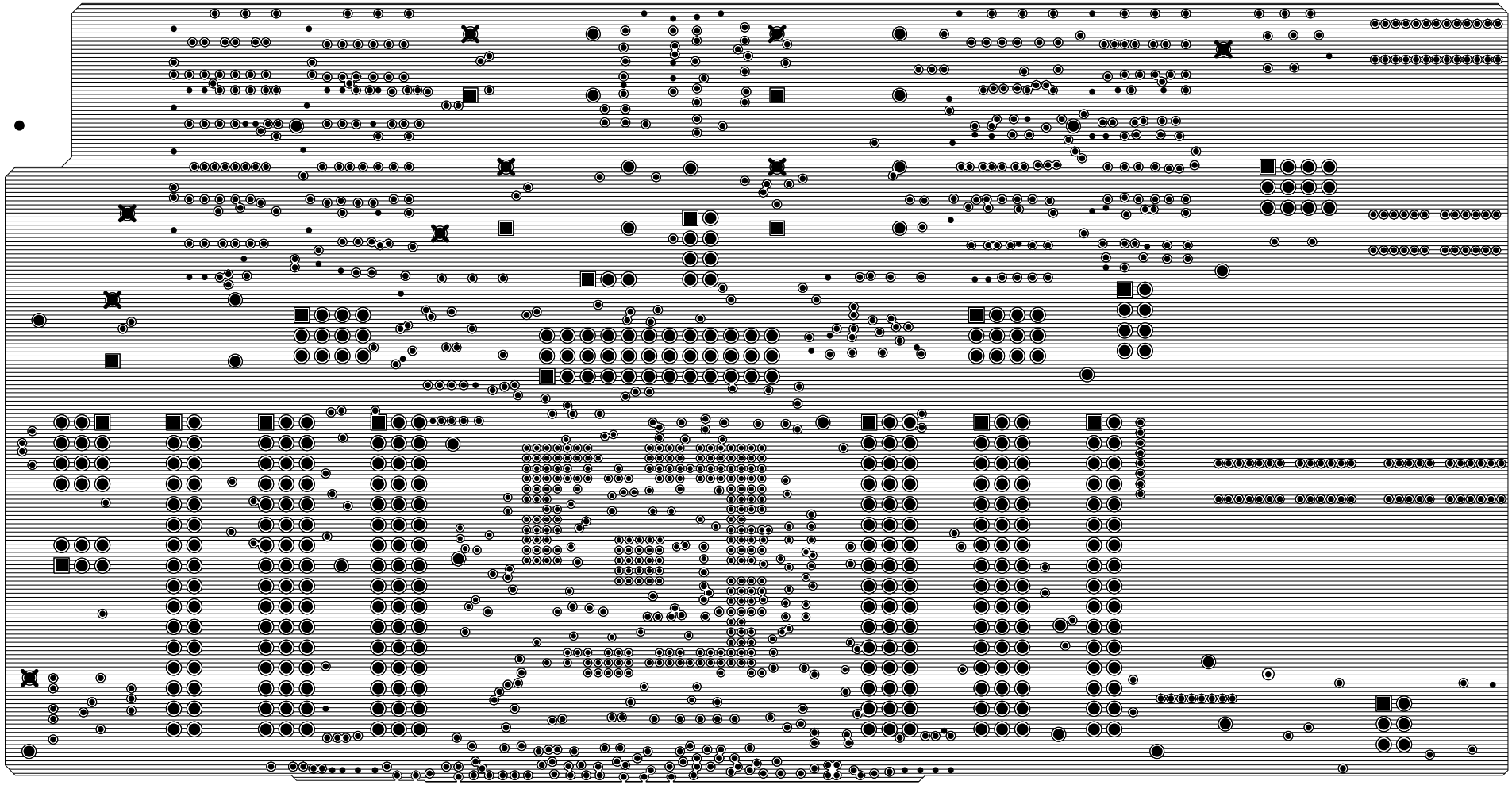


GND2 PLANE

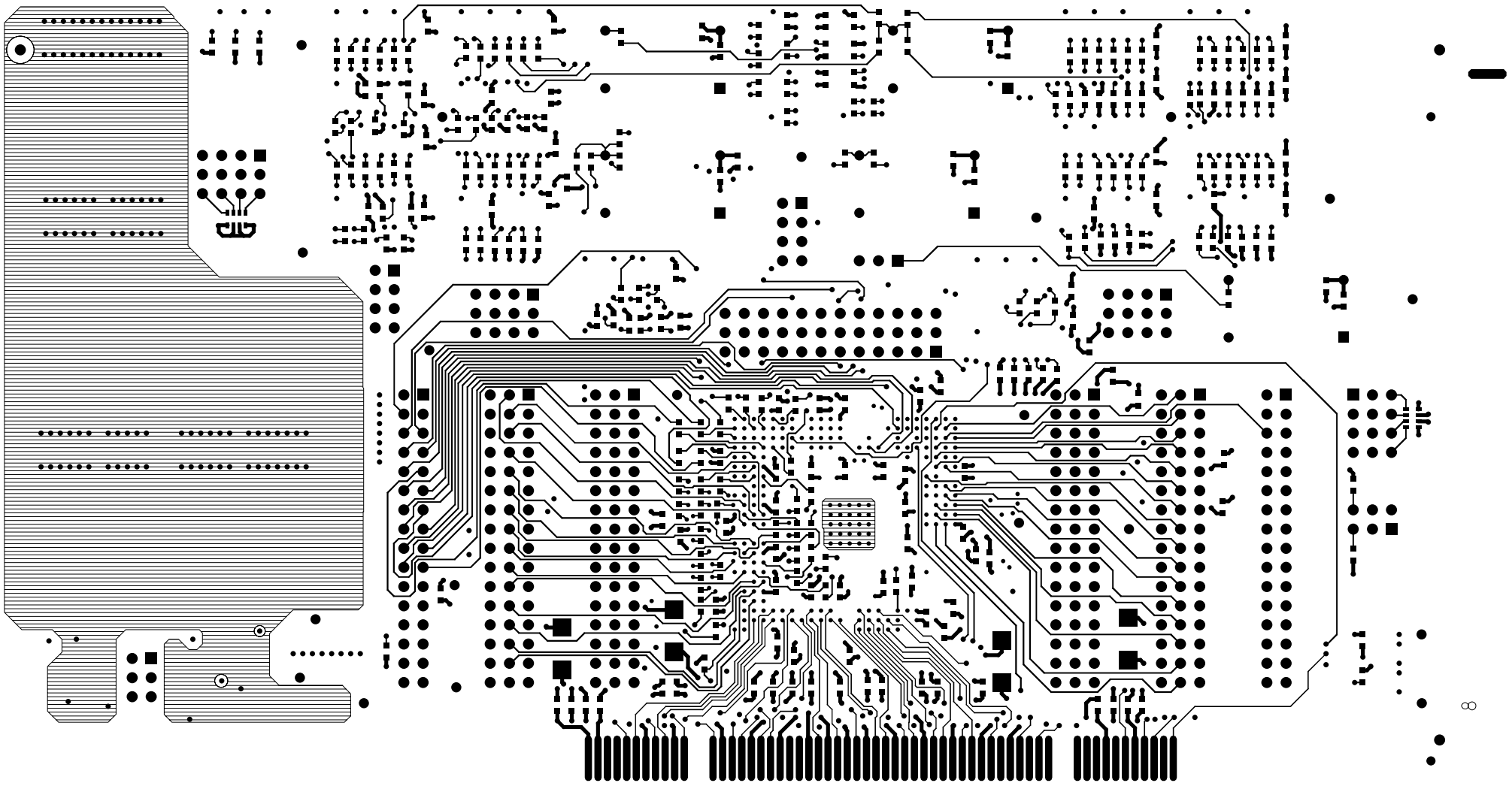


5

VCC2 PLANE

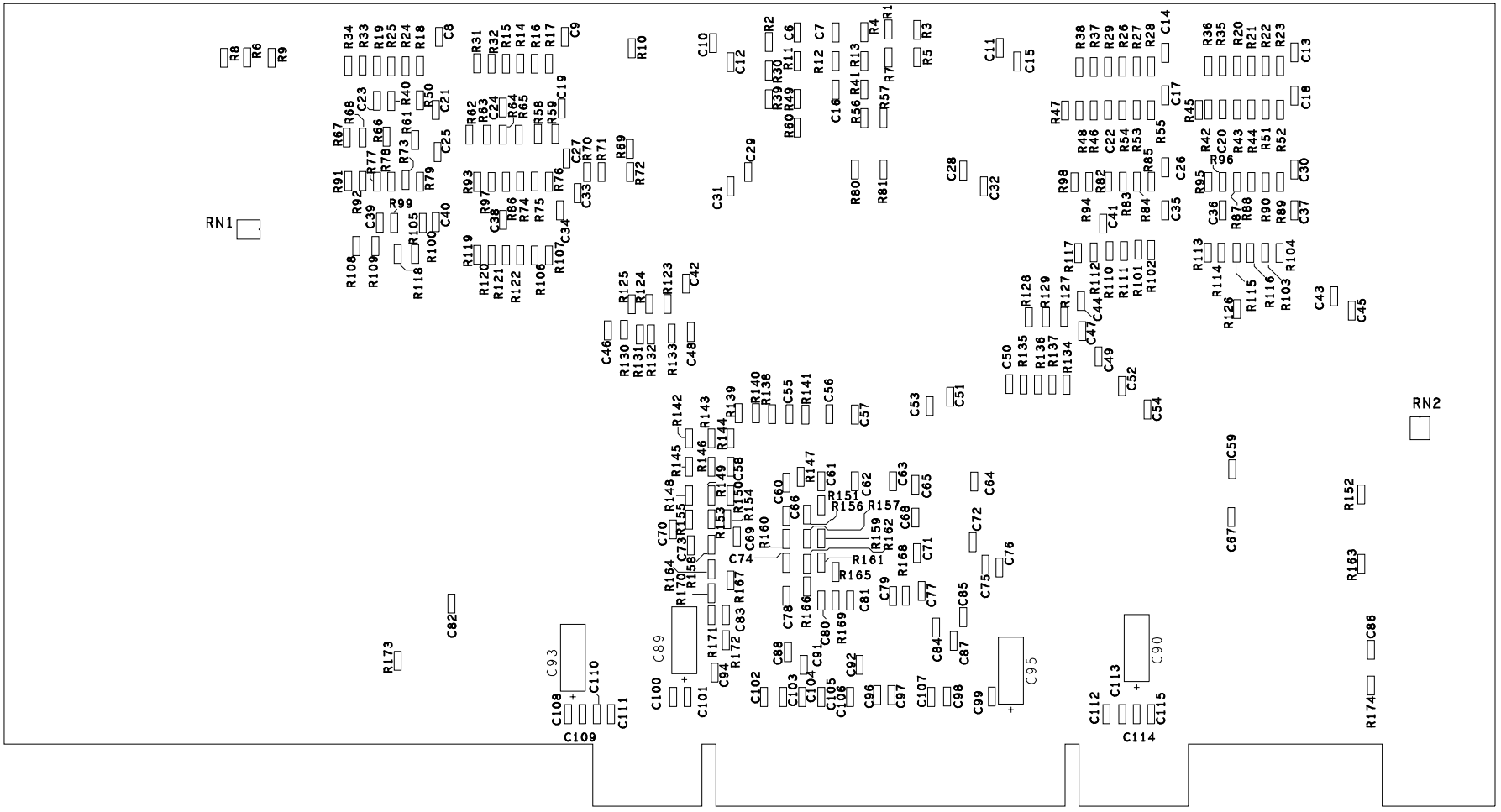


BOTTOM LAYER



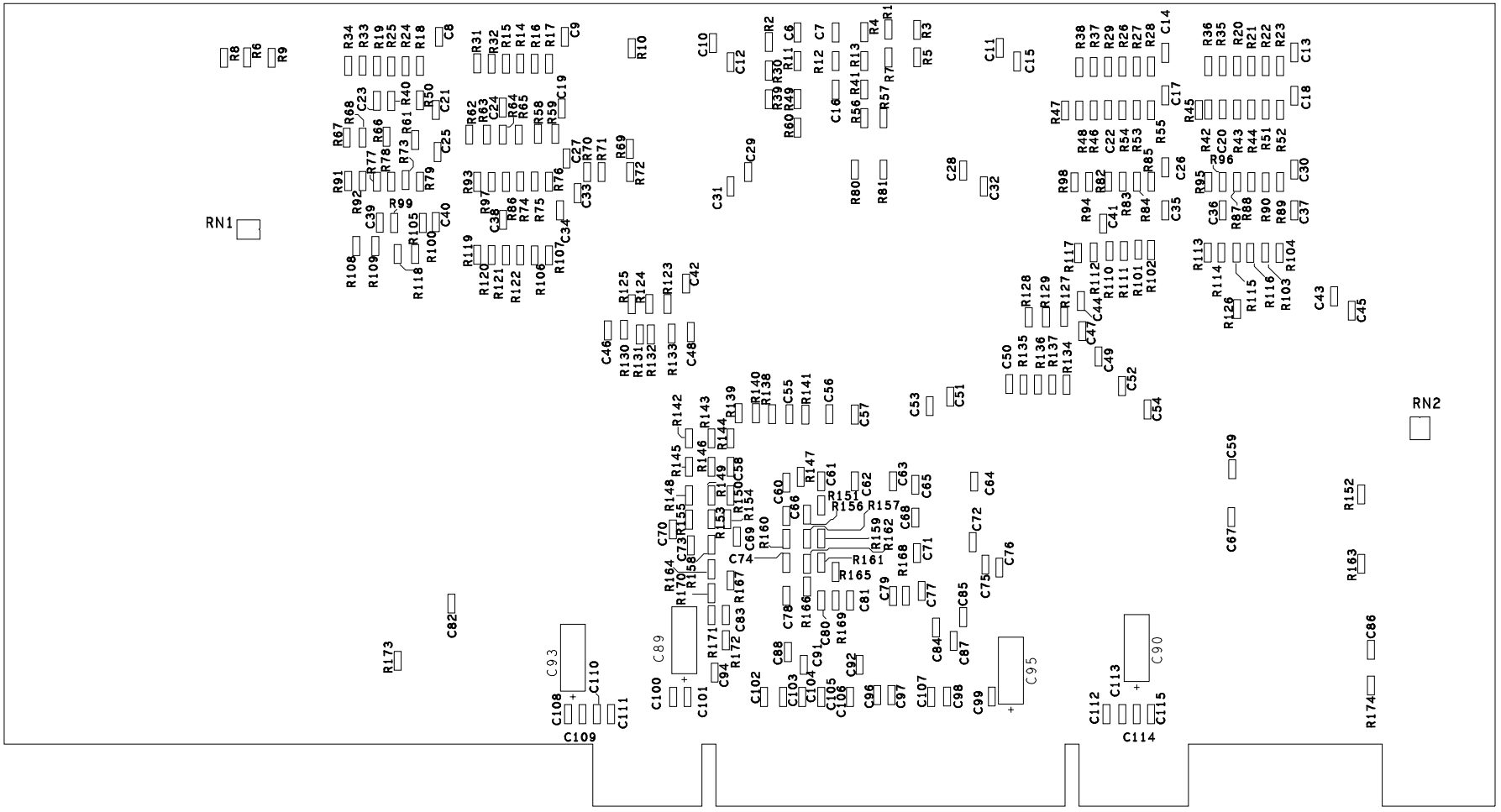
PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

SILK SCREEN BOTTOM



PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

SILK SCREEN BOTTOM



PMC-SIERRA FREEDM-32P672 DEV. KIT REV. 2.0 2000

12 REFERENCES

[1] FREEDM™-32P672 DEVELOPMENT KIT Statement of Work (Issue 2: August 1999, Doc no. PMC-990913)

[2] FREEDM™-32P672 Development kit TEST PLAN (Issue 1, Document no PMC-990860)

[3] FREEDM™-32P672 Device Data Sheet (Issue 2:May 1999, Doc. No. PMC-990262)

[4] Requirement Specifications for FREEDM™-32P672 DEVELOPMENT KIT (PM7380DK.1.0.RS.1.0)

[5] Voltage regulator MIC39150 Device Datasheet. (Manufacturer MICREL, Inc)

[6] Voltage regulator LT1528CQ Device Datasheet. (Manufacturer Linear Technology, Inc)

[7] Designing PC Board Heat Sinks (Application Hint 17, by MICREL Inc)

[8] Oscillator S13R8R Device Datasheet. (Manufacturer: CONNOR –WINFIELD CORPORATION)

[9] Oscillator socket 1107741 Device Datasheet. (Manufacturer: ARIES Electronics, Inc)

[10] Clock Driver CDC341 Device Datasheet. (Manufacturer: Texas Instruments)

[11] Single row header PZCXXSAAN Device Datasheet. (Manufacturer: Sullins Electronics)

[12] Dual row header PZCXXDAAN Device Datasheet. (Manufacturer: Sullins Electronics)

[13] Jumper 2006A Device Datasheet (Manufacturer: Oupiin)

NOTES

CONTACTING PMC-SIERRA, INC.

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