PM73121

AAL1GATOR II

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE AAL1GATOR II

APPLICATION NOTE

ISSUE 1: FEBRUARY 2000

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	February 2000	Creation of Document.

CONTENTS

1 REFERENCES

[1] ATM Forum, “UTOPIA, an ATM-PHY Layer Specification, Level 1”, V. 2.01, Foster City, CA USA, March 1994.

[2] ATM Forum, “UTOPIA, an ATM-PHY Layer Specification, Level 2”, V. 1.0, Foster City, CA USA, June 1995.

[3] PMC-Sierra, PMC-1980620, “AAL1 SAR Processor Data Sheet”, Issue 3

[4] ATM Forum, “Circuit Emulation Service – Interoperability Specification (CES-IS)”, V. 2.0, Foster City, CA USA, August 1996.

[5] ANSI T1 Recommendation T1.630, “Broadband ISDN-ATM Adaptation Layer for Constant Bit Rate Services, Functionality and Specification”, NY, NY, 1993.

[6] ITU-T Recommendation I.363.1, “B-ISDN ATM Adaptation Layer Specification: Type 1 AAL”, August 1996.

2 ACRONYMS

AAL1	ATM Adaptation Layer 1
ACS	ATM Circuit Steering
AMON	ATM Monitoring
AMS	Audio/Visual Multimedia Service
ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
CAS	Channel Associated Signaling
CBR	Constant Bit Rate
CCS	Common Channel Signaling
CDV	Cell Delay Variation
CDVT	Cell Delay Variation Tolerance
CES	Circuit Emulation Service
CLP	Cell Loss Priority
CRC	Cyclic Redundancy Check
CRC-10	10-bit Cyclic Redundancy Check
CSD	Cell Service Decision
CSI	Convergence Sublayer Indication
DAC	Digital-to-Analog Converter
DACS	Digital Access Cross-connect System
DDS	Digital Data Service
DS0	Digital Signal Level 0
DS1	Digital Signal Level 1

DS3	Digital Signal Level 3
E1	European Digital Signal Level 1
E3	European Digital Signal Level 3
E4	European Digital Signal Level 4
ESF	Extended Super Frame
FCT	Fairchild TTL Compatible
FIFO	First-In, First-Out
FPGA	Field Programmable Gate Array
FXO	Foreign Exchange Office
FXS	Foreign Exchange Subscriber
GFC	Generic Flow Control
HEC	Header Error Check
LI	Line Interface
LIU	Line Interface Unit
LSB	Least Significant Bit
M13	Multiplexer Level 1 to Level 3
MIAC	Memory Interface and Arbitration Controller
MIB	Management Information Base
mod	Modulo
MPEG2	Motion Picture Experts Group 2
MPHY	Multi-PHY
MSB	Most Significant Bit
MULDEM	Multiplexer/Demultiplexer
OAM	Operations, Administration, and Maintenance

OC-1	Optical Carrier Level 1
OC-3	Optical Carrier Level 3
PBX	Private Branch Exchange
PCR	Peak Cell Rate
PDH	Plesiochronous Digital Hierarchy
PHY	Physical
PLL	Phase-Locked Loop
PCM	Pulse Coded Modulation
PRBS	Pseudorandom Bit Sequence
PTI	Payload Type Indicator
RALP	Receive Adaptation Layer Processor
RATM	Receive UTOPIA ATM Layer
RFTC	Receive Frame Transfer Controller
RL	Receive Line
RMON	Remote Monitoring
RUTOPIA	Receive UTOPIA
RX	Receive
SAR	Segmentation And Reassembly
SDF-FR	Structured Data Format, Frame-based
SDF-MF	Structured Data Format, Multiframe-based
SDU	Service Data Unit
SF	Super Frame
SN	Sequence Number
SNP	Sequence Number Protection

SOC	Start-Of-Cell
SONET	Synchronous Optical Network
SP	Supervisory Processor
SPHY	Single PHY
SRAM	Static Random Access Memory
SRTS	Synchronous Residual Time Stamp
TALP	Transmit Adaptation Layer Processor
TATM	Transmit UTOPIA ATM Layer
TDM	Time Division Multiplexing
TFTC	Transmit Frame Transfer Controller
TL	Transmit Line
TLIP	Transmit Line Interface Processor
TTL	Transistor-to-Transistor Logic
TUTOPIA	Transmit UTOPIA
TX	Transmit
UDF	Unstructured Data Format
UDF-HS	Unstructured Data Format, High Speed
UDF-ML	Unstructured Data Format, Multiple Line
UI	Unit Intervals
UNI	User Network Interface
UPC	Usage Parameter Control
UTOPIA	Universal Test and Operations Physical Interface for ATM
VC	Virtual Circuit
VCI	Virtual Circuit Identifier

VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VP	Virtual Path
VPI	Virtual Path Identifier

3 BACKGROUND AND OVERVIEW

PMC-Sierra's PM73121 AAL1 Segmentation and Reassembly (SAR) processor provides DS1, E1, E3, or DS3 line interface access to an ATM Adaptation Layer One (AAL1) Constant Bit Rate (CBR) ATM Network.

Due to the versatility of the AAL1gator II, the data book (PMC-1980620) is quite lengthy. In order to help customers quickly find the answers to their questions the following list of frequently asked questions and their answers has been compiled.

If further clarification is required, please contact PMC-Sierra's technical support team at apps@pmc-sierra.com.

4 ANSWERS TO FREQUENTLY ASKED QUESTIONS

Q1) Are there any reference designs or application notes available for the AAL1gator II?

A1) Yes, there are reference designs and application notes available for the AAL1gator II.

The AAL1gator II Reference Design (PMC-1990206) shows an implementation strategy for the AAL1gator II in a Multi Service Access Concentrator environment using the PM4351 COMET, PM4344 TQUAD and the PM6344 EQUAD.

The AAL1gator II Software Driver, complete with both a user's guide and source code in C-language, gives examples of how to program a host to work with the AAL1gator II.

PMC-Sierra Sales Representatives have copies of these documents available for distribution. It is suggested that customers periodically query their local PMC-Sierra Sales Representative for the latest documentation on the AAL1gator II.

PMC-Sierra also has a World Wide Web site at www.pmc-sierra.com from which documentation can be ordered or downloaded. Furthermore, customers can register themselves on the Web site to be notified in the event of changes to the documentation.

Q2) Is there a software driver available for the AAL1gator II?

A2) Yes. The AAL1gator II software driver can be obtained from PMC-Sierra's web site (www.pmc-sierra.com) without any charges after registration.

Q3) Which ATM Forum CES specification does the AAL1gator II comply with?

A3) The AAL1gator II complies with ATM Forum CES specification Version 2.0, January 1997.

Q4) How does the AAL1gator II fulfill the ATM Forum CES counter requirements?

A4) In the AAL1gator II, the counters are implemented on a per-VC basis. The device supports 256 VC's, and each VC has its own set of CES v2.0 counters. Therefore, each ATM cell stream has its own counters and statistics, independent of all other ATM cell streams.

The CES specification requires 32-bit counters. The AAL1gator II provides 16-bit counters in hardware. Software can poll and latch these hardware counters to build 32-bit counters in software.

Q5) Why does the AAL1gator II have two frame sync inputs (*L_FSYNC and *L_MSYNC) instead of one at the framer interface?

A5) The two inputs allow users to have a common configuration for multiframe and frame applications. Some framers provide only a 125 us frame pulse, while other framers provide a 12-, 16-, or 24-frame multiframe pulse. The AAL1gator II can interface to any such framer, by providing both frame and multiframe inputs. Pulses on both *L_FSYNC and *L_MSYNC inputs are not required – either input can be grounded, depending on the application. A frame is indicated by a rising edge on the TL_FSYNC or RL_FSYNC input. A multiframe is indicated by a rising edge on the TL_MSYNC or RL_MSYNC input. The device free-runs in the absence of these signals and may accept *L_FSYNC and *L_MSYNC which have only occasional rising edges.

In SDF-FR mode, the *L_MSYNC signals are optional and usually grounded – a 125 us frame pulse is typically connected from the framer or external logic to the *L_FSYNC inputs. In SDF-MF mode, either a multiframe pulse is typically connected to the *L_MSYNC inputs, or a 125 us frame pulse is connected to the *L_FSYNC inputs, and the other frame sync input is grounded. If the *L_MSYNC inputs are grounded, the AAL1gator II assumes its own multiframe alignment, which is acceptable in most applications if the framer repeats the signalling during an entire multiframe.

If any of the *L_FSYNC or *L_MSYNC signals occurs at an improper time, the AAL1gator II executes a resynchronization procedure.

Q6) Why does the AAL1gator II have a 0 to 32 ms tolerance for CDVT?

A6) Cell arrival-time jitter is called Cell Delay Variation (CDV). The CDV tolerance is completely programmable by the user and can be set anywhere within a 0 to 32 ms range. PMC-Sierra has provided up to 32 ms because an ATM network is asynchronous and therefore the voice traffic in cell form can bunch up due to delays along a segment. The AAL1gator II can insert delay (R_CDVT) to allow for unequal spacing between cells. This is analogous to using a FIFO in an asynchronous path.

Q7) What is the maximum cell arrival jitter that the reassembly process will tolerate without producing errors on the E1/DS1/DS3 interface?

A7) In E1 mode the maximum buffer depth is 512 frames and therefore the CDV tolerance is based on filling up the receive buffer to the halfway point of 256

frames. In this mode, the AAL1gator-II can handle up to [256 frames x (1/8 ms per frame)] = 32 ms of CDV.

For the structured T1 and E1_w_T1_sig modes, the maximum buffer depth is 384 frames. So, the midpoint of the buffer is 192 frames. This becomes [192 frames x (1/8 ms per frame)] = 24 ms of CDV tolerance.

For the unstructured modes, one frame is considered to be 256 bits. Therefore, the maximum CDV tolerance can be figured out by multiplying 256 bits/frame by the TDM clock rate, times 256 frames (half the buffer depth). So, the CDV tolerance is

For unstructured T1: [(1/1.544 MHz) x 256 x 256] = 42 ms of CDV tolerance

For unstructured E1: [(1/2.048 MHz) x 256 x 256] = 32 ms of CDV tolerance

For unstructured DS3: [(1/44.746 MHz) x 256 x 256] = 1.4 ms of CDV tolerance

For unstructured E3: [(1/34.368 MHz) x 256 x 256] = 1.9 ms of CDV tolerance

Q8) What delays occur in the AAL1gator II?

A8) In the receive(ATM to TDM) direction, delay is dominated by the R_CDVT setting. In this direction, the delay will be only fractionally more than the configured R_CDVT. Other minor sources of delay are approximately 20 µs in the line interface and approximately 10 µs in the cell interface. In addition, if cells arrive in a burst, the device may push back on the UTOPIA interface, causing a delay at that interface.

In the transmit (TDM to ATM) direction, there are four delay components: assembly (packetization) delay, CSD scheduling delay, cell construction delay, and UTOPIA delay.

The delay is dominated by the time it takes to accumulate enough data to build a cell. This delay is known as assembly delay and is calculated by determining the number of frames required to build a cell. This value is the FRAMES_PER_CELL field in the QUEUE_CONFIG word in the transmit queue table. If you multiply this value by 125 us you will get the assembly delay for all cells on that queue.

The second component of delay in the transmit direction is the delay incurred within the Cell Service Decision block (CSD). The CSD circuit produces a relatively optimal cell generation time. It has a calendar queue table and produces accurate schedules. The CSD makes cell scheduling decisions only on frame boundaries (every 125 us); therefore, many of the delay and cell delay variation characteristics of the scheduler have a frame based component.

Delay is incurred when the actual start time for cell generation deviates from the scheduled start time for cell generation. This delay will occur when multiple cell scheduling events occur simultaneously. The actual delay produced is configuration dependent, but has the following properties:

- Within a line, the VCs are processed in a consistent order. The delay from processing these VCs is dependent on how many other VCs on that line are scheduled to send cells during the same frame. The VCs that expire in a given frame will be serviced in ascending numerical order. To minimize this delay, queue should be added at different times.

- The actual frame expiration order is recorded in a FIFO. This minimizes the CDV generated when there are more VCs due to be generated in a frame than can be sent in a frame.

- Staggering the frame synchronization among the eight lines may lower the CDV produced by the CSD for cells that are scheduled simultaneously on different lines.

The third component of delay for the transmitter is the actual cell construction time. It typically takes around 8-10 us to build a cell. This delay can vary depending on the amount of contention on the RAM interface at the time the cell is being built.

The fourth and final component of delay for the transmitter is the time it takes for the cell to make it out to the UTOPIA bus. This delay is usually quite small (a couple of microseconds) unless there is UTOPIA back pressure.

Q9) What is the general guideline for setting the Receive Maximum Buffer (R_MAX_BUF) size?

A9) The R_MAX_BUF is set to at least [2 x R_CDVT] or [R_CDVT + (2 x FRAMES_PER_CELL)], whichever is larger. The primary issue is that R_MAX_BUF should be set large enough to prevent a buffer overrun. An important factor to consider is the typical swing in buffer depth which occurs during each cell arrival. For an unstructured VC, the buffer depth instantaneously increases by only about 1.5 frames (256-bit increments) during each cell arrival. The 2 x R_CDVT setting is more appropriate in this case. For a single-DS0 connection, the buffer depth instantaneously increases by 47 frames during each cell arrival, a much larger variation than an unstructured VC. In this case, the R_CDVT +(2 x FRAMES_PER_CELL) setting is more appropriate.

Q10) Is it possible to send timeslot 0 with the device?

A10) Yes, it is possible. The AAL1gator II can assign any timeslot to any VC. If timeslot 0 travels through the framer or is bypassed by the framer, then it can be

assigned to any VC or can be combined with any other timeslots to any VC. For information on handling signaling information, please refer to the data sheets of PMC-Sierra's T1 framers (PM4341A T1XC, PM4344 TQUAD, PM4388 TOCTL) and PMC-Sierra's E1 framers (PM6341 E1XC, PM6344 EQUAD, PM6388 EOCTL).

Q11) Can the AAL1gator II be used to send compressed video?

A11) Yes, although the Audio/Visual Multimedia (AMS) Implementation Agreement has chosen AAL5 for the transport of Motion Pictures Experts Group 2 (MPEG2), the AAL1gator II can be used to send compressed video in either structured or unstructured form.

Q12) For the AAL1gator II UTOPIA interface, are both the UTOPIA cell mode and the octet mode supported? Do these modes need to be set or controlled?

A12) The AAL1gator II supports both the UTOPIA cell mode and the octet mode, in byte-by-byte or cell-by-cell modes. For the transmit side, the AAL1gator II will not write a cell until it has a full cell to send. The PHY layer can direct the AAL1gator II to stop writing a cell at anytime. After the PHY layer tells the AAL1gator II to stop writing cells, the AAL1gator II will pause or stop sending the cell until it is notified by the PHY layer to continue. For the receive side, the AAL1gator II requests a cell when there is a space available for a full cell. The AAL1gator II performs both byte-by-byte and cell-by-cell mode transfers, depending on the PHY layer.

Q13) If the AAL1gator II is used in the 8-line mode, can bytes from different lines be mixed into the same cell?

A13) No, bytes from different lines cannot be mixed.

Q14) The following loopback features are needed to assist in board-level testing and fault isolation: cell transmit to cell receive at the UTOPIA interface, and line transmit to line receive at the line interface. Can these loopbacks be attained?

A14) While the AAL1gator II does not have these features, the UTOPIA-side loopback can be accomplished through the switch, and the line-side loopback can be accomplished through PMC-Sierra's framers.

Q15) What is the maximum rate at which the AAL1gator II can accept OAM cells?

A15) The device can accept OAM cells at a peak rate faster than it can process the non-OAM cells. It has an OAM receive buffer that is 256 cells deep. The microprocessor could probably dequeue an OAM cell in approximately 10 accesses as it would need to read the header and the cell type, then update the

pointer. Each access can average about 500 ns, leading to a peak cell time of 5 µs. This translates to a peak rate near 45,000 cells per second, a burst tolerance of 256 cells, and a sustainable cell rate near the peak rate (45,000 cells per second).

Note that this assumes that no data cells are being received. If data cells are being received, enough bandwidth needs to be reserved to handle the data cells. See the Peak Cell Rate section in the data sheet to see the peak cell rate for different configurations. In general, OAM cells are sent at a relatively low data rate (only a few per second per VC). So OAM bandwidth is not an issue.

Q16) What priority do OAM cells have compared to traffic cells in the cell transmit direction? How does OAM cell insertion affect the CDV?

A16) OAM cells have higher priority than data cells. Therefore, care should be taken to not produce excessive CDV in the non-OAM cells by bursty generation of OAM cells. One possible implementation would be to limit the transmission of OAM cells sent per operating system tick.

Q17) Does the AAL1gator II perform HEC error detection?

A17) No, the AAL1gator II does not perform HEC error detection because the UTOPIA specification (refer to [1] and [2] of the references) indicates that the HEC checking should be performed in the PHY layer.

Q18) What is the local clock SYS_CLK used for, and what are the requirements for using it?

A18) Within the AAL1gator II the system clock SYS_CLK operates the state machines, the memory interface, and the microprocessor interface. It is set to 38.88 MHz (derived from the equation 155.52 ÷ 4), 50 ppm or less for E1/T1 modes and up to 40 MHz for DS3 mode. If the nominal setting of the internal frequency synthesizer or the provided external frequency synthesizer is used, it should be network-derived; otherwise, it can be freerunning. It must meet duty cycle requirements as well.

If the internal clock synthesizers are used to generate standards-compliant T1/E1 frequencies, SYS_CLK must be 38.88 MHz +/- 50 ppm.

Q19) Does the AAL1gator II accept deframed data in both structured and unstructured formats (for example, 192 bits)? If not, then must the framer have a pass-through mode?

A19) No, the AAL1gator II accepts deframed data in unstructured mode only. Yes, the framer or circuit around the framer must have a pass-through mode, such as the pass-through mode supported by PMC-Sierra's framers.

Q20) If a buffer is composed of multiple T1 frames stored in memory, how are underruns/overruns detected for a VC or a channel?

A20) Read and write pointers are maintained per VC.

Q21) Are there any restrictions on the size and use of partially filled cells?

A21) Partially filled cells can be used as long as the cell generation rate per queue is slower than once per frame. For unstructured lines, this means that the BYTES_PER_CELL must be between 33 and 47. For structured applications, the BYTES_PER_CELL number must exceed the number of DS0 channels allocated to the queue. For example, a two channel queue can have the number set from 3 to 47. This limitation exists because only one cell can be scheduled per queue per frame. Refer to “QUEUE_CONFIG Word Format” on page 135 of [3].

An additional requirement is that partially filled cells only be used to the extent that they do not cause the cell rate to exceed the maximum allowable cell rate for the operating mode. Partially filled cells amount to a bandwidth multiplier. Consider one T1 line with each DS0 having its own VCI. Normally a cell would be generated for each of these 24 queues, about once every 47 frames, which is the limit of the specification. However, if the partially filled level is set to 2, then there would be 24 cells generated every two frames. See section on Peak cell rates for more information.

Q22) Does the AAL1gator II drive the SRAM control signals (/MEM_WE(0), /MEM_WE(1), /MEM_OE, and /MEM_CS) during microprocessor accesses to the SRAM (refer to section 4.3.2 “Memory Interface Signals” on page 84 of [3])?

A22) Yes. It also drives the external transceiver signals.

Q23) The address maps for the transmit data structures and the receive data structures appear to address down to a word (16 bits) with an address range of 00000h to 1FFFFh. What is the purpose of address bit 17 (ADDR17)?

A23) ADDR17 selects between the external SRAM (00000h to 1FFFFh) and the internal device CMDREG register (20000h).

Q24) The 3008 divider is only for fully populated unstructured cells. For partially filled or structured cells, the divider needs to change. Is this supported in the AAL1gator II?

A24) No, SRTS is supported only for full cells in the two UDF modes.

Q25) Can the AAL1gator II switch from SRTS to adaptive clock recovery on the fly?

A25) Yes, if both are externally generated. Both SRTS and adaptive information are always generated. No configuration is needed. The external circuit must select between the information provided by the AAL1gator II.

Q26) When is Adaptive Clocking not recommended?

A26) The ATM Forum and ITU do not recommend adaptive clocking for voice because the effects of CDV cannot be removed and wander will always result.

Q27) How does the AAL1gator II scheduler work? Is it completely round robin, or does it use a "more intelligent" algorithm? Also, if it is completely round robin, how large of a CDV or CDVT is introduced by this device?

A27) The AAL1gator II uses a frame-based calendar queue service algorithm to schedule cells for transmission. A detailed explanation of the CSD circuit is provided in section 3.2 "Cell Service Decision (CSD) Circuit" on page 33 of [3]. The scheduler chosen for the AAL1gator II will provide relatively minimal CDV. However, the magnitude of the CDV introduced by this circuit depends on the configuration.

Q28) The AAL1gator II supports multiple VC services, but does it also support VP services? For example, can the AAL1gator II identify different services and extract OAM cells from different VCs?

A28) No.

Q29) Can the AAL1gator II generate a different OAM cell other than the current VC?

A29) Yes. Two OAM cells with arbitrary VPI/VCI values can be stored in the T_OAM_QUEUE cell buffers, available for transmission. When ready for transmission, the OAM cell has high priority and is sent with its own VPI/VCI, regardless of the content of any other cell.

Q30) Can the AAL1gator II be tied to a reference clock, similar to synchronizing SONET devices to a reference clock? Can this be done for all synchronous-locked designs?

A30) Yes. The AAL1gator II can be used within an all-synchronous network-clocked design for either structured or unstructured data formats.

Q31) In DS3 mode, does the AAL1gator II generate DS3 AIS signals when LOS is detected from the DS3 network, when cell loss is detected from the ATM network, and when the reassembly buffer underruns?

A31) The AAL1gator II cannot generate a DS3 AIS signal during any of the three following conditions. The following external workarounds are required for these conditions:

For DS3 LOS, the DS3 framer/LIU should detect the LOS condition and notify the microprocessor. The microprocessor can then mux an externally-generated DS3 AIS signal into the AAL1gator II RL_SER(0) pin.

For reassembly buffer underrun, the first step is to detect the underrun. The R_UNDERRUN bit in the R_LINE_STATE word of the R_QUEUE_TBL is not used in UDF-HS mode, so another method must be used to detect underrun of the Rx Data Buffer. To detect the underrun state, the microprocessor should periodically clear and poll the CELL_RECEIVED bit in the R_ERROR_STKY word of the R_QUEUE_TBL. If this bit is not set during a timeout period, the Rx Data Buffer has entered the underrun state. The timeout period can be calculated based on the R_CDVT value. When the microprocessor detects that the AAL1gator II has entered the underrun state, it can then configure the DS3 framer/LIU to transmit the DS3 AIS alarm signal.

During a reassembly buffer underrun, the AAL1gator II default is to send out the 16-bit pattern stored in R_COND_DATA_0 at address 8480h.

For cell loss, there is no simple workaround for inserting a DS3 AIS signal; however, a single cell would account for only 376 bits of a DS3 frame, which is only 8% of a DS3 frame, so actually inserting only a small portion of a DS3 AIS signal may not accomplish much, since downstream equipment may not recognize this DS3 frame fragment as a DS3 AIS.

Q32) How are data and signaling organized in the cell?

A32) The organization of the data and signaling complies to the following specifications:

- Signaling - follows ITU-T Recommendation I.363.1, given in [6] of the references. The AAL1gator II places the signaling into a series of nibbles following the data every E1 multiframe, or T1 Extended Super Frame (ESF), or pair of T1 Super Frame (SF) multiframes.

- Data - follows ITU-T Recommendation I.363.1, given in [6] of the references.

Q33) How does the AAL1gator II process the D4 frames?

A33) As far as AAL1gator II is concerned, the D4 framing is Superframe (SF) framing, a 12-frame T1 multiframe. No additional configuration is necessary when switching between SF and ESF formats. All that is needed is to setup the chip for T1 SDF-MF mode, and then, supply a multiframe pulse once every 12 frames (or multiple of 12 frames) on all sync inputs.

Q34) How do I get the AAL1gator II started?

A34) The following steps are required when starting the AAL1gator II:

- Zero out all memory.
- Load the “ROM Tables” into memory.
- Initialize “Composite Line Register”.
- Initialize 8 “Line Structure Mode Registers”.
- Set the CMD_REG_ATTN bit with the SW_RESET bit set in the CMDREG. This causes the AAL1gator II to write the DEVICE_REV memory location and read the COMP_LIN_REG and eight LIN_STR_MODE locations into internal registers.
- Take the chip out of software reset by clearing the SW_RESET bit in the CMDREG.
- Configure various queues (VCs) using “Tx/Rx Queue Tables” and “Rx Channel to Queue Table”.
- “Start” the VC’s to build cells.

For more information regarding the register fields, please refer to [3].

Q35) How do I “start” a VC?

A35) Use the Command Register (CMDREG) and T_ADD_QUEUE table for this purpose.

- Set a bit in the T_ADD_QUEUE table for each queue you want to start. Add queues one at a time for better CDV.
- Set the CSD_ATTN bit in the CMDREG. This causes the AAL1gator II to “OR” the T_ADD_QUEUE table with the frame zero entry of the Transmit Calendar Table, which schedules the first cell to be built.

Q36) How do I configure the AAL1gator II to support AMON, RMON, and ACS, as stated on "Circuit Interface Features" on page 1 of [3].

A36) The AAL1gator II can multicast AAL1 cells during cell generation. This results in two or more identical AAL1 cell streams, one of which can be configured to have a different ATM cell header, to facilitate steering a cell stream to monitoring, analysis, and troubleshooting equipment for an AMON, RMON, or ACS function. To accomplish this multicast, set the fields in the T_CHAN_ALLOC word (refer to "T_CHANNEL_ALLOC(15:0) Word Format" on page 138 of [3]) to overlapping values on different queues.

5 NOTES

6 CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com

PMC- 1991575 Issue date: February 2000