PM5372

TSE™

TRANSMISSION SWITCH ELEMENT

DATASHEET

Proprietary and Confidential

Released

Issue 7: November, 2001

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Revision History

Issue No.	Issue Date	Details of Change
7	November 2001	Changed signoff page. Fixed Initialization procedure instruction referencing addresses 0N83h, 0N8Bh, 0N93h, 0N9Bh Updated voltage limits on digital/LVDS pins in Absolute Maximum Ratings table. Deleted Ambient Temperature spec. Fixed 1.8V Supply Voltage spec. Added note to LCVI that it is change from no LCV to LCV that cause LCVI. A string of LCVs will only produce 1 LCVI . Consolidated power information (sequencing/filtering) to Power Information Section. Added power requirements section. Removed IDDOP for the power supplies from the D.C Characteristics table. Updated Thermal section. Thermal section now indicates device suitable industrial applications when used with heat sink. Updated LVDS Hot Swap Section. Added RC filter example schematic in Power Filtering section Updated TelecomBus Control Character Table
6	August 2001	Reworded DLCV description: Added warning of LCV counter saturation if DLCV set high, and clarified to indicate that inverted data would have valid and invalid 8B/10B characters as result of DLCV high Changed the name of the IDLESEL control signal ECHAR_OVWR, and made corresponding changes to the description of the ID[9:0] data bits Updated thermal information in sec 18 Revised power sequencing information, added max junction temp, Theta JA and Theta JC information, and chart of Theta JA vs. airflow Added sections for LVDS hot swap information, power down calculations, and trace length versus FIFO depth calculation Changed name of ETSE register bit in register 0NAAH to EACTIVE, hid references to TCBMODE in sec 9.2 and in description of register 0NB0H The device ID field is now “0001 instead of “0000” in register 0010H. The JTAG Version number has been changed to 1H in Table 16. The J0MASK bit has been added to registers 0N80H, 0N88H, 0N90H, 0N98H to support applications which require floating input links to remain activated. Added the IJ0RORDR bit to register 0NA2. Added the EJ0R0RDR bit to register ONAA.
5	March 2001	Added warning of LCV counter saturation if DLCV set high.in register descriptions Changed the name of the IDLESEL control signal to CHARACTER OVERWRITE, and made corresponding changes to the description of the ID[9:0] data bits

Issue No.	Issue Date	Details of Change
		Updated Reliability information (sec 23), and thermal information in sec 18. Revised power sequencing information, added max junction temp, Theta JA and Theta JC information, and chart of Theta JA vs. airflow Added sections for LVDS hot swap information, power down calculations, and trace length versus FIFO depth calculation . Changed name of ETSE register bit in register 0NAAH to EACTIVE, removed references to TCBMODE in sec 9.2 and in description of register 0NB0H Revised sec 9.2 and 9.2.1 to further de-document TeleCombus mode. Changed VIL(max) to 0.8V and VT+ to 2.2V based on characterization report. Revised Theta JA vs. Airflow table and Theta JC value with 560UBGA information. Updated operating power to 9.86W. Changed operating temperature range to T_C = -40°C to Tj=120C. Revised section on J0 Synchronization.
4	October 2000	Added instructions to check CSU lock status and to center transmit FIFOs in Section 12.5. Added Section 12.8. Added diagnostic note in TJ0FP pad description, amended TDI pad description to indicate there is no pull up resistor on the pad, removed part of RES/RESK pad description from datasheet, removed ATMSB, and DTMSB register bits from datasheet, redocumented clear behavior of indication register bits when WCIMODE=1, amended legal range of values for RJ0DLY: 1 to 9719, added explanatory text to BUSY register bits, removed RXLBSEL from datasheet, added functional timing diagram for page switching using SPSEL, IPSEL, and EPSEL register bits, corrected TJ0DLY description to indicate that the time to TJ0FP is TJ0DLY+2, amended DLCV register bit description, amended CENTER register bit description, to indicate that FIFO depth is 3-4 deep following centering operation, removed RDC mode from J0INS register bit description, corrected Boundary Scan Register Table: previously reverse ordered, and OEB_D(I) incorrectly identified as IO_CELL, updated System “J0” Timing diagram, added input pad tolerance, output pad overshoot, latchup current for RESK in Absolute Maximum Ratings table, added typical and max operating currents to D.C Characteristics table, corrected mechanical information table with respect to package thickness.
3	April 2000	Finalized pin out, register setting and functions
2	January 2000	Register Description modification, package and pinout information, added functional timing descriptions and scan test registers, changed tolerances of 1.8V supply to +-5%.
1	June 1999	Document created

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1 Features

- Implements a Time-Space-Time fabric with STS-1/AU-3 granularity
- Provides 64 ingress STS-12 links for a total of 64*12 = 768 STS-1 streams
- Provides 64 egress STS-12 links consisting of 768 STS-1 streams
- Supports non-blocking permutation switching of 768 STS-1 flows at STS-1 granularity
- Interfaces to STS-48 and STS-192 devices by aggregating 4 and 16 STS-12 flows respectively
- Supports multicast and broadcast of STS-1 streams
- Supports multi-plane (inverse multiplexed) switch architectures in conjunction with the PM5310 TBS™ device and PM7390 S/UNI®-MACH48
- Recovers clock and data at each ingress port, synchronizes with an internal 77.76 MHz clock, and produces egress streams with a common 777.6 MHz clock
- Detects and reports inactive or errored LVDS links via the microprocessor interface
- Supports two sets of switch settings and a controlled method of changing settings on STS-1 frame boundaries
- Supports multiple fabric architectures that range from 40 Gb/s (one device) to 160 Gb/s (four devices) in a single stage, and up to 2.5 Tb/s using multi-stage fabrics
- Ingress to egress STS-1 switching latency of approximately 840ns
- Supported by an efficient algorithm to compute control settings for all permutation loads for all supported fabric architectures. Algorithms are also available for multicast/broadcast allocation
- 1.8V CMOS core and 3.3V CMOS/LVDS input/output
- Requires no external RAMs or logic parts
- Provides a standard IEEE 1149.1 JTAG port
- Power Consumption of 8.3 W (typical)
- Packaged in a 560 pin 40mm by 40mm UltraBGA
- Supports a 16-bit microprocessor interface that is used to initialize the device, to write switch settings into on-chip control tables, and to monitor device performance

2 Applications

- Optical Cross Connects
- STS-1 Cross Connects
- Multi-service provisioning platforms
- SONET/SDH Add/Drop Multiplexers
- SONET/SDH Digital Cross Connects

3 References

1. ANSI – T1.105-1995, “Synchronous Optical Network (SONET) – Basic Description including Multiplex Structure, Rates, and Formats”, 1995

2. Bell Communications Research – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, Revision 2, January 1999

3. ITU, Recommendation G.707 – “Digital Transmission Systems – Terminal equipments – General”, March 1996

4. IEEE 802.3, “Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications”, Section 36.2, 1998

5. A.X. Widmer and P.A. Franaszek, “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code,” IBM Journal of Research and Development, Vol. 27, No 5, September 1983, pp 440-451

6. U.S. Patent No. 4,486,739, P.A. Franaszek and A.X. Widmer, “Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code,” December 4, 1984

7. IEEE Std 1596.3-1996, “IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)”, Approved March 21, 1996

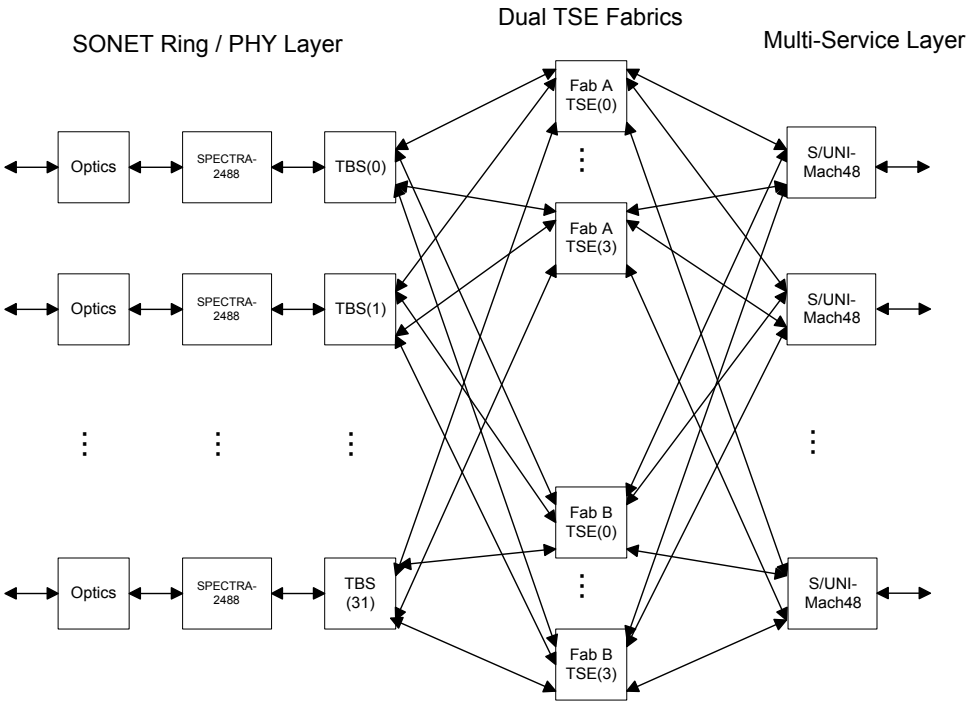
8. L.R. Ford, D.R. Fulkerson, “Flows in Networks’’, Maximum Cardinality Matchings in Bipartite Graphs

4 Application Examples

4.1 Motivating Applications

The PM5372 device is principally used in applications where cross-connecting of STS-1/AU-3 streams is required. Such applications include Add-Drop Multiplexers, STS-1 Cross-Connects, Optical Cross-Connects and Multi-Service Provisioning Platforms. Multi-Service Provisioning Platforms may also use an STS-1 cross-connect fabric to decouple the physical layer from the service layer. These products may integrate the DCS, ADM, switching, routing and broadcast capabilities. Part of an example architecture is illustrated in Figure 1. In this application, the cross-connect fabric consists of the TSE™ devices. The TSE devices support a Time-Space-Time switch architecture. Note that the following example has two complete TSE fabrics to support "1+1" fabric redundancy. The TSEs labeled *Fab A* compose the primary or working fabric. The TSEs labeled *Fab B* compose the secondary or protect fabric.

Figure 1 Representative TSE Application

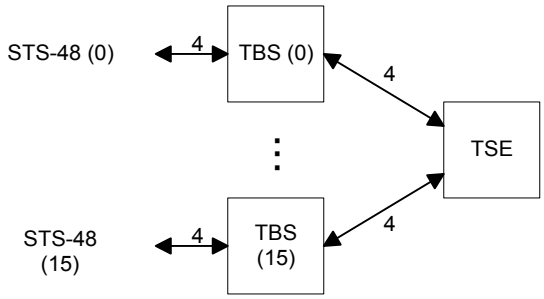


4.2 TSE Fabric Scaling

Independent of the application described above, the TSE is a general STS-1/AU-3 granularity fabric. As a fabric, it supports multiple architectures which scale in aggregate bandwidth from 40 Gb/s to 2.5 Tb/s (and larger, until limited by packaging concerns). Fabrics up to 160 Gb/s (i.e. 4 TSE devices) are supported in a single stage architecture. All fabrics are rearrangably non-blocking under all 100% loaded permutations of unicast traffic. Scaling of these TSE architectures is accomplished by two mechanisms: division of the fabric into multiple *planes*, and deepening of the fabric into multiple *stages*, where each stage may be of some power-of-two *height*, up to a maximum depending on the number of *stages*. A plane of TSEs within a fabric is defined as a group of connected TSEs unconnected to other TSE groups in the fabric. A multiple plane fabric requires distributing the connections of each serializer's I/O to all planes. The PM5310 TBS device with its four serial streams, can be used to implement a one, two, or four plane fabric.

Figure 2 illustrates the simplest TSE fabric. One TSE is connected to 16 full-duplex STS-48 loads via 16 TBS devices, providing an aggregate switch bandwidth of 40 Gb/s using one TSE and 16 TBS devices. The TBS devices in Figure 2 are used only to serialize Parallel TelecomBuses (P-TCB). Where OC-48 load devices have Serial TelecomBuses (S-TCB) interfaces, the TBS devices are unnecessary. Each STS-48 load is connected by four full-duplex links. The links from the Loads to the TBS devices are Parallel TelecomBuses (P-TCB), which are 4 * 8 bits at 77.76 MHz; all links to/from TSE devices are Serial TelecomBuses (S-TCB), which are 4 * 777.6 MHz LVDS links. In each *depth* one TSE fabric, the TSE devices form non-blocking Time-Space-Time fabrics.

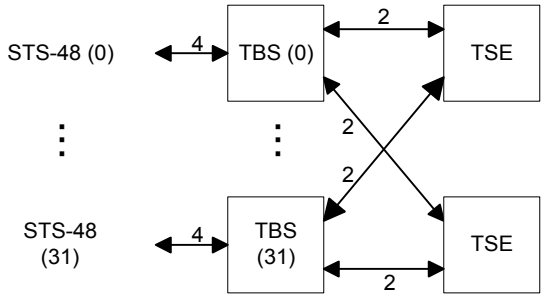
Figure 2 Fabric with One Plane of Depth One.



(STS-48 Sources = 16; Aggregate Bandwidth = 40 Gb/s; TSE Chip Count = 1; TBS Chip Count = 16)

Figure 3 illustrates a two-plane TSE fabric. Each of 32 full-duplex STS-48 loads on 32 TBS devices are connected by two LVDS links each to each of two TSE devices. The aggregate switch bandwidth is 80 Gb/s at a cost of two TSE devices and 32 TBS devices.

Figure 3 Fabric with Two Planes of Depth One.

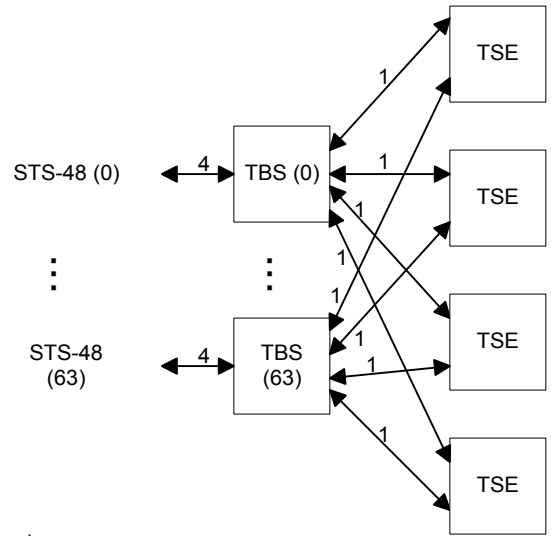


(STS-48 Sources = 32; Aggregate Bandwidth = 80 Gb/s; TSE Chip Count = 2; TBS Chip Count = 32)

In multi-plane TSE fabrics, TBS devices (or Load devices with equivalent S-TCB ports) perform the load balancing required by the inverse-multiplexed (i.e., multi-plane) TSE fabric.

Figure 4 illustrates a four-plane TSE fabric, representing the largest STS-48 fabric with a *depth* of one. Each of 64 full-duplex STS-48 loads on 64 TBS devices are connected by one LVDS link each to each of four TSE devices. The aggregate switch bandwidth is 160 Gb/s at a cost of four TSE devices and 64 TBS devices.

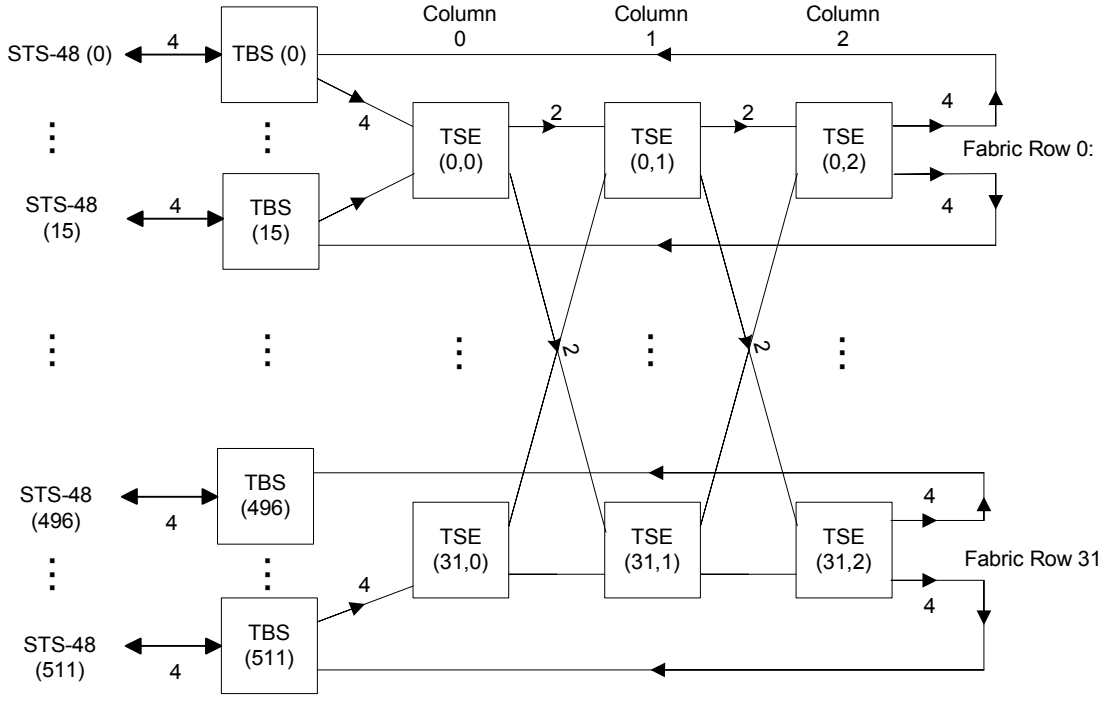
Figure 4 Fabric with Four Planes of Depth One.



(STS-48 Sources = 64; Aggregate Bandwidth = 160 Gb/s; TSE Chip Count = 4; TBS Chip Count = 64)

Figure 5 illustrates a three *stage* TSE fabric (*depth* = 3), with a *height* of 32. Each of 512 full-duplex STS-48 loads on 512 TBS devices are connected by four LVDS links each to a TSE. The receive ports for each TSE in Column 0 is connected to the 4 transmit LVDS links of 16 TBS devices, for example TSE(0,0) receives from TBS(0) through TBS(15). The transmit LVDS links of each TSE in column 0 fan out to all 32 TSEs in column 1, with 2 links per transmit/receive device pair. Transmit links for column 1 TSEs fan out similarly to column 2 TSEs. Transmit links of column 2 TSEs connect back to the TBS devices. Each column 2 TSE connects with 16 TBS devices, with 4 transmit LVDS links per device pair, for example TSE(0,2) transmits to TBS(0) through TBS(15).The aggregate switch bandwidth is 1,280 Gb/s using 96 TSE devices and 512 TBS devices.

Figure 5 Fabric with One Plane of Depth Three and Height Thirty-Two.

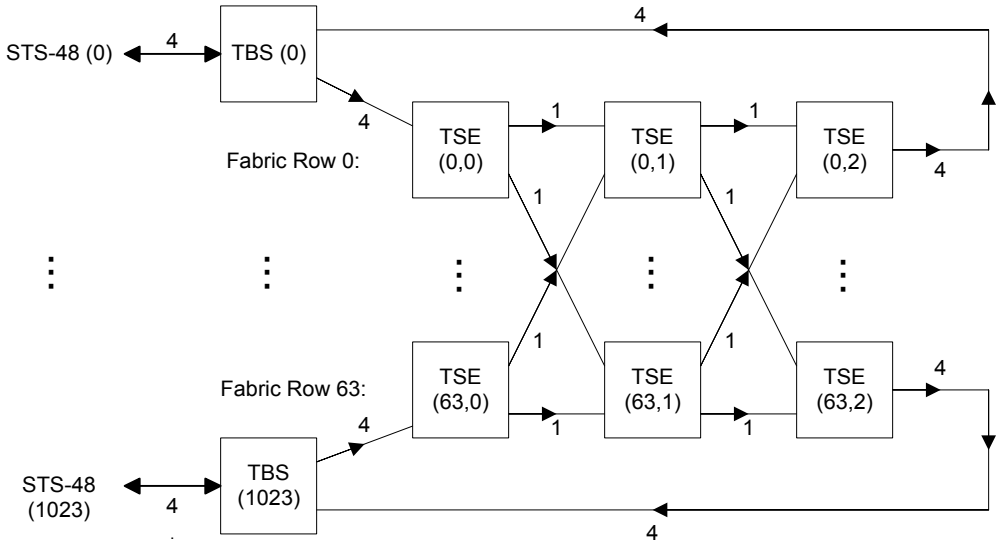


(STS-48 Sources = 512; Aggregate Bandwidth 1280 Gb/s; TSE Chip Count = 96; TBS Chip Count = 512)

Fabrics with *depth* greater than one have redundant internal time stages where TSE devices communicate with TSE devices. These redundant stages can be set to the identity mapping at startup, and then ignored during system operation.

Figure 6 illustrates the largest single-plane, three-stage fabric that has an aggregate bandwidth of 2560 Gb/s. The difference between this example and the one shown in Figure 5 is that this one extends the fabric to its full *height* of 64 TSE devices, whereas the fabric in Figure 5 limited the *height* to 32 TSE devices.

Figure 6 Fabric with One Plane of Depth Three and Height Sixty-Four



(STS-48 Sources = 1024; Aggregate Bandwidth = 2560 Gb/s; TSE Chip Count = 192; TBS Chip Count = 1024)

Larger TSE fabrics can be constructed in several ways by extending the architectural techniques shown above. In particular, the fabric shown in Figure 6 can be sliced into two or four *planes* (for STS-48), yielding fabrics up to 5120 Gb/s or 10,240 Gb/s, respectively. Furthermore, five stages of TSE devices can be used to build *deeper* fabrics (which permit greater *height*). Additionally, STS-192 fabrics with up to 16 planes of TSE devices can be constructed.

4.3 Redundant Fabrics

All of the TSE fabrics discussed above can be replicated to form dual redundant fabrics (as shown in Figure 1) for 1+1 Equipment Protection. Support for this feature is independent of the TSE - it requires error detection and dual ports in the feeder devices (e.g. TBS and the S/UNI-MACH48) as well as dual LVDS ports and failure switch-over logic in the TBS.

4.4 Non-STS-48 Loads

The TSE also supports both STS-12 and STS-192 loads. Each STS-12 device consumes only one parallel port (8 bits at 77.76 MHz) on a TBS or S/UNI-MACH48, whereas an STS-48 device consumes all four parallel ports (4 * 8 bits at 77.76 MHz) on a TBS or S/UNI-MACH48. Each STS-192 device consumes all four parallel ports on four TBS or S/UNI-MACH48 devices. The TSE/TBS (or S/UNI-MACH48) fabric sees only sets of STS-12 ports; as the TSE/TBS (S/UNI-MACH48) fabric supports any STS-1 to STS-1 permutation, the possible collection of STS-1s or STS-12s into STS-48s or STS-192s is immaterial to the fabric.

STS-192 loads permit TSE fabrics to grow to eight or sixteen planes, in which two or one STS-12 LVDS links are used to communicate between the STS-192 sources and the multiple planes of the fabric. In such fabrics, TSE devices can be used to gather/scatter traffic from lower aggregate rate devices into the multi-plane fabric (it is necessary that all such lower rate devices be able to communicate with all planes of any fabric).

Where STS-12 loads are used in multi-plane fabrics, the TBS is used to distribute and gather traffic across the multiple planes of the fabric. It is also possible to use an additional TSE to perform this STS-12 grooming function for up to 32 STS-12 sources.

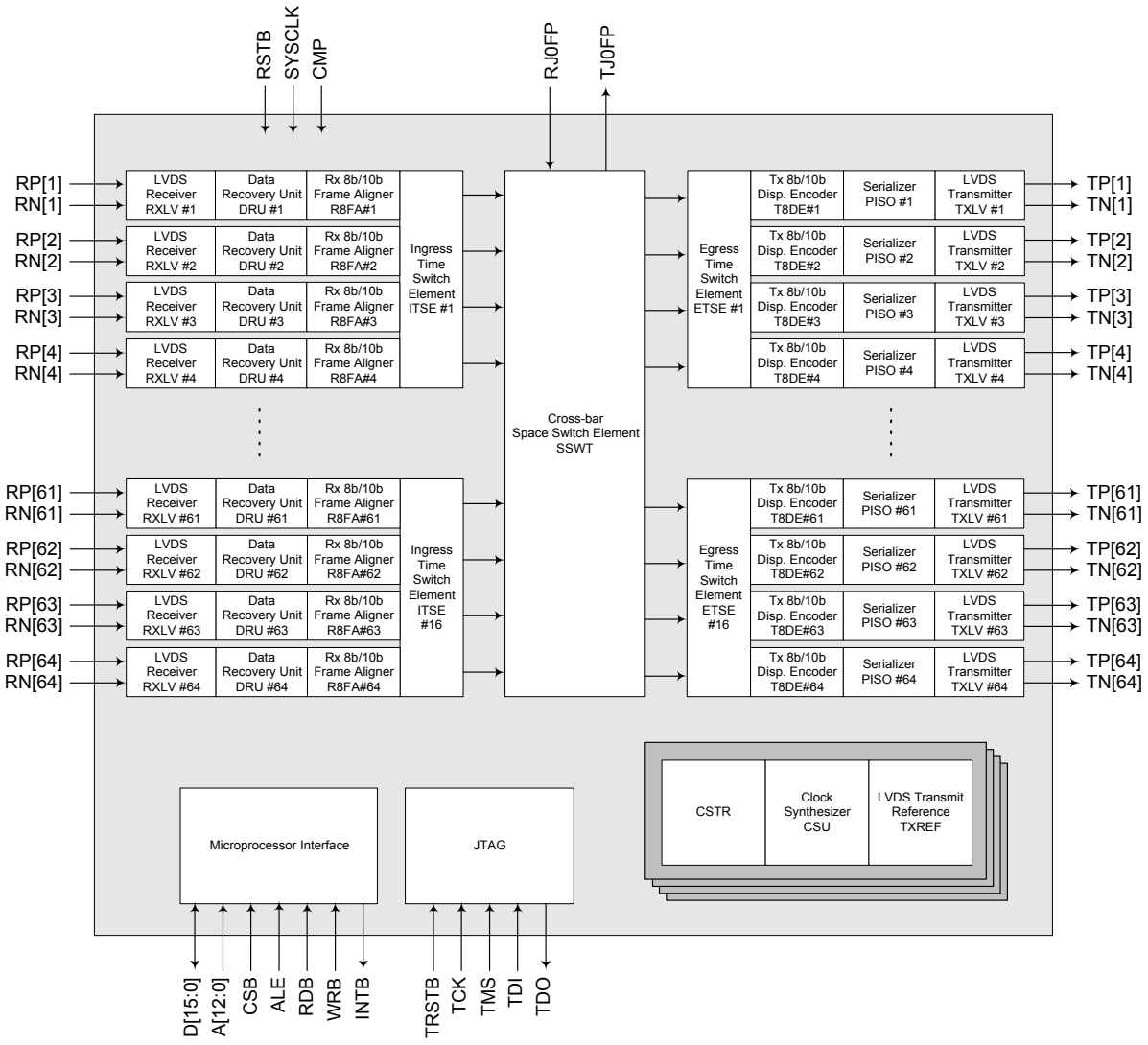
4.5 TSE Fabric Packaging

TSE fabrics can be packaged on PCBs in a variety of ways. The 777.6 MHz LVDS serial links are used to communicate between the port cards and the fabric cards. With careful PCB, connector, and back-plane design, no bus drivers will be required.

In such packaging of TSE fabrics, the concentration of all the TSE devices onto special fabric cards, and the non-involvement of the TBS devices in the switching function (they only serialize the TelecomBus and provide the fan-out to (possible) dual fabrics) permit all Automatic Protection Switching (APS) switch setting changes to be concentrated on the fabric cards; general connection establishment setup requires access to the connected TBS devices.

5 Block Diagram

Block Diagram



6 Description

The PM5372 TSE is a monolithic CMOS integrated circuit that performs STS-1 granularity cross-connecting.

The TSE receives data on 64 777.6 MHz LVDS links. Each link contains a STS-12/STM-4 stream. Bytes on the links are carried as 8B/10B characters. At minimum, each stream must include a 8B/10B special framing character to allow the TSE to character and frame align the stream. Additionally, the TSE can support a serial TelecomBus protocol, in which TelecomBus control signals are encoded as 8B/10B special characters. Data is switched through the TSE in 8B/10B code words. The TSE performs character and frame alignment on each stream. The TSE aligns data from multiple sources prior to switching the data. Data alignment is achieved by synchronizing the Frame Aligners in transmitting their aligned frame data. The TSE switches the STS-12 aligned data streams at STS-1 granularity through Time, Space, and then Time switch stages. The time switch stages perform timeslot interchange on the STS-12 data stream. The Space switch stage switches data from one STS-12 pipe to another. Each time slot is switched independently in the Space switch stage.

The TSE supports software configurable dual-page switch settings. This permits new switch settings to be stored in the inactive page of control settings, while the TSE operates on the active page of control settings. The TSE switches between control setting pages on STS-1 frame boundaries for hitless switchover through the device page select pin CMP. Block-by-block switchover is facilitated by software configurable page select bits.

The TSE transmits data on 64 777.6 MHz LVDS links. As on the receive side, a link contains a STS-12/STM-4 stream, encoded as 8B/10B characters. Prior to transmission and following switching, the TSE must reprocess each stream for correct 8B/10B disparity.

The function of the TSE is explained with respect to the block diagram. The flow in the block diagram is left-to-right. The left-most three units on each of the 64 STS-12 flows (LVDS Receiver, Data Recovery Unit, and Receive 8B/10B Frame Aligner) receive, decode and align the incoming flows. The Ingress Time Switch Elements perform timeslot interchange on the STS-12 stream. The Space Switch Element permits arbitrary permutations over space during each time step. The Egress Time Switch Elements implements another STS-12 timeslot interchange. The right-most three units (Transmit 8B/10B Disparity Encoder, Serializer, and LVDS Transmitter) re-encode, serialize and transmit the output streams. Switch control is distributed among the time and space switching modules. Switch control is organized into pages of control words which determine what permutations are implemented for each of the twelve STS-1 positions (in time) at each of the 64 ports (in space) for the switching stage. The Microprocessor Interface is used to initialize the TSE and to access the switch control settings. JTAG is supported on non-LVDS signal for board testing. The three modules (CSTR, CSU, and TXREF) provide clock and voltage references for the other LVDS modules.

Multiple fabric architectures can be supported, although the focus is on fabrics which are non-blocking under 100% permutation loads. The TSE also supports multicast capabilities.

7 Pin Diagram

The TSE is packaged in a custom Ultra-BGA with 560 balls.

Pin Diagram Top Left Corner

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
A	VSS	VSS	VSS	VSS	A[4]	A[7]	A[10]	VDDI	VSS	TP[50]	VSS	TP[52]	VSS	RN[51]	VSS	TP[53]	VSS	TP[56]	VSS
B	VSS	VDDO	VDDO	VDDO	A[5]	A[8]	A[11]	NC	TP[49]	TN[50]	NC	TN[52]	RN[50]	RP[51]	RN[52]	TN[53]	TP[55]	TN[56]	AVDL
C	VSS	VDDO	VDDO	VDDO	A[6]	VDDI	VDDI	NC	TN[49]	TP[51]	VDDI	RN[49]	RP[50]	AVDL	RP[52]	TP[54]	TN[55]	RN[53]	VDDI
D	VSS	VDDO	VDDO	VDDO	VDDI	A[9]	VDDI	ATB0[4]	ATB1[4]	TN[51]	AVDH	RP[49]	VDDI	VDDI	AVDH	TN[54]	VDDI	RP[53]	AVDH
E	A[3]	A[2]	A[0]	A[1]															
F	VSS	VDDI	NC	AVDH															
G	RESK	RES	RN[48]	RP[48]															
H	VSS	RN[47]	RP[47]	AVDL															
J	RN[46]	RP[46]	RN[45]	RP[45]															
K	VSS	TP[48]	TN[48]	AVDH															
L	TP[47]	TN[47]	TP[46]	TN[46]															
M	VSS	TP[45]	TN[45]	VDDI															
N	RN[44]	RP[44]	RN[43]	RP[43]															
P	VSS	RN[42]	RP[42]	AVDH															
R	VDDI	AVDL	RN[41]	RP[41]															
T	VSS	TP[44]	TN[44]	VDDI															
U	TP[43]	TN[43]	TP[42]	TN[42]															
V	TP[41]	TN[41]	CSU_AVDL	CSU_AVDL															
W	RN[40]	RP[40]	CSU_AVDL	CSU_AVDH															
Y	RN[38]	RP[38]	RN[39]	RP[39]															

Pin Diagram Top Right Corner

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
RN[54]	RN[56]	TP[57]	TP[59]	VSS	VDDI	VSS	RN[60]	VSS	TP[63]	VSS	RN[62]	VSS	RESK	VSS	A[12]/TRS	VSS	VSS	VSS	VSS	A
RP[54]	RP[56]	TN[57]	TN[59]	TP[60]	AVDL	RN[58]	RP[60]	TP[61]	TN[63]	TP[64]	RP[62]	RN[63]	RES	NC	SYSCLK	VDDO	VDDO	VDDO	VSS	B
RN[55]	CSU_AVDL	CSU_AVDL	TP[58]	TN[60]	RN[57]	RP[58]	RN[59]	TN[61]	TP[62]	TN[64]	RN[61]	RP[63]	RN[64]	NC	RJ0FP	VDDO	VDDO	VDDO	VSS	C
RP[55]	CSU_AVDH	CSU_AVDL	TN[58]	VDDI	RP[57]	AVDH	RP[59]	VDDI	TN[62]	AVDH	RP[61]	AVDL	RP[64]	AVDH	VDDI	VDDO	VDDO	VDDO	VSS	D
																CMP	CSB	TDO	VDDI	E
																WRB	ALE	RDB	VDDI	F
																VDDI	VDDI	TJ0FP	INTB	G
																ATB0[1]	NC	NC	VDDI	H
																ATB1[1]	TN[1]	TP[1]	VSS	J
																TN[3]	TP[3]	TN[2]	TP[2]	K
																AVDH	VDDI	NC	VSS	L
																RP[1]	RN[1]	TN[4]	TP[4]	M
																VDDI	RP[2]	RN[2]	VSS	N
																VDDI	AVDL	RP[3]	RN[3]	P
																AVDH	RP[4]	RN[4]	VSS	R
																TN[6]	TP[6]	TN[5]	TP[5]	T
																VDDI	TN[7]	TP[7]	VSS	U
																RP[5]	RN[5]	TN[8]	TP[8]	V
																AVDH	VDDI	AVDL	VSS	W
																RP[7]	RN[7]	RP[6]	RN[6]	Y

Pin Diagram Bottom Left Corner

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
AA	VSS	AVDL	VDDI	AVDH															
AB	TP[40]	TN[40]	RN[37]	RP[37]															
AC	VSS	TP[39]	TN[39]	VDDI															
AD	TP[37]	TN[37]	TP[38]	TN[38]															
AE	VSS	RN[36]	RP[36]	AVDH															
AF	RN[35]	RP[35]	AVDL	VDDI															
AG	VSS	RN[34]	RP[34]	VDDI															
AH	TP[36]	TN[36]	RN[33]	RP[33]															
AJ	VSS	NC	VDDI	AVDH															
AK	TP[34]	TN[34]	TP[35]	TN[35]															
AL	VSS	TP[33]	TN[33]	ATB1[3]															
AM	VDDI	NC	NC	ATB0[3]															
AN	D[14]	VDDI	VDDI	D[15]															
AP	VDDI	D[11]	D[13]	D[12]															
AR	VDDI	D[8]	D[10]	D[9]															
AT	VSS	VDDO	VDDO	VDDO	VDDI	AVDH	RP[32]	AVDL	RP[29]	AVDH	TN[30]	VDDI	RP[27]	AVDH	RP[25]	VDDI	TN[26]	CSU_AVDL	CSU_AVDH
AU	VSS	VDDO	VDDO	VDDO	RSTB	NC	RN[32]	RP[31]	RN[29]	TN[32]	TP[30]	TN[29]	RN[27]	RP[26]	RN[25]	TN[28]	TP[26]	CSU_AVDL	CSU_AVDL
AV	VSS	VDDO	VDDO	VDDO	TRSTB	NC	RES	RN[31]	RP[30]	TP[32]	TN[31]	TP[29]	RP[28]	RN[26]	AVDL	TP[28]	TN[27]	TN[25]	RP[24]
AW	VSS	VSS	VSS	VSS	NC	VSS	RESK	VSS	RN[30]	VSS	TP[31]	VSS	RN[28]	VSS	VDDI	VSS	TP[27]	TP[25]	RN[24]

Pin Diagram Bottom Right Corner

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
																CSU_AVDH	CSU_AVDL	RP[8]	RN[8]	AA
																CSU_AVDL	CSU_AVDL	TN[9]	TP[9]	AB
																TN[10]	TP[10]	TN[11]	TP[11]	AC
																VDDI	TN[12]	TP[12]	VSS	AD
																RP[9]	RN[9]	AVDL	VDDI	AE
																AVDH	RP[10]	RN[10]	VSS	AF
																RP[11]	RN[11]	RP[12]	RN[12]	AG
																VDDI	TN[13]	TP[13]	VSS	AH
																TN[14]	TP[14]	TN[15]	TP[15]	AJ
																AVDH	TN[16]	TP[16]	VSS	AK
																RP[13]	RN[13]	RP[14]	RN[14]	AL
																AVDL	RP[15]	RN[15]	VSS	AM
																RP[16]	RN[16]	RES	RESK	AN
																AVDH	NC	NC	VSS	AP
																VDDI	TMS	TCK	TDI	AR
RP[23]	AVDH	RP[21]	VDDI	TN[22]	AVDH	VDDI	VDDI	RP[17]	AVDH	TN[19]	ATB1[2]	ATB0[2]	D[7]	D[4]	D[1]	VDDO	VDDO	VDDO	VSS	AT
RN[23]	VDDI	RN[21]	TN[23]	TP[22]	RP[20]	AVDL	RP[18]	RN[17]	VDDI	TP[19]	TN[17]	NC	VDDI	D[5]	D[2]	VDDO	VDDO	VDDO	VSS	AU
RP[22]	AVDL	TN[24]	TP[23]	TN[21]	RN[20]	RP[19]	RN[18]	TN[20]	NC	TN[18]	TP[17]	NC	VDDI	D[3]	D[0]	VDDO	VDDO	VDDO	VSS	AV
RN[22]	VSS	TP[24]	VSS	TP[21]	VSS	RN[19]	VSS	TP[20]	VSS	TP[18]	VSS	VDDI	D[6]	VDDI	VDDI	VSS	VSS	VSS	VSS	AW

8 Pin Description

Table 1 Pin Description LVDS Ports (256 Signals)

Pin Name	Type	Pin No.	Function
RP[1] RN[1] RP[2] RN[2] RP[3] RN[3] RP[4] RN[4] RP[5] RN[5] RP[6] RN[6] RP[7] RN[7] RP[8] RN[8] RP[9] RN[9] RP[10] RN[10] RP[11] RN[11] RP[12] RN[12] RP[13] RN[13] RP[14] RN[14] RP[15] RN[15] RP[16] RN[16] RP[17] RN[17] RP[18] RN[18] RP[19] RN[19] RP[20] RN[20] RP[21] RN[21] RP[22] RN[22] RP[23] RN[23] RP[24]	Analog LVDS Input	M4 M3 N3 N2 P2 P1 R3 R2 V4 V3 Y2 Y1 Y4 Y3 AA2 AA1 AE4 AE3 AF3 AF2 AG4 AG3 AG2 AG1 AL4 AL3 AL2 AL1 AM3 AM2 AN4 AN3 AT12 AU12 AU13 AV13 AV14 AW14 AU15 AV15 AT18 AU18 AV20 AW20 AT20 AU20 AV21	**Receive Serial Data.** The differential receive serial data links (RP[64:1]/RN[64:1]) carry the receive SONET/SDH STS-12 frame data from upstream sources in bit serial format. Each differential pair RP[*X*]/RN[*X*] carries a constituent STS-12 stream. Data on RP[*X*]/RN[*X*] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit ‘a’ is transmitted first and the bit ‘j’ is transmitted last. All RP[*X*]/RN[*X*] differential pairs must be frequency locked and phase aligned (within a certain tolerance) to each other. RP[64:1]/RN[64:1] are nominally 777.6 MHz data streams. Unused RP[X]/RN[X] pad pairs can be left floating , or can be grounded. In either case the analog blocks (RXLV and the DRU) can be disabled to reduce power consumption. Tying one pin high and the corresponding pin of an input pair low will apply voltage across the internal termination resistor, which will increase system power consumption.

Pin Name	Type	Pin No.	Function
RN[24]		AW21	
RP[25]		AT25	
RN[25]		AU25	
RP[26]		AU26	
RN[26]		AV26	
RP[27]		AT27	
RN[27]		AU27	
RP[28]		AV27	
RN[28]		AW27	
RP[29]		AT31	
RN[29]		AU31	
RP[30]		AV31	
RN[30]		AW31	
RP[31]		AU32	
RN[31]		AV32	
RP[32]		AT33	
RN[32]		AU33	
RP[33]		AH36	
RN[33]		AH37	
RP[34]		AG37	
RN[34]		AG38	
RP[35]		AF38	
RN[35]		AF39	
RP[36]		AE37	
RN[36]		AE38	
RP[37]		AB36	
RN[37]		AB37	
RP[38]		Y38	
RN[38]		Y39	
RP[39]		Y36	
RN[39]		Y37	
RP[40]		W38	
RN[40]		W39	
RP[41]		R36	
RN[41]		R37	
RP[42]		P37	
RN[42]		P38	
RP[43]		N36	
RN[43]		N37	
RP[44]		N38	
RN[44]		N39	
RP[45]		J36	
RN[45]		J37	
RP[46]		J38	
RN[46]		J39	
RP[47]		H37	
RN[47]		H38	
RP[48]		G36	
RN[48]		G37	
RP[49]		D28	
RN[49]		C28	
RP[50]		C27	
RN[50]		B27	

Pin Name	Type	Pin No.	Function
RP[51] RN[51] RP[52] RN[52] RP[53] RN[53] RP[54] RN[54] RP[55] RN[55] RP[56] RN[56] RP[57] RN[57] RP[58] RN[58] RP[59] RN[59] RP[60] RN[60] RP[61] RN[61] RP[62] RN[62] RP[63] RN[63] RP[64] RN[64]		B26 A26 C25 B25 D22 C22 B20 A20 D20 C20 B19 A19 D15 C15 C14 B14 D13 C13 B13 A13 D9 C9 B9 A9 C8 B8 D7 C7	
TP[1] TN[1] TP[2] TN[2] TP[3] TN[3] TP[4] TN[4] TP[5] TN[5] TP[6] TN[6] TP[7] TN[7] TP[8] TN[8] TP[9] TN[9] TP[10] TN[10] TP[11] TN[11] TP[12] TN[12]	Analog LVDS Output	J2 J3 K1 K2 K3 K4 M1 M2 T1 T2 T3 T4 U2 U3 V1 V2 AB1 AB2 AC3 AC4 AC1 AC2 AD2 AD3	**Transmit Serial Data.** The differential transmit working serial data links (TP[64:1]/TN[64:1]) carry the transmit SONET/SDH STS-12 frame data to downstream sinks in bit serial format. Each differential pair carries a constituent STS-12 stream. Data on TP[*X*]/TN[*X*] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. All TP[*X*]/TN[*X*] differential pairs are frequency locked and phase aligned (within a certain tolerance) to each other. TP[64:1]/TN[64:1] are nominally 777.6 MHz data streams. Unused TP[X]/TN[X] pad pairs can be left unconnected.

Pin Name	Type	Pin No.	Function
TP[13]		AH2	
TN[13]		AH3	
TP[14]		AJ3	
TN[14]		AJ4	
TP[15]		AJ1	
TN[15]		AJ2	
TP[16]		AK2	
TN[16]		AK3	
TP[17]		AV9	
TN[17]		AU9	
TP[18]		AW10	
TN[18]		AV10	
TP[19]		AU10	
TN[19]		AT10	
TP[20]		AW12	
TN[20]		AV12	
TP[21]		AW16	
TN[21]		AV16	
TP[22]		AU16	
TN[22]		AT16	
TP[23]		AV17	
TN[23]		AU17	
TP[24]		AW18	
TN[24]		AV18	
TP[25]		AW22	
TN[25]		AV22	
TP[26]		AU23	
TN[26]		AT23	
TP[27]		AW23	
TN[27]		AV23	
TP[28]		AV24	
TN[28]		AU24	
TP[29]		AV28	
TN[29]		AU28	
TP[30]		AU29	
TN[30]		AT29	
TP[31]		AW29	
TN[31]		AV29	
TP[32]		AV30	
TN[32]		AU30	
TP[33]		AL38	
TN[33]		AL37	
TP[34]		AK39	
TN[34]		AK38	
TP[35]		AK37	
TN[35]		AK36	
TP[36]		AH39	
TN[36]		AH38	
TP[37]		AD39	
TN[37]		AD38	
TP[38]		AD37	
TN[38]		AD36	
TP[39]		AC38	

Pin Name	Type	Pin No.	Function
TN[39]		AC37	
TP[40]		AB39	
TN[40]		AB38	
TP[41]		V39	
TN[41]		V38	
TP[42]		U37	
TN[42]		U36	
TP[43]		U39	
TN[43]		U38	
TP[44]		T38	
TN[44]		T37	
TP[45]		M38	
TN[45]		M37	
TP[46]		L37	
TN[46]		L36	
TP[47]		L39	
TN[47]		L38	
TP[48]		K38	
TN[48]		K37	
TP[49]		B31	
TN[49]		C31	
TP[50]		A30	
TN[50]		B30	
TP[51]		C30	
TN[51]		D30	
TP[52]		A28	
TN[52]		B28	
TP[53]		A24	
TN[53]		B24	
TP[54]		C24	
TN[54]		D24	
TP[55]		B23	
TN[55]		C23	
TP[56]		A22	
TN[56]		B22	
TP[57]		A18	
TN[57]		B18	
TP[58]		C17	
TN[58]		D17	
TP[59]		A17	
TN[59]		B17	
TP[60]		B16	
TN[60]		C16	
TP[61]		B12	
TN[61]		C12	
TP[62]		C11	
TN[62]		D11	
TP[63]		A11	
TN[63]		B11	
TP[64]		B10	
TN[64]		C10	

Table 2 Pin Description TSE Control and Clocking (5 Signals)

Pin Name	Type	Pin No.	Function
SYSCLK	Input	B5	**System Clock.** The system clock signal (SYSCLK) is the master clock for the TSE device. SYSCLK must be a 77.76 MHz clock, with a nominal 50% duty cycle.
RJ0FP	Input	C5	**Receive Serial Interface Frame Pulse.** The receive serial interface frame pulse signal (RJ0FP) provides system timing for the receive serial interface. RJ0FP is supplied in common to all devices in a system containing one or more TSE devices. RJ0FP is set high once every 9720 SYSCLK cycles, or multiple thereof. A software configurable delay from RJ0FP is used to indicate that the J0 frame boundary 8B/10B characters have been delivered on all the receive serial data links (RP[64:1]/RN[64:1]) and are ready for processing by the time-space-time switching elements. RJ0FP is sampled on the rising edge of SYSCLK.
TJ0FP	Output	G2	**Transmit Serial Interface Frame Pulse.** The transmit serial interface frame pulse signal (TJ0FP) should be treated as an asynchronous output which can be used to give a rough estimate of when the J0 character is transmitted on the serial TelecomBus. TJ0FP is set high once every 9720 SYSCLK cycles. The pulse timing relative to the STS-12 frame is determined by the TJ0DLY register. It is recommended that the register is set so the TJ0FP pulse indicates that the J0 frame boundary 8B/10B character has been serialised out on all the transmit serial data links (TP[64:1]/TN[64:1]). TJ0FP is for diagnostic purposes only and is not intended as a reference for timing.
CMP	Input	E4	**Connection Memory Page.** The transmit connection memory page select signal (CMP) controls the selection of the connection memory page in TSE. In each block with connection memory, CMP is XORed with a software configurable page select bit. When the result is high, connection memory page 1 is selected. When the result is low, connection memory page 0 is selected. CMP is sampled on the rising edge of SYSCLK at the RJ0FP frame position. Refer to CMP functional timing for an indication of when a change to CMP takes effect.
RSTB	Input	AU35	**Reset Enable Bar.** The active low reset signal (RSTB) provides an asynchronous reset for the TSE. RSTB is a Schmitt triggered input with an integral pull-up resistor.

Table 3 Pin Description Microprocessor Interface (34 Signals)

Pin Name	Type	Pin No.	Function
CSB	Input	E3	**Chip Select Bar.** The active low chip select signal (CSB) controls microprocessor access to registers in the TSE device. CSB is set low during TSE Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses. If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.
RDB	Input	F2	**Read Enable Bar.** The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the TSE device. RDB is set low and CSB is also set low during TSE Microprocessor Interface Port

Pin Name	Type	Pin No.	Function
			register read accesses. The TSE drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	F4	**Write Enable Bar.** The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the TSE device. WRB is set low and CSB is also set low during TSE Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AN36 AN39 AP37 AP36 AP38 AR37 AR36 AR38 AT7 AW7 AU6 AT6 AV6 AU5 AT5 AV5	**Microprocessor Data Bus.** The bi-directional data bus, D[15:0] is used during TSE Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit.
A[12]/TRS A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	A5 B33 A33 D34 B34 A34 C35 B35 A35 E39 E38 E36 E37	**Microprocessor Address Bus.** The microprocessor address bus (A[12:0]) selects specific Microprocessor Interface Port registers during TSE register accesses. A[12] is also the Test Register Select (TRS) address pin and selects between normal and test mode register accesses. TRS is set high during test mode register accesses, and is set low during normal mode register accesses.
ALE	Input	F3	**Address Latch Enable.** The address latch enable signal (ALE) is active high and latches the address pins (A[12:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the TSE to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Open Drain Output	G1	**Interrupt Request Bar**. The active low interrupt enable signal (INTB) output goes low when an TSE interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

Table 4 Pin Description JTAG Port (5 Signals)

Pin Name	Type	Pin No.	Function
TCK	Input	AR2	**Test Clock.** The JTAG test clock signal (TCK) provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	AR3	**Test Mode Select.** The JTAG test mode select signal (TMS) controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	AR1	**Test Data Input.** The JTAG test data input signal (TDI) carries test data into the TSE via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. A 30 Kohm external pull-up resistor is recommended on this pin.
TDO	Tri-state	E2	**Test Data Output.** The JTAG test data output signal (TDO) carries test data out of the TSE via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	AV35	**Test Reset Bar.** The active low JTAG test reset signal (TRSTB) provides an asynchronous TSE test access port (TAP) controller reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. The TAP controller must be placed in the Test-Logic-Reset state after applying power to the device to guarantee correct device operation. This is easily accomplished by connecting TRSTB to the RSTB input and performing a device reset, but is not necessary if another method of resetting the TAP controller is implemented.

Table 5 Pin Description External Resistors (8 Signals)

Pin Name	Type	Pin No.	Function
RES[4] RES[3] RES[2] RES[1]	Analog Input	B7 G38 AV33 AN2	**Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between each positive resistor reference pin RES[I] and the corresponding Kelvin ground contact RESK[I].
RESK[4] RESK[3] RESK[2] RESK[1]	Analog Input	A7 G39 AW33 AN1	**Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between each positive resistor reference pin RES[I] and the corresponding Kelvin ground contact RESK[I].

Table 6 Pin Description Analog Test Bus (8 Signals)

Pin Name	Type	Pin No.	Function
ATB0[4] ATB0[3] ATB0[2] ATB0[1]	Analog	D32 AM36 AT8 H4	These pins are used for PMC testing only and should be directly connected to ground.
ATB1[4]	Analog	D31	These pins are used for PMC testing only and should be directly connected

Pin Name	Type	Pin No.	Function
ATB1[3] ATB1[2] ATB1[1]		AL36 AT9 J4	to ground.

Pin Description Digital Core Power (56 Signals)

Pin Name	Type	Pin No.	Function
VDDI[55:0]	Power	A15 A32 AA37 AC36 AD4 AE1 AF36 AG36 AH4 AJ37 AM39 AN37 AN38 AP39 AR39 AR4 AT13 AT14 AT17 AT24 AT28 AT35 AU11 AU19 AU7 AV7 AW25 AW5 AW6 AW8 C21 C29 C33 C34 D12 D16 D23 D26 D27 D33 D35 D5 E1 F1 F38	The digital core power pins (VDDI[55:0]) should be connected to a well-decoupled +1.8 V DC supply.

Pin Name	Type	Pin No.	Function
		G3 G4 H1 L3 M36 N4 P4 R39 T36 U4 W3	

Table 7 Pin Description Digital I/O Power (36 Signals)

Pin Name	Type	Pin No.	Function
VDDO[35:0]	Power	AT2 AT3 AT36 AT37 AT38 AT4 AU4 AU3 AU36 AU37 AU38 AU2 AV2 AV3 AV36 AV37 AV38 AV4 B2 B3 B36 B37 B38 B4 C2 C3 C36 C37 C38 C4 D2 D3 D36 D37 D38 D4	The digital I/O power pins (VDDO[35:0]) should be connected to a well-decoupled +3.3 V DC supply.

Table 8 Pin Description Analog Low Voltage Power (28 signals)

Pin Name	Type	Pin No.	Function
CSU_AVDL[11:0]	Power	AA3 AB3 AB4 AT22 AU21 AU22 C18 C19 D18 V36 V37 W37	The CSU analog power pins (CSU_AVDL[11:0]) should be connected to a +1.8 V DC supply. See filtering recommendations in section 15.3. Note that the CSU_AVDL is included in references to AVDL throughout this document unless otherwise noted.
AVDL[15:0]	Power	AA38 AE2 AF37 AM4 AT32 AU14 AV19 AV25 B15 B21 C26 D8 H36 P3 R38 W2	The analog power pins (AVDL[27:0]) should be connected to a +1.8 V DC supply. See filtering recommendations in section 15.3. Note that the CSU_AVDL is included in references to AVDL throughout this document unless otherwise noted.

Table 9 Pin Description Analog Power

Pin Name	Type	Pin No.	Function
AVDH[23:0]	Power	AA36 AE36 AF4 AJ36 AK4 AP4 AT11 AT15 AT19 AT26 AT30 AT34 D10 D14 D21 D25	The analog power pins (AVDH[23:0]) should be connected to a +3.3V DC supply. See filtering recommendations in section 15.3. Note that the CSU_AVDH is included in references to AVDH throughout this document unless otherwise noted.

Pin Name	Type	Pin No.	Function
		D29 D6 F36 K36 L4 P36 R4 W4	
CSU_AVDH [4:1]	Power	AA4 AT21 D19 W36	The CSU analog power quiet pins (CSU_AVDH[4:1]) should be connected to a +3.3V DC supply. See filtering recommendations in section 15.3. Note that the CSU_AVDH is included in references to AVDH throughout this document unless otherwise noted.

Table 10 Pin Description Ground (76 signals)

Pin Name	Type	Pin No.	Function
VSS[75:0]	Ground	W1 U1 T39 R1 P39 N1 M39 L1 K39 J1 H39 F39 D39 D1 C39 C1 B39 B1 AW9 AW4 AW39 AW38 AW37 AW36 AW34 AW32 AW30 AW3 AW28 AW26 AW24 AW2 AW19 AW17 AW15	The ground pins (VSS[75:0]) should be connected to GND.

Pin Name	Type	Pin No.	Function
		AW13 AW11 AW1 AV39 AV1 AU39 AU1 AT39 AT1 AP1 AM1 AL39 AK1 AJ39 AH1 AG39 AF1 AE39 AD1 AC39 AA39 A8 A6 A4 A39 A38 A37 A36 A31 A3 A29 A27 A25 A23 A21 A2 A16 A14 A12 A10 A1	

Table 11 Pin Description No Connect (20 signals)

Pin Name	Type	Pin No.	Function
NC[19:0]		AJ38 AM37 AM38 AP2 AP3 AU34 AU8	The No Connect pins (NC[19:0]) should be left floating.

Pin Name	Type	Pin No.	Function
		AV11 AV34 AV8 AW35 B29 B32 B6 C32 C6 F37 H2 H3 L2	
Total Pins All Pin Description Tables: 560			

Notes on Pin Descriptions

1. All inputs and bi-directionals present minimum capacitive loading. All non-LVDS inputs and bi-directionals except schmitt trigger inputs (RSTB, TRSTB and SYSCLK) operate at TTL logic levels
2. Inputs RSTB, ALE, TMS and TRSTB have internal pull-up resistors.
3. All outputs except the LVDS links have 8mA drive capability – this includes TJ0FP, TDO, INTB and D[15:0]).
4. The VDDI, AVDL, and CSU_AVDL power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the TSE. Similarly, the VDDO, AVDH, and CSU_AVDH power pins must be connected externally to avoid device malfunction or damage.
5. The VDDI, VDDO, AVDH, AVDL, CSU_AVDH, and CSU_AVDL power pins all share a common ground.

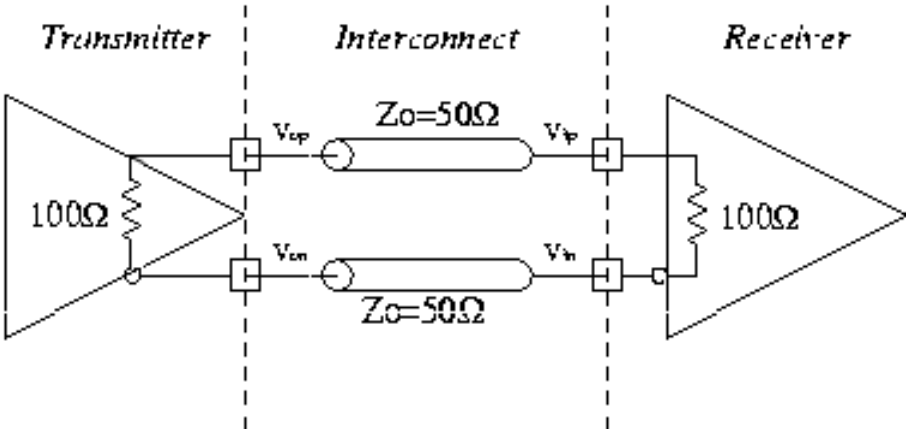
9 Functional Description

9.1 LVDS Overview

The LVDS family of cells allow the implementation of 777.6 Mb/s LVDS links. A reference clock of 77.76MHz is required. Four 777.6 Mb/s LVDS links form a high-speed serial TelecomBus interface for passing an STS-48 aggregate data stream.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated in Figure 7. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 7 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76MHz SYSCLK) and then serialized at the line rate on the LVDS output pins by a 777.6MHz clock synthesized from SYSCLK. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate. It is expected that the clock source of the transmitter is the same as the clock source of the receiver to ensure the data throughput at both ends of the link are identical.

Data is guaranteed to contain sufficient transition density to allow reliable operation of the data recovery units by 8B/10B block coding and decoding provided by the T8DE and R8FA blocks.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Specifically, a worst case eye opening of 0.7UI and 100mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors and up to 1m of backplane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately 350mV.

The LVDS system is comprised of the LVDS Receiver (RXLV), LVDS Transmitter (TXLV), Transmitter reference (TXREF), data recovery unit (DRU), parallel to serial converter (PISO), and Clock Synthesis Unit (CSU).

9.1.1 LVDS Receiver (RXLV)

The RXLV block is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Receiver according to the IEEE 1596.3-1996 LVDS Specification.

The RXLV block is the receiver in Figure 7, accepting up to 777.6 Mb/s LVDS signals from the transmitter, over RP[X]/RN[X] pins, amplifying them and converting them to digital signals, then passing them to a data recovery unit (DRU). Holding to the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than 100mV, with no hysteresis. These are LVDS receivers not CMOS. If a link is unused there is no electrical problem in leaving RP/RN floating (as opposed to a CMOS input). Power dissipation is the same regardless of whether the input is connected or not. No damage to the device will occur.

Unused links should be disabled in software. In this case the power for that link will be nearly 0mW. There is no requirement for how quickly this should be done. It simply results in lower power dissipation since circuitry will be shut down. This is not mandatory for the device to operate properly but is a good practice since it improves margins.

Hot-swapping is supported. The channel can be left enabled at all time and the device will sync up once the far end transmitter is connected. There will be no effect on other channels.

There are 64 instances of the RXLV block on the TSE.

9.1.2 LVDS Transmitter (TXLV)

The TXLV block is a 777.6 Mbit/s Low Voltage Differential Signaling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS Specification.

The TXLV accepts 777.6 Mbit/s differential data from a “parallel-in, serial-out” (PISO) circuit and then transmits the data off-chip as a low voltage differential signal on TP[X]/TN[X] pins.

The TXLV uses a reference current and voltage from the TXLVREF block to control the output differential voltage amplitude and the output common-mode voltage.

Unused links should be disabled in software. In this case the power for that link will be nearly 0mW. There is no requirement for how quickly this should be done. It simply results in lower power dissipation since circuitry will be shut down. This is not mandatory for the device to operate properly but is a good practice since it improves margins.

Hot-swapping is supported. The channel can be left enabled at all time and the device will sync up once the far end receiver is connected. There will be no effect on other channels.

There are 64 instances of the TXLV block on the TSE.

9.1.3 LVDS Transmit Reference (TXREF)

The TXLVREF provides an on-chip bandgap voltage reference (1.20V ±5%) and a precision current to the TXLV (777.6 Mb/s LVDS Transmitter) block's. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude.

The precision currents are generated by forcing the reference voltage across an external, off-chip 3.16kΩ (±1%) resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

There are four instances of the TXREF on the TSE.

9.1.4 Data Recovery Unit (DRU)

The DRU is a fully integrated data recovery and serial to parallel converter that can be used for 777.6 Mb/s NRZ data. 8B/10B block code is used to guarantee transition density for optimal performance.

The DRU recovers data and outputs a 10-bit word synchronized with a line rate divided-by-10 gated clock to allow frequency deviations between the data source and the local oscillator. The output clock is not a recovered clock. The DRU accumulates 10 data bits and outputs them on the next clock edge. If 10 bits are not available for transfer at a given clock cycle, the output clock is gated.

The DRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ±100ppm.

There are 64 instances of the DRU on the TSE.

9.1.5 Parallel to Serial Converter (PISO)

The PISO_1250 is a parallel-to-serial converter designed for high-speed transmit operation, supporting up to 777.6 Mb/s.

There are 64 instances of the PISO on the TSE.

9.1.6 Clock Synthesis Unit (CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for use by the transmitter.

There are 4 instances of the CSU on the TSE.

9.2 Receive 8B/10B Frame Aligner (R8FA)

The R8FA block performs 8B/10B character alignment and SONET STS-12 frame alignment on an unaligned bit stream received from a DRU block. A total of 64 R8FA blocks are instantiated in the TSE device.

R8Fas recovers 8B/10B character alignment by searching for the 8B/10B J0 frame alignment control character, which is used to identify the start of STS-12 flows. In addition, the TSE's STS-1 switching mechanism requires that all incoming STS-12s be mutually aligned within a certain tolerance. The 64 R8Fas in each TSE must present frame aligned 10b samples of aligned STS-12 flows to the switching stages.

The R8FA contains a FIFO to accommodate jitter, wander, and phase alignment differences between the timing domain of the receive LVDS links and the system clock timing domain. The FIFO also enables alignment of the multiple R8Fas in transmitting frames to the switching blocks.

Table 12 show the 8B/10B characters that the R8FA recognizes. All 8B/10B characters in Table 12 are reserved for TelecomBus control characters. The TSE doesn't do any processing on the TelecomBus control characters (with the exception of K28.5). The TSE will accepts incorrect disparity characters without signaling LCVs for those characters noted in the table.

Table 12 TelecomBus Control Characters

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Signal Description	Disparity Violation Allowed
K28.5	001111 1010	110000 0101	Transport J0 frame alignment	No
K28.0-	001111 0100	-	High-order path H3 byte, no negative justification event	Yes
K28.0+	-	110000 1011	High-order path PSO byte, positive	Yes

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Signal Description	Disparity Violation Allowed
			justification event	
K.28.4-	001111 0010	-	High-order path AIS	Yes
K28.6	001111 0110	110000 1001	High-order path J1 frame alignment	No
K27.7-	110110 1000		Low order path frame alignment #1	Yes
K27.7+		001001 0111	Low order path frame alignment #2	Yes
K28.7-	001111 1000		Low order path frame alignment #3	Yes
K28.7+		110000 0111	Low order path frame alignment #4	Yes
K29.7-	101110 1000		Low order path frame alignment #5	Yes
K29.7+		010001 0111	Low order path frame alignment #6	Yes
K30.7-	011110 1000		Low order path frame alignment #7	Yes
K30.7+		100001 0111	Low order path frame alignment #8	Yes
K23.7	111010 1000	000101 0111	Non low-order path payload overhead bytes (RSOH, MSOH, POH, R, V1, V2, V3, V4)	No
K.28.4+	-	110000 1101	Low-order path AIS	Yes

Microprocessor access to the R8FA allows the control and monitoring of its activities. Character and frame alignment status can be forced and monitored. 8B/10B line code violations are monitored in a performance monitor counter. LCV propagation is software configurable. LCVs are either mapped to a valid characters (D12.3) or forced to an LCV on the transmit link. FIFO errors due to improper RJ0DLY setting can also be monitored. The R8FA also provides reset, enable and test control over its associated DRU and RXLV analog blocks.

9.2.1 Character Alignment

The character alignment sub-block locates character boundaries in the incoming 8B/10B data stream. The aligner logic may be in one of two states, SYNC state and HUNT state. It uses the 8B/10B J0 frame alignment control character (K28.5+, K28.5-) used to encode the SONET/SDH J0 byte to locate character boundaries and to enter the SYNC state. It monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in IEEE std. 802.3.

The character alignment sub-block recognizes an extended set of 8B/10B control characters. The character decode block permits running disparity violations for these specific codes (as shown in Table 2): K28.0-, K28.0+, K28.4-, K28.4+, K27.7-, K27.7+, K 28.7-, K28.7+, K29.7-, K29.7+, K30.7-, K30.7+.

Excessive LCVs are used to transition the character alignment logic to the HUNT state.

Normal operation occurs when the character alignment sub-block is in the SYNC state. 8B/10B characters are written to the FIFO using the character alignment of the K28.5 character that caused entry to the SYNC state. Mimic K28.5 characters at other alignments are ignored. The receive data is constantly monitored for line code violations. If 5 or more LCVs are detected in a window of 15 characters, the character alignment sub-block transitions to the HUNT state. It will search all possible alignments in the receive data for the K28.5 character. In the mean time, the original character alignment is maintained until a K28.5 character is found. At that point, the character alignment is moved to this new location and the sub-block transitions to the SYNC state.

9.2.2 Frame Alignment

The frame alignment sub-block monitors the data from the character aligner sub-block for the J0 byte. An out of position J0 counter counts K28.5 characters that are out of position. The state of this counter conditions transitions in and out of the aligned state.

The block will frame align on the datastream if all the following conditions are satisfied:

1. There are two K28.5 characters in the datastream separate by 9720 SYSCLK cycles (125.0 us)

2. The R8FA was character aligned throughout that 125.0 us period

3. The out of position J0 counter is not = 3. Note that when out of frame alignment, this counter is cleared by 2 K28.5 characters separated by 125.0 us. So if this counter was 3, then the first 2 properly spaced K28.5 characters will clear the counter, and a third properly spaced K28.5 will satisfy condition 1.

Frame alignment is lost when either:

1. The block is forced out of frame alignment via software via the R8FA Control and Status FOFA register bit.

2. The R8FA loses character alignment (either due to software control or the 5 LCVs within 15 characters).

3. An out of position J0 count of 3 is reached.

The out of position J0 counter is incremented for each K28.5 character it encounters that is out of position with respect to the current frame alignment. The counter saturates at 3. When the block is frame aligned, the counter is cleared by an in position K28.5 character. When the block is not aligned, the counter is cleared by the next occurrence of next 2 K28.5 characters appearing separated by 125.0 us.

9.2.3 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domain of the associated receive LVDS link and that of the system clock (SYSCLK). Aligned 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the line clock rate. Data is read from the FIFO at every SYSCLK cycle.

9.2.4 Frame Counter

The Frame Counter sub-block keeps track of the octet identity of the outgoing data stream. It is initialized by a delayed version of the RJ0FP signal. It adjusts the read pointer so the J0 byte location in the FIFO is sampled at specific device wide event. All R8Fas are then aligned to transmit their J0 byte at this event.

9.3 Ingress Time Switch Element (ITSE)

The ITSE accepts STS-12-aligned cyclic groups of twelve STS-1 samples over twelve time steps from the R8Fas, and distributes these samples in an arbitrary Time permutation to the Space Switch Stage. The time permutation is determined by the contents of two switching control register sets or pages, each of which describes which STS-1 sample should be output during the i^{th} ($1 <= i <= 12$) STS-1 time slot. These control registers are accessible via the microprocessor bus. Selection of the switching page is determined by the device CMP pin, and on a per ITSE basis through the microprocessor control interface.

The ITSE can also be set in a BYPASS mode in which no switching is done. When in BYPASS mode, the latency of the ITSE is the same as when it is in DYNAMIC (switching) mode.

The ITSE is implemented as 2x12 STS-1 buffers, one to accumulate the incoming stream and the other to accept twelve STS-1s in parallel and then deliver these samples in the order specified by the switching control registers.

9.4 Space Switch Stage (SSWT)

The SSWT accepts fully aligned STS-12 streams from Ingress Time Stages at 77.76 MHz. The space stage implements a space switch for each of the twelve times in the cyclic STS-12 time structure, and delivers the STS-1 samples to the intended Egress LVDS Stages.

The SSWT is equivalent to a crossbar, with separate switch settings taken from control tables for each egress channel for each 8B/10B time period (77.76 MHz). Multicast is supported by permitting any number of output columns to take a sample from any input row at the same time.

The SSWT contains two sets or pages of control registers to control the switching function. Each set of control registers consists of twelve registers (one per time step) of six bits (to select among 64 sources) for each of 64 egress ports. These registers are accessible from the microprocessor interface; they constitute 2*12*6*64 = 9216 bits. Selection of the switching page is determined by the device CMP pin, or through the microprocessor control interface.

Another control register in the SSWT allows specification of the delay between the system synchronization pulse and J0 arrivals at the TSE receive analog blocks.

The SSWT is implemented by a set of input-selector muxes at each output.

9.5 Egress Time Switch Element (ETSE)

The ETSE accepts STS-12-aligned cyclic groups of twelve STS-1 samples over twelve time steps from the Space Switch, and outputs these samples in an arbitrary Time permutation to the Egress Ports. The time permutation is determined by the contents of two switching control register sets or pages, each of which describes which STS-1 sample should be output during the ith (1 <= i <=12) STS-1 time slot. These control registers are accessible via the microprocessor bus. Selection of the switching page is determined by the device CMP pin, and on a per ETSE basis through the microprocessor control interface.

The ETSE can also be set in a BYPASS mode in which no switching is done. When in BYPASS mode, the latency of the ETSE is the same as when it is in DYNAMIC (switching) mode.

The egress time stage is implemented as two 12 STS-1 buffers, one to accumulate the incoming stream and the other to accept twelve STS-1s in parallel and then deliver these samples in the order specified by the switching control settings.

9.6 Transmit 8B/10B Disparity Encoder (T8DE)

The T8DE block corrects the running disparity of an 8B/10B character stream and buffers data in a FIFO before transmission to the PISO block. A total of 64 T8DE blocks are instantiated in the TSE device.

The input data to the T8DE blocks originated from the R8FA blocks at which point they have correct running disparity. However, due to the time and space re-arrangement activities of the TSE, the running disparity is no longer consistent. The T8DE block inverts the 6B and 4B sub-characters to ensure correct running disparity.

The T8DE will not correct running disparity violations for these specific codes: K28.0-, K28.0+, K28.4-, K28.4+, K27.7-, K27.7+, K 28.7-, K28.7+, K29.7-, K29.7+, K30.7-, K30.7+, K23.7-, K23.7+.

The timing of egress LVDS signals requires that this block include a FIFO to cross from the internal TSE time domain to the time domain of the egress LVDS units. The clocks driving these two domains originate in the same master clock, but may have varying skew.

Microprocessor access to the T8DE allows the control and monitoring of its activities. FIFO status can be monitored and corrected. The T8DE can be configured to insert J0s into the datastream. The T8DE also provides reset, enable and test control over its associated PISO and TXLV analog blocks.

9.7 Clock Synthesis and Transmit Reference Digital Wrapper (CSTR)

The CSTR is an digital wrapper for the CSU and TXREF LVDS analog locks. It provides microprocessor access for resetting and disabling the CSU. It also monitors the lock state of the CSU on the system clock.

9.8 Fabric Latency

The flow of STS-1 samples from ingress LVDS to egress LVDS has variable latency, depending on the timing of the arriving LVDS stream, and the clock variation on the egress LVDS drivers. A reasonable estimate of the TSE's latency can be arrived at by making assumptions about the depths of the receive and transmit FIFOs: we assume the "J0" timing is set to maintain about 12 samples in the ingress FIFO; the egress FIFO is designed to be centered at 4 samples – so typically delay due to FIFOs will be 16 clock cycles. Maximum delay through the FIFOs can be 32 cycles. The R8FA imposes an additional 6 cycles of latency in addition to the ingress FIFO delay. The T8DE imposes 4 cycles of latency in addition to the egress FIFO delay. The latency through the time and space switch stages is 32 cycles. Data latency through the analog blocks is around 90 ns or 7 clock cycles with 5 cycles delay through the RX analog blocks and 2 cycles delay through the transmit analog blocks. By summing all the delays the typical latency of the TSE is 65 clock cycles or 836 ns. With worst case conditions in both FIFOs, latency rises to 81 clock cycles or 1044 ns.

9.9 JTAG Support

The TSE provides JTAG support for testing device interconnection on a PC board.

9.10 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the TSE to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the TSE. The register set is accessed as shown in the Register Memory Map table below. Addresses that are not shown are not used and must be treated as Reserved.

The ports are organized into 16 Port Sets. A Port Register Set is specified for each Port Set. Registers for Port Register Set 1 are specified in the register memory map. For the remaining Port Register Sets, only the range of registers is specified. As with Port Register Set 1 not all addresses within a range correspond to actual registers. To obtain a corresponding register for port set N+1, take the register address for Port Register Set 1 and replace address bits A[11:8] with N. The grouping of the Receive and Transmit LVDS ports to a port register set is defined as follows: Port Register Set N+1 controls blocks associated with receive LVDS links RP[4N+4:4N+1]/RN[4N+4:4N+1]. This includes RXLV, DRU, and R8FA blocks 4N+4 down to 4N+1, and ITSE block N+1. Port Register Set N+1 controls blocks associated with transmit LVDS links TP[4N+4:4N+1]/TN[4N+4:4N+1]. This includes ETSE block N+1, T8DE, PISO, and TXLV blocks 4N+4 down to 4N+1.

Register Memory Map

Address	Register
0000	TSE Master Reset
0001	TSE Master Clock Activity and Accumulation Trigger
0002	TSE Master Configuration
0003	TSE Master Interrupt Block Identifier
0004	TSE Master R8FA Interrupt Source #1
0005	TSE Master R8FA Interrupt Source #2
0006	TSE Master R8FA Interrupt Source #3
0007	TSE Master R8FA Interrupt Source #4
0008	TSE Master T8DE Interrupt Source #1
0009	TSE Master T8DE Interrupt Source #2
000A	TSE Master T8DE Interrupt Source #3
000B	TSE Master T8DE Interrupt Source #4
000C	TSE Master ITSE Interrupt Source
000D	TSE Master ETSI Interrupt Source
000E	TSE Master CSTR Interrupt Source
000F	TSE Master User Defined
0010	TSE Master JTAG ID High
0011	TSE Master JTAG ID Low

Address	Register
0012-001F	Reserved
0020	CSTR #1 Control
0021	CSTR #1 Interrupt Enable and CSU Lock Status
0022	CSTR #1 Interrupt Indication
0023	CSTR #1 Reserved
0024	CSTR #2 Control
0025	CSTR #2 Configuration and Status
0026	CSTR #2 Interrupt Status
0027	CSTR #2 Reserved
0028	CSTR #3 Control
0029	CSTR #3 Configuration and Status
002A	CSTR #3 Interrupt Status
002B	CSTR #3 Reserved
002C	CSTR #4 Control
002D	CSTR #4 Configuration and Status
002E	CSTR #4 Interrupt Status
002F	CSTR #4 Reserved
0030-003F	Reserved
0040	SSWT RJ0FP Delay
0041	SSWT Indirect Control Address
0042	SSWT Indirect Control Data
0043	SSWT Interrupt Enable
0044	SSWT Interrupt Status
0045-0046	SSWT Reserved
0047	SSWT TJ0FP Delay
0048 – 007F	Reserved
0080-00FF	**Port Register Set 1 – ports 1-4**
0080	Port Register Set 1: R8FA #1 Control and Status
0081	Port Register Set 1: R8FA #1 Interrupt Status
0082	Port Register Set 1: R8FA #1 LCV Count
0083	Port Register Set 1: RXLV #1 and DRU #1 Control
0084 – 0087	Port Register Set 1: Reserved
0088	Port Register Set 1: R8FA #2 Control and Status
0089	Port Register Set 1: R8FA #2 Interrupt Status
008A	Port Register Set 1: R8FA #2 LCV Count
008B	Port Register Set 1: RXLV #2 and DRU #2 Control
008C – 008F	Port Register Set 1: Reserved

Address	Register
0090	Port Register Set 1: R8FA #3 Control and Status
0091	Port Register Set 1: R8FA #3 Interrupt Status
0092	Port Register Set 1: R8FA #3 LCV Count
0093	Port Register Set 1: RXLV #3 and DRU #3 Control
0094 – 0097	Port Register Set 1: Reserved
0098	Port Register Set 1: R8FA #4 Control and Status
0099	Port Register Set 1: R8FA #4 Interrupt Status
009A	Port Register Set 1: R8FA #4 LCV Count
009B	Port Register Set 1: RXLV #4 and DRU #4 Control
009C – 009F	Port Register Set 1: Reserved
00A0	Port Register Set 1: ITSE #1 Indirect Address
00A1	Port Register Set 1: ITSE #1 Indirect Data
00A2	Port Register Set 1: ITSE #1 Configuration
00A3	Port Register Set 1: ITSE #1 Interrupt Status
00A4 – 00A7	Port Register Set 1: Reserved
00A8	Port Register Set 1: ETSE #1 Indirect Address
00A9	Port Register Set 1: ETSE #1 Indirect Data
00AA	Port Register Set 1: ETSE #1 Configuration
00AB	Port Register Set 1: ETSE #1 Interrupt Status
00AC – 00AF	Port Register Set 1: Reserved
00B0	Port Register Set 1: T8DE #1 Control and Status
00B1	Port Register Set 1: T8DE #1 Interrupt Status
00B2 – 00B3	Port Register Set 1: T8DE #1 Reserved
00B4	Port Register Set 1: T8DE #1 Test Pattern
00B5	Port Register Set 1: TXLV #1and PISO #1 Control
00B6-00B7	Port Register Set 1: Reserved
00B8	Port Register Set 1: T8DE #2 Control and Status
00B9	Port Register Set 1: T8DE #2 Interrupt Status
00BA – 00BB	Port Register Set 1: T8DE #2 Reserved
00BC	Port Register Set 1: T8DE #2 Test Pattern
00BD	Port Register Set 1: TXLV #2 and PISO #2Control
00BE- 00BF	Port Register Set 1: Reserved
00C0	Port Register Set 1: T8DE #3 Control and Status
00C1	Port Register Set 1: T8DE #3 Interrupt Status
00C2 – 00C3	Port Registers Set 1: T8DE #3 Reserved
00C4	Port Register Set 1: T8DE #3 Test Pattern
00C5	Port Register Set 1: TXLV #3 and PISO #3 Control

Address	Register
00C6-00C7	Port Register Set 1: Reserved
00C8	Port Register Set 1: T8DE #4 Control and Status
00C9	Port Register Set 1: T8DE #4 Interrupt Status
00CA – 00CB	Port Register Set 1: T8DE #4 Reserved
00CC	Port Register Set 1: T8DE #4 Test Pattern
00CD	Port Register Set 1: TXLV #4 and PISO #4 Control
00CE – 00FF	Port Register Set 1: Reserved
0100-017F	Reserved
0180-01FF	**Port Register Set 2– ports 5-8**
0200-027F	Reserved
0280-02FF	**Port Register Set 3– ports 9-12**
0300-037F	Reserved
0380-03FF	**Port Register Set 4– ports 13-16**
0400-047F	Reserved
0480-04FF	**Port Register Set 5– ports 17-20**
0500-057F	Reserved
0580-05FF	**Port Register Set 6– ports 21-24**
0600-067F	Reserved
0680-06FF	**Port Register Set 7– ports 25-28**
0700-077F	Reserved
0780-07FF	**Port Register Set 8– ports 29-32**
0800-087F	Reserved
0880-08FF	**Port Register Set 9– ports 33-36**
0900-097F	Reserved
0980-09FF	**Port Register Set 10– ports 37-40**
0A00-0A7F	Reserved
0A80-0AFF	**Port Register Set 11– ports 41-44**
0B00-0B7F	Reserved
0B80-0BFF	**Port Register Set 12– ports 45-48**
0C00-0C7F	Reserved
0C80-0CFF	**Port Register Set 13– ports 49-52**
0D00-0D7F	Reserved
0D80-0DFF	**Port Register Set 14– ports 53-56**
0E00-0E7F	Reserved
0E80-0EFF	**Port Register Set 15– ports 57-60**
0F00-0F7F	Reserved
0F80-0FFF	**Port Register Set 16– ports 61-64**

Address	Register
1000 – 1FFF	Reserved for Test

Notes on Register Memory Map:

1. For all register accesses, CSB must be set low.
2. Addresses that are not shown must be treated as Reserved.
3. A[12] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

10 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the TSE. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[12]) is low.

Notes on Normal Mode Register Bits:

1. Unused bits have no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.
2. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.
3. Writing into read-only normal mode register bit locations does not affect TSE operation unless otherwise noted.
4. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the TSE operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register 0000H: TSE Master Reset, Identity

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register allows separate software reset of digital and analog circuitry on the TSE.

ARESET

The ARESET bit allows the analog circuitry in the TSE to be reset under software control. If the ARESET bit is a logic one, all the TSE analog circuitry is held in reset. ARESET must be held at logic 1 for at least 100us to ensure correct reset of the CSU. This bit is not self-clearing. Therefore, a logic zero must be written to bring the TSE out of reset. Holding the TSE in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET bit, thus negating the analog software reset.

DRESET

The DRESET bit allows the digital circuitry in the TSE to be reset under software control. If the DRESET bit is a logic one, all the TSE digital circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the TSE out of reset. Holding the TSE in a reset state places it into a low power, digital stand-by mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 0001H: TSE Master Clock Activity and Accumulation Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	TIP	X
Bit 0	R	SYSCLKA	X

This register provides activity monitoring on the SYSCLK TSE input. Writing to this register also initiates a transfer of counts from the performance monitor accumulation registers to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent saturation of counters, accumulation intervals should be regular. The bits in this register are not affected by write accesses.

SYSCLKA

The SYSCLK active (SYSCLKA) bit monitors for low to high transitions on the SYSCLK clock input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

TIP

The Transfer in Progress (TIP) initiates and monitors the state of R8FA LCV count performance meter register transfers. Writing (any value) to this register initiates a device-wide accumulation interval transfer and loads all the performance meter registers in the TSE. TIP is set to logic one while the transfer is in progress, and is set to a logic zero when the transfer is complete. Also if individual performance meter register transfers are initiated (by writing directly to the individual register), TIP will monitor the state of those transfers as well. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0002H: TSE Master Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved[8]	1
Bit 14	R/W	WCIMODE	0
Bit 13	R/W	ILCV	0
Bit 12		Unused	X
Bit 11	R/W	Reserved[7]	0
Bit 10	R/W	Reserved[6]	1
Bit 9	R/W	Reserved[5]	0
Bit 8	R/W	ETSE_MODE	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved[4]	0
Bit 4	R/W	Reserved[3]	0
Bit 3	R/W	Reserved[2]	0
Bit 2	R/W	Reserved[1]	0
Bit 1	R/W	Reserved[0]	0
Bit 0	R/W	ITSE_MODE	0

This register configures the function of the 8B/10B encoders, decoder and the time switch blocks in the TSE.

ITSE_MODE:

The ITSE mode bit (ITSE_MODE) control the function of ITSE blocks #1 through #16. If ITSE_MODE is set to low, ITSE switching is controlled by the contents of the selected connection memory. If ITSE_MODE is set high, the ITSE performs no switching function.

Reserved[8:0]

The Reserved[8:0] bits must be set to the indicated default value for correct operation of the TSE device.

ETSE_MODE

The ETSE mode bit (ETSE_MODE) control the function of ETSE blocks #1 through #16. If ETSE_MODE is set to low, ITSE switching is controlled by the contents of the selected connection memory. If ETSE_MODE is set high, the ETSE performs no switching function.

ILCV

The insert LCV bit (ILCV) controls the insertion of illegal 8B/10B characters in the datastream. If a Line Code Violation is detected by an R8FA, and ILCV is logic 1, the TSE will overwrite the character with the LCV with an illegal character (1110110100 or 0001001011). The insertion of an illegal character prevents LCVs due to disparity errors being masked by the T8DE. If ILCV is logic 0, LCV characters are masked, and replaced with a legal data character, D12.3. Masking LCVs prevents floating links from disrupting framing

WCIMODE

The write clear interrupt mode bit (WCIMODE) controls whether interrupt status bits are cleared on a read or a write to the corresponding register. If WCIMODE is logic 1, all interrupt status bits in interrupt status register are cleared when a logic high is written to the corresponding interrupt bit. Otherwise, interrupt status bits are cleared on a register read.

Register 0003H: TSE Master Interrupt Block Identifier

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	ID_CSTRI	X
Bit 4	R	ID_SSWTI	X
Bit 3	R	ID_ETSEI	X
Bit 2	R	ID_ITSEI	X
Bit 1	R	ID_T8DEI	X
Bit 0	R	ID_R8FAI	X

This register allows the source of an active interrupt to be identified down to the block function level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

ID_R8FAI

The ID_R8FAI bit is high when an interrupt request is active from one of the 64 Receive 8B/10B Frame Aligner (R8FA) blocks. The particular R8FA block which set the interrupt can be identified by reading the TSE R8FA Interrupt Source registers. The ID_R8FAI bit is cleared when the interrupt is cleared.

ID_T8DEI

The ID_T8DEI bit is high when an interrupt request is active from one of the 64 Transmit 8B/10B Disparity Encoder (T8DE) blocks. The particular T8DE block which set the interrupt can be identified by reading the TSE T8DE Interrupt Source registers. The ID_T8DEI bit is cleared when the interrupt is cleared.

ID_ITSEI

The ID_ITSEI bit is high when an interrupt request is active from one of the 16 Ingress Time Switch Element (ITSE) blocks. The particular ITSE block which set the interrupt can be identified by reading the TSE ITSE Interrupt Source registers. The ID_ITSEI bit is cleared when the interrupt is cleared.

ID_ETSEI

The ID_ETSEI bit is high when an interrupt request is active from one of the 16 Egress Time Switch Element (ETSE) blocks. The particular ETSE block which set the interrupt can be identified by reading the TSE ETSE Interrupt Source registers. The ID_ETSEI bit is cleared when the interrupt is cleared.

ID_SSWTI

The ID_SSWTI bit is high when an interrupt request is active from the Space Switch Stage block. The ID_SSWTI bit is cleared when the interrupt is cleared.

ID_CSTRI

The ID_CSTRI bit is high when an interrupt request is active from one of the CSTR blocks and indicates a change in the lock status of a CSU. The particular CSTR block which set the interrupt can be identified by reading the TSE CSTR Interrupt Source registers. The ID_CSTRI bit is cleared when the interrupt is cleared.

Reserved

The Reserved bit must be set to the indicated default value for proper function of the TSE device.

Register 0004H: TSE Master R8FA Interrupt Source #1

Bit	Type	Function	Default
Bit 15	R	R8FAI[16]	X
Bit 14	R	R8FAI[15]	X
Bit 13	R	R8FAI[14]	X
Bit 12	R	R8FAI[13]	X
Bit 11	R	R8FAI[12]	X
Bit 10	R	R8FAI[11]	X
Bit 9	R	R8FAI[10]	X
Bit 8	R	R8FAI[9]	X
Bit 7	R	R8FAI[8]	X
Bit 6	R	R8FAI[7]	X
Bit 5	R	R8FAI[6]	X
Bit 4	R	R8FAI[5]	X
Bit 3	R	R8FAI[4]	X
Bit 2	R	R8FAI[3]	X
Bit 1	R	R8FAI[2]	X
Bit 0	R	R8FAI[1]	X

This register is used to indicate interrupts generated from the R8FA blocks #1 through #16.

R8FAI[16:1]

The R8FA #*X* interrupt event indication (R8FAI[X]) transitions to logic 1 when a hardware interrupt event is sourced from R8FA #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0005H: TSE Master R8FA Interrupt Source #2

Bit	Type	Function	Default
Bit 15	R	R8FAI[32]	X
Bit 14	R	R8FAI[31]	X
Bit 13	R	R8FAI[30]	X
Bit 12	R	R8FAI[29]	X
Bit 11	R	R8FAI[28]	X
Bit 10	R	R8FAI[27]	X
Bit 9	R	R8FAI[26]	X
Bit 8	R	R8FAI[25]	X
Bit 7	R	R8FAI[24]	X
Bit 6	R	R8FAI[23]	X
Bit 5	R	R8FAI[22]	X
Bit 4	R	R8FAI[21]	X
Bit 3	R	R8FAI[20]	X
Bit 2	R	R8FAI[19]	X
Bit 1	R	R8FAI[18]	X
Bit 0	R	R8FAI[17]	X

This register is used to indicate interrupts generated from the R8FA blocks #17 through #32.

R8FAI[32:17]

The R8FA #*X* interrupt event indication (R8FAI[X]) transitions to logic 1 when a hardware interrupt event is sourced from R8FA #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0006H: TSE Master R8FA Interrupt Source #3

Bit	Type	Function	Default
Bit 15	R	R8FAI[48]	X
Bit 14	R	R8FAI[47]	X
Bit 13	R	R8FAI[46]	X
Bit 12	R	R8FAI[45]	X
Bit 11	R	R8FAI[44]	X
Bit 10	R	R8FAI[43]	X
Bit 9	R	R8FAI[42]	X
Bit 8	R	R8FAI[41]	X
Bit 7	R	R8FAI[40]	X
Bit 6	R	R8FAI[39]	X
Bit 5	R	R8FAI[38]	X
Bit 4	R	R8FAI[37]	X
Bit 3	R	R8FAI[36]	X
Bit 2	R	R8FAI[35]	X
Bit 1	R	R8FAI[34]	X
Bit 0	R	R8FAI[33]	X

This register is used to indicate interrupts generated from the R8FA blocks #33 through #48.

R8FAI[48:33]

The R8FA #*X* interrupt event indication (R8FAI[X]) transitions to logic 1 when a hardware interrupt event is sourced from R8FA #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0007H: TSE Master R8FA Interrupt Source #4

Bit	Type	Function	Default
Bit 15	R	R8FAI[64]	X
Bit 14	R	R8FAI[63]	X
Bit 13	R	R8FAI[62]	X
Bit 12	R	R8FAI[61]	X
Bit 11	R	R8FAI[60]	X
Bit 10	R	R8FAI[59]	X
Bit 9	R	R8FAI[58]	X
Bit 8	R	R8FAI[57]	X
Bit 7	R	R8FAI[56]	X
Bit 6	R	R8FAI[55]	X
Bit 5	R	R8FAI[54]	X
Bit 4	R	R8FAI[53]	X
Bit 3	R	R8FAI[52]	X
Bit 2	R	R8FAI[51]	X
Bit 1	R	R8FAI[50]	X
Bit 0	R	R8FAI[49]	X

This register is used to indicate interrupts generated from the R8FA blocks #49 through #64.

R8FAI[64:49]

The R8FA #*X* interrupt event indication (R8FAI[X]) transitions to logic 1 when a hardware interrupt event is sourced from R8FA #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0008H: TSE Master T8DE Interrupt Source #1

Bit	Type	Function	Default
Bit 15	R	T8DEI[16]	X
Bit 14	R	T8DEI[15]	X
Bit 13	R	T8DEI[14]	X
Bit 12	R	T8DEI[13]	X
Bit 11	R	T8DEI[12]	X
Bit 10	R	T8DEI[11]	X
Bit 9	R	T8DEI[10]	X
Bit 8	R	T8DEI[9]	X
Bit 7	R	T8DEI[8]	X
Bit 6	R	T8DEI[7]	X
Bit 5	R	T8DEI[6]	X
Bit 4	R	T8DEI[5]	X
Bit 3	R	T8DEI[4]	X
Bit 2	R	T8DEI[3]	X
Bit 1	R	T8DEI[2]	X
Bit 0	R	T8DEI[1]	X

This register is used to indicate interrupts generated from the T8DE blocks #1 through #16.

T8DEI[16:1]

The T8DE #*X* interrupt event indication (T8DEI[X]) transitions to logic 1 when a hardware interrupt event is sourced from T8DE #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 0009H: TSE Master T8DE Interrupt Source #2

Bit	Type	Function	Default
Bit 15	R	T8DEI[32]	X
Bit 14	R	T8DEI[31]	X
Bit 13	R	T8DEI[30]	X
Bit 12	R	T8DEI[29]	X
Bit 11	R	T8DEI[28]	X
Bit 10	R	T8DEI[27]	X
Bit 9	R	T8DEI[26]	X
Bit 8	R	T8DEI[25]	X
Bit 7	R	T8DEI[24]	X
Bit 6	R	T8DEI[23]	X
Bit 5	R	T8DEI[22]	X
Bit 4	R	T8DEI[21]	X
Bit 3	R	T8DEI[20]	X
Bit 2	R	T8DEI[19]	X
Bit 1	R	T8DEI[18]	X
Bit 0	R	T8DEI[17]	X

This register is used to indicate interrupts generated from the T8DE blocks #17 through #32.

T8DEI[32:17]

The T8DE #*X* interrupt event indication (T8DEI[X]) transitions to logic 1 when a hardware interrupt event is sourced from T8DE #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 000AH: TSE Master T8DE Interrupt Source #3

Bit	Type	Function	Default
Bit 15	R	T8DEI[48]	X
Bit 14	R	T8DEI[47]	X
Bit 13	R	T8DEI[46]	X
Bit 12	R	T8DEI[45]	X
Bit 11	R	T8DEI[44]	X
Bit 10	R	T8DEI[43]	X
Bit 9	R	T8DEI[42]	X
Bit 8	R	T8DEI[41]	X
Bit 7	R	T8DEI[40]	X
Bit 6	R	T8DEI[39]	X
Bit 5	R	T8DEI[38]	X
Bit 4	R	T8DEI[37]	X
Bit 3	R	T8DEI[36]	X
Bit 2	R	T8DEI[35]	X
Bit 1	R	T8DEI[34]	X
Bit 0	R	T8DEI[33]	X

This register is used to indicate interrupts generated from the T8DE blocks #33 through #48.

T8DEI[48:33]

The T8DE #*X* interrupt event indication (T8DEI[X]) transitions to logic 1 when a hardware interrupt event is sourced from T8DE #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 000BH: TSE Master T8DE Interrupt Source #4

Bit	Type	Function	Default
Bit 15	R	T8DEI[64]	X
Bit 14	R	T8DEI[63]	X
Bit 13	R	T8DEI[62]	X
Bit 12	R	T8DEI[61]	X
Bit 11	R	T8DEI[60]	X
Bit 10	R	T8DEI[59]	X
Bit 9	R	T8DEI[58]	X
Bit 8	R	T8DEI[57]	X
Bit 7	R	T8DEI[56]	X
Bit 6	R	T8DEI[55]	X
Bit 5	R	T8DEI[54]	X
Bit 4	R	T8DEI[53]	X
Bit 3	R	T8DEI[52]	X
Bit 2	R	T8DEI[51]	X
Bit 1	R	T8DEI[50]	X
Bit 0	R	T8DEI[49]	X

This register is used to indicate interrupts generated from the T8DE blocks #49 through #64.

T8DEI[64:49]

The T8DE #*X* interrupt event indication (T8DEI[X]) transitions to logic 1 when a hardware interrupt event is sourced from T8DE #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 000CH: TSE Master ITSE Interrupt Source

Bit	Type	Function	Default
Bit 15	R	ITSEI[16]	X
Bit 14	R	ITSEI[15]	X
Bit 13	R	ITSEI[14]	X
Bit 12	R	ITSEI[13]	X
Bit 11	R	ITSEI[12]	X
Bit 10	R	ITSEI[11]	X
Bit 9	R	ITSEI[10]	X
Bit 8	R	ITSEI[9]	X
Bit 7	R	ITSEI[8]	X
Bit 6	R	ITSEI[7]	X
Bit 5	R	ITSEI[6]	X
Bit 4	R	ITSEI[5]	X
Bit 3	R	ITSEI[4]	X
Bit 2	R	ITSEI[3]	X
Bit 1	R	ITSEI[2]	X
Bit 0	R	ITSEI[1]	X

This register is used to indicate interrupts generated from the ITSE blocks #1 through #16.

ITSEI[16:1]

The ITSE #*X* interrupt event indication (ITSEI[X]) transitions to logic 1 when a hardware interrupt event is sourced from ITSE #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 000DH: TSE Master ETSE Interrupt Source

Bit	Type	Function	Default
Bit 15	R	ETSEI[16]	X
Bit 14	R	ETSEI[15]	X
Bit 13	R	ETSEI[14]	X
Bit 12	R	ETSEI[13]	X
Bit 11	R	ETSEI[12]	X
Bit 10	R	ETSEI[11]	X
Bit 9	R	ETSEI[10]	X
Bit 8	R	ETSEI[9]	X
Bit 7	R	ETSEI[8]	X
Bit 6	R	ETSEI[7]	X
Bit 5	R	ETSEI[6]	X
Bit 4	R	ETSEI[5]	X
Bit 3	R	ETSEI[4]	X
Bit 2	R	ETSEI[3]	X
Bit 1	R	ETSEI[2]	X
Bit 0	R	ETSEI[1]	X

This register is used to indicate interrupts generated from the ETSE blocks #1 through #16.

ETSEI[16:1]

The ETSE #*X* interrupt event indication (ETSEI[X]) transitions to logic 1 when a hardware interrupt event is sourced from ETSE #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 000EH: TSE Master CSTR Interrupt Source

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CSTRI[4]	X
Bit 2	R	CSTRI[3]	X
Bit 1	R	CSTRI[2]	X
Bit 0	R	CSTRI[1]	X

This register is used to indicate interrupts generated from the CSTR blocks #1 through #4.

CSTRI[4:1]

The CSTR #*X* interrupt event indication (CSTRI[X]) transitions to logic 1 when a hardware interrupt event is sourced from CSTR #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register 000FH: TSE Master User Defined

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

FREE[7:0]

The FREE[7:0] register bits do not perform any function. They are free for user defined read/write operations.

Register 0010H: TSE Master JTAG ID High

Bit	Type	Function	Default
Bit 15	R	ID[3]	0
Bit 14	R	ID[2]	0
Bit 13	R	ID[1]	0
Bit 12	R	ID[0]	1
Bit 11	R	DEVID[15]	0
Bit 10	R	DEVID[14]	1
Bit 9	R	DEVID[13]	0
Bit 8	R	DEVID[12]	1
Bit 7	R	DEVID[11]	0
Bit 6	R	DEVID[10]	0
Bit 5	R	DEVID[9]	1
Bit 4	R	DEVID[8]	1
Bit 3	R	DEVID[7]	0
Bit 2	R	DEVID[6]	1
Bit 1	R	DEVID[5]	1
Bit 0	R	DEVID[4]	1

The TSE Master JTAG ID registers hold the JTAG identification code for the device. The device revision number and device id are available through these registers.

DEVID[15:0]

The DEVID bits can be read to distinguish the TSE from other devices. DEVID returns 5372H when read. DEVID[3:0] bits are found in Register 0011H: TSE Master JTAG ID Low.

ID[3:0]

The ID bits can be read to provide a binary TSE revision number.

Register 0011H: TSE Master JTAG ID Low

Bit	Type	Function	Default
Bit 15	R	DEVID[3]	0
Bit 14	R	DEVID[2]	0
Bit 13	R	DEVID[1]	1
Bit 12	R	DEVID[0]	0
Bit 11	R	MID[10]	0
Bit 10	R	MID[9]	0
Bit 9	R	MID[8]	0
Bit 8	R	MID[7]	0
Bit 7	R	MID[6]	1
Bit 6	R	MID[5]	1
Bit 5	R	MID[4]	0
Bit 4	R	MID[3]	0
Bit 3	R	MID[2]	1
Bit 2	R	MID[1]	1
Bit 1	R	MID[0]	0
Bit 0	R	JID	1

JID

The JID bit is bit 0 in the JTAG identification code.

MID[10:0]

The MID bits provide the manufacturer identify field in the JTAG identification code. MID returns 066H when read.

DEVID[15:0]

The DEVID bits can be read to distinguish the TSE from other devices. DEVID returns 5372H when read. DEVID[15:4] bits are found in Register 0010H: TSE Master JTAG ID High.

Register 0020H, 00024H, 0028H, 002CH: CSTR #1 – #4 Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved[11]	0
Bit 14	R/W	Reserved[10]	0
Bit 13	R/W	Reserved[9]	0
Bit 12	R/W	Reserved[8]	0
Bit 11	R/W	Reserved[7]	0
Bit 10	R/W	Reserved[6]	1
Bit 9	R/W	Reserved[5]	0
Bit 8	R/W	Reserved[4]	0
Bit 7	R/W	Reserved[3]	0
Bit 6	R/W	Reserved[2]	0
Bit 5	R/W	Reserved[1]	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved[0]	1

This register provides reset control and enable control for CSTR blocks #1 through #4

Reserved[11:0]

The Reserved[11:0] bits must be set to the indicated default value for correct operation of the TSE.

CSU_RSTB

The CSU_RSTB signal is a software reset signal that forces the CSU into reset. The CSU is reset when the CSU_RSTB is logic 0. The CSU is also reset by the TSE master analog reset signal. When the CSU is reset, the reset signal should be held for at least 100us.

CSU_ENB

The CSU enable control signal (CSU_ENB) bit forces the CSU into low power configuration. The CSU is disabled when CSU_ENB is logic 1. The CSU is enabled when CSU_ENB is logic 0.

Register 0021H, 00025H, 0029H, 002DH: CSTR #1 – #4 Interrupt Enable and CSU Lock Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

This register configures the operation of CSTR blocks #1 through #4.

LOCKE

The CSU lock interrupt enable bit (LOCKE) controls the contribution of CSU lock state interrupts by the CSTR to the device interrupt INTB. When LOCKE is high, INTB is asserted low when the CSU lock state changes. Interrupts due to CSU lock state are masked when LOCKE is set low.

LOCKV

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit has successfully locked with the system clock. LOCKV is set low when the CSU has not successfully locked with the reference clock. LOCKV is set high if when the CSU has locked with the reference clock.

Register 0022H, 00026H, 002AH, 002EH: CSTR #1 – #4 Interrupt Indication

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOCKI	X

This register reports the interrupt status of CSTR blocks #1 through #4.

LOCKI

The CSU lock interrupt status bit (LOCKI) reports and acknowledges changes in the CSU lock state. LOCKI is set high when the CSU achieves lock with the reference clock or loses its lock to the reference clock. LOCKI is cleared on a read to this register when WCIMODE is logic 0. LOCKI is cleared on a write of logic 1 to LOCKI when WCIMODE is logic 1. INTB is asserted low when both LOCKE and LOCKI are high. If LOCKE is asserted, LOCKI must be cleared before INTB will be reasserted.

Register 0040H: SSWT RJ0FP Delay

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	RJ0DLY[13]	0
Bit 12	R/W	RJ0DLY[12]	0
Bit 11	R/W	RJ0DLY[11]	0
Bit 10	R/W	RJ0DLY[10]	0
Bit 9	R/W	RJ0DLY[9]	0
Bit 8	R/W	RJ0DLY[8]	0
Bit 7	R/W	RJ0DLY[7]	0
Bit 6	R/W	RJ0DLY[6]	0
Bit 5	R/W	RJ0DLY[5]	0
Bit 4	R/W	RJ0DLY[4]	0
Bit 3	R/W	RJ0DLY[3]	0
Bit 2	R/W	RJ0DLY[2]	0
Bit 1	R/W	RJ0DLY[1]	0
Bit 0	R/W	RJ0DLY[0]	0

This register controls the delay from the RJ0FP input signal to the time when the TSE may safely process the J0 characters delivered by the receive data links (RP [64:1]/RN[64:1]).

RJ0DLY[13:0]

The receive transport frame delay bits (RJ0DLY[13:0]) controls the delay from the RJ0FP pulse clock cycle, in SYSCLK cycles, inserted by the TSE before processing the J0 characters delivered by the receive serial data links. RJ0DLY is set such that after the specified delay, all active receive links would have delivered the J0 character to the receive FIFO in the R8FA. RJ0DLY has valid range between 1 to 9719 inclusive. The relationships of RJ0FP, RJ0DLY[13:0] and the system configuration are described in Figure 20, Figure 21, and Figure 22.

Register 0041H: SSWT Indirect Control Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	PGSEL	0
Bit 12		Unused	X
Bit 11	R/W	TSLOT[3]	0
Bit 10	R/W	TSLOT[2]	0
Bit 9	R/W	TSLOT[1]	0
Bit 8	R/W	TSLOT[0]	1
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	DOUTSEL[5]	0
Bit 4	R/W	DOUTSEL[4]	0
Bit 3	R/W	DOUTSEL[3]	0
Bit 2	R/W	DOUTSEL[2]	0
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the SSWT outgoing stream number, time slot number, and control page number used to access the space switch control blocks of the SSWT outgoing data streams. Writing to this register triggers an indirect register access and transfers the contents of the indirect mux control data register to an internal holding register.

DOUTSEL[5:0]

DOUTSEL[5:0] selects the Space switch control block in an indirect MUX Control Access. The correspondence between DOUTSEL, SSWT output port and the connected ETSE input port are as follows.

DOUTSEL[5:0]	ETSE Block #	ETSE Input Port #	Transmit Serial Link (TP[*X*]/TN[*X*])
0	1	1	1
1	1	2	2
2	1	3	3
3	1	4	4
.	.	.	.
4N	N+1	1	4N+1

4N+1	N+1	2	4N+2
4N+2	N+1	3	4N+3
4N+3	N+1	4	4N+4
.	.	.	.
63	16	4	64

TSLOT[3:0]

The indirect time-slot number bits (TSLOT[3:0]) indicate the time-slot to be configured or interrogated in the indirect access. For the data incoming to the SSWT, time-slots 1 to 12 are valid. Indices 0 and 13 to 15 are invalid. An invalid index will result in immediate deassertion of the busy bit and undefined results in the DINSEL register. The following table shows valid TSLOT values.

Table 13 Control Word Index

TSLOT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PGSEL

The PGSEL specifies the Control page of the Space switch control block in an indirect MUX Control Access. When PGSEL is logic 0, Control page 0 is selected. When PGSEL is 1, Control page 1 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the space switch control blocks. The address to the control registers is constructed from the DOUTSEL[5:0] and TSLOT[3:0] fields. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the DINSEL[6:0] data register. Writing a logic one to RWB triggers an indirect read operation. Addressing of the switch control block is the same as in an indirect write operation. The data read can be found in DINSEL[6:0] after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written to trigger an indirect access, and will stay high until the access is complete, at which point BUSY will be cleared (set low). This register should be polled to determine when data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence. Any indirect operation that is initiated while BUSY is still high will be corrupted. The BUSY bit shows a default of "X". This does not require the bit to be cleared after a reset since the bit resets to 0 a few clock cycles after a reset. The bit is undefined for a short period (a few clock cycles) after a reset but the user will never read "1" as the bit would clear before the bit is queried.

Register 0042H: SSWT Indirect Control Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	DINSEL[5]	0
Bit 4	R/W	DINSEL[4]	0
Bit 3	R/W	DINSEL[3]	0
Bit 2	R/W	DINSEL[2]	0
Bit 1	R/W	DINSEL[1]	0
Bit 0	R/W	DINSEL[0]	0

This register contains data to be written into the control word in an indirect write access, or the data read from the control word in an indirect read access for the SSWT block.

DINSEL[5:0]

The DINSEL[5:0] specifies one control word within a page of a Space Switch control block. In an indirect write operation, the control words must be set up in this register before triggering the indirect write. When read back, DINSEL[5:0] reflects the value written until the completion of a subsequent indirect channel read operation. The control word directs which of the 64 input data words is selected for the output timeslot. The correspondence between DINSEL, SSWT input ports, and the attached ITSE output ports is shown in the following table.

DINSEL[5:0]	ITSE Block #	ITSE Output Port #	Receive Serial Link (RP[*X*]/RN[*X*])
0	1	1	1
1	1	2	2
2	1	3	3
3	1	4	4

DINSEL[5:0]	ITSE Block #	ITSE Output Port #	Receive Serial Link (RP[*X*]/RN[*X*])
.	.	.	.
4N	N+1	1	4N+1
4N+1	N+1	2	4N+2
4N+2	N+1	3	4N+3
4N+3	N+1	4	4N+4
.	.	.	.
63	16	4	64

Register 0043H: SSWT Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	SACTIVE	X
Bit 1	R/W	SPSEL	0
Bit 0	R/W	SCOAPE	0

This register provides interrupt enable control for the SSWT block

SCOAPE

The change of active page interrupt enable bit (SCOAPE) masks the contribution of the change of active page event indication bit (SCOAPI) in the SSWT block to INTB. When SCOAPE is high, INTB is asserted low when SCOAPI is high. INTB is not affected by the value of SCOAPI when SCOAPE is low.

SPSEL

The page select (SPSEL) bit is used in the selection of the current active page for the mux control blocks. This bit is logically XORed with the value of CMP to determine the next control page selection.

SACTIVE

The active page indication (SACTIVE) bit indicates which control page is currently active in the muxing blocks. When this bit is logic 0 then page 0 is active. When this bit is logic 1 then page 1 is active.

Register 0044H: SSWT Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	SCOAPI	X

This register provides the interrupt status of the SSWT block.

SCOAPI

The change of active page interrupt (SCOAPI) reports a change in the active page event for the SSWT. SCOAPI is set high when a change of active page has occurred since the last clear for the register. SCOAPI is cleared on a read to this register when WCIMODE is logic 0. SCOAPI is cleared on a write of logic 1 to SCOAPI when WCIMODE is logic 1. INTB is asserted low when both SCOAPE and SCOAPI are high. IF SCOAPE is asserted, SCOAPI must be cleared before INTB will be reasserted.

Register 0047H: SSWT TJ0FP Delay

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	TJ0DLY[13]	0
Bit 12	R/W	TJ0DLY[12]	0
Bit 11	R/W	TJ0DLY[11]	0
Bit 10	R/W	TJ0DLY[10]	0
Bit 9	R/W	TJ0DLY[9]	0
Bit 8	R/W	TJ0DLY[8]	0
Bit 7	R/W	TJ0DLY[7]	0
Bit 6	R/W	TJ0DLY[6]	0
Bit 5	R/W	TJ0DLY[5]	1
Bit 4	R/W	TJ0DLY[4]	0
Bit 3	R/W	TJ0DLY[3]	0
Bit 2	R/W	TJ0DLY[2]	1
Bit 1	R/W	TJ0DLY[1]	1
Bit 0	R/W	TJ0DLY[0]	0

This register controls the delay from the RJ0FP input signal to the assertion of the TJ0FP signal, meant to signify the transmission of J0s from all transmit ports TP[64:1]/TN[64:1].

TJ0DLY[13:0]

The transmit transport frame delay bits (TJ0DLY[13:0]) controls the delay from the RJ0FP pulse clock cycle, in SYSCLK cycles, inserted by the TSE before asserting the TJ0FP signal. The delay between RJ0FP and the assertion of TJ0FP will be TJ0DLY + 2 cycles. It is suggested that TJ0DLY is set so TJ0FP assertion signifies the departure of all J0s from the transmit ports. If TJ0FP is used for that purpose, TJ0DLY should be set to RJ0DLY+ 47. Figure 21 illustrates the relationship between RJ0FP, RJ0DLY and TJ0DLY.

Register 0N80H, 0N88H, 0N90H, 0N98H: Port Set #1 - #16 R8FA #1 - #4 Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	J0MASK	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	RXINV	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This set of registers provides control and reports the status of R8FA blocks #1 through #64. Registers 0N80H, 0N88H, 0N90H and 0N98H are associated with R8FA blocks #1 to #4 respectively, in Port Set N+1.

FOCA

The force out-of-character-alignment bit (FOCA) control the operation of the character alignment block in the corresponding R8FA block. A 0-1 transition on this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). Before another force operation can be performed, FOCA must first be set to logic 0.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block in the corresponding R8FA block. A 0-1 transition on this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). Before another force operation can be performed, FOFA must first be set to logic 0.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block in the corresponding R8FA block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block in the corresponding R8FA block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out of character alignment interrupt enable bit (OCAE) masks the contribution of the change of character alignment event indication bit (OCAI) in the corresponding R8FA block to INTB. When OCAE is high, INTB is asserted low when OCAI is high. INTB is not affected by the value of OCAI when OCAE is low.

OFAE

The out of frame alignment interrupt enable bit (OFAE) masks the contribution of the change of frame alignment event indication bit (OFAI) in the corresponding R8FA block to INTB. When OFAE is high, INTB is asserted low when OFAI is high. INTB is not affected by the value of OFAI when OFAE is low.

LCVE

The line code violation interrupt enable bit (LCVE) masks the contribution of the line code violation event indication bit (LCVI) in the corresponding R8FA block to INTB. When LCVE is high, INTB is asserted low when LCVI is high. INTB is not affected by the value of LCVI when LCVE is low.

FUOE

The FIFO underrun/overrun status interrupt enable bit (FUOE) masks the contribution of the FIFO underrun/overrun event indication bit (FUOI) in the corresponding R8FA block to INTB. When FUOE is high, INTB is asserted low when FUOI is high. INTB is not affected by the value of FUOI when FUOE is low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set high to force insertion of the high order path AIS, K28.4- character in the data stream if the corresponding R8FA block is in the out of frame alignment state.

RXINV

The receive data invert bit (RXINV) controls the active polarity of the incoming data stream. When RXINV is set high, the data is complemented before any processing by the corresponding R8FA. When RXINV is set low, data is not complemented before R8FA processing.

J0MASK

The J0 masking bit (J0MASK) controls the overwriting of K28.5 characters in the datastream. When J0MASK is set high, K28.5 characters are replaced by either D12.3-: “001101 0011” or D12.3+: “001101 1100” characters. This mode of operation prevents spurious K28.5 characters resulting from floating links or bit errors from passing through the TSE and disrupting framing in downstream devices. When J0MASK is set low, K28.5 characters on the datastream are not replaced. If J0/Z0 switching is enabled using the IJ0RORDER and EJ0RORDR bits, then J0 masking is recommended to prevent reordering of the K28.5 character and disruption of downstream framers.

Reserved

The Reserved bit must be set to the indicated default value for correct operation of the TSE.

Register 0N81H, 0N89H, 0N91H, 0N99H: Port Set #1 - #16 R8FA #1 - #4 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

These registers report interrupt status due to change of character alignment events and detection of line code violations for the R8FA blocks #1 - #64. Registers 0N81H, 0N89H, 0N91H and 0N99H are associated with R8FA blocks #1 - #4 respectively, in Port Set N+1.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state events for the R8FA block. OCAI is set high when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state since the last clear for the register. OCAI is cleared on a read to this register when WCIMODE is logic 0. OCAI is cleared on a write of logic 1 to OCAI when WCIMODE is logic 1. INTB is asserted low when both OCAE and OCAI are high. If OCAE is asserted, OCAI must be cleared before INTB will be reasserted.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state events for the R8FA block. OFAI is set high when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is cleared on a read to this register when WCIMODE is logic 0. OFAI is cleared on a write of logic 1 to OFAI when WCIMODE is logic 1. INTB is asserted low when both OFAE and OFAI are high. IF OFAE is asserted, OFAI must be cleared before INTB will be reasserted.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation events for the R8FA block. LCVI is set high when the character alignment block detects a line code violation in the incoming data stream. LCVI is cleared on a read to this register when WCIMODE is logic 0. LCVI is cleared on a write of logic 1 to LCVI when WCIMODE is logic 1. INTB is asserted low when both LCVE and LCVI are high. IF LCVE is asserted, LCVI must be cleared before INTB will be reasserted. Note that an uninterrupted stream of line code violations will produce a single LCVI event as it is the transition from not detecting and LCV to detecting an LCV that causes LCVI to be set.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun events for the R8FA block. FUOI is set high when R8FA detects that the FIFO read and write pointers are within one slot of each other. FUOI is cleared on a read to this register when WCIMODE is logic 0. FUOI is cleared on a write of logic 1 to FUOI when WCIMODE is logic 1. INTB is asserted low when both FUOE and FUOI are high. IF FUOE is asserted, FUOI must be cleared before INTB will be reasserted.

Register 0N82H, 0N8AH, 0N92H, 0N9AH: Port Set #1 - #16 R8FA #1 - #4 Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

These registers report the number of line code violations in the previous accumulation period for the R8FA block #1 through #64.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to the TIP register or by writing to this register. Within 10 us of either event, the internally accumulated error count is transferred to the LCV registers and the internal error counter is simultaneously reset to begin a new cycle of error accumulation.

When the Diagnose Line Code Violation bit (DLCV) in an upstream device is set to logic 1 in order to create line code violations, it is possible to saturate this register.

Register 0N83H, 0N8BH, 0N93H, 0N9BH: Port Set #1 - #16 RXLV and DRU #1 - #4 Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved[7]	1
Bit 14	R/W	Reserved[6]	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved[5]	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	Reserved[4]	0
Bit 8	R/W	Reserved[3]	0
Bit 7	R/W	Reserved[2]	0
Bit 6	R/W	Reserved[1]	0
Bit 5	R/W	DRU_CTRL[3]	0
Bit 4	R/W	DRU_CTRL[2]	0
Bit 3	R/W	DRU_CTRL[1]	0
Bit 2	R/W	DRU_CTRL[0]	0
Bit 1	R/W	Reserved[0]	0
Bit 0		Unused	X

These registers drive the control signals for RXLV and DRU blocks #1 through #64.

Reserved[4:0]

The Reserved[4:0] bits must be set to the indicated default value for correct operation of the TSE.

DRU_CTRL[3:0]

The DRU_CTRL[3:0] bits control the DRU CTRL[3:0] inputs. **The DRU_CTRL[3:0] bus is reset to 0000, but needs to be set to 1101 following a reset for correct operation of the TSE.**

A_RSTB

The A_RSTB bit is a soft-reset for the Data Recovery Unit Analog block. Setting A_RSTB to logic 0 will reset the block.

Reserved[5]

The Reserved[5] bit is set to logic 0 on reset, but needs to be set to logic 1 following reset for correct operation of the TSE.

RX_ENB

The RXLV enable bit (RX_ENB) bit controls the operation of RXLV block #X. Setting RX_ENB to logic 0 enables the block. Setting RX_ENB to logic 1 disables the block.

DRU_ENB

The DRU enable bit (DRU_ENB) bit controls the operation of Data Recovery Unit Analog block #X. Setting DRU_ENB to logic 0 enables the block. Setting DRU_ENB to logic 1 disables the block.

Reserved[7:6]

The Reserved[7:6] bits must be set to the indicated default value for correct operation of the TSE.

Register 0NA0H: Port Set #1 - #16, ITSE Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

These registers provide the ITSE output port identifier, the time-slot number and the control page select used to access the control pages in the ITSE blocks #1 through #16. Writing to this register triggers an indirect register access.

DOUTSEL[1:0]

The Data Output Select (DOUTSEL[1:0]) bits select which ITSE output port configuration is accessed by the current indirect transfer. Data from timeslot TSIN[3:0] of incoming datastream DINSEL[1:0] is transferred to timeslot TSOUT[3:0] to the output port selected by DOUTSEL[1:0].

ITSE Block #N+1 (N from 0 – 15)		
DOUTSEL[1:0]	**ITSE Output Port #**	**Receive Serial Link RP[*X*]/RN[*X*]**
00	1	4N+1
01	2	4N+2
10	3	4N+3
11	4	4N+4

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) select bits for the ITSE block indicate the STS-1/STM-0 output time slot within the datastream selected by DOUTSEL[1:0] that is accessed in the current indirect access. Valid time-slot values are ‘b0001 to ‘b1100.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect access. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages for the ITSE block. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the ITSE Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the ITSE Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access for the ITSE block. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. These registers should be polled to determine when new data is available in the ITSE Indirect Data Register or when another write access can be initiated. The BUSY bit shows a default of “x”. This does not require the bit to be cleared after a reset since the bit resets to 0 a few clock cycles after a reset. The bit is undefined for a short period (a few clock cycles) after a reset but the user will never read “1” as the bit would clear before the bit is queried.

Register 0NA1H: Port Set #1 - #16 ITSE Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved[7]	0
Bit 12	R/W	Reserved[6]	0
Bit 11	R/W	Reserved[5]	0
Bit 10	R/W	Reserved[4]	0
Bit 9	R/W	Reserved[3]	0
Bit 8	R/W	Reserved[2]	0
Bit 7	R/W	TSIN[3]	0
Bit 6	R/W	TSIN[2]	0
Bit 5	R/W	TSIN[1]	0
Bit 4	R/W	TSIN[0]	0
Bit 3	R/W	Reserved[1]	0
Bit 2	R/W	Reserved[0]	0
Bit 1	R/W	DINSEL[1]	0
Bit 0	R/W	DINSEL[0]	0

These registers contain the data read from the control pages after an indirect read operation or the to be data written to the control pages in an indirect write operation for the ITSE block.

DINSEL[1:0]

The Data Input Select (DINSEL[1:0]) bits report the ITSE input port identifier read after an indirect read operation has completed for the ITSE block. The input port identifier to be written to the control pages must be set in DINSEL[1:0] before triggering a write. DINSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation.

Reserved[7:0]

The Reserved[7:0] bits must be set as shown for correct operation of the TSE.

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) bits report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. TSIN [3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Time slots b'0001 to 'b1100are valid. Writing an invalid time-slot value results in undefined behavior.

TSIN[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

Register 0NA2H: Port Set #1 - #16 ITSE Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	IACTIVE	X
Bit 2	R/W	IPSEL	0
Bit 1	R/W	IJ0RORDR	0
Bit 0	R/W	ICOAPE	0

These registers provide page selection, active page indication, J0 reordering mode, and interrupt masking control for ITSE blocks #1 through #16.

ICOAPE

The change of active page interrupt enable bit (ICOAPE) masks the contribution of the change of active page event indication bit (ICOAPI) in the ISTI block to INTB. When ICOAPE is high, INTB is asserted low when ICOAPI is high. INTB is not affected by the value of ICOAPI when ICOAPE is low.

IJ0RORDR

The incoming J0 reorder bit controls the reordering of J0/Z0 bytes in the four STS-12 datastreams through the *n*th ITSE block. Time slot interchange of the J0/Z0 bytes in the *n*th ITSE is suspended when J0/Z0 reordering is disabled. When IJ0RORDR is set low, the J0/Z0 bytes are not reordered. When IJ0RORDR is set high, J0/Z0 byte reordering is enabled. If J0 reordering is enabled, J0 masking should also be enabled in the upstream R8Fas to prevent K28.5 characters from being switched to a position other than J0. J0 masking is done using the J0MASK bit in register 0N80H, 0N88H, 0N90H, and 0N98H.

IPSEL

The page select (IPSEL) bit is used in the selection of the current active. This bit is logically XORed with the value of the CMP signal to determine which control page is currently active. If the XOR result is logic 1, control page 1 is selected. Otherwise, control page 0 is selected.

IACTIVE

The active page indication (IACTIVE) bit indicates which control page is currently active in the associated muxing blocks. When this bit is logic 0 then page 0 is active. When this bit is logic 1 then page 1 is active.

Register 0NA3H: Port Set #1 - #16, ITSE Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ICOAPI	X

These registers provide the interrupt status of ITSE blocks #1 through #16.

ICOAPI

The change of active page interrupt (ICOAPI) reports a change in the active page event for the ITSE. ICOAPI is set high when a change of active page has occurred since the last clear for the register. ICOAPI is cleared on a read to this register when WCIMODE is logic 0. ICOAPI is cleared on a write of logic 1 to ICOAPI when WCIMODE is logic 1. INTB is asserted low when both ICOAPE and ICOAPI are high. IF ICOAPE is asserted, ICOAPI must be cleared before INTB will be reasserted.

Register 0NA8H: Port Set #1 - #16, ETSE Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

These registers provide the ETSE output port identifier, the time-slot number and the control page select used to access the control pages for ETSE blocks #1 through #16. Writing to this register triggers an indirect register access.

DOUTSEL[1:0]

The Data Output Select (DOUTSEL[1:0]) bits select which ETSE output port configuration is accessed by the current indirect transfer. Data from timeslot TSIN[3:0] of incoming data of incoming datastream DINSEL[1:0] is transferred to timeslot TSOUT[3:0] to the output port selected by DOUTSEL[1:0].

ETSE Block #N+1 (N from 0 – 15)		
DOUTSEL[1:0]	**ETSE Output Port #**	**Transmit Serial Link TP[X]/TN[X]**
00	1	4N+1
01	2	4N+2
10	3	4N+3
11	4	4N+4

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) select bits for the ETSE block indicate the STS-1/STM-0 output time slot within the datastream selected by DOUTSEL[1:0] that is accessed in the current indirect access. Valid time-slot values are ‘b0001 to ‘b1100.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect access. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages for the ITSE block. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the ITSE Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the ITSE Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access for the ITSE block. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. These registers should be polled to determine when new data is available in the ITSE Indirect Data Register or when another write access can be initiated. The BUSY bit shows a default of “x”. This does not require the bit to be cleared after a reset since the bit resets to 0 a few clock cycles after a reset. The bit is undefined for a short period (a few clock cycles) after a reset but the user will never read “1” as the bit would clear before the bit is queried.

Register 0NA9H: Port Set #1 - #16, ETSE Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	ECHAR_OVWR[1]	0
Bit 12	R/W	ECHAR_OVWR[0]	0
Bit 11	R/W	Reserved[1]	0
Bit 10	R/W	Reserved[0]	0
Bit 9	R/W	ECOVD[9]	0
Bit 8	R/W	ECOVD[8]	0
Bit 7	R/W	TSIN[3]/ECOVD[7]	0
Bit 6	R/W	TSIN[2]/ECOVD[6]	0
Bit 5	R/W	TSIN[1]/ECOVD[5]	0
Bit 4	R/W	TSIN[0]/ECOVD[4]	0
Bit 3	R/W	ECOVD[3]	0
Bit 2	R/W	ECOVD[2]	0
Bit 1	R/W	DINSEL[1]/ECOVD[1]	0
Bit 0	R/W	DINSEL[0]/ECOVD[0]	0

These registers contain the data read from the control pages after an indirect read operation or the to be data written to the control pages in an indirect write operation for ETSE blocks #1 through #16.

DINSEL[1:0]

The Data Input Select (DINSEL[1:0]) bits report the ETSE input port identifier read after an indirect read operation has completed for the ETSE block. The input port identifier to be written to the control pages must be set to DINSEL[1:0] before triggering a. DINSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. DINSEL[1:0] also doubles as ECOVD[1:0]

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) bits report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. TSIN [3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Time slots #1 to #12 are valid. Writing an invalid time-slot value results in undefined behavior. TSIN[3:0] also doubles as ECOVD[7:4].

TSIN[3:0]	STS-1/STM-0 time slot #
0000	Invalid Time Slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

ECOVD[9:0]

The Character Overwrite data bits (ECOVD[9:0]) reports the data read after an indirect read operation has completed. The data to be written to the control pages must be set up in this register before triggering a write. ECOVD[9:0] reflects the last value read or written until the completion of a subsequent indirect read operation. ECOVD[9:0] represents the data written to the DINSEL port/ TSOUT timeslot of the ETSE block provided the ECHAR_OVWR[1:0] bits are logic b'11. Otherwise, DINSEL and TINSEL control the output for the specified port/timeslot.

Reserved[1:0]

The Reserved[1:0] bits must be set as shown for correct operation of the TSE.

ECHAR_OVWR[1:0]

The Character Overwrite Data Insertion Control bits (ECHAR_OVWR[1:0]) report the value of the ECHAR_OVWR[1:0] bits read after an indirect read operation has completed. The value of the ECHAR_OVWR[1:0] bits to be written to the control pages must be set up in this register before triggering a write. ECHAR_OVWR[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. The value of the ECHAR_OVWR[1:0] bits control the source of the data bits that the muxing block outputs. When set to logic b'00 the muxing block samples and reorders the holding buffers. When set to logic b'11 then muxing block directly outputs the idle data (ECOVD[9:0]). ECHAR_OVWR values of 'b01 and 'b10 are invalid.

Register 0NAAH: Port Set #1 - #16, ETSE Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	EACTIVE	X
Bit 2	R/W	EPSEL	0
Bit 1	R/W	EJ0RORDR	0
Bit 0	R/W	ECOAPE	0

These registers provide page selection, active page indication, J0 reordering mode, and interrupt masking control for ETSE blocks #1 through #16.

ECOAPE

The change of active page interrupt enable bit (ECOAPE) masks the contribution of the change of active page event indication bit (ECOAPI) in the ETSI block to INTB. When ECOAPE is high, INTB is asserted low when ECOAPI is high. INTB is not affected by the value of ECOAPI when ECOAPE is low.

EJ0RORDR

The egress J0 reorder bit controls the reordering of J0/Z0 bytes in the four STS-12 datastreams through the *n*th ETSE block. Time slot interchange of the J0/Z0 bytes in the *n*th ETSE is suspended when J0/Z0 reordering is disabled. When EJ0RORDR is set low, the J0/Z0 bytes are not reordered. When EJ0RORDR is set high, J0/Z0 byte reordering is enabled. If J0 reordering is enabled, J0 masking should also be enabled in all R8Fas to prevent K28.5 characters from being switched to a position other than J0. J0 masking is done using the J0MASK bit in register 0N80H, 0N88H, 0N90H, and 0N98H, for 0<= N <= 15.

EPSEL

The page select (EPSEL) bit is used in the selection of the current active. This bit is logically XORed with the value of the CMP signal to determine which control page is currently active. If the XOR result is logic 1, control page 1 is selected. Otherwise, control page 0 is selected.

EACTIVE

The active page indication (EACTIVE) bit indicates which control page is currently active in the associated muxing blocks. When this bit is logic 0 then page 0 is active. When this bit is logic 1 then page 1 is active.

Register 0NABH: Port Set #1 - #16, ETSE Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ECOAPI	X

These registers provide the interrupt status of ETSE blocks #1 through #16.

ECOAPI

The change of active page interrupt (ECOAPI) reports a change in the active page event for the ITSE. ECOAPI is set high when a change of active page has occurred since the last clear for the register. ECOAPI is cleared on a read to this register when WCIMODE is logic 0. ECOAPI is cleared on a write of logic 1 to ECOAPI when WCIMODE is logic 1. INTB is asserted low when both ECOAPE and ECOAPI are high. IF ECOAPE is asserted, ECOAPI must be cleared before INTB will be reasserted.

Register 0NB0H, 0NB8H, 0NC0H, 0NC8H: Port Set #1 - #16, T8DE #1 - #4 Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	J0INS	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	1
Bit 0	R/W	DLCV	0

These registers provide control and report the status of T8DE blocks #1 through #64.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violations in the outgoing data stream. When DLCV is logic 1, the encoded data is continuously inverted and will result in a varying number of line code violations at the receiver depending on its configuration. An immediate line code violation is generated since an incorrect disparity character is transmitted. As long as DLCV is set, further line code violations will be transmitted following the transmission of an TelecomBus control character. Note that TelecomBus control characters are not affected by the DLCV bit but are passed unaltered. This results in a continuous stream of disparity errors in a receiving R8FA while DLCV is high. Note that this stream of disparity errors will eventually saturate the LCV[15:0] counters in the receiving device. When DLCV is logic 0, no code inversion is performed.

CENTER:

The FIFO centering control bit (CENTER) controls the separation of the T8DE FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be 3 or 4 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

Reserved

The Reserved bit must be set to the indicated default value for correct operation of the TSE.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, TP[9:0] in the T8DE Test Pattern register is selected for output. TPINS takes precedence over J0INS, inserted K28.5 will be overwritten with the test pattern.

FIFOERRE

The FIFO underrun/overrun error interrupt enable bit (FIFOERRE) masks the contribution of the FIFO underrun/overrun event indication bit (FIFOERRI) in the T8DE block to INTB. When FIFOERRE is high, INTB is asserted low when FIFOERRI is high. INTB is not affected by the value of FIFOERRI when FIFOERRE is low.

J0INS

The J0 byte Insertion (J0INS) controls the insertion of first J0 bytes in the outgoing data stream. When this bit is set to logic 1, a K28.5 character is inserted at the J0 byte position on every frame, overwriting the data in that position (TSE inserted AIS included). When J0INS is set to logic 0, the outgoing data stream is not modified.

Register 0NB1H, 0NB9H, 0NC1H, 0NC9H: Port Set #1 - # 16 T8DE #1 - #4 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

These registers report the interrupt status for T8DE blocks #1 through #64.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFOERRI is set high when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is cleared on a read to this register when WCIMODE is logic 0. FIFOERRI is cleared on a write of logic 1 to FIFOERRI when WCIMODE is logic 1. INTB is asserted low when both FIFOERRE and FIFOERRI are high. IF FIFOERRE is asserted, FIFOERRI must be cleared before INTB will be reasserted.

Register 0NB4H, 0NBCH, 0NC4H, 0NCCH: Port Set #1 - #16 T8DE #1 - #4 Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

These registers store the test pattern for test pattern insertion for T8DE blocks #1 through #64.

TP[9:0]

The Test Pattern register (TP[9:0]) for T8DE block #X contains the test pattern conditionally inserted into output data stream #X. TP[9:0] is inserted into the output data stream when the TPINS bit is set high.

Register 0NB5H, 0NBDH, 0NC5H, 0NCDH: Port Set #1 - #16, TXLV and PISO Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved[8]	0
Bit 10	R/W	Reserved[7]	0
Bit 9	R/W	Reserved[6]	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved[5]	0
Bit 5	R/W	Reserved[4]	0
Bit 4	R/W	Reserved[3]	0
Bit 3	R/W	Reserved[2]	0
Bit 2	R/W	Reserved[1]	1
Bit 1	R/W	Reserved[0]	1
Bit 0	R/W	ARSTB	1

These registers control the operation of LVDS Transmit and PISO blocks #1 through #64

ARSTB

The analog reset bit (ARSTB) resets the associated TXLV and PISO blocks. When ARSTB is set to logic 0, the TXLV and PISO are reset.

Reserved[8:0]

The Reserved[8:0] bits must be set to the indicated default value for correct operation of the TSE.

PISO_ENB

The PISO enable bit (PISO_ENB) controls the operation of the PISO block. PISO_ENB is set to logic 1 to disable the PISO block. PISO_ENB is set to logic 0 to enable the PISO block.

TXLV_ENB

The TXLV enable bit (TXLV_ENB) controls the operation of TXLV block. TXLV_ENB is set to logic 1 to disable the TXLV block. TXLV_ENB is set to logic 0 to enable the TXLV block.

11 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TSE. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[12]) is high.

In addition, the TSE also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

11.1 JTAG Test Port

The TSE JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 14 Instruction Register (Length – 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 15 Identification Register

Length	32 bits
Version Number	1H
Part Number	5372H
Manufacturer's Identification Code	0CDH
Device Identification	153720CDH

Table 16 Boundary Scan Register Length – 57 bits

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
Tj0FP	0	OUT_CELL		oeb_d(13)	29	OUT_CELL	0
HIZ	1	OUT_CELL		d(12)	30	IO_CELL	0
VSS	2	OUT_CELL		oeb_d(12)	31	OUT_CELL	1
INTB	3	OUT_CELL		d(11)	32	IO_CELL	1
ALE	4	IN_CELL		oeb_d(11)	33	OUT_CELL	0
WRB	5	IN_CELL		d(10)	34	IO_CELL	0
RDB	6	IN_CELL		oeb_d(10)	35	OUT_CELL	0
CSB	7	IN_CELL		d(9)	36	IO_CELL	0

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
CMP	8	IN_CELL		oeb_d(9)	37	OUT_CELL	0
a(12)	9	IN_CELL		d(8)	38	IO_CELL	1
SYSCLK	10	IN_CELL		oeb_d(8)	39	OUT_CELL	0
RJ0FP	11	IN_CELL		RSTB	40	IN_CELL	0
a(11)	12	IN_CELL		d(7)	41	IO_CELL	1
a(10)	13	IN_CELL		oeb_d(7)	42	OUT_CELL	1
a(9)	14	IN_CELL		d(6)	43	IO_CELL	1
a(8)	15	IN_CELL		oeb_d(6)	44	OUT_CELL	0
a(7)	16	IN_CELL		d(5)	45	IO_CELL	1
a(6)	17	IN_CELL		oeb_d(5)	46	OUT_CELL	1
a(5)	18	IN_CELL		d(4)	47	IO_CELL	0
a(4)	19	IN_CELL		oeb_d(4)	48	OUT_CELL	0
a(3)	20	IN_CELL		d(3)	49	IO_CELL	1
a(2)	21	IN_CELL		oeb_d(3)	50	OUT_CELL	0
a(1)	22	IN_CELL		d(2)	51	IO_CELL	1
a(0)	23	IN_CELL		oeb_d(2)	52	OUT_CELL	0
d(15)	24	IO_CELL		d(1)	53	IO_CELL	1
oeb_d(15)	25	OUT_CELL	1	oeb_d(1)	54	OUT_CELL	0
d(14)	26	IO_CELL	0	d(0)	55	IO_CELL	0
oeb_d(14)	27	OUT_CELL	1	oeb_d(0)	56	OUT_CELL	0
d(13)	28	IO_CELL	1				

NOTES:

- OEB_D[15:0] is the active low output enable for D[15:0].
- When set high, INTB will be set to high impedance.
- HIZ is the active low output enable for all OUT_CELL types except OEB_D[15:0], and INTB
- TJ0FP will be the first bit to appear on TDO when the scan chain is shifted out.

11.1.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 8 Input Observation Cell (IN_CELL)

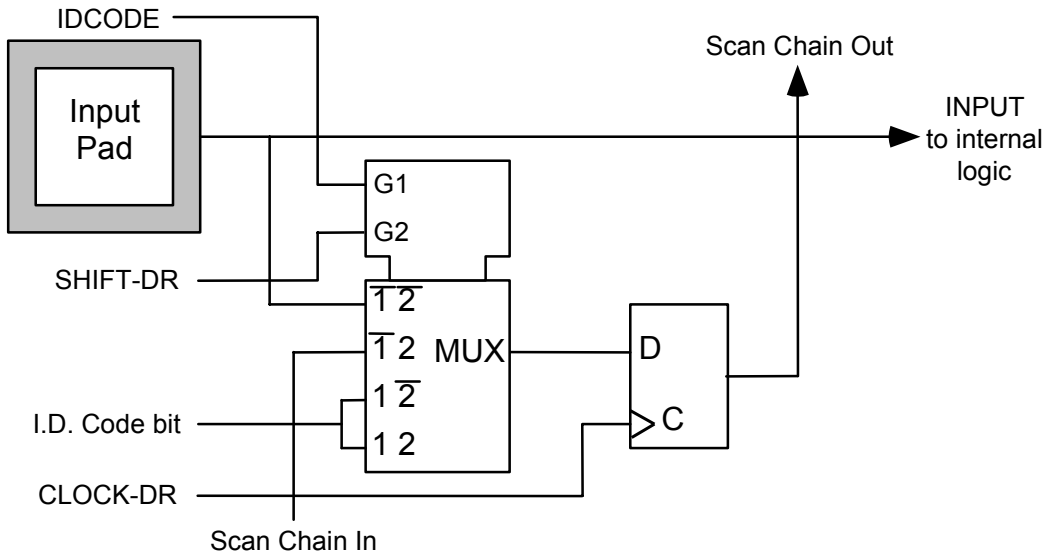


Figure 9 Output Cell (OUT_CELL)

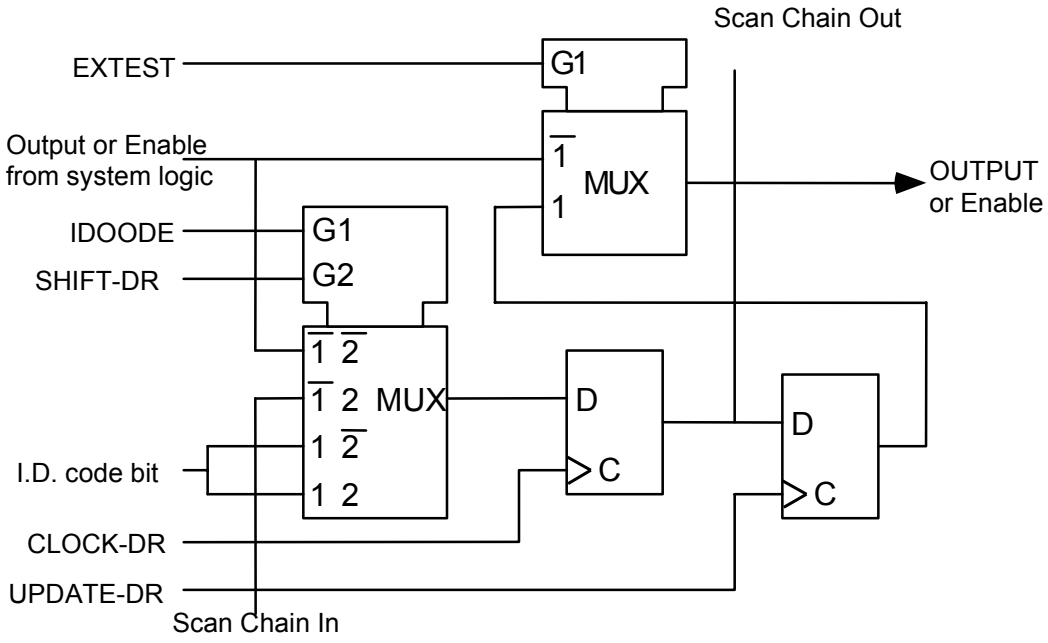


Figure 10 Bi-directional Cell (IO_CELL)

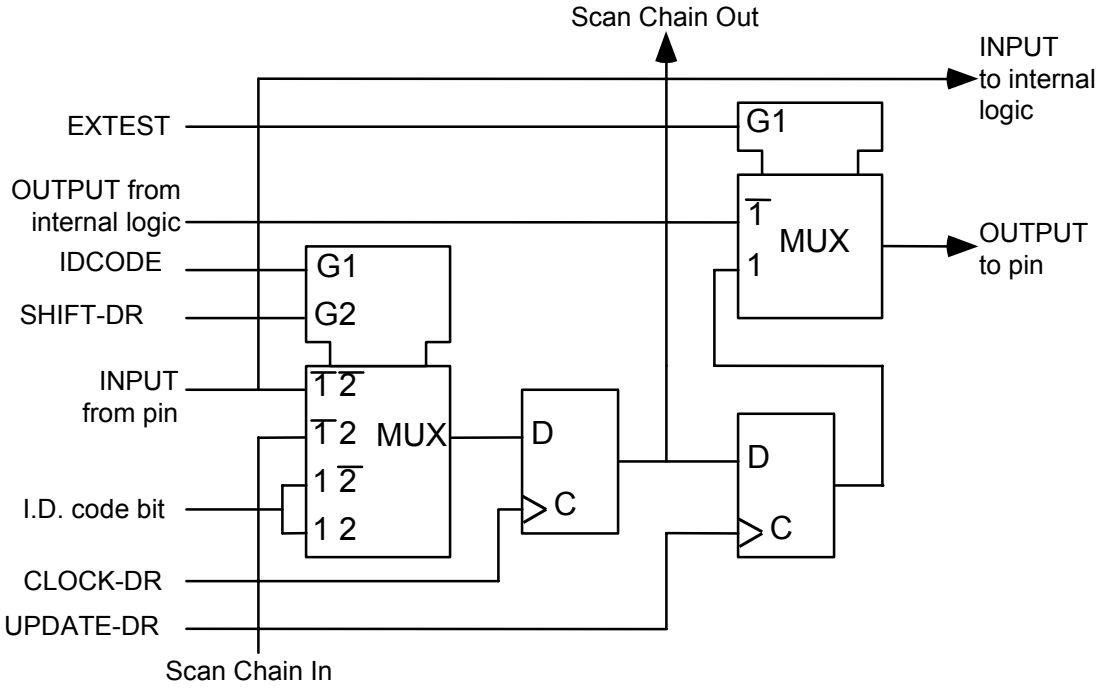
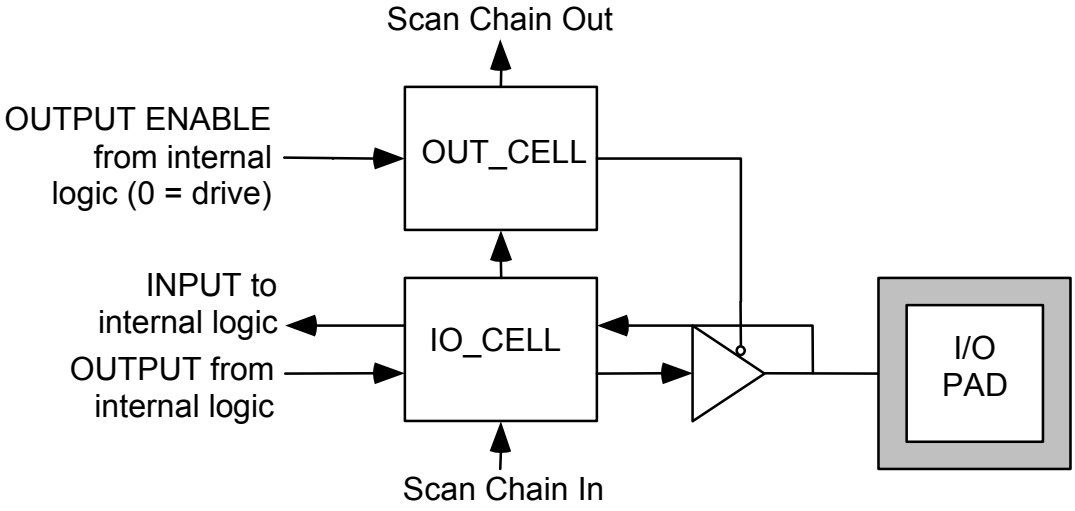


Figure 11 Layout of Output Enable and Bi-directional Cells



12 Operation

There are several important aspects regarding the operation of TSE-based cross-connect fabrics; these are dealt with in turn in the following sections.

12.1 Power Conservation

In order to realize power savings, unused LVDS links may be disabled individually. This is accomplished by setting the RX_ENB and DRU_ENB to logic "1" for the receive channels, and by setting the TXLV_ENB and PISO_ENB registers to logic "1" for the transmit channels.

For greater power savings, each face (group of 16 links) of the TSE can be powered down individually if none of the LVDS links are in use. In addition to disabling the receive and transmit channels for the face, setting the CSU_ENB register bit to logic "1" will idle the corresponding CSU, which will greatly reduce power. The power reductions are summarized in the following table:

Table 17 Power Reduction for Disabled Links

Block	Control Bit	Power Reduction (in mW)			Remarks
		VDDI	AVDL	AVDH	
TXLV	TX_ENB=1	0	0	54	
RXLV	RX_ENB=1	0	5	7	
DRU	DRU_ENB=1	16/20	0	0	16 mW if the CSU is active, otherwise 20
PISO	PISO_ENB=1	10	0	0	
CSU	CSU_ENB=1	0	350	50	
Bi-directional Link		26	5	61	TXLV, RXLV, DRU, and PISO Disabled
Face		480	430	1026	16 links, CSU Disabled

Note:

These power reductions are approximate and have not been characterized.

12.2 LVDS Optimizations

The LVDS interface implemented on the TBS and TSE follows the IEEE 1596.3-1996 specification with some minor exceptions. The changes are implemented to customize and optimize the LVDS interface for the system and are described in detail below. Even with these differences the LVDS interface should be compatible with the physical layer of other LVDS interfaces. The differences from the IEEE specification include:

1. Faster rise/fall times (200 – 400) ps versus the specified (300 – 500) ps. Faster edge rates are commonly used with higher speed LVDS interfaces in the industry to ease the interfacing. The IEEE 1596.3-1996 edge rates are optimized for data rates below 400 Mbps Hysteresis is not implemented in the receive LVDS interface.

2. Hysteresis is used in many implementations to negate the effect of noise that may exist on unused LVDS links. Hysteresis was not implemented in the CHESS™ set devices to minimize circuit complexity, power and cost. Instead, the RX interfaces and the DRUs for unused links can be disabled (powered down) through register control in order to prevent sensitivity to noise on these links

3. The LVDS transmitter contains an on-chip 100-ohm termination. Most implementations have single 100-ohm termination on the receiver. By implementing a double termination (on both the LVDS receiver and transmitter) a higher signal integrity and matching is ensured.

4. Although not a difference with the Layer 1 IEEE 1596.3-1996 specification, the Layer 2 8B/10B encoding is discussed here for completeness. 8B/10B encoding guarantees transition density as compared to scrambled encoding, which provides only a certain probability of transition density. This guaranteed transition density allows a simpler and more power-effective data recovery unit, provides a more robust serial interface (greater trace or back-plane distance achievable). It also negates the need for complete SONET framing since the A1A2 and J0 bytes can be encoded into special escape characters of the LVDS data stream.

5. The device uses 20% resistors; not 10% as specified by the LVDS specification. They are 20% resistors since that was the highest tolerance resistor available for on-chip applications. However, because they are integrated on-chip, this LVDS interface can achieve much better signal integrity than one with off-chip terminations.

12.3 LVDS Hot Swapping

The LVDS electrical interface differs from a standard CMOS interface; there is no inherent problem in leaving the LVDS inputs floating. Note that the LVDS receiver consists of a differential amplifier with a wide common-mode range. The power dissipation is independent of the data transitions (that is, if the input is connected). There is an internal 100 Ω termination across the positive and negative input. Floating inputs will settle to an arbitrary voltage (between VDD and VSS) determined by leakage paths. Regardless of this arbitrary voltage, the input structure of the receiver will operate in its proper range and the receiver output will be logic 1 or 0 depending on internal offsets. Noise events (power supply noise, crosstalk) may induce the receiver to toggle randomly, generating "ambiguous" data.

Unused links should be disabled in software. This will ensure that the power consumption for those links will be reduced to nearly 0 mW. There is no requirement for how quickly the link should be disabled. Disabling the link simply results in lower power dissipation since the circuitry will be shut down. This action is not mandatory, but is good practice.

During a hot-swapping situation, there will be no electrical damage on the LVDS inputs provided that maximum ratings are not exceeded (see absolute maximum ratings section 14). The “hot-swap” channel can be left enabled and the device will sync up once the far end transmitter is connected. There are no effects on other channels. Hot swapping of cards is still allowed by reprogramming of the links in software.

12.4 LVDS Trace Lengths

The TSE utilizes 64 different input and output differential LVDS pairs. It is critical to match the lengths of the positive and negative traces of each differential pair to minimize skew and maximize the eye opening. However, matching one differential pair to another pair is not as important. The high-speed serial LVDS links are connected to a 24 word (10 bit byte) FIFO. Of this 24 word FIFO, 8 words should be allocated for clock skew and wander between cards or within devices. The remaining 16 words are then available to accommodate clock skew and wander between cards or within devices, along with differences in trace lengths between LVDS pairs.

The 16 word FIFO yields an allowable inter-link delay differential of 205.8 ns or 41.2m. This is calculated as follows:

16 words x 10 bits/word = 160 bits of margin in FIFO

1/(777.6 Mb/s) = 1.29 ns/bit on the serial link

160 bits x 1.29 ns/bit = 205.8 ns of margin = 16 clock cycles (at 77.76 MHz)

A transmission speed of 2/3 the speed of light, this corresponds to a trace length difference of 41.2m:

$205.8x10^{9}$s x 2/3 x $3x10^{8}$ m/s = 41.2 m

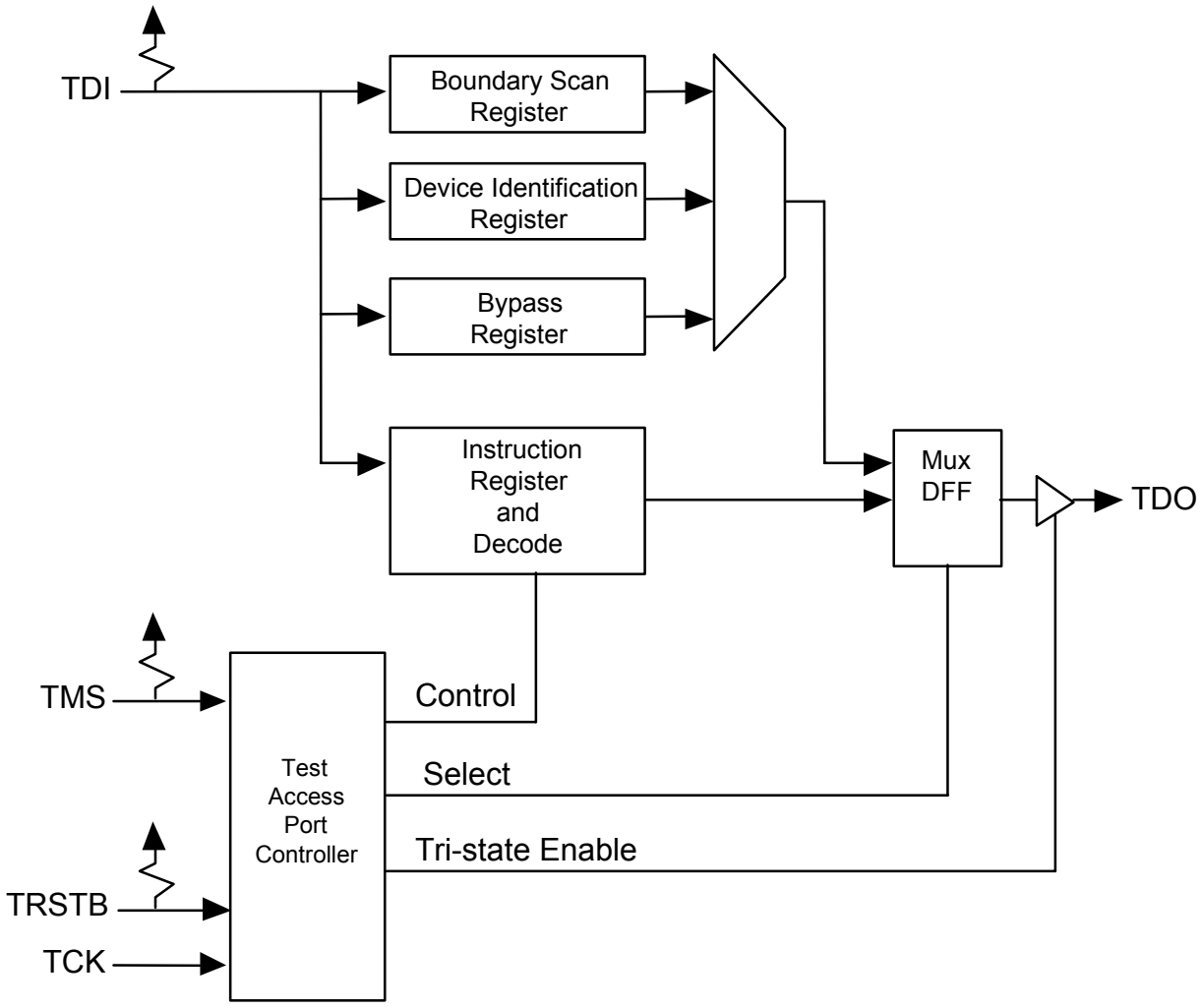
However, it is important to note that the LVDS interface itself is designed to drive 1m of backplane plus only 30cm of trace length on either side. Since this 1.6m of trace length is smaller than the maximum trace length differential computed above, the TSE's ability to tolerate trace length differential will not be a limiting factor for designs.

The total available trace length of 1.6m corresponds to 8ns of delay or a worst case difference of 0.6 clock cycles (77.76 MHz) between any two LVDS links. Low loss cable or an optical interface can be used to connect to the LVDS interface to realize greater back-plane distances.

12.5 JTAG Support

The TSE supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 12 Boundary Scan Architecture



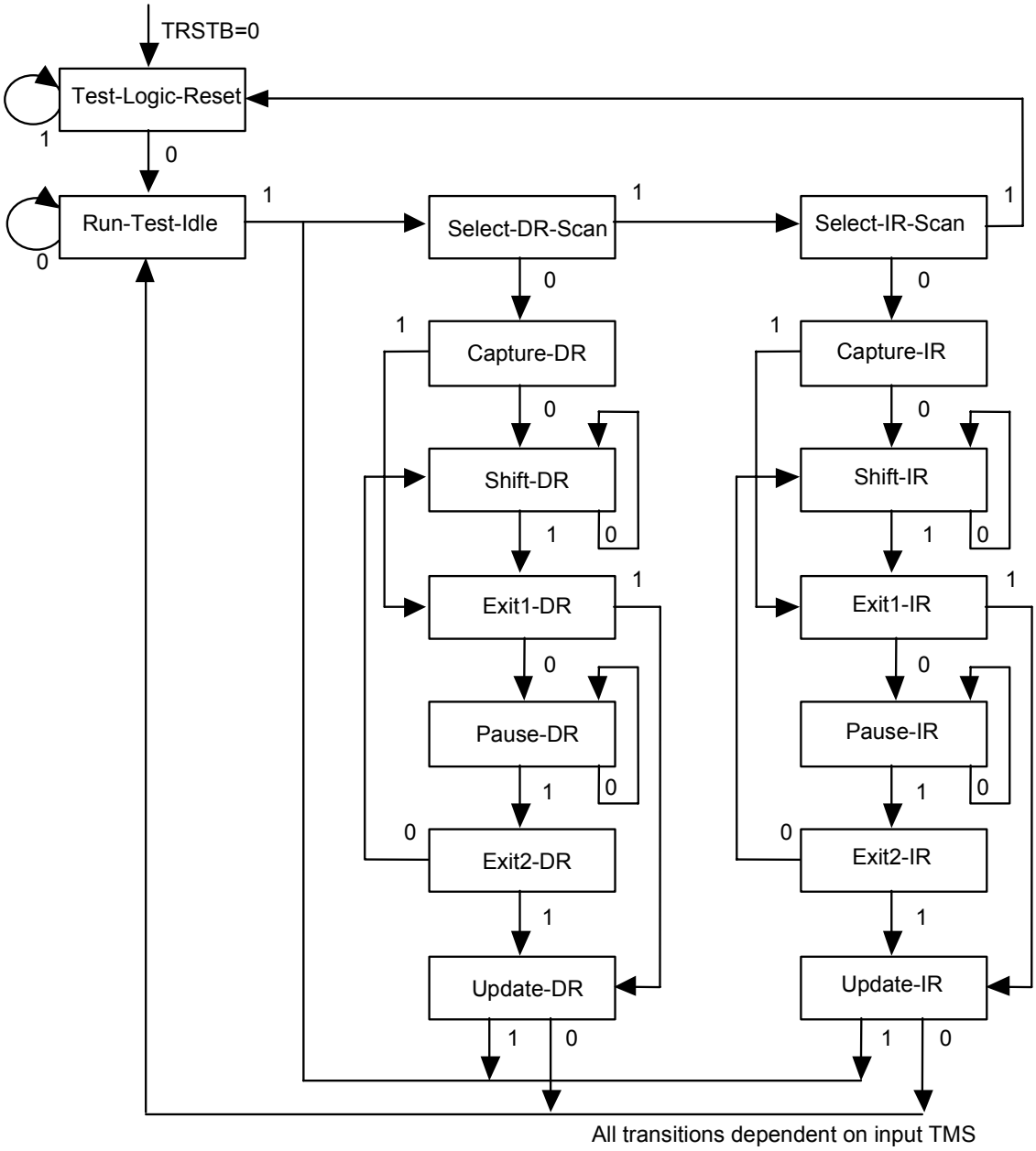
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

12.5.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 13 TAP Controller Finite State Machine



12.5.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

12.5.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

12.6 Initialization Procedure

The following is a suggested initialization procedure which may be helpful when writing initialization code for the TSE.

Set the TSE Master Configuration register to: ETSE_MODE=0, ITSE_MODE=0, set addr 002h to 8400h

Set the CSU Control registers to: CSU_ENB=0, CSU_RSTB=1
set addresses 0020h, 0024h, 0028h, 002Ch to 0409h

Set the SSWT RJ0FP Delay register 0040H as per section 1.1

Set the SSWT TJ0FP Delay Register 0047H as per section 1.1

Set the R8FA 1 – 64 Analog Control register to: DRU_ENB=0, RX_ENB=0 and DRU_CONTROL=1101
set addresses 0N83h, 0N8Bh, 0N93h, and 0N9Bh (N=0 to F) to CC34h

Set the ITSE 1- 16 time slot switching settings as per switching requirements.

Set the ETSE 1-16 time slot switching settings as per switching requirements.

Set the SSWT 1-16 space switching settings as per switching requirements.

Set the T8DE 1 – 64 Analog Control registers to: TXLV_ENB=0, PISO_ENB=0
set addresses 0NB5h, 0NBDh, 0NC5h, and 0NCDh (N=0 to F) to 0007h

Ensure that the CSUs show stable “locked” status by reading registers 0x21/0x22, 0x25/0x26, 0x29/0x2A and 0x2D/0x2E:
Read registers 0x21, 0x25, 0x29 and 0x2D – expect to see 0x01 representing the interrupt from changes in lock state during reset.
Read registers 0x21, 0x25, 0x29 and 0x2D again – expect to see 0x00 indicating stable lock status.
Read registers 0x22, 0x26, 0x2A and 0x2E – expect to see LOCKV bit set to 1 indicating that the CSUs are stable in the locked state.

After the CSUs have locked, the transmit FIFOs must be re-centered since they will have suffered over-run or under-run conditions while the CSUs were not locked. To re-center the FIFOs, write a 1 to the CENTER bit in all 64 of the T8DE Control and Status registers (0NB0h, 0NB8h, 0NC0h, and 0NC8h where N=0 to F).

Enable all interrupts on the device by writing registers as follows:

CSTR 1 – 4 Addr 0021h, 0025h, 0029h, and 002Dh to ----------1b

SSWT Addr 0043h to ----------1b

R8FA 1- 64 Addr 0N80h 0N88h, 0N90h, 0N08h (N=1 to 15) to --------1111----b

ITSE 1- 16 Addr 0NA2h (N=0 to 15)to 00001h

ETSE 1- 16 Addr 0NAAh (N=0 to 15)to 00001h

T8DE Addr 0NB0h, 0NB8h, 0NC0h, 0NC8h to ----------1----b

12.7 Interrupt Service Routine

The TSE will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

Read the registers 0003H – 000EH to find the functional block(s) which caused the interrupt.

Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

Service the interrupt(s).

If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

12.8 Interpreting the Status of Receive Decoders

The receive decoder blocks (R8FA) produce interrupts based on four receiver conditions or events: OCA (Out of Character Alignment), OFA (Out of Frame Alignment), FUO (FIFO Underrun/Overrun) and LCV (Line Code Violation). Understanding the relationships between these conditions can help to diagnose device status. These conditions have the following inter-relationships:

OCA implies OFA until character alignment is re-achieved. OCA will most likely cause some LCVs but not necessarily a continual stream of them. Since character boundaries are not known, framing and disparity are effectively meaningless anyway.

OFA, by itself, does not cause any of the other conditions.

FUO may produce zero, one or many LCVs, depending on how the FIFO overrun/underrun occurs.

Persistent LCVs (five or more in any sequence of 15 characters) cause OCA.

12.9 Accessing Indirect Registers

Indirect registers are used to conserve address space in the TSE. Writing the indirect address register accesses indirect registers. The following steps should be followed for writing to indirect registers:

Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

Write the desired configurations for the channel into the indirect data registers.

Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

Read the indirect data registers to find the state of the register bits for the selected channel number.

12.10 Using the Performance Monitoring Features

The performance monitor counters within the TSE are the R8FA line code violation counters. The counters will saturate and not roll over if they reach their maximum value.

A device update of all the counters can be achieved by writing to the TSE Master Clock Activity and Accumulation Trigger register (0001H). The TIP bit in the TSE Master Clock Activity and Accumulation Trigger register can be polled to determine when all the counter values have been transferred and are ready to be read.

12.11 "J0" Synchronization of the TSE in a CHESS™ System

Any TSE/TBS fabric can be viewed as a collection of different stages. For example, a Time-Space-Time switch could be constructed with five datapath stages:

1. Ingress load devices (e.g. SPECTRA-2488™)
2. Ingress TBS devices
3. TSE devices
4. Egress TBS devices
5. Egress load devices (e.g. SPECTRA-2488)

Note that in some cases, one physical device may serve in two stages, such as stages 1 and 5 or stages 2 and 4. STS-12 frames are pipelined through this fabric in a regular fashion, under control of a single clock frequency (77.76 MHz). In order to maintain valid framing for the group of STS-12 streams, the datapath devices must be coordinated with one another. The first step in this coordination is the use of a global frame synchronization pulse to mark the position of frame boundaries as they enter the fabric. However, since each device in the system datapath sees the STS-12 frames at a different latency than other devices, there must be a mechanism to account for the individual latencies at different points along the datapath.

The most significant source of delay is the cumulative latency of the devices that lie along the system datapath. To accommodate different system arrangements, a synchronization frame pulse and a programmable frame delay register are used to re-frame the STS-12 streams for each system datapath device. In the TSE, this FIFO is 24-words deep and is controlled by the RJ0FP pin along with the RJ0DLY register. This frame delay register is used to inform the TSE of the latency between a frame pulse on the RJ0FP pin and the presence of J0 characters in the FIFOs so that a re-framing mechanism can be triggered at the appropriate time. Because the J0 characters may lie at different FIFO depths, due to skew between links, this re-framing can be achieved by realigning the FIFO read pointers to match the J0 positions.

In addition to device latencies, there are other sources of delay. Furthermore, these delays may vary from link to link. For example, clock skew or differential trace lengths impose uneven delays on individual links. The 24-word depth of the FIFOs allows these delays to be equalized as part of the re-framing process. When the RJ0FP-RJ0DLY trigger signals the occurrence of a frame boundary, the TSE will adjust the FIFOs read positions to realign the STS-12 streams' J0 characters with one another. As long as the J0 characters from all the STS-12 streams are indeed simultaneously present in their respective FIFOs when this occurs, the TSE will effectively re-align the streams as part of the re-framing process. The large FIFO depth allows the TSE to compensate for such differential delays as trace lengths that vary by several meters. Smaller delay variances, such as those due to clock jitter, can be absorbed automatically by the serial receive links. If they prove to be too large for such absorption, they will then be corrected through the FIFO re-framing process.

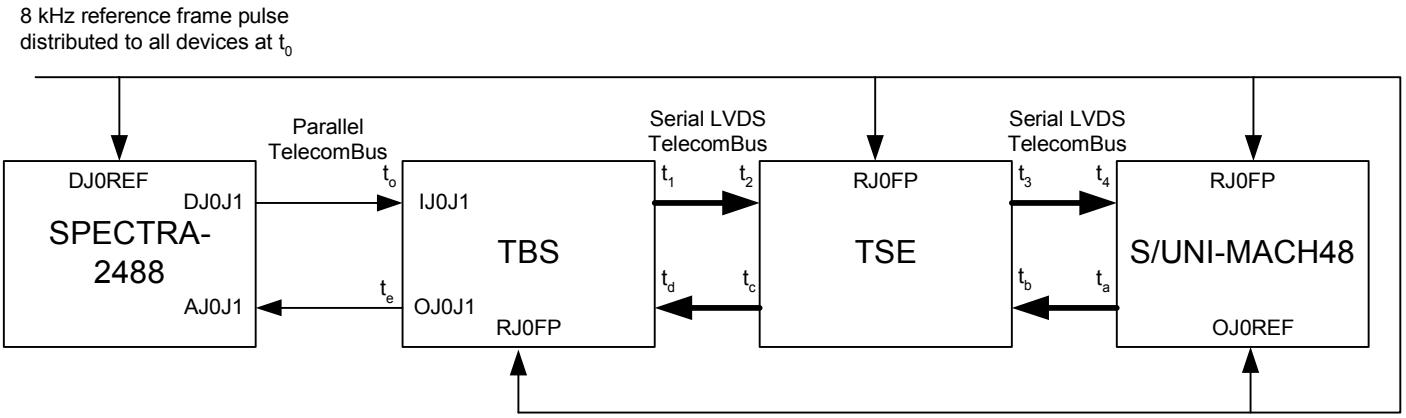
In order to guarantee that the RJ0FP-RJ0DLY trigger will happen when all streams' J0 characters are simultaneously present within the FIFOs, it is important to choose correct values for the frame delay register. The following example explains how frame delay register values are chosen for the devices of a sample system. Consider the implementation shown in Figure 14. All devices receive the global frame pulse simultaneously at time t0 (ignoring any trace length differentials). The SPECTRA-2488 emits the J0 byte onto the TelecomBus upon receiving the global frame pulse on the DJ0REF input. This action is entirely independent of receiving a J0 byte from the optical line. SPECTRA-2488 pointer adjustments will define the start of the payload envelope (the J1 byte indicates start of payload) and this payload will be outputted over the TelecomBus. The SPECTRA-2488 can be viewed as the master by which the synchronization of the other CHESS devices is determined. The TBS expects the four incoming eight bit 77.76 MHz TelecomBus data paths to be synchronized and upon processing emits the serialized data with J0 character 33 clock cycles after receiving the J0 on the parallel TelecomBus. The J0 byte on each of the twelve independent 777.6 MHz LVDS links are not exactly simultaneous and may have a slight amount of skew relative to each other (because of presence of an 8 word FIFO on the LVDS transmitter output). The LVDS links are then mated to the TSE through a back-plane. The TSE is programmed (via indirect register access of the RJ0DLY[13:0] word) to expect the J0 byte a certain number of clock cycles after it receives the global frame pulse.

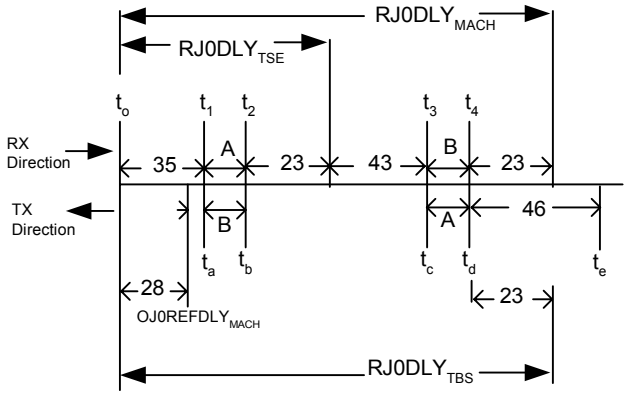
The ingress FIFOs permit a variable latency in J0 arrival of up to 16 clock cycles. That is, the largest tolerable delay between the slowest and fastest LVDS link of the 64 TSE LVDS links is 16 bytes. Consequently, the external system must ensure that the relative delays between all the 64 receive LVDS links be less than 16 bytes. The minimum value for the internal programmable delay (RJ0DLY[13:0]) is the delay to the last (slowest) J0 character plus 15 bytes. The maximum value is the delay to the first (fastest) J0 character plus 31 bytes. The actual programmed delay should be based on the delay of the "slowest" of the 64 links – the link in which J0 arrives last plus a small safety margin of 1 or 2 words. The magnitude of the clock cycle delay is bounded by two parameters. First, the programmed delay register RJ0DLY is 14 bits. This implies that a clock cycle delay of 214 –1 or 16,383 clock cycles can be programmed. However, the second parameter, the frame rate (125 µs), bounds the delay to one STS-12 frame or 9719 (9719 unique values) clock cycles (125 µs x 77.76 MHz), after which the next SONET frame begins. The TSE, upon receiving the global frame pulse, will wait the programmed amount of time (56 clock cycles + cable length delays) before prompting each of the 64 links to emit their J0 character.

The number of clock cycles can be determined by simply adding the relevant device and cable length latencies.

This synchronization mechanism is flexible enough to accommodate system paths with different cumulative device latencies. Consider a TSE that is mated to a S/UNI-MACH48 on one link and a SPECTRA-2488 feeding a TBS on the other link. The alternate data paths have different delays; the SPECTRA-2488/TBS link has a greater delay than the S/UNI-MACH48 link delay. In this case, the S/UNI-MACH48 is programmed to emit the J0 pulse later than SPECTRA-2488 (but aligned with the TBS serial output) such that the J0 from both sources arrive at the TSE within the allowed 16-clock cycle window. The S/UNI-MACH48 programmed delay is 24 clock cycles after the receipt of the frame pulse.

Figure 14 "J0" Synchronization Control





In the line side RX direction:

1. An 8kHz frame pulse is received by all devices at time t_0
2. Upon receipt of the 8kHz frame pulse, the SPECTRA-2488 outputs data (and J0) onto the TelecomBus at time t_0
3. The TBS emits the serialized J0 8B/10B character approximately 35 clock cycles later at time t_1
4. The J0 character arrives at the input of the TSE A clock cycles later at time t_2. A and B represents the clock cycle delay of the links.
5. The TSE RJ0DLY value can be set to create a receive FIFO depth of approximately half the FIFO length of 24 characters. The J0 character will be in the FIFO along with 11 more characters approximately 23 clock cycles after the J0 character enters the TSE input. The cumulative time in SYSCLK cycles from t_0 to t_z plus the extra 23 clock cycle delay into the TSE receive FIFO is the the time that should be used for the RJ0DLY value.
6. The TSE emits the J0 characters approximately 43 clock cycles after the J0 characters are read out of the receive FIFOs (t_0 + RJ0DLY) at time t_3.
7. The J0 character is present at the MACH48 device B clock cycles later at time t_4
8. The S/UNI-MACH48 RJ0DLY value should be set using the same method as used to set the TSE RJ0DLY value. (RJ0DLY = J0 character arrival time + 23 clock cycles to fill the receive FIFO halfway.

In the line side TX direction:

1. An 8kHz frame pulse is received by all devices at time t_0
2. Approximately 7 + OJ0REF SYSCLK cycles after receiveing the the 8 kHz frame pulse on OJ0REF, the S/UNI-MACH-48 outputs the J0 character to the TSE device . Since the arrival of J0 characters at the TSE receivers from the TBS and the S/UNI-MACH-48 must be aligned, the OJ0REFDLY value at the S/UNI-MACH28 should be set to the cumulative latency of the TBS in SYSCLK cycles (33-36) minus the 7 delay between OJ0REF and the J0 character output when OJ0REFDLY=0.
3. The TSE outputs the J0 character at time t_c
4. The TBS receives the J0 character at time t_d. Approximately 23 clock cycles following the arrival of the J0 character, the TBS receive FIFO will be half full. The cumulative time from t_0 to t_d in SYSCLK cycles plus the additional 23 cycle delay into the TBS receive FIFOs should be used for the TBS RJ0DLY value.

NOTE: In all cases J0 character arrival times specified are the nominal arrival times. This is because the TX FIFO can impose a +/-4 cycle delay on the data. The nominal time assumes the additional delay by the TX FIFO imposed is 0 cycles in all cases. The calculated RJ0DLY values provided in the example will work in any case - the receive FIFOs may just be more or less full than stated (12 characters full), depending on the state of the upstream TX FIFO.

12.12 Synchronized Control Setting Changes

The TSE supports dual switch control settings. These dual settings permit one to be operational while the other is updated as a result of some new connection requests. The CMP input selects the current operational switch control settings. CMP is sampled by the TSE on the base timing pulse *t.* The internal blocks sample the registered CMP value as they receive the next J0 character –at least a delay of RJ0DLY. The new CMP value is applied on the first A1 character of the second following STS-12 frame. This switchover is hitless; the control change which does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted (see the discussion of the connection routing algorithm in this document).

12.13 Fabric Rules of Composition.

There are rules governing how the TSE, the TBS, the Load devices (SPECTRA-2488, SPECTRA-4X155, and S/UNI-MACH48), can be combined to form legal fabrics. A hypothetical Load device with an on-board TBS is also considered. This section describes the interconnecting buses, gives a behavioral description of the four components, lists the rules of composition for fabric formation, and gives several examples of legal fabrics.

12.13.1 Interconnections

The various components communicate via two full-duplex channel types: Parallel TelecomBuses (P-TCB) and Serial TelecomBuses (S-TCB). The S-TCBs are always point-to-point. The P-TCBs can be either point-to-point, or can be combined with one stage of wired-or multiplexing. Both buses carry 4*STS-12 = STS-48 streams (i.e., they can be thought of as a single STS-48 flow, or as four independent STS-12 flows – the TSE will always treat each STS-1 independently in any case.) In the diagrams below, P-TCBs are drawn as heavy directed arrows; S-TCBs are drawn as lighter arrows.

12.13.2 Behavioural Descriptions of Components

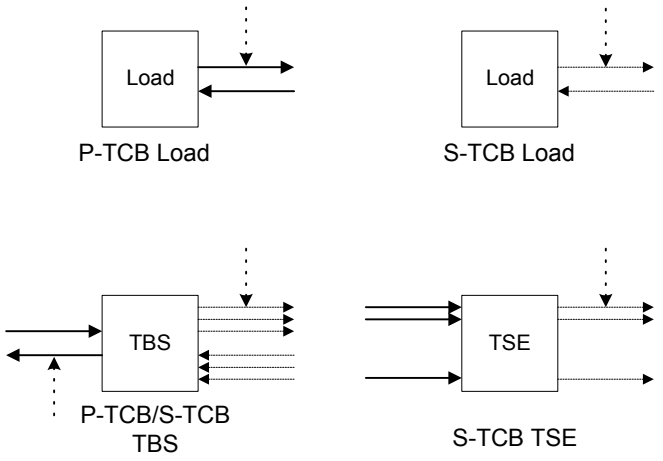
Load: Load devices (SPECTRA-2488) have one full-duplex P-TCB port. We ignore the line side of these devices. Loads are represented in Figure 15.

TBS: TBS devices have one P-TCB port and three S-TCB ports. The TBS can take any of 3*48 STS-1s from the ingress S-TCBs and place it in any of 48 STS-1 slots in the egress P-TCB. In the other direction, the TBS can fill any of the 3*48 egress S-TCB slots with any STS-1 taken from the ingress P-TCB.

TSE: TSE devices have 64 full-duplex S-TCB ports. The TSE implements a full Time:Space:Time switching function, as described in this document.

Each component emits synchronized STS frames with a time delay controlled by the timing signal described in the "J0 Synchronization" section. These timing signals are indicated by the arrows directed at the egress ports of each component.

Figure 15 Fabric Components



(heavy data flow lines are P-TCBs; light data flow lines are S-TCBs; arrows to data flow lines are timing controls).

12.13.3 Rules of Composition

No connections other than egress P-TCB to ingress P-TCB and egress S-TCB to ingress S-TCB are permitted.

Each TSE fabric must have a central column (or multiple columns) of TSE devices through which all traffic is switched.

All traffic must arrive at the central TSE column at the same time (with respect to STS-12 frames).

All paths from any LOAD's egress P-TCB to any LOAD's ingress P-TCB must traverse sequences that are identical in time and components as they pass through the TSE core. Where the common core path extends out to the Load devices, this rule includes paths from any LOAD A to any LOAD B, the reverse paths from B to A, and any self-loops from A to A or B to B. As mentioned below, some Loads may be further from the core, their paths being extended by the use of extra TSE devices which serve as gather/scatter devices for low aggregate bandwidth Loads. These extended path portions need not be identical to other paths, but they must be traversed before and after the common core paths.

Time delays on all longest simplex paths must begin with zero at the source LOAD (The longest paths are those paths that are extended, if any. Normally, all paths are "longest" and all begin at time zero.). The time delays on all paths must be strictly increasing, and the delays on all path delays must be identical when they reach the TSE core column.

12.13.4 Examples of Legal Composition

The following figures give examples of legal fabric compositions. Appropriate time delays are indicated by monotonically increasing integers.

Figure 16 LOAD:LOAD Null Fabrics.

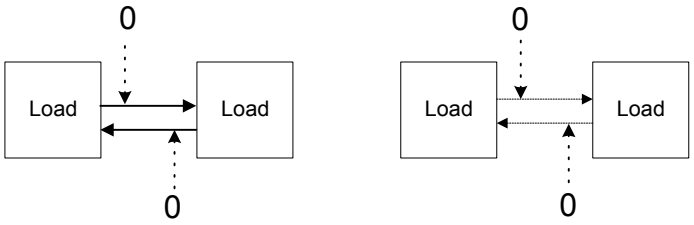


Figure 17 TBS Fabrics (non-redundant).

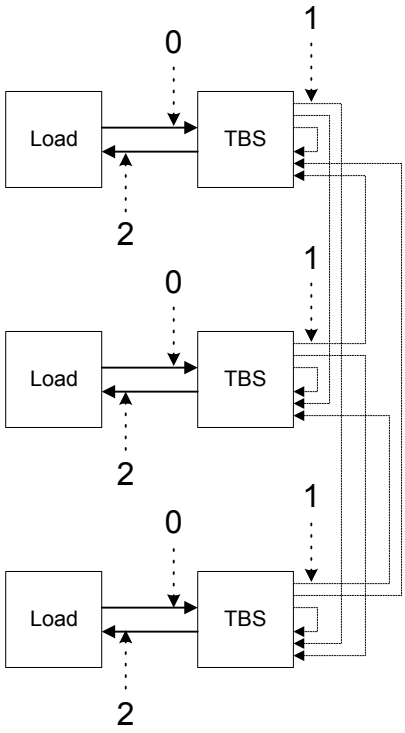
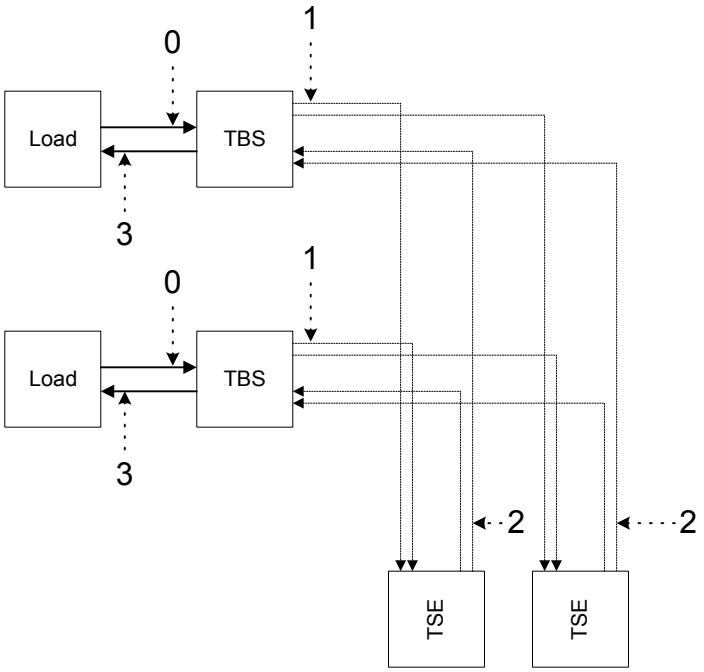


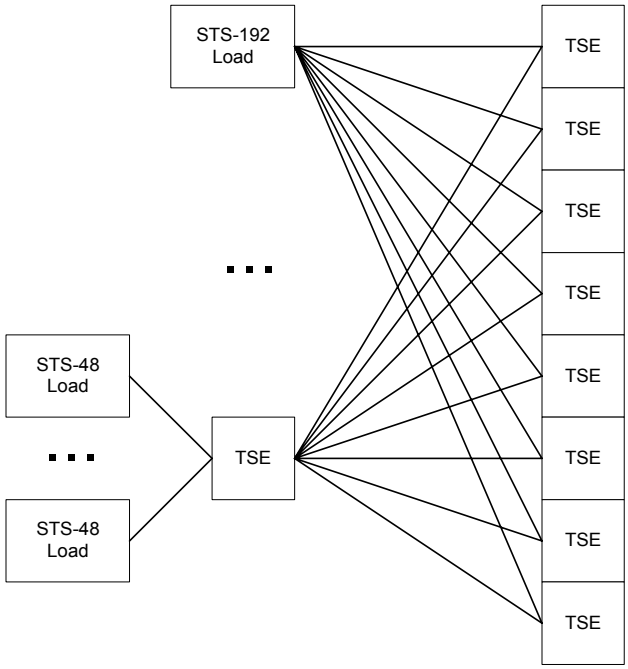
Figure 18 TSE Fabric (redundant).



Where STS-12 and/or STS-3 devices are connected to TSE fabrics, these same rules apply, but the TBS devices connect to multiple load devices. In multi-plane TSE fabrics, TBS devices which service these lower rate devices serve as traffic distributors and collectors to permit STS-12/3 samples to be switched to and from any STS-1 in the fabric.

An example of the use of a TSE as a gather/scatter device in an eight plane TSE fabric is illustrated in Figure 19 below. The point of this figure is to illustrate the need for unequal path lengths that meet at the same time in the TSE core.

Figure 19 TSE Fabric with Differing Path Lengths

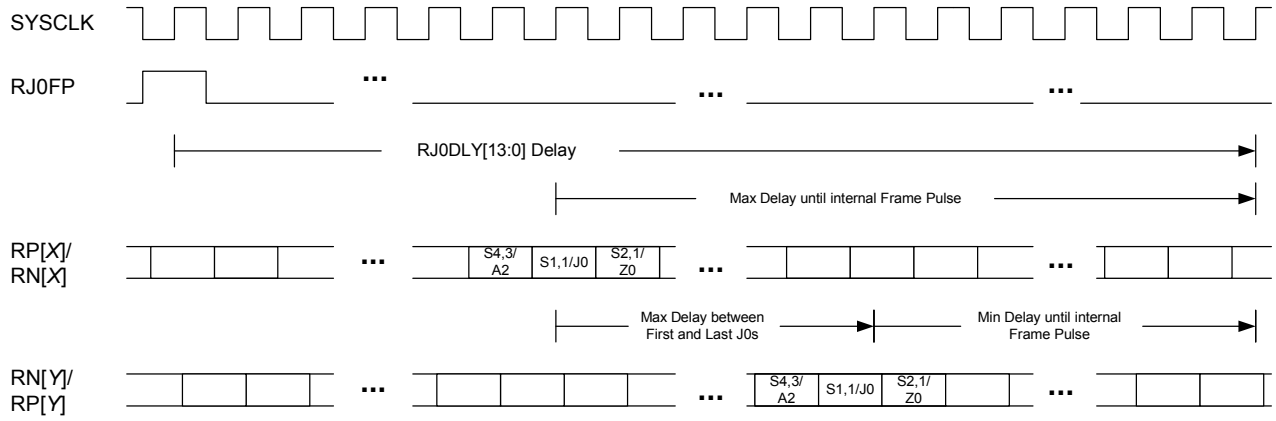


13 Functional Timing

13.1 Receive Interface Timing

Figure 20 below, shows the relative timing of the receive interface. The LVDS links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RJ0FP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other but are frequency locked. The delay from RJ0FP being sampled high to the first and last J0 character is shown in Figure 20. In this example, the first J0 is delivered on link RN[X]/RP[X]. The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, link RN[Y]/RP[Y] is shown to be the slowest. The minimum value for the internal programmable delay (RJ0DLY[13:0]) is the delay to the last J0 character plus 15. The maximum value is the delay to the first J0 character plus 30. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes. The relative phases of the links in Figure 20 are shown for illustrative purposes only. Links may have different delays relative to other links than what is shown.

Figure 20 Receive Interface Timing



13.2 Transmit Interface Timing

Figure 21 below shows the delay from assertion of RJ0FP to the transmit serial data links. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 8 cycles. The minimum delay (RJ0DLY + 40 SYSCLK cycles) is shown to be incurred by one of the transmit serial data links (TP[*X*]/TN[*X*]). The maximum delay (RJ0DLY + 47 cycles) is shown to be incurred by another transmit serial data links (TP[*Y*]/TN[*Y*]). The suggested setting for TJ0DLY results in a TJ0FP pulse at the time at which all the transmit serial links have transmitted their respective J0 characters. The maximum delay from RJ0FP to the transmission of a J0 pulse is RJ0DLY + 47 cycles. Therefore the suggested setting for TJ0DLY is RJ0DLY+ 47. The relative phases of the links in Figure 21 are shown for illustrative purposes only. Links may have different delays than what is shown.

Figure 21 Transmit Interface Timing

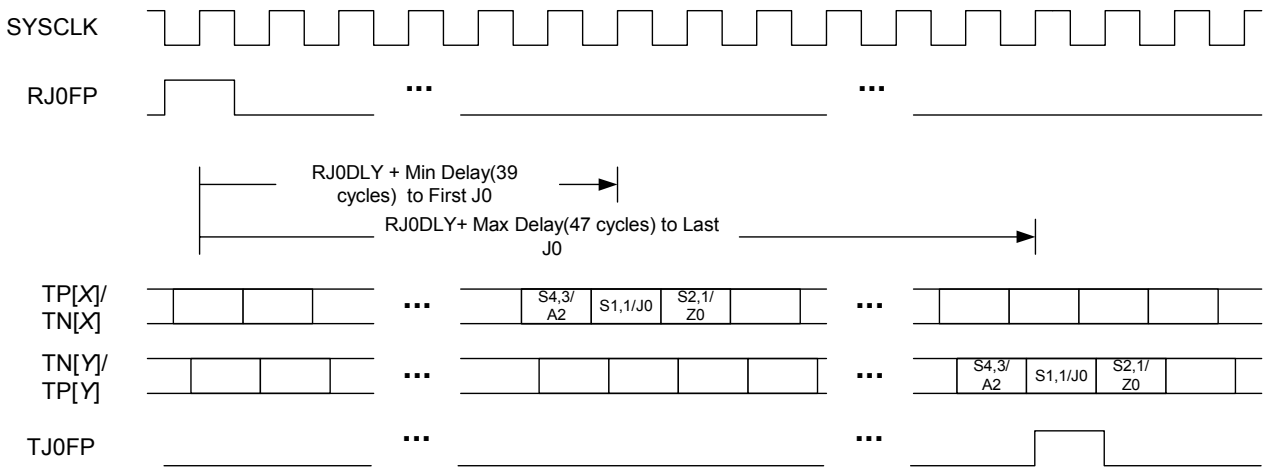


Figure 22 below shows the delay from CMP to the transmit serial data links. CMP is valid only at the RJ0FP pulse time, whether RJ0FP is pulsed or not. It is ignored at other locations in the transport frame. A change in value to the connection memory page signal (CMP) results in changing the active switch settings. Given that CMP is sampled on the RJ0FP pulse time 0, the first data that is switched according to the newly selected connection memory page are the A1 bytes of the second frame following the first J0 byte transmitted by the TSE after offset RJ0DLY + 40 cycles. In more absolute terms, the first A1s transmitted by the TSE between offset RJ0DLY + 40 + 19416 cycles and RJ0DLY + 47 + 19416 cycles, represent the first data switched according the connection memory page selected by CMP at the RJ0FP pulse time 0.

Figure 22 CMP Timing

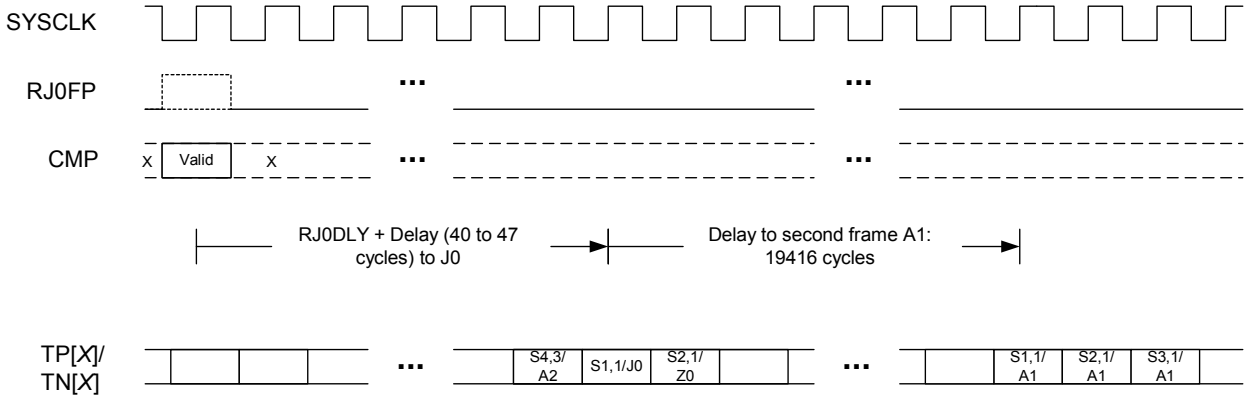
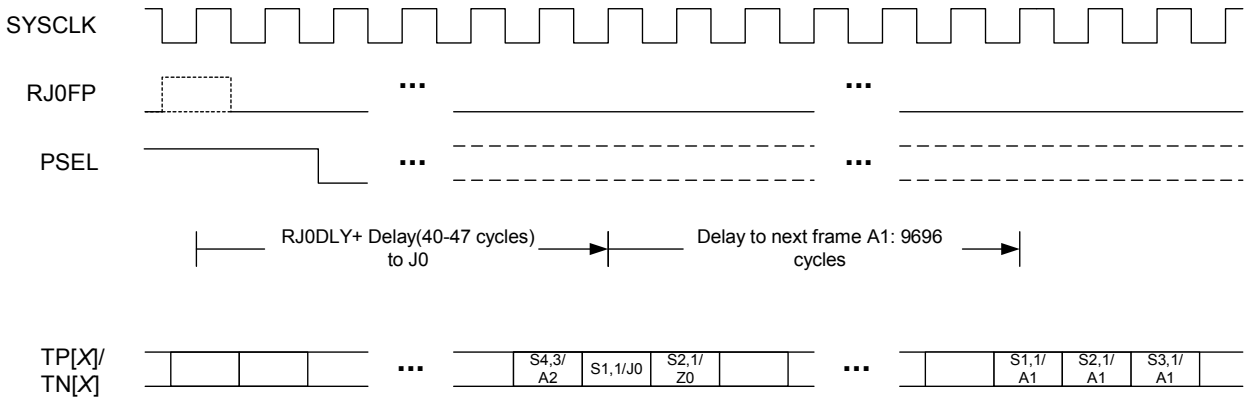


Figure 23 below shows the delay from the PSEL bits, SPSEL, IPSEL, and EPSEL, to their effect datastream at the transmit serial data links. The PSEL bits are written asynchronously with respect to the system clock, so use of the PSEL bits to effect switching connection memory pages should be avoided if switching on a particular frame is required. Additionally the user can avoid changing PSEL bits close to the point in time when PSEL bits are sampled by the synchronous logic. If the frame pulse occurs at time 0, IPSEL is sampled at time RJ0DLY, SPSEL is sampled at time RJ0DLY+15, and EPSEL is sampled at time RJ0DLY+17. Switchover is delayed internally for approximately a frame. Page switchover occurs on frame boundaries, with the A1 bytes switching on the new settings. The frame switched by the newly selected connection memory page first appears on the transmit serial data links between offset RJ0DLY+40+9699 cycles and RJ0DLY+47+9696 cycles.

Figure 23 PSEL Timing



14 Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions. Note: if a voltage is applied to an input pin when the device is powered down, the current needs to be limited below 20mA and the maximum voltage rating does not apply.

Table 18 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
1.8V Supply Voltage (VDDI, AVDL, CSU_AVDL)	-0.3V to +2.5V
3.3V Supply Voltage (VDDO, AVDH, CSU_AVDH)	-0.3V to +4.6V
input pad tolerance	-2V < VDDO < +2V for 10ns, 100mA max
output pad overshoot limits	-2V < VDDO < +2V for 10ns, 20mA max
Voltage on Any Digital Pin	-0.5V to VDDO+0.5V
Voltage on LVDS Pin	-0.5V to AVDH + 0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current on RN[I], RP[I], TN[I], TP[I] pins	±90 mA
Latch-Up Current on RESK pin	±50 mA
Latch-Up Current	±100 mA except RN[I], RP[I], TN[I], TP[I], and RESK
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

15 Power Information

15.1 Power Requirements

Table 19 Power Requirements

Conditions	Parameter	Typ 1,3	High4	Max2	Units
all serial links enabled	$IDDOP_{VDDI}$ (1.8V)	2300	-	2540	mA
	$IDDOP_{AVDL}$ (1.8 V)	775	-	962	mA
	$IDDOP_{VDDO}$ (3.3 V)	1.4	-	2.4	mA
	$IDDOP_{AVDH}$ (3.3 V)	837	-	889	mA
	$IDDOP_{CSU\_AVDH}$ (3.3 V)	42	-	48	mA
	Total Power	8.4	9.2	-	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, Tj=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system.
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current. Outputs are assumed to be loaded with 30pF (if not otherwise specified).
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system.
4. High power values are a “normal high power” estimate, calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: Tj=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics.

15.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. The 1.8 V supplies can come up at the same time or after the 3.3 V supplies as long as the 1.8V supplies never exceed the 3.3V supplies by more than 0.3V.

2. Analog supplies must not exceed digital supplies of the same nominal voltage by more than 0.3V.

3. Data applied to I/O pins must not exceed VDDO by more than 0.3V unless the data is current-limited to 20 mA *.

There are no power-up ramp rate restrictions.

The TSE must be powered down according to the same restrictions above.

* These rules are intended to allow for hot-swap of LVDS signals, as the differential links are appropriately current-limited.

15.3 Power Supply Filtering

The following power supply filtering is recommended to achieve maximum power supply noise tolerance. See Figure 24 for an example RC Filter.

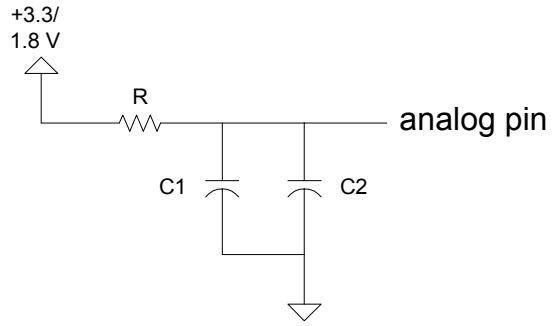
CSU_AVDH: 3.3 ohm, 100nF, 10nF

CSU_AVDL: 0.47 ohm, 4.7 uF, 10nF

Other AVDH: 3.3 ohm, 1.0uF, 10nF

Other AVDL: 0 ohm, 100nF, 10nF

Figure 24 Sample RC Filter



16 D.C. Characteristics

T_a=-40°C to T_j=+125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 5% (Typical Conditions: T_J = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V)

Table 20 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply at 1.8V	1.71	1.8	1.89	Volts	
V_{AVDL}	Power Supply at 1.8V	1.71	1.8	1.89	Volts	
V_{VDDO}	Power Supply at 3.3V	3.135	3.3	3.465	Volts	
V_{AVDH}	Power Supply at 3.3V	3.135	3.3	3.465	Volts	
V_{CSU_AVDH}	Power Supply at 3.3V	3.135	3.3	3.465	Volts	
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage	.1V		0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4		2.8	Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.2			Volts	Applies to SYSCLK, RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to SYSCLK, RSTB and TRSTB only.
I_{ILPU}	Input Low Current	-200	-50	-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2 and 3.

C_{IN}	Input Capacitance		5		PF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		PF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		PF	t_A=25°C, f = 1 MHz
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity			100	mV	
R_{IN}	LVDS Differential Input Impedance	85	100	115	Ω	
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	85	110	115	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing.)

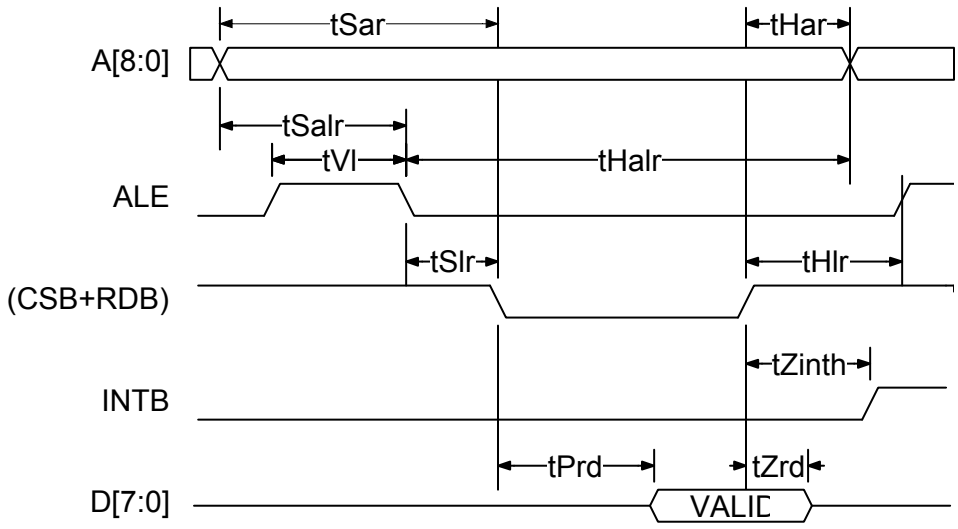
17 Microprocessor Interface Timing Characteristics

Ta=-40°C to Tj=+125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 5%
(Typical Conditions: T_J = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V)

Table 21 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tSar	Address to Valid Read Set-up Time	10		ns
tHar	Address to Valid Read Hold Time	5		ns
tSalr	Address to Latch Set-up Time	10		ns
tHalr	Address to Latch Hold Time	10		ns
tVl	Valid Latch Pulse Width	5		ns
tSlr	Latch to Read Set-up	0		ns
tHlr	Latch to Read Hold	5		ns
tPrd	Valid Read to Valid Data Propagation Delay		70	ns
tZrd	Valid Read Negated to Output Tri-state		20	ns
tZinth	Valid Read Negated to INTB High (WCIMODE=0)		50	ns

Figure 25 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_{L}, tS_{LR}, and tH_{LR} are not applicable.

5. Parameter tH_{AR} is not applicable if address latching is used.

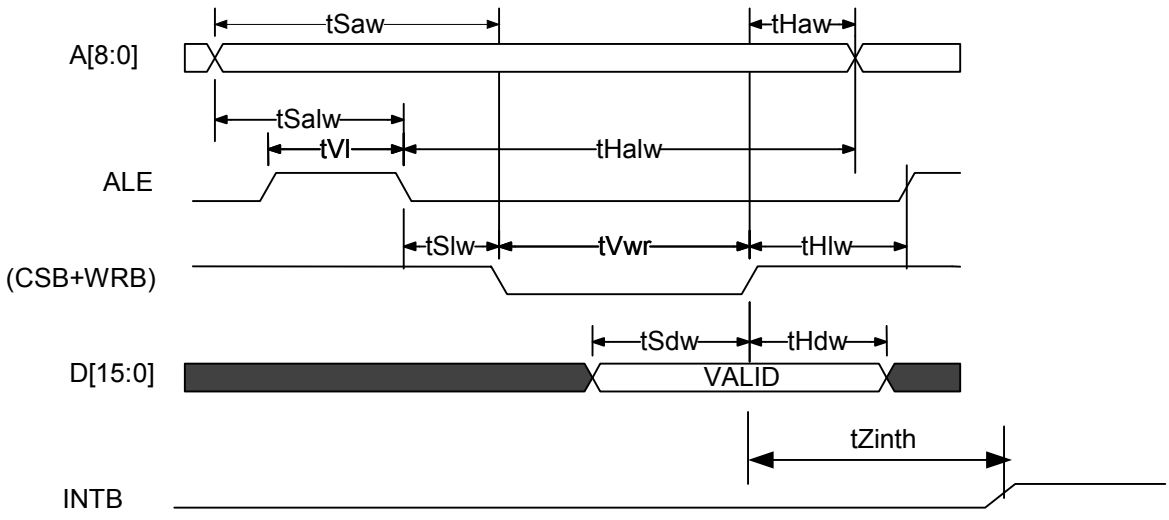
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 22 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
$t^{S}AW$	Address to Valid Write Set-up Time	10		ns
$t^{S}DW$	Data to Valid Write Set-up Time	20		ns
$t^{S}ALW$	Address to Latch Set-up Time	10		ns
$t^{H}ALW$	Address to Latch Hold Time	10		ns
$t^{V}L$	Valid Latch Pulse Width	5		ns
$t^{S}LW$	Latch to Write Set-up	0		ns
$t^{H}LW$	Latch to Write Hold	5		ns
$t^{H}DW$	Data to Valid Write Hold Time	5		ns
$t^{H}AW$	Address to Valid Write Hold Time	5		ns
$t^{V}WR$	Valid Write Pulse Width	40		ns
$t^{Z}INTH$	Valid Write Negated to INTB High (WCIMODE = 1)		50	ns

Figure 26 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2 In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.

3 Parameter tH_{AW} is not applicable if address latching is used.

4 When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5 When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 A.C. Timing Characteristics

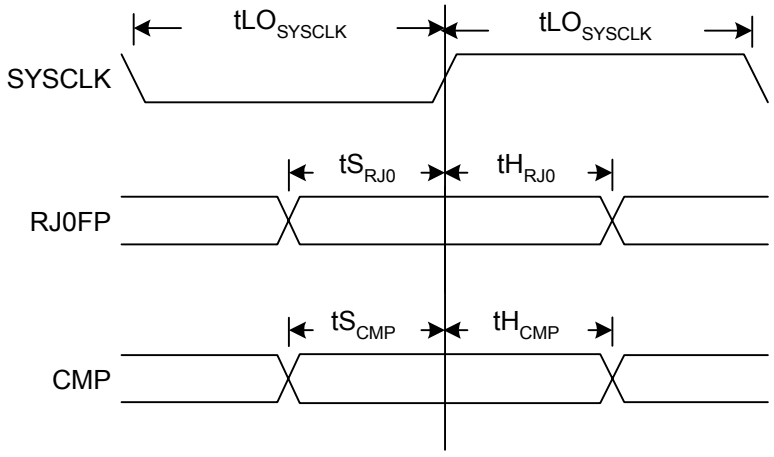
Ta=-40°C to Tj=+125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 5%
(Typical Conditions: T_J = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V)

18.1 Input Timing

Table 23 TSE Input Timing (Figure 27)

Symbol	Description	Min	Max	Units
FSYSCLK	SYSCLK Frequency (nominally 77.76 MHz)	77.76-100ppm	77.76+100ppm	MHz
tHISYSCLK	SYSCLK High Pulse Width	5		ns
tLOSYSCLK	SYSCLK Low Pulse Width	5		ns
tSCMP	CMP Set-Up Time	3		ns
tHCMP	CMP Hold Time	0		ns
tSRJ0	RJ0FP Set-Up Time	3		ns
tHRJ0	RJ0FP Hold Time	0		ns

Figure 27 TSE Input Timing



Notes on Input Timing:

- When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

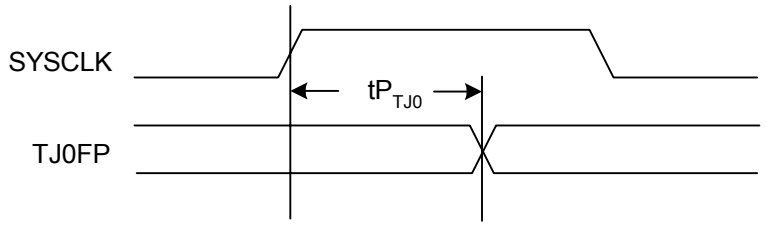
- When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

18.2 Output Timing

Table 24 TSE Output Timing (Figure 28)

Symbol	Description	Min	Max	Units
tP_{TJ0}	SYSCLK High to TJ0FP Valid	1	22	ns

Figure 28 TSE Output Timing



Notes on Output Timing:

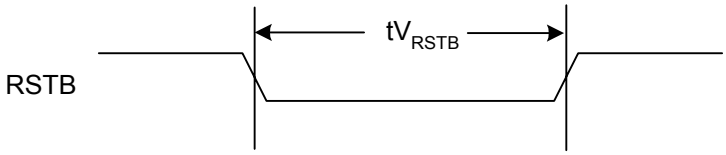
- Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
- Output propagation delays are measured with a 30 pF load on the outputs except where indicated.

18.3 Reset Timing

Table 25 RSTB Timing (Figure 29)

Symbol	Parameter	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 29 RSTB Timing



18.4 Serial TelecomBus Interface

Table 26 Serial TelecomBus Interface

Symbol	Description	Min	Typical	Max	Units
fRLVDS	RP[64:1], RN[64:1] Bit Rate	$10f_{SYSCLK}$ - 100ppm	$10f_{SYSCLK}$	$10f_{SYSCLK}$ - 100ppm	Mbps
tFALL	VODM fall time, 80%-20%, (RLOAD=100Ω ±1%)	200	300	400	ps
tRISE	VODM rise time, 20%-80%, (RLOAD=100Ω ±1%)	200	300	400	ps
tSKEW	Differential Skew			50	ps

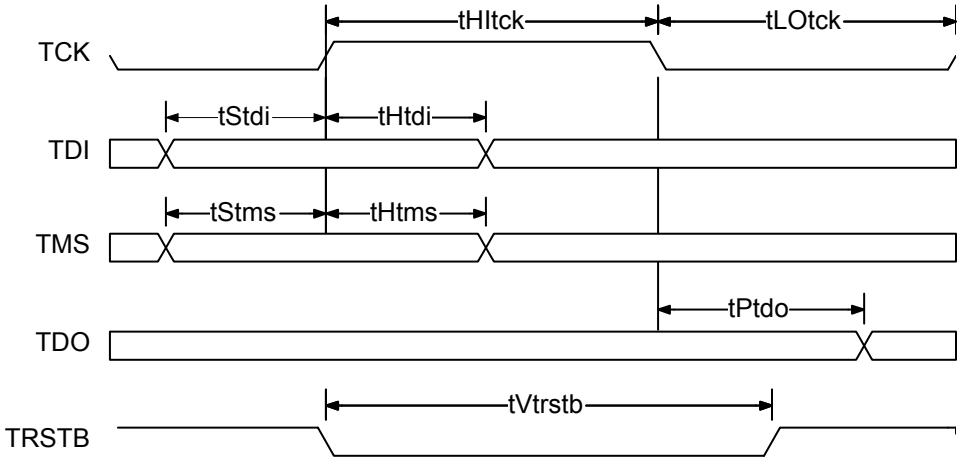
The min and max f_{RLVDS} specification is to accommodate transients between generated clocks. The mean data rate must be exactly $10f_{SYSCLK}$. FIFO overrun/underrun in the R8FA and T8DE will result if the mean data rate differs from $10f_{SYSCLK}$. A common system clock needs to be used for all devices with serial TelecomBus interfaces.

18.5 JTAG Port Interface

Table 27 JTAG Port Interface (Figure 30)

Symbol	Description	Min	Max	Units
FTCK	TCK Frequency		4	MHz
tHItck	TCK HI Pulse Width	100		ns
tLOtck	TCK LO Pulse Width	100		ns
tStms	TMS Set-up time to TCK	25		ns
tHtms	TMS Hold time to TCK	25		ns
tStdi	TDI Set-up time to TCK	25		ns
tHtdi	TDI Hold time to TCK	25		ns
tPtdo	TCK Low to TDO Valid	2	35	ns
tVtrstb	TRSTB Pulse Width	100		ns

Figure 30 JTAG Port Interface Timing



19 Ordering Information

PART NO.	DESCRIPTION
PM5372-BI	560 Ultra Ball Grid Array (UBGA)

20 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 28 Outside Plant Thermal Information

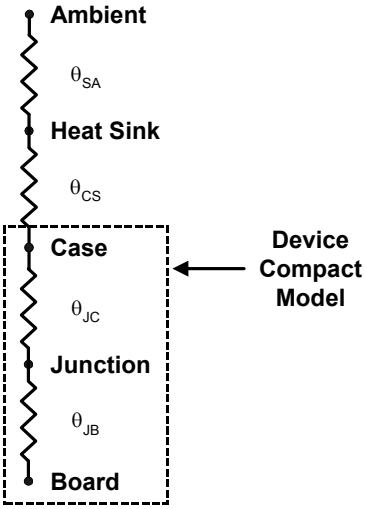
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 29 Device Compact Model[3]

θ_{JC}	0.1 °C/W
θ_{JB}	4.0 °C/W

Table 30 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	[(105-70)/P]-θ_{JC} °C/W[5]
θ_{SA} and θ_{CS} are required for long-term operation	



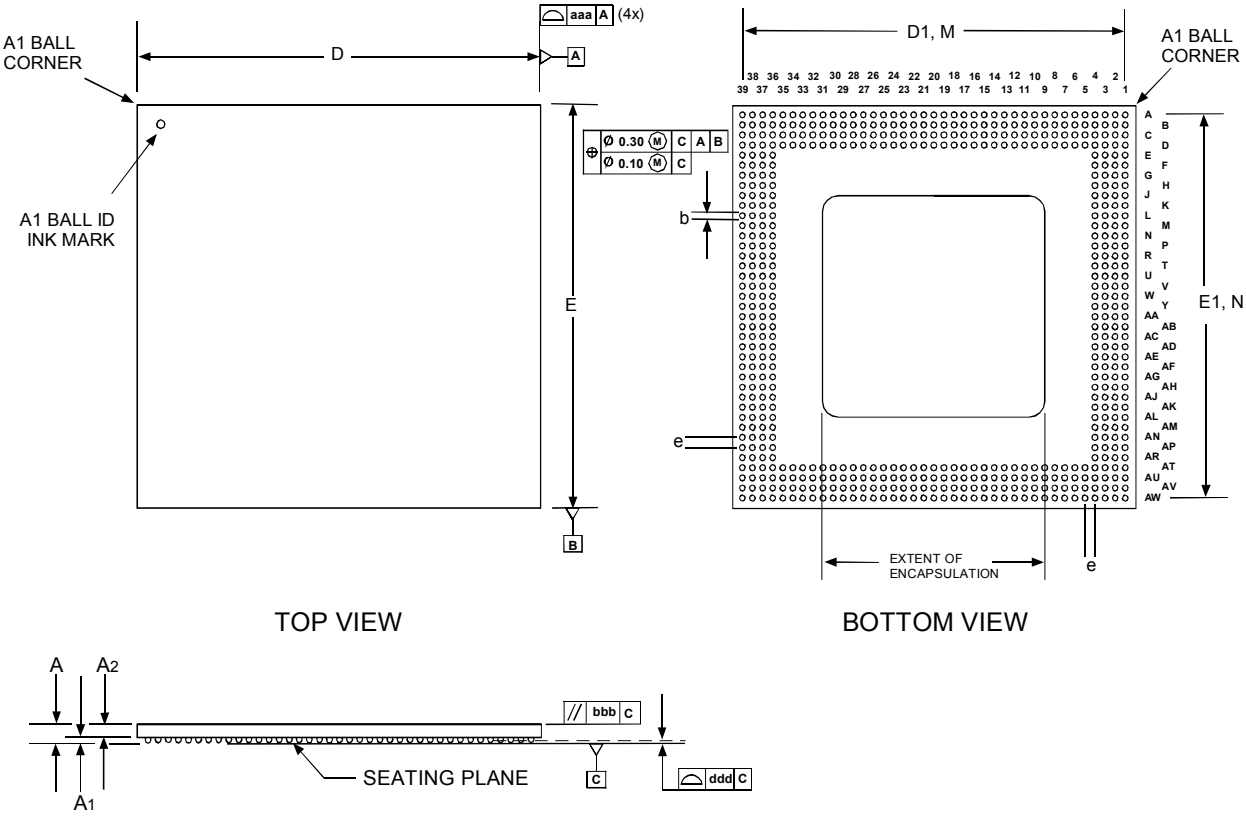
Operating power is dissipated in the package at the worst-case power supply. Power depends upon the operating mode. Please refer to 'High' power values in section 15.1Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core.
3. junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8.

4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place. In this formula P is the operating power.

21 Mechanical Information



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 560 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 40 x 40 x 1.47 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	d	e	aaa	bbb	ccc	ddd	S
Min.	1.32	0.40	0.92	39.90	-	39.90	-		0.50	-	-	-	-	-	-	-
Nom.	1.47	0.50	0.97	40.00	38.00	40.00	38.00	39x39	0.63	-	1.00	-	-	-	-	-
Max.	1.62	0.60	1.02	40.10	-	40.10	-		0.70	-	-	0.20	0.25	0.20	0.20	-