Specification Update

1. Revision History

Date of revision	Version	Description
January 30, 1998	A	Creation with mask A5108 (included)
July 16, 1998	B	Clarification of ERRATA C251G1D–20, Addition of ERRATA C251G1D–23
September 8, 1998	C	Re–organization with new ERRATA and new references

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2. Preface

This document is an update to the specifications contained in Table 1.

TSC80251G1 products implement a C251 architecture compliant to INTEL's MCS®251. Hence some of INTEL's specification update apply to TEMIC products. This includes INTEL's core stepping as outlined in Table 2.

Note: *This document only applies to TEMIC's products and does not imply any product from INTEL has the same behavior. INTEL's Errata references are provided for information only when they are documented by Intel Corporation. Please refer to INTEL's documents if you intend to use INTEL's products in your system. Please refer to TEMIC's documents if you intend to use TEMIC's products in your systems.*

Table 1. Affected Documents/Related Documents

Title	Reference
TSC80251G1D Datasheet	Rev. C – October 14, 1998
TSC80251G1D Design Guide – October 1998	Rev. C – October 8, 1998
TSC80251 Programmer's Guide 1996	Rev. B – October 23, 1996

Table 2. TEMIC Products to INTEL's Core Version Reference

TEMIC Products	INTEL's Core Version			
	A	B	C	D
TSC80251G1D–yyyyy				✓
TSC251G1Dzzzz–yyyyy				✓

Notes:
yyyyy provides voltage range, speed, temperature range, packaging and conditioning options.
zzzz provides the customer code for MaskROM.
Please refer to Ordering Information in the Data Sheet for full information on the options.

3. Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specifications (see Table 1).

Note:
Errata from mask 5096 have been removed from this specification update. The Errata list of mask 5096 is available upon request for customers who have ordered mask ROM products with this version. The production ROMless and the new mask ROM derivatives are using mask 5108.

Table 3. Codes Used in Summary Table

Page	
(Page)	Page location of item in this document.
Status	
Doc	Document change or update will be implemented.
Fix	This erratum is intended to be fixed in a future version of the component.
No Fix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

4. Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to TSC80251G1D derivatives. TEMIC may fix some of the errata in a future version of the component, and account for the other outstanding issues through documentation or specification changes as noted.

Table 4. Errata List

TEMIC Reference	INTEL Reference	Page	Status	Errata
C251G1D–01	N.A.	4	Fix	I^2C Repeated Start Condition in Master Mode
C251G1D–02	(1)	5	Fix	JBC Instruction
C251G1D–03	980009	5	Fix	Interrupt Handling Unit In–Process Stacking
C251G1D–04	N.A.	6	Fix	UART Start Bit Detection
C251G1D–05	N.A.	6	Fix	CCFx Clear Failure in Polling Mode
C251G1D–06	N.A.	7	Fix	CCFx Always Set when Match
C251G1D–07	N.A.	7	Fix	EWC–PCA Watchdog Reset

Note:
1. Not reported when releasing this specification update.

Table 5. Specification Changes

TEMIC Reference	INTEL Reference	Page	Status	Specification Changes
				None

Table 6. Specification Clarifications

TEMIC Reference	INTEL Reference	Page	Status	Specification Clarifications
				None

Table 7. Documentation Changes

TEMIC Reference	INTEL Reference	Page	Status	Documentation Changes
				None

5. Errata

Reference	Erratum
C251G1D–01	**I^2C Repeated Start Condition in Master Mode**

Problem

When the TSC80251G1D derivative is the I^2C master, if STO flag is cleared and STA flag is set between two transfers and before the STOP condition of the first transfer is emitted, a repeated start condition is properly emitted but state F8h is set instead of 10h and SI flag is not set.

Example

In the example hereafter, the second transfer is started before the stop condition appears on the bus.

```
            ORG    FF:0000h
            ljmp   MAIN

MAIN:       mov    SSCON,#60h        ; send start condition
            jnb    SI,$              ; wait status 08h
            mov    SSDAT,#A0h        ; slave address
            clr    SI                ; send address
            jnb    SI,$              ; wait status 20h or 18h
            setb   STO               ; stop condition
            clr    SI                ; send stop condition

            mov    SSCON,#60h        ; start an other transfer
            ...
```

Implication

After the problem has been triggered, the I^2C bus is no longer available as it is fully occupied by the TSC80251G1D microcontroller emitting a start condition.

Workaround

To avoid problem, when starting a new transfer, STO flag should not be cleared, only STA flag should be set.

The instruction

```
            mov    SSCON,#60h        ; start an other transfer
```

Becomes

```
            setb   STA               ; start condition
```

Affected Products

All TSC80251G1D are affected.

Reference	Erratum
C251G1D–02	JBC Instruction

Problem

The JBC instruction uses a Read–Read–Modify–Write instruction. The write back is performed in any case, regardless of the value of the bit. A bit set by hardware between the first read and the second read is overwritten by the final write back.

Implication

Information is lost. This error affects the external interrupts flag (IE0 and IE1) of TCON register, the synchronous serial interrupt flag (SSI) of SSCON register and the keyboard interrupt flags (P1F.n, n=0..7) of P1F register.

Workaround

The workaround for this erratum is not to use the JBC instruction with the concerned flags.

Affected Products

All TSC80251G1D products are affected.

Reference	Erratum
C251G1D–03	Interrupt Handling Unit In–Process Stacking

Problem

After an interrupt has been successfully polled, an interrupt request is posted and the interrupt level is pushed on the interrupt in process stack which prevents any other interrupt occurring at a the same or at a lower level to be granted before the winning interrupt has returned. Then the interrupt request is waiting for the completion of the executing instruction to be processed. If a new interrupt has just been polled at an higher level when the pending interrupt request is being processed, the highest level interrupt will be pushed and granted but the previously waiting interrupt will be lost and its level will never be popped from the stack.

A TRAP instruction leads to a priority interrupt processing occurring at the end of its execution. This leads to the same trouble if an interrupt request is pending during TRAP execution.
Note: *The Hardware Breakpoint Trap used by emulators on the ICE bond–out is not affected by this trouble.*

Implication

The interrupts at the lowest levels will be permanently disabled.

Workaround

Use only two priority levels and do not execute TRAP in sections where interrupts are enabled.
Note: *NMI uses one independent priority level and cannot be disabled.*

Affected Products

All TSC80251G1D products are affected.

Reference	Erratum
C251G1D–04	UART Start Bit Detection

Problem

In asynchronous modes (1, 2 or 3), a START bit cannot be detected less than 1/16 bit time after a received STOP bit.

Implication

The frames received by the TSC80251G1D derivatives are corrupted if there is only one STOP bit with no delay between two received characters.

Workaround

The workaround is depending on the application:

- Have a delay between the characters transmitted to a TSC80251G1D derivative
- Send more than one STOP bit (e.g. 1.5 or 2 stop bits) when communicating with a TSC80251G1D derivative

Slightly increasing the TSC80251G1D receive baud rate might work but is not recommended. This will reduce the frequency excursion tolerance and may only be practicable when using low baud rates.

Affected Products

All TSC80251G1D are affected.

Reference	Erratum
C251G1D–05	CCFx Clear Failure in Polling Mode

Problem

When set by hardware, a CCFx flag (x= 0..4) is locked for one peripheral cycle (6 states). A clear instruction will not operate if it is writing to the flag during this period.

Implication

When a CCFx flag is tested and cleared in a polling loop, the clear instruction may fail clearing the flag. Then the flag can be found set several times with only one actual event. Considering the minimum interrupt processing latency, this cannot occur in Interrupt Mode.

Workaround

Wait or keep on clearing the flag at least 6 states after it has been set by hardware:

```
loop_ccf0:...
          ...
          jnb    CCF0,loop_ccf0    ; polling loop until CCF0 is set
          jb     CCF0,0            ; jump always, more than 5 states delay
          clr    CCF0              ; clear instruction will work
          ...                      ; unless an new event occurred
```

Affected Products

All TSC80251G1D are affected.

Reference	Erratum
C251G1D–06	CCFx Always Set when Match

Problem

When the EWC Timer/Counter is not running, an alternate path is used to trigger the CCFx flag (x= 0..4) in the CCON register, irrespective of MATx value. This should not be the case when MATx is cleared, as highlighted in figure 5.3 of the referred Design Guide (see Table 1).

Implication

When the EWC Timer/Counter is not running, CCFx flag will be set when CH/CL are matching CCAPxH/CCAPxL and ECOMx is set, even if MATx is cleared.

Workaround

Avoid having CH/CL matching CCAPxH/CCAPxL if CR is cleared in CCON when ECOMx is set and MATx is cleared in CCAPMx.

Affected Products

All TSC80251G1D are affected.

Reference	Erratum
C251G1D–07	EWC–PCA Watchdog Reset

Problem

If CH/CL and CCAP4H/CCAP4L are matching when the software watchdog mode is configured on PCA module 4, an immediate reset occurs.

Example

In the example hereafter, the microcontroller resets immediately after setting WDTE.

```
WDT_INIT: mov    CCAPM4,#01001000b  ; set ECOM4 and MAT4
          setb   WDTE               ; enable WDT reset
          mov    CCAP4L,#DELAY_L    ; load comparison value
          mov    CCAP4H,#DELAY_H
          setb   CR                 ; start PCA timer
          ...
```

Implication

An internal reset is generated when configuring the PCA software watchdog (CH/CL and CCAP4H/CCAP4L are matching after reset).

Workaround

PCA counter and Channel comparison values must be set before PCA Channel 4 configuration.

The above example becomes:

```
WDT_INIT: mov    CCAP4L,#DELAY_L    ; load comparison value
          mov    CCAP4H,#DELAY_H
          mov    CCAPM4,#01001000b  ; set ECOM4 and MAT4
          setb   WDTE               ; enable WDT reset
          setb   CR                 ; start PCA timer
          ...
```

Affected Products

All TSC80251G1D products are affected.

6. Specification Changes

This section is intentionally left blank.

7. Specification Clarifications

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8. Documentation Changes

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