
MS52C182A**Preliminary**

65,536-Word X 16-Bit or 131,072-Word X 8-Bit STATIC RAM +
524,288-Word X 16-Bit or 1,048,576-Word X 8-Bit One Time PROM

DESCRIPTION

The MS52C182A is a 65,536 -word by 16 -bit / 131,072-word by 8-bit electrically switchable 1Mb static RAM and 524,288-word by 16-bit / 1,048,576-word by 8-bit electrically switchable 8Mb One Time PROM featuring 2.7V to 3.6V power supply operation and direct LVTTTL input / output compatibility. Since the circuitry is completely static, external clocks are unnecessary, making this device very easy to use.

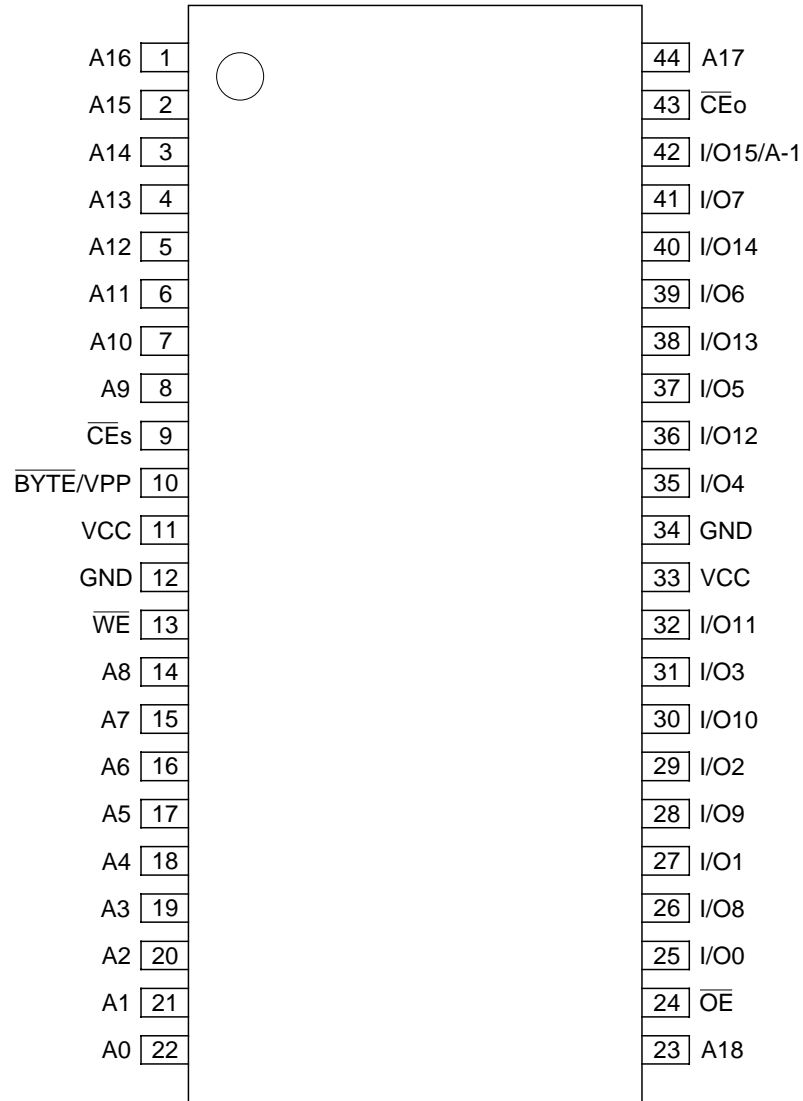
The MS52C182A is packaged in 44-pin plastic TSOP and 48-pin FBGA (9mmx10mm) ,suited for use in handy terminal and other application which required small space.

FEATURES

- 65,536-word x 16-bit / 131,072-word x 8-bit configuration SRAM and 524,288-word x 16-bit / 1,048,576-word x 8-bit configuration OTP
- Power supply voltage : 2.7 to 3.6V
- Fully static operation
- Operating temperature range : Ta= -20 to 70°C
- Access time : 100nS MAX (Vcc=2.7V)
80nS MAX (Vcc=3.0V)
- Common address inputs and data inputs / outputs for SRAM and OTP
- Input / Output LVTTTL compatible
- 3-state output
- Data retention available at power supply voltage 1.5V for SRAM
- Package options :

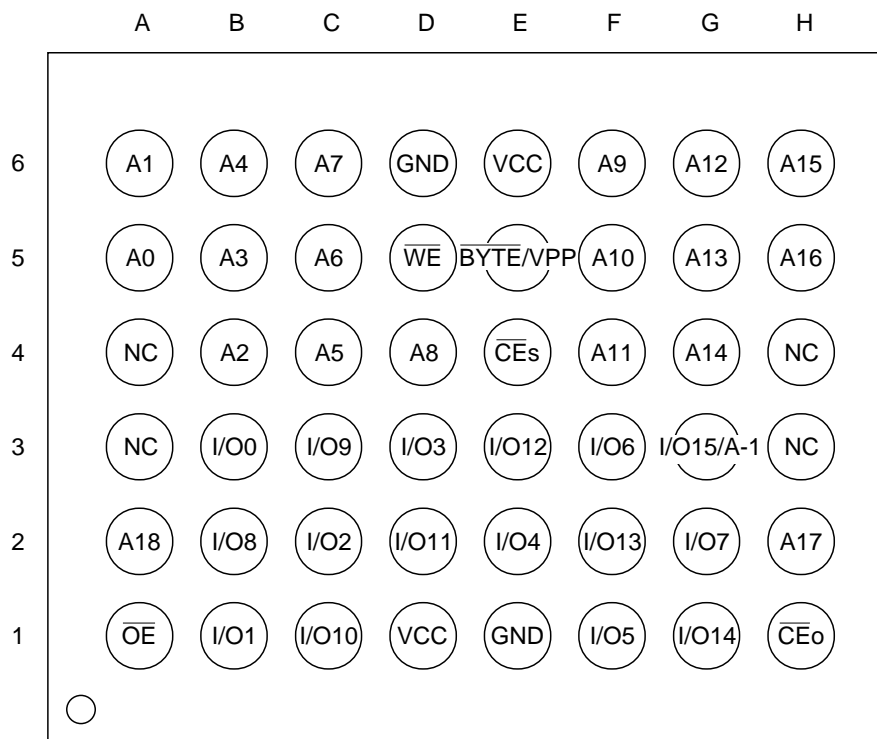
44-pin plastic TSOP (Type II)	(TSOP44-P-400-0.8)	(Product : MS52C182ATA)
48-pin plastic FBGA	(FBGA48-P-0910-0.8)	(Product : MS52C182ALA)

PIN CONFIGURATION (TOP VIEW)



44-pin TSOP (II)

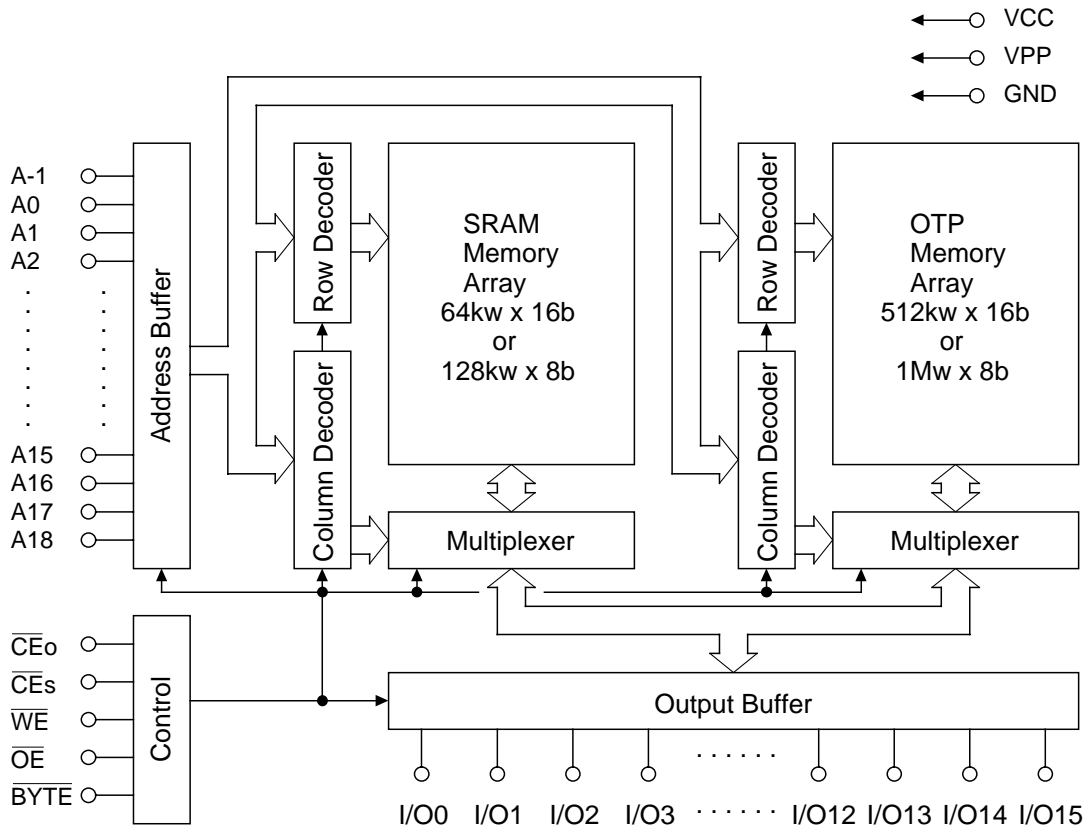
PIN CONFIGURATION (TOP VIEW)



48-pin FBGA

Pin Name	Function
A -1 - A15	Common Address Inputs
A16 - A18	Address Inputs for OTP
\overline{CEs}	Chip Enable for SRAM
\overline{CEo}	Chip Enable for OTP
\overline{WE}	Write Enable for SRAM
\overline{OE}	Common Output Enable
I/O0 - I/O15	Common Data Inputs / Outputs
VCC	Common Power Supply
$\overline{BYTE/VPP}$	Common Mode Switch & Program Power Supply for OTP
GND	Common Ground
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

Operating Mode		\overline{CE}_o	\overline{CE}_s	\overline{WE}	\overline{OE}	BYTE / VPP	VCC	I/O0 - I/O7	I/O8 - I/O14	I/O15 / A-1
Standby		H	H	*	*	H	2.7V to 3.6V	High-Z	High-Z	High-Z
		H	H	*	*	L		High-Z	High-Z	*
SRAM Read	16-Bit	H	L	H	H	H		High-Z	High-Z	High-Z
		H	L	H	L	H		DOUT	DOUT	DOUT
	8-Bit	H	L	H	H	L		High-Z	High-Z	*
		H	L	H	L	L		DOUT	High-Z	L / H
SRAM Write	16-Bit	H	L	L	*	H		DIN	DIN	DIN
	8-Bit	H	L	L	*	L		DIN	High-Z	L / H
OTP Read	16-Bit	L	H	*	H	H		High-Z	High-Z	High-Z
		L	H	*	L	H		DOUT	DOUT	DOUT
	8-Bit	L	H	*	H	L	High-Z	High-Z	*	
		L	H	*	L	L	DOUT	High-Z	L / H	

Note : 1. * = Don't Care ("H" or "L")
 2. It is forbidden to apply $\overline{CE}_o="L"$ and $\overline{CE}_s="L"$ simultaneously.

FUNCTION TABLE (Continued)

Operating Mode	\overline{CE}_0	\overline{CE}_s	\overline{WE}	\overline{OE}	\overline{BYTE} /VPP	VCC	I/O0 - I/O7	I/O8 - I/O14	I/O15 / A-1
OTP Program	L	H	*	H	9.75V	4.0V	DIN	DIN	DIN
OTP Program Inhibit	H	H	*	H			High-Z	High-Z	High-Z
OTP Program Verify	H	H	*	L			DOUT	DOUT	DOUT

Note : 1. * = Don't Care ("H" or "L")

2. It is forbidden to apply $\overline{CE}_0="L"$ and $\overline{CE}_s="L"$ simultaneously.

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VCC	Respect to GND	-0.5 to 5.0	V
	VPP		-0.5 to 11.5	V
Input Voltage	VI		-0.5* to Vcc+0.5	V
Output Voltage	VO		-0.5* to Vcc+0.5	V
Power Dissipation	PD	Ta=25°C	0.7	W
Operating Temperature	Topr	—	-20 to 70	°C
Storage Temperature	Tstg	—	-55 to 125	°C

* -1.2VMin. for pulse width less than 30nS.

Recommended Operating Conditions

(Ta= -20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VCC	—	2.7	—	3.6	V
	VPP		-0.5	—	Vcc+0.5	V
	GND		0	0	0	V
SRAM Data Retention Voltage	VCCH	—	1.5	—	3.6	V
Input High Voltage	VIH	Vcc=2.7 to 3.6	2.2	—	Vcc+0.5	V
Input Low Voltage	VIL		-0.5*	—	0.4	V

* -1.2VMin. for pulse width less than 30nS.

DC Characteristics (1)

(V_{CC}=3.0V±0.3V, T_a=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC}	-1.0	—	1.0	μA
Output Leakage Current	I _{LO}	$\overline{CE}_o=V_{IH}$, $\overline{CE}_s=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =0 to V _{CC}	-1.0	—	1.0	μA
Output High Voltage	V _{OH}	I _{OH} =-500μA	V _{CC} -0.5	—	—	V
Output Low Voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V
Standby Power Supply Current	I _{CCS}	$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ V _{IN} =0 to V _{CC}	—	—	10	μA
	I _{CCS1}	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IH}$ V _{IN} =V _{IH} or V _{IL}	—	—	0.3	mA
Operating Power Supply Current	I _{CCA} (SRAM)	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IL}$ $\overline{OE}=V_{IH}$ V _{IN} =V _{IH} /V _{IL} T _{CYC} =100nS	—	—	35	mA
		$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \leq 0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V _{IH} ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V T _{CYC} =1μS	—	—	10	mA
	I _{CCA} * (OTP)	$\overline{CE}_o=V_{IL}$ $\overline{CE}_s=V_{IH}$ $\overline{OE}=V_{IH}$ V _{IN} =V _{IH} /V _{IL} T _{CYC} =100nS	—	—	35	mA
		$\overline{CE}_o \leq 0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V _{IH} ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V T _{CYC} =1μS	—	—	20	mA
V _{PP} Power Supply Current	I _{PP}	$\overline{BYTE}/V_{PP}=V_{CC}$	—	—	10	μA

* Read Current

DC Characteristics (2)

(V_{CC}=3.3V±0.3V, T_a=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC}	-1.0	—	1.0	μA
Output Leakage Current	I _{LO}	$\overline{CE}_o=V_{IH}$, $\overline{CE}_s=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =0 to V _{CC}	-1.0	—	1.0	μA
Output High Voltage	V _{OH}	I _{OH} =-500μA	V _{CC} -0.5	—	—	V
Output Low Voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V
Standby Power Supply Current	I _{CCS}	$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ V _{IN} =0 to V _{CC}	—	—	10	μA
	I _{CCS1}	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IH}$ V _{IN} =V _{IH} or V _{IL}	—	—	0.3	mA
Operating Power Supply Current	I _{CCA} (SRAM)	$\overline{CE}_o=V_{IH}$ $\overline{CE}_s=V_{IL}$ $\overline{OE}=V_{IH}$ V _{IN} =V _{IH} /V _{IL} TCYC=80nS	—	—	40	mA
		$\overline{CE}_o \geq V_{CC}-0.2V$ $\overline{CE}_s \leq 0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V _{IH} ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V TCYC=1μS	—	—	15	mA
	I _{CCA*} (OTP)	$\overline{CE}_o=V_{IL}$ $\overline{CE}_s=V_{IH}$ $\overline{OE}=V_{IH}$ V _{IN} =V _{IH} /V _{IL} TCYC=80nS	—	—	40	mA
		$\overline{CE}_o \leq 0.2V$ $\overline{CE}_s \geq V_{CC}-0.2V$ $\overline{OE} \geq V_{CC}-0.2V$ V _{IH} ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V TCYC=1μS	—	—	25	mA
V _{PP} Power Supply Current	I _{PP}	$\overline{BYTE}/V_{PP}=V_{CC}$	—	—	10	μA

* Read Current

SRAM AC Characteristics

SRAM Read Cycle (1)

(V_{CC}=3.0V±0.3V, T_a=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t _{RC}	—	100	—	nS
Address Access Time	t _{AA}	—	—	100	nS
$\overline{C\!E}$ s Access Time	t _{CO}	—	—	100	nS
$\overline{O\!E}$ Access Time	t _{OE}	—	—	50	nS
$\overline{C\!E}$ s to Output in Low-Z	t _{CLZ}	—	10	—	nS
$\overline{O\!E}$ to Output in Low-Z	t _{OLZ}	—	5	—	nS
Output Hold from Address Change	t _{OH}	—	10	—	nS
$\overline{C\!E}$ s to Output in High-Z	t _{CHZ}	—	—	35	nS
$\overline{O\!E}$ to Output in High-Z	t _{OHZ}	—	—	35	nS

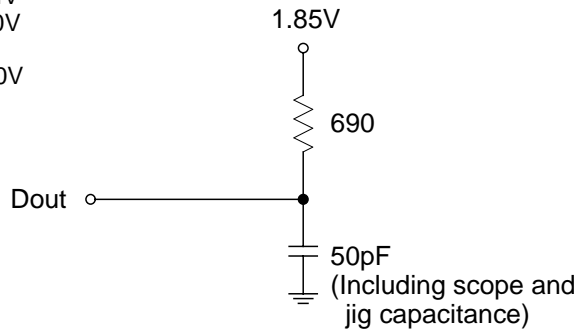
SRAM Write Cycle (1)

(V_{CC}=3.0V±0.3V, T_a=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t _{WC}	—	100	—	nS
Address Setup Time	t _{AS}	—	0	—	nS
Write Pulse Width	t _{WP}	—	75	—	nS
Write Recovery Time	t _{WR}	—	0	—	nS
Data Setup Time	t _{DS}	—	40	—	nS
Data Hold Time	t _{DH}	—	0	—	nS
$\overline{W\!E}$ to Output in High-Z	t _{WHZ}	—	—	35	nS
$\overline{C\!E}$ s to End of Write	t _{CW}	—	90	—	nS
Address Valid to End of Write	t _{AW}	—	90	—	nS
Output Active from End of Write	t _{WLZ}	—	5	—	nS

Test Condition

- Input Pulse Levels ----- 0.4V/2.4V
- Input Timing Reference Levels ----- 0.8V/2.0V
- Output Load ----- 50pF
- Output Timing Reference Levels ----- 0.8V/2.0V
- Input Rise and Fall Time ----- 5nS



SRAM Read Cycle (2)(V_{CC}=3.3V±0.3V, T_a=-20 to 70°C)

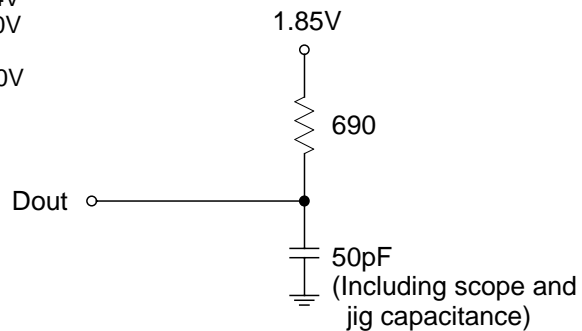
Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t _{RC}	—	80	—	nS
Address Access Time	t _{AA}	—	—	80	nS
$\overline{\text{CE}}$ s Access Time	t _{CO}	—	—	80	nS
$\overline{\text{OE}}$ Access Time	t _{OE}	—	—	40	nS
$\overline{\text{CE}}$ s to Output in Low-Z	t _{CLZ}	—	10	—	nS
$\overline{\text{OE}}$ to Output in Low-Z	t _{OLZ}	—	5	—	nS
Output Hold from Address Change	t _{OH}	—	10	—	nS
$\overline{\text{CE}}$ s to Output in High-Z	t _{CHZ}	—	—	30	nS
$\overline{\text{OE}}$ to Output in High-Z	t _{OHZ}	—	—	30	nS

SRAM Write Cycle (2)(V_{CC}=3.3V±0.3V, T_a=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t _{WC}	—	80	—	nS
Address Setup Time	t _{AS}	—	0	—	nS
Write Pulse Width	t _{WP}	—	60	—	nS
Write Recovery Time	t _{WR}	—	0	—	nS
Data Setup Time	t _{DS}	—	35	—	nS
Data Hold Time	t _{DH}	—	0	—	nS
$\overline{\text{WE}}$ to Output in High-Z	t _{WHZ}	—	—	30	nS
$\overline{\text{CE}}$ s to End of Write	t _{CW}	—	70	—	nS
Address Valid to End of Write	t _{AW}	—	70	—	nS
Output Active from End of Write	t _{WLZ}	—	5	—	nS

Test Condition

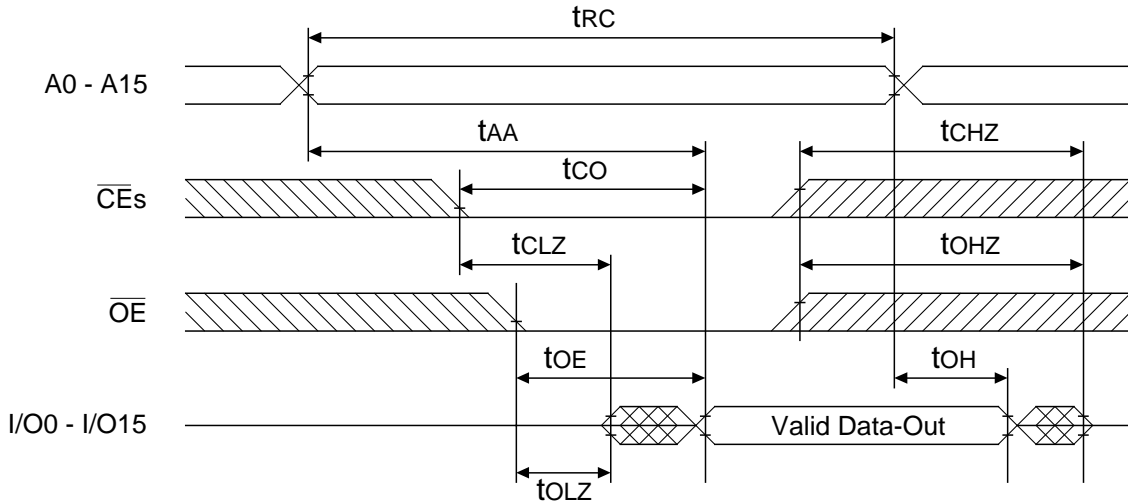
Input Pulse Levels ----- 0.4V/2.4V
 Input Timing Reference Levels ----- 0.8V/2.0V
 Output Load ----- 50pF
 Output Timing Reference Levels ----- 0.8V/2.0V
 Input Rise and Fall Time ----- 5nS



SRAM Timing Diagrams

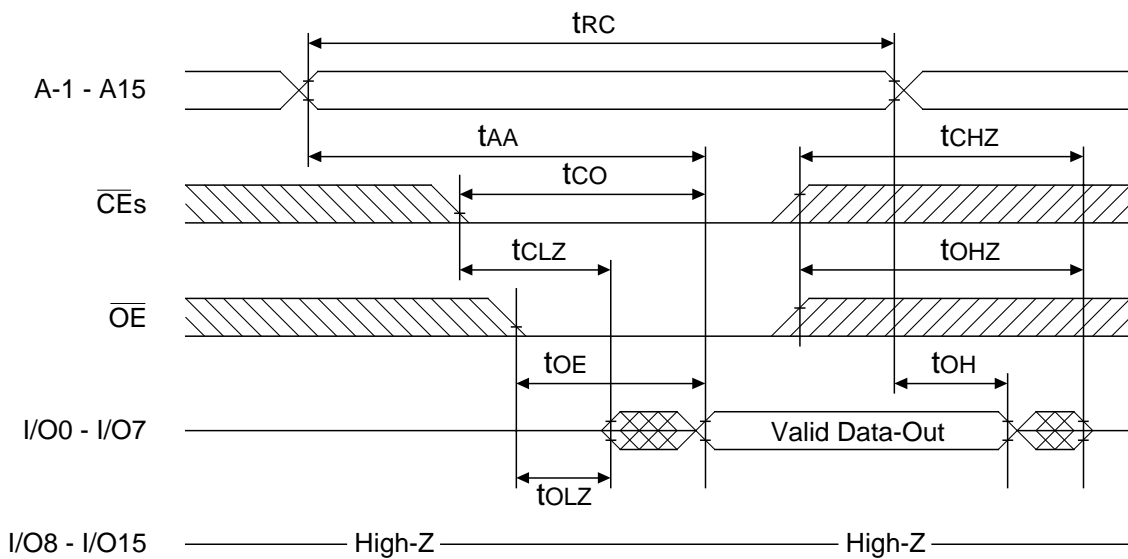
SRAM Read Cycle (1)

16-bit Read Mode (BYTE=VIH)



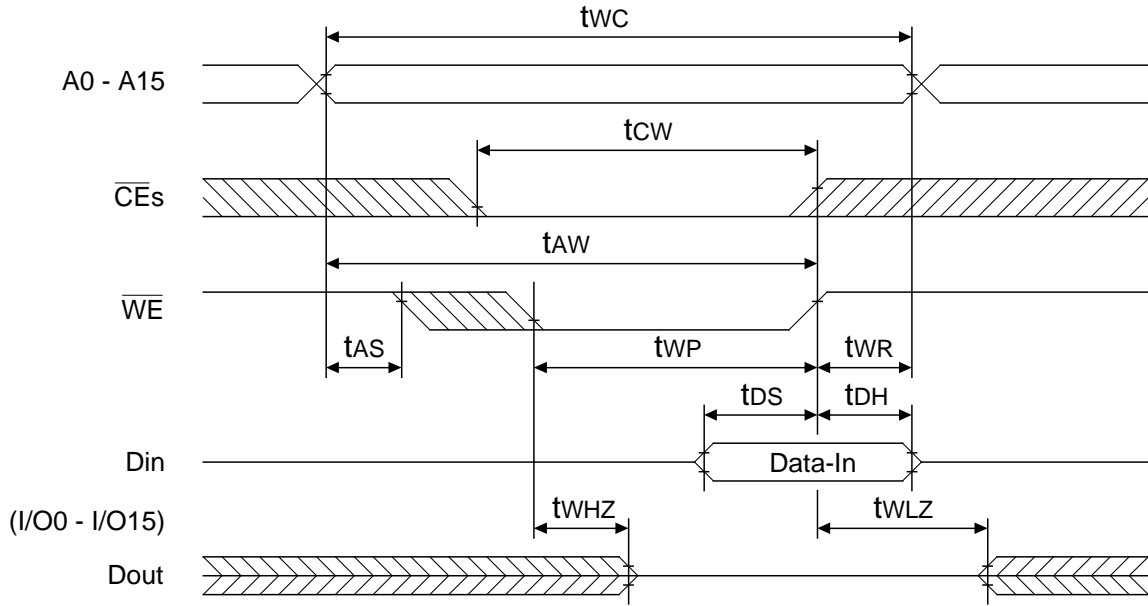
SRAM Read Cycle (2)

8-bit Read Mode (BYTE=VIL)

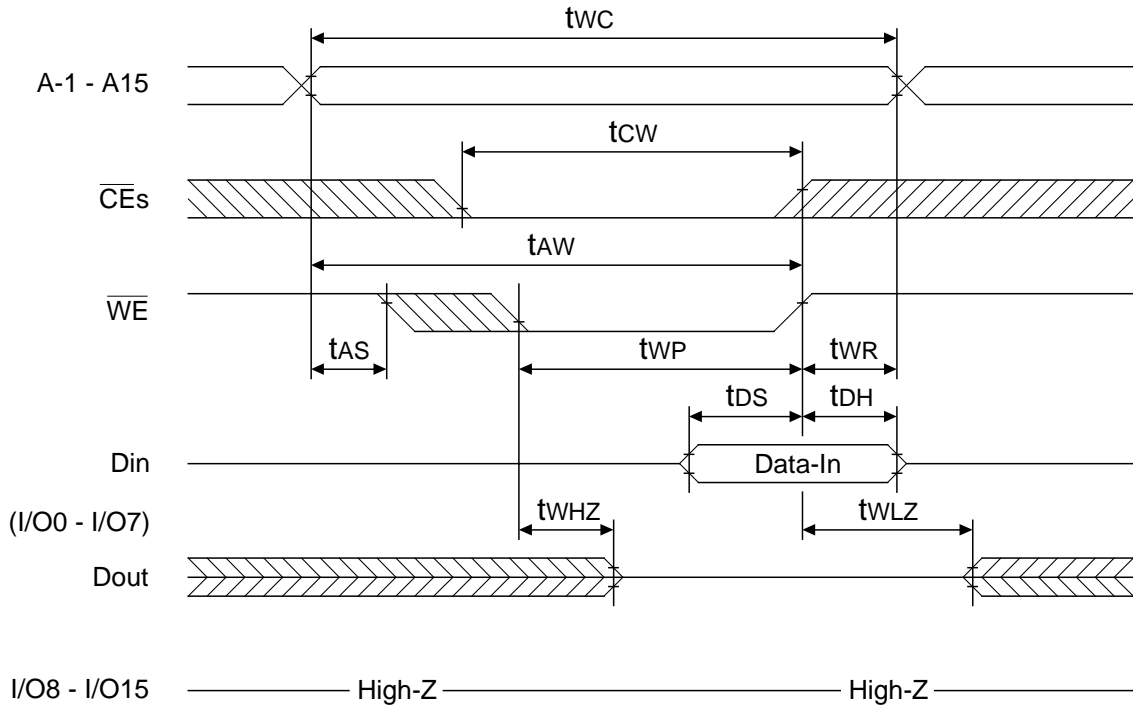


- Notes : 1. A read cycle of SRAM occurs during the overlap of $\overline{CEo}="H"$, $\overline{CEs}="L"$, $\overline{OE}="L"$ and $\overline{WE}="H"$.
 2. t_{OHZ} , t_{CHZ} are specified by the time when DATA is floating , not defined by the output level.

SRAM Write Cycle (1)
16-bit Write Mode (BYTE=VIH)



SRAM Write Cycle (2)
8-bit Write Mode (BYTE=VIL)

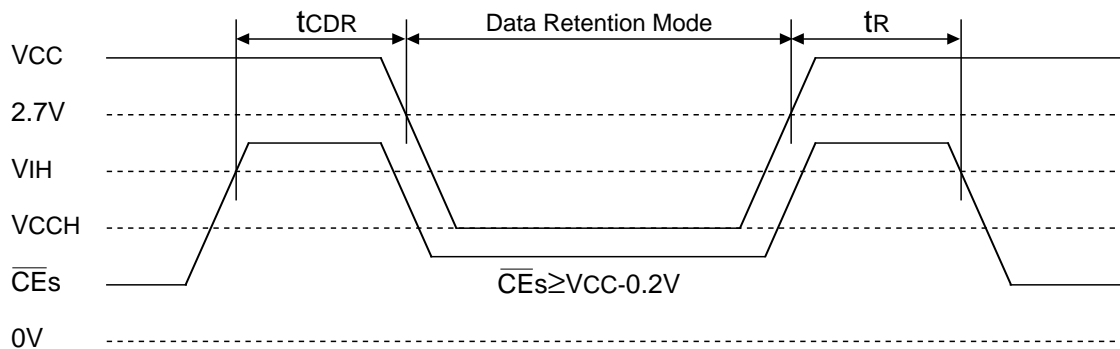


- Notes :
1. A write cycle of SRAM occurs during the overlap of $\overline{CE}_0="H"$, $\overline{CE}_s="L"$ and $\overline{WE}="L"$.
 2. \overline{OE} may be either of "H" or "L" in the write cycle of SRAM.
 3. t_{AS} is specified from $\overline{CE}_s="L"$ or $\overline{WE}="L"$, whichever occurs last.
 4. t_{WP} is an overlap time of $\overline{CE}_s="L"$ and $\overline{WE}="L"$.
 5. t_{WR} , t_{DS} , t_{DH} are specified from $\overline{CE}_s="H"$ or $\overline{WE}="H"$, whichever occurs first.
 6. t_{WHZ} is specified by the time when DATA output is floating , not defined by the output level.
 7. When I/O pins are in the output mode , don't apply the inverted input signal to the output pins.

SRAM Data Retention Characteristics

(Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V _{CCH}	$\overline{CE}_0 \geq V_{CC} - 0.2V$ $\overline{CE}_s \geq V_{CC} - 0.2V$ $V_{IN} = 0 \text{ to } V_{CC}$	1.5	—	—	V
Data Retention Power Supply Current	I _{CCH}	$V_{CC} = 1.5V$ $\overline{CE}_0 \geq V_{CC} - 0.2V$ $\overline{CE}_s \geq V_{CC} - 0.2V$ $V_{IN} = 0 \text{ to } V_{CC}$	—	—	3	μA
Chip Deselect to Data Retention Time	t _{CDR}	—	0	—	—	nS
Operation Recovery Time	t _R	—	5	—	—	mS



OTP AC Characteristics (1)**OTP Read Cycle (1)**(V_{CC}=3.0V±0.3V, T_a=-20 to 70°C)

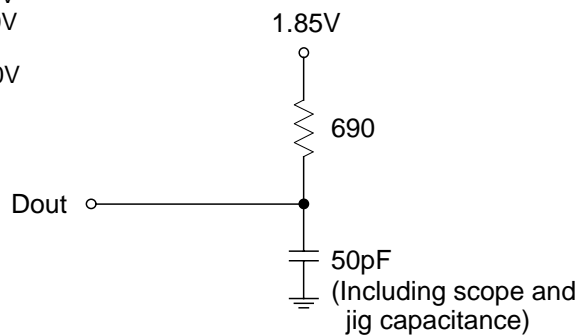
Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t _{RC}	—	100	—	nS
Address Access Time	t _{AA}	$\overline{CE}_0 = \overline{OE} = V_{IL}$	—	100	nS
\overline{CE}_0 Access Time	t _{CO}	$\overline{OE} = V_{IL}$	—	100	nS
\overline{OE} Access Time	t _{OE}	$\overline{CE}_0 = V_{IL}$	—	50	nS
\overline{CE}_0 to Output in High-Z	t _{CHZ}	$\overline{OE} = V_{IL}$	0	40	nS
\overline{OE} to Output in High-Z	t _{OHZ}	$\overline{CE}_0 = V_{IL}$	0	35	nS
Output Hold from Address Change	t _{OH}	$\overline{CE}_0 = \overline{OE} = V_{IL}$	0	—	nS

OTP Read Cycle (2)(V_{CC}=3.3V±0.3V, T_a=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t _{RC}	—	80	—	nS
Address Access Time	t _{AA}	$\overline{CE}_0 = \overline{OE} = V_{IL}$	—	80	nS
\overline{CE}_0 Access Time	t _{CO}	$\overline{OE} = V_{IL}$	—	80	nS
\overline{OE} Access Time	t _{OE}	$\overline{CE}_0 = V_{IL}$	—	50	nS
\overline{CE}_0 to Output in High-Z	t _{CHZ}	$\overline{OE} = V_{IL}$	0	40	nS
\overline{OE} to Output in High-Z	t _{OHZ}	$\overline{CE}_0 = V_{IL}$	0	35	nS
Output Hold from Address Change	t _{OH}	$\overline{CE}_0 = \overline{OE} = V_{IL}$	0	—	nS

Test Condition

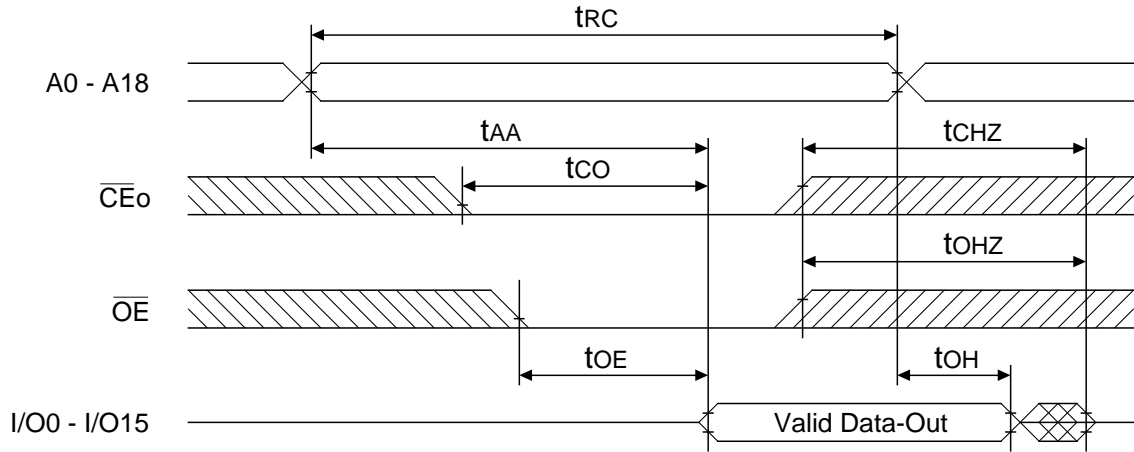
Input Pulse Levels ----- 0.4V/2.4V
 Input Timing Reference Levels ----- 0.8V/2.0V
 Output Load ----- 50pF
 Output Timing Reference Levels ----- 0.8V/2.0V
 Input Rise and Fall Time ----- 5nS



OTP Timing Diagrams

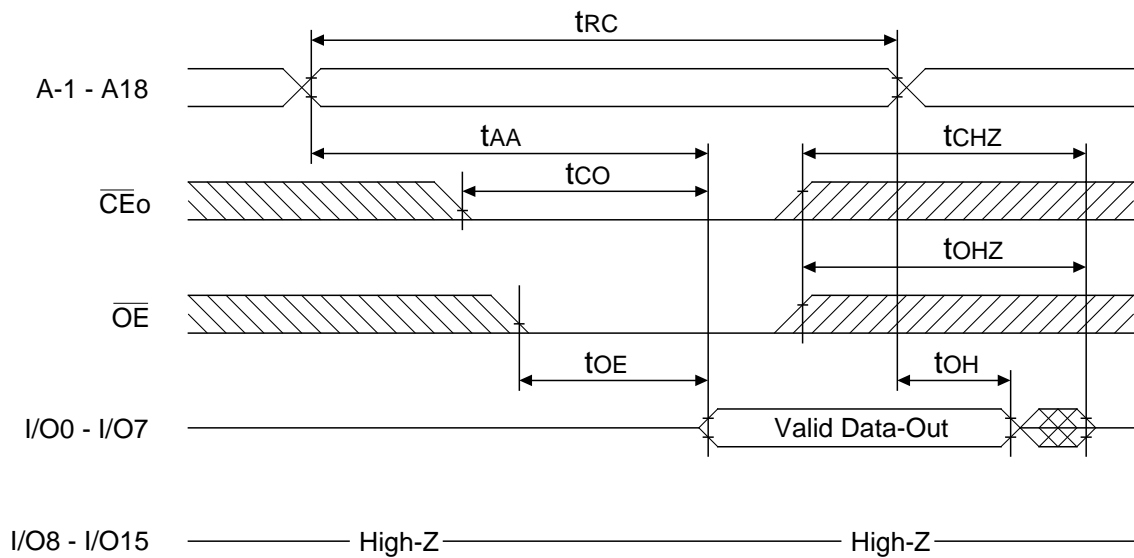
OTP Read Cycle (1)

16-bit Read Mode (BYTE=VIH)



OTP Read Cycle (2)

8-bit Read Mode (BYTE=VIL)



- Notes : 1. A read cycle of OTP occurs during the overlap of \overline{CE}_0 ="L", \overline{CE}_s ="H" and \overline{OE} ="L".
 2. t_{OHZ} , t_{CHZ} are specified by the time when DATA is floating , not defined by the output level.

OTP DC Characteristics

OTP Programming Operation

(Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I _{LI}	V _I =V _{CC} +0.5V	—	—	10	μA
Program Power Supply Current	I _{PP2}	$\overline{CE}_0=V_{IL}$	—	—	50	mA
Power Supply Current	I _{CC}	—	—	—	50	mA
Input High Voltage	V _{IH}	—	3.0	—	V _{CC} +0.5	V
Input Low Voltage	V _{IL}	—	-0.5	—	0.8	V
Output High Voltage	V _{OH}	I _{OH} =-500μA	2.4	—	—	V
Output Low Voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.45	V
Program Voltage	V _{PP}	—	9.5	9.75	10.0	V
V _{CC} Voltage	V _{CC}	—	3.9	4.0	4.1	V

OTP AC Characteristics (2)

OTP Programming Operation

(V_{CC}=4.0V±0.1V, V_{PP}=9.75V±0.25V, Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address Setup Time	t _{AS}	—	2	—	—	μS
\overline{OE} Setup Time	t _{OES}	—	2	—	—	μS
Data Setup Time	t _{DS}	—	2	—	—	μS
Address Hold Time	t _{AH}	—	0	—	—	μS
Data Hold Time	t _{DH}	—	2	—	—	μS
\overline{OE} to Output in High-Z	t _{DFP}	—	0	—	130	nS
V _{PP} Power Setup Time	t _{VS}	—	2	—	—	μS
Program Pulse Width	t _{PW}	—	9	10	11	μS
Data Valid from \overline{OE}	t _{OE}	—	—	—	150	nS

Pin Check Function

Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer.

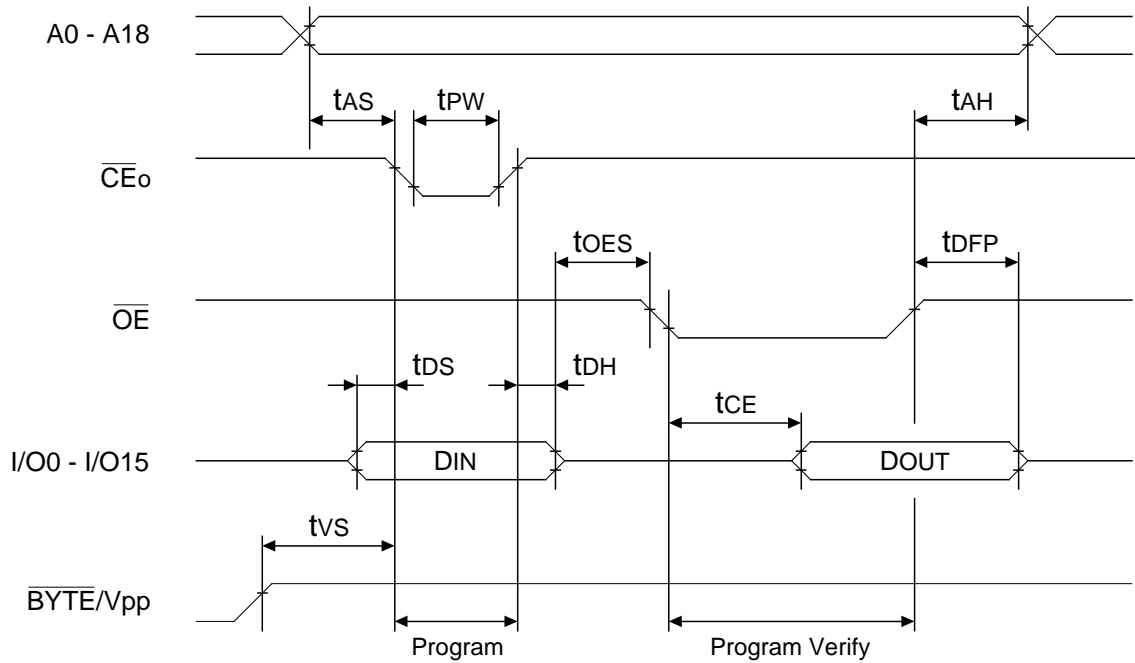
Setting up address as the following condition call the preprogrammed codes on device outputs.

(V_{CC}=3.3V±0.3V, $\overline{CE}_0=V_{IL}$, $\overline{BYTE}/V_{pp}=V_{IH}$, Ta=25°C±5°C)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	DATA
0	1	0	1	0	1	0	1	0	VH*	0	1	0	1	0	1	0	0	1	FF00
1	0	1	0	1	0	1	0	1	VH*	1	0	1	0	1	0	1	1	0	00FF

*:VH=8V

OTP Programming Waveform



Note : When OTP is programming mode , \overline{CE}_o should be "H" level.

Capacitance

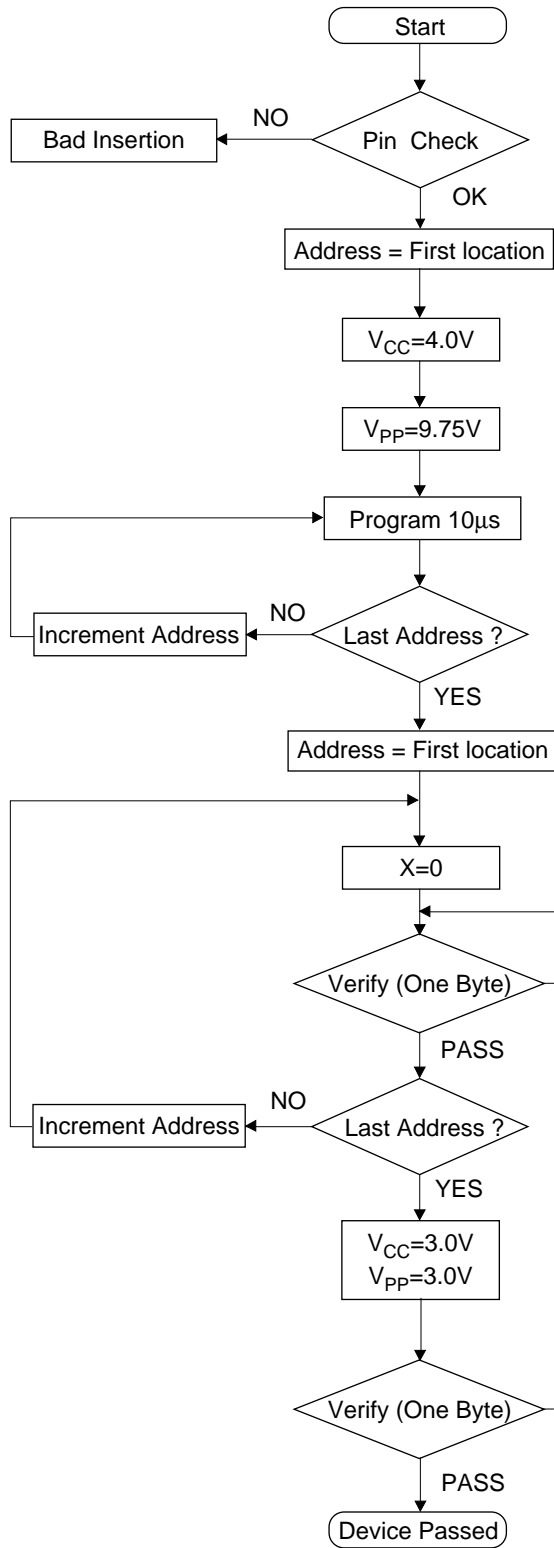
($V_{cc}=3.3V$, $T_a=25^\circ C$, $f=1MHz$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	CIN1	V I=0V	—	—	10	pF
\overline{BYTE}/V_{PP} Capacitance	CIN2		—	—	60	pF
Input/Output Capacitance	CI/O	VO=0V	—	—	10	pF

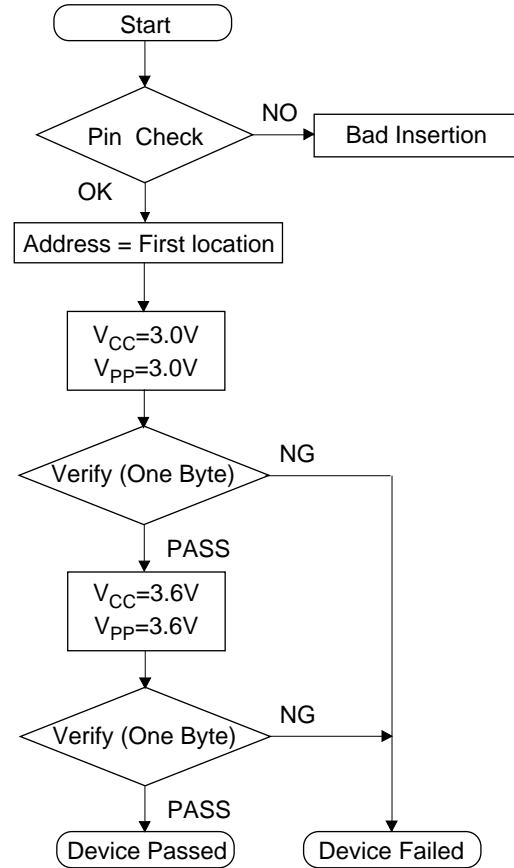
Note : This parameter is periodically sampled and not 100% tested.

OTP Programming / Verify Flow Chart

Programming



Verify



NOTICE

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