M66010FP/GP

24-BIT I/O EXPANDER

DESCRIPTION

M66010 Semiconductor Integrated Circuit inputs 24-bit data in series and outputs it in parallel and vice versa, using shift register function.
Equipped with 2 independent shift registers, one for serial-to-parallel, the other for parallel-to-serial, this IC is able to read serial input data into a shift register while converting data from parallel to serial. Parallel input/output pins are set to input or output according to the bit.
The M66010 is useful in a wide range of applications, such as MCU (micro controller unit) input/output port extension and serial bus system data communication.

FEATURES

- Two-way serial data communication with MCU
- Serial data intake possible during parallel-to-serial conversion
- Parallel input/output switchable according to the bit
- Low power dissipation: 100µW maximum per package
  (V_{CC} =5V, Ta = 25˚C, quiescent)
- Schmidt input (DI, CLK, $\overline{S}$, $\overline{CS}$)
- Open drain output (DO, D1 thru D24)
- Parallel data input and output (D1 thru D24)
- Wide operating supply voltage range (V_{CC} = 2V ~ 6V)

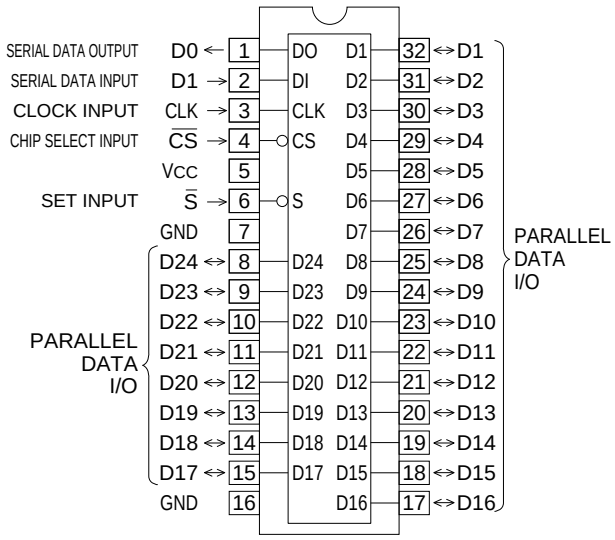
APPLICATION

MCU-related serial-parallel data conversion, serial bus control by MCU, etc.

FUNCTION

The M66010 is produced by using the silicon gate CMOS (complementary metal-oxide semiconductor) technology. It is distinguished for low power dissipation and high noise resistance.
Because two independent shift registers are built in, one for serial-to-parallel, the other for parallel-to-serial, this IC is able to read serial input data into a shift register while converting parallel data into serial data.
One cycle of latching 24-bit parallel data and outputing it in series while taking in serial data from MCU is initiated by $\overline{CS}$'s shift from "H" to "L". At $\overline{CS}$ fall edges, 24-bit parallel data is latched, and output in series from pin DO synchronously with shift clock fall edges. At shift clock rise edges, serial data is taken in from MCU via pin DI. The data is read into shift register. The 25th and following shift clock pulses are ignored and read-in operation is masked. The pin D0 status shifts to high-impedance. As $\overline{CS}$ is then shifted from "L" to "H", 24-bit serial data taken in via pin DI is output in parallel to pins D1 thru D24. Because parallel output pins are the n-channel open drain output type, write data "H" for pins which should be set to input.

PIN CONFIGURATION (TOP VIEW)

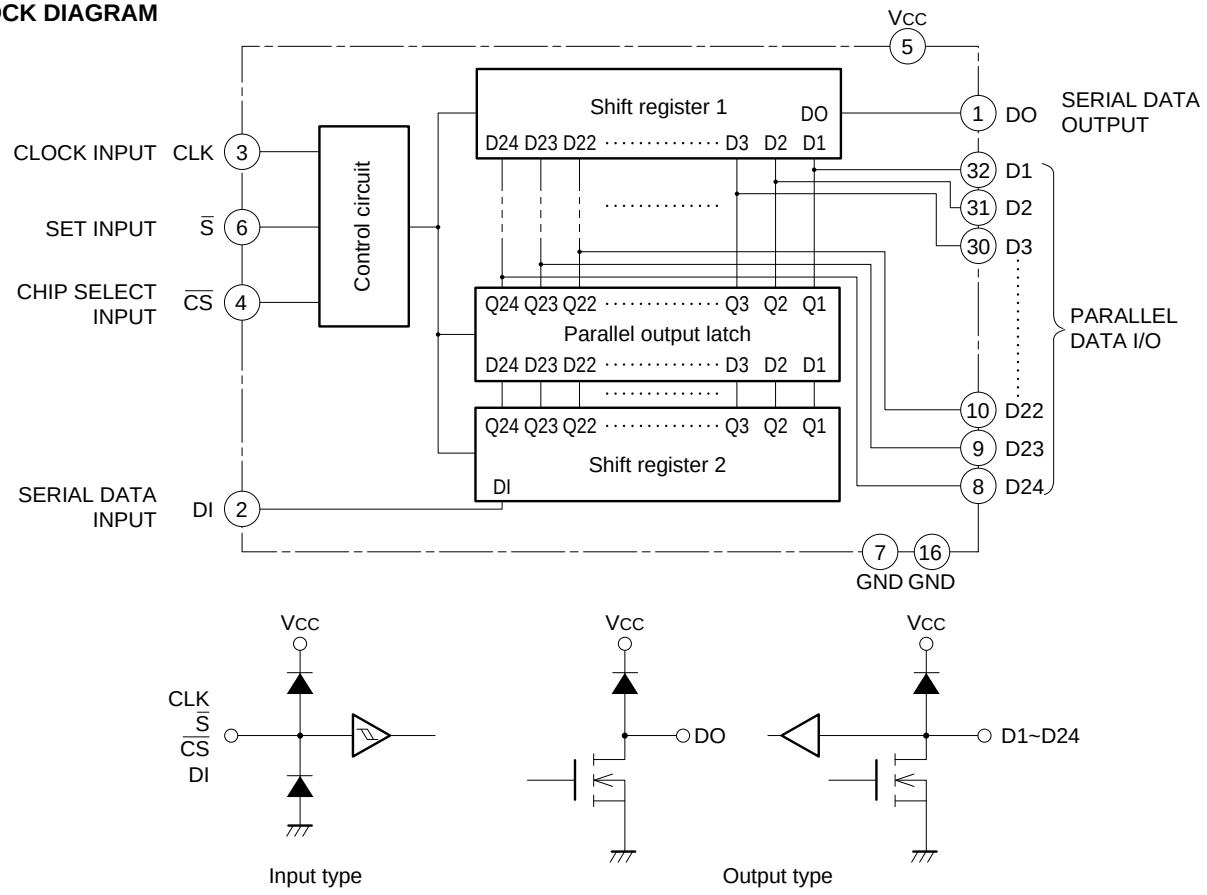


Outline 32P2W-A
32P2U-B

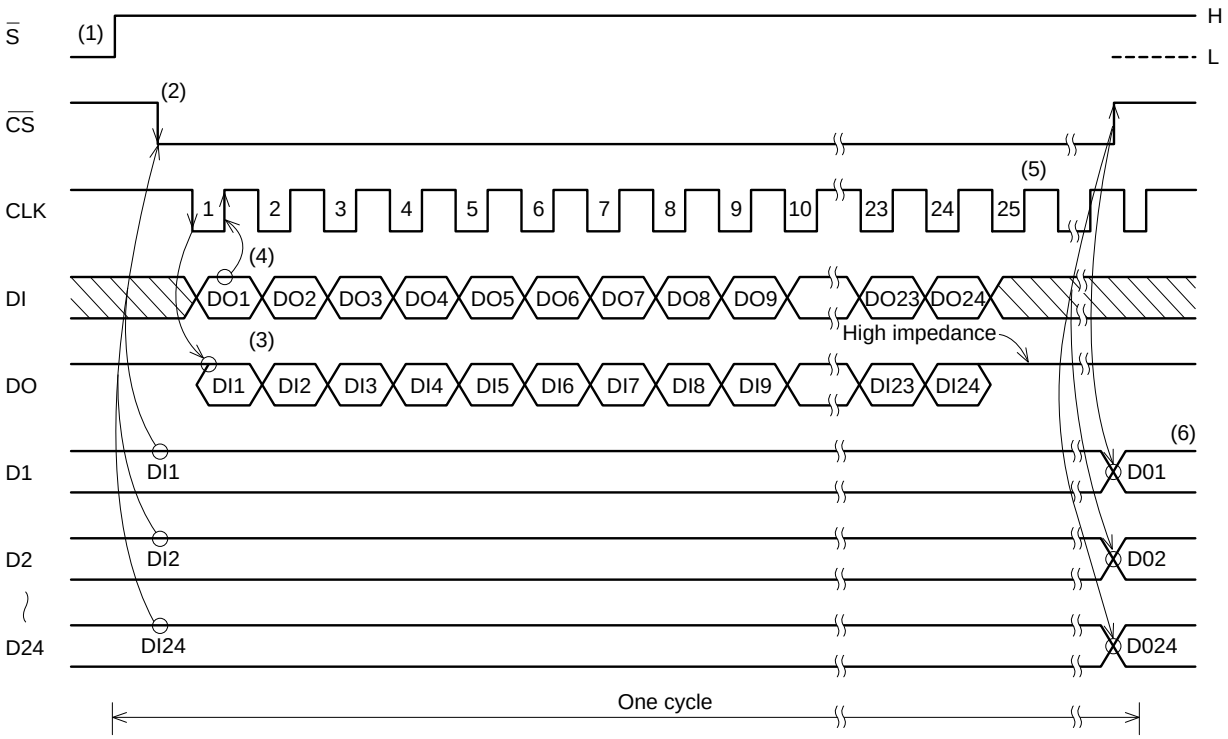
OPERATION

(1) When power is turned on, the status of pins D0 and D1 thru D24 is unstable. Their status turns high-impedance when $\overline{S}$ is shifted to "L".
(2) At $\overline{CS}$ fall edges, the status of pins D1 thru D24 is loaded on shift register 1.
(3) At CLK fall edges, 24-bit data loaded as described above is output in series from pin D0.
(4) At CLK rise edges, 24-bit serial data is taken in from pin DI and written on shift register 2.
(5) The 25th and following CLK pulses are ignored, and serial data write is discontinued. Pin D0 status turns high-impedance.
(6) At $\overline{CS}$ rise edges, data written as described in (4) is output to pins D1 thru D24.
(7) Shift register 1 loads data added from outside as well as AND tie data which has the same contents as data latched by serial output latch.
(8) If the $\overline{CS}$ rises before CLK reaches the 24th bit, parallel output latch latches data which has been written on shift register, and output it to pins D1 thru D24.
(9) Pins D1 thru D24 are switched between input and output according to serial data input to pin DI. Pins for which "H" is written are set to input.

BLOCK DIAGRAM



OPERATION TIMING CHART



ABSOLUTE MAXIMUM RATINGS (T_a = –20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
I_{IK}	Input protection diode current	V_I<0V	–20	mA
		V_I>V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O<0V	–20	mA
		V_O>V_{CC}	20	
I_{GND}	GND current	GND	–150	mA
T_{stg}	Storage temperature		–65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	–20		75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 2 ~ 6V unless otherwise noted)

Symbol	Parameter	Test conditions		Limits					Unit
				Ta=25°C			Ta= –20~75°C		
				Min.	Typ.	Max.	Min.	Max.	
V_{T+}	Upper threshold voltage	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA	CLK, $\overline{CS}$, $\overline{S}$, DI	0.35 × V_{CC}		0.8 × V_{CC}	0.35 × V_{CC}	0.8 × V_{CC}	V
V_{T-}	Lower threshold voltage	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA		0.2 × V_{CC}		0.65 × V_{CC}	0.2 × V_{CC}	0.65 × V_{CC}	V
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA	D1 ~ D24	0.75 × V_{CC}			0.75 × V_{CC}		V
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20μA				0.25 × V_{CC}		0.25 × V_{CC}	V
V_{OL}	Open drain low-level output voltage	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=5mA			0.4		0.5	V
I_O	Output leakage current	V_I=V_{T+}, V_{T-} V_{CC}=6V	V_O=V_{CC}			1.0		10.0	μA
			V_O=GND			–1.0		–10.0	
I_{IH}	High-level Input leakage current	V_I=V_{CC}	V_{CC}=6.0V			0.1		1.0	μA
I_{IL}	Low-level output leakage current	V_I=GND	V_{CC}=6.0V			–0.1		–1.0	μA
I_{CC}	Static power dissipation	V_I=V_{CC}, GND	V_{CC}=6.0V			20.0		200.0	μA

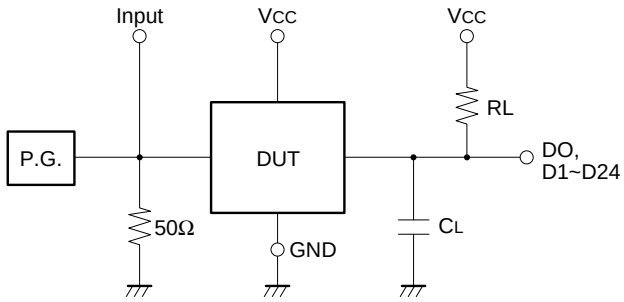
SWITCHING CHARACTERISTICS (V_{CC} = 5V)

Symbol	Parameter	Test conditions	Limits					Unit
			Ta=25°C			Ta= –20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
f_{max}	Input clock maximum repetitive frequency	C_L=50pF R_L=1kΩ (Note)	2.5			1.9		MHz
t_{PLZ}	"L–Z" and "Z–L" outputs propagation time CLK-DO				300		400	ns
t_{PZL}					300		400	ns
t_{PLZ}	"L–Z" and "Z–L" outputs propagation time $\overline{CS}$-D1 to D24				300		400	ns
t_{PZL}					300		400	ns
t_{PLZ}	"L–Z" outputs propagation time $\overline{S}$=DO, D1 to D24				300		400	ns

TIMING CONDITIONS (V_{CC} = 5V)

Symbol	Parameter	Test conditions	Limits					Unit
			Ta=25˚C			Ta= –20~75˚C		
			Min.	Typ.	Max.	Min.	Max.	
t_w	CLK, $\overline{CS}$ and $\overline{S}$ pulse width		200			260		ns
t_{su}	DI setup time (in response to CLK)		100			130		ns
	$\overline{CS}$ setup time (in response to CLK)		100			130		
	DI thru D24 setup time (in response to $\overline{CS}$)		100			130		
t_h	DI hold time (in response to CLK)		100			130		ns
	$\overline{CS}$ hold time (in response to CLK)		100			130		
	D1 thru D24 hold time (in response to $\overline{CS}$)		100			130		
t_{rec}	$\overline{CS}$ recovery time (in response to $\overline{S}$)		100			130		ns

NOTE: TEST CIRCUIT



(1) Pulse generator (PG) characteristics: t_r=t_f=6ns (10% ~ 90%)
(2) Capacitance C_L includes connection floating capacitance and probe input capacitance.

TIMING CHARTS