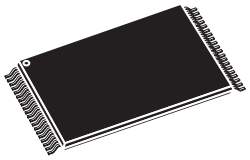
M39432

Single Chip 4 Mbit Flash and 256 Kbit Parallel EEPROM Memory

- 3.3V±10% SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPARATIONS
- 120ns ACCESS TIME (Flash and EEPROM blocks)
- WRITE, PROGRAM and ERASE STATUS BITS
- CONCURRENT MODE (Read Flash while writing to EEPROM)
- 100,000 ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- LOW POWER CONSUMPTION
  - Stand-by mode: 40µA
  - Automatic Stand-by mode
  - Deep Power Down mode
- 64 bytes ONE TIME PROGRAMMABLE MEMORY
- STANDARD EPROM/OTP MEMORY PACKAGE
- EXTENDED TEMPERATURE RANGES



TSOP40 (NC)
10 x 20 mm

DESCRIPTION

The M39432 is a memory device combining Flash and EEPROM into a single chip and using single supply voltage. The memory is mapped in two blocks: 4 Mbit of Flash memory and 256 Kbit of EEPROM memory. Each space is independant for writing, in concurrent mode the Flash Memory can be read while the EEPROM is being written.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{EE}$	EEPROM Block Enable
$\overline{EF}$	Flash Block Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
R/$\overline{B}$	Ready/Busy Output
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

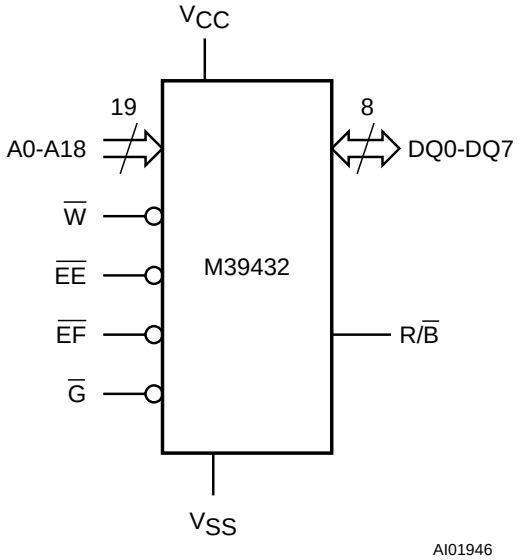
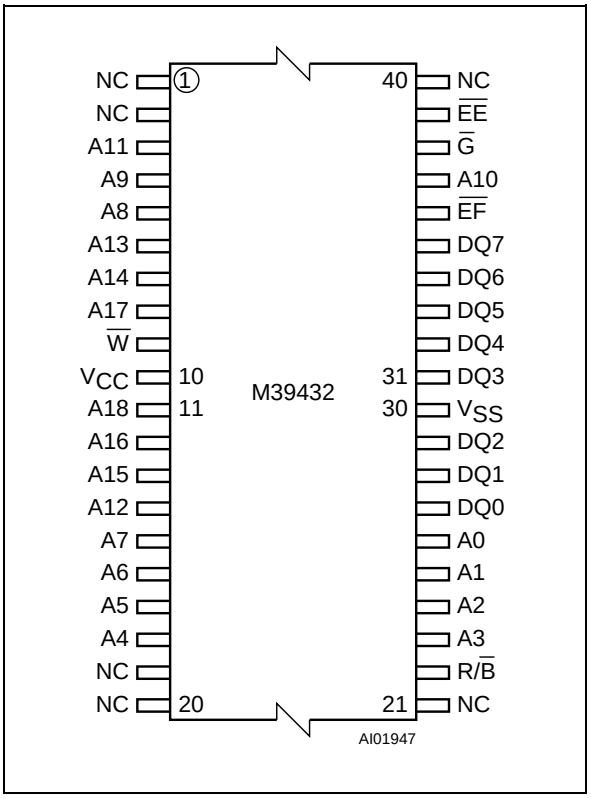


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}, V_G, V_{EF} (2)	A9, $\overline{G}$, $\overline{EF}$ Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

Figure 2. TSOP Pin Connections



Warning: NC = Not Connected.

DESCRIPTION (Cont'd)

An additional 64 bytes of EPROM are One Time Programmable.

The M39432 EEPROM array may be written by byte or by page of 64 bytes and the integrity of the data can be secured with the help of the Software Data Protection (SDP).

The M39432 Flash Memory array offers 8 blocks of 64 Kbytes, each sector may be erased individually, and programmed Byte-by-Byte. Each block can be separately protected and unprotected against program and erase. Block erasure may be suspended, while data is read from other blocks of the Flash array (or EEPROM memory block), and then resumed. The Flash array is functionally compatible with the M29W040 4 Mbit Single Voltage Flash Memory.

During a Program or Erase cycle in the Flash array or during a Write in the EEPROM memory block, the status of the M39432 internal logic can be read on the Data Outputs DQ7,DQ6, DQ5 and DQ3.

PIN DESCRIPTION

Address Inputs (A0-A18). The address inputs for the memory array are latched during a write operation. A0-A14 access locations in the EEPROM memory block A0-A18 access locations in the Flash memory block. The memory block selected is given by the state on the $\overline{EE}$ and $\overline{EF}$ inputs respectively.

When a specific voltage (V_{ID}) is applied on the A9 address input, additional specific areas can be accessed: Read the Manufacturer identifier, Read the Flash block identifier, Read/Write the EEPROM block identifier, Verify the Flash Block Protection Status.

Figure 3. Flash Memory Map and Block Address Table

A18	A17	A16		TOP ADDRESS	BOTTOM ADDRESS
1	1	1	64K Bytes Block	7FFFFh	70000h
1	1	0	64K Bytes Block	6FFFFh	60000h
1	0	1	64K Bytes Block	5FFFFh	50000h
1	0	0	—	4FFFFh	40000h
0	1	1	—	3FFFFh	30000h
0	1	0	—	2FFFFh	20000h
0	0	1	64K Bytes Block	1FFFFh	10000h
0	0	0	64K Bytes Block	0FFFFh	00000h

AI01362B

Data Input/Output (DQ0-DQ7). A write operation inputs one byte which is latched when $\overline{E}$ (or $\overline{EF}$) and Write Enable $\overline{W}$ are driven active.

Data read is valid when one Chip Enable (Chip Enable Flash or Chip Enable EEPROM) and Output Enable are driven active. The output is high impedance when the chip is deselected (both $\overline{E}$ and $\overline{EF}$ driven high) or the outputs are disabled ($\overline{G}$ driven high).

Read operations are used to output the contents from the memory, the Manufacturer identifier, the Flash Sector protection Status, the Flash block Identifier, the EEPROM identifier or the OTP row content.

Memory Block Enable ($\overline{E}$ and $\overline{EF}$). The Memory Block Enable ($\overline{E}$ or $\overline{EF}$) activates the memory control logic, input buffers, decoders and sense amplifiers. When the $\overline{E}$ input is driven high, the EEPROM memory block is not selected; when the $\overline{EF}$ input is driven high, the Flash memory block is not selected. Attempts to access both EEPROM and Flash blocks ($\overline{E}$ low and $\overline{EF}$ low) are forbidden. Switching between the two memory block enables ($\overline{E}$ and $\overline{EF}$) must not be made on the same clock cycle, a delay of greater than t_{EHFL} must be inserted.
The M39432 is in standby when both $\overline{EF}$ and $\overline{E}$ are High (when no internal Erase or programming is running). The power consumption is reduced to the standby level and the outputs are in the high impedance state, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

After 150ns of inactivity and when the addresses are driven at CMOS levels, the chip automatically enters a pseudo standby mode where consumption is reduced to the CMOS standby value, while the outputs continue to drive the bus.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. The data outputs are in the high impedance state when the Output Enable $\overline{G}$ is High.

During Sector Protect and Sector Unprotect operations, the $\overline{G}$ input must be forced to V_{ID} level (12V + 0.5V) (for Flash memory block only).

Write Enable ($\overline{W}$). Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

Ready/Busy (R/$\overline{B}$). The Ready/Busy pin outputs the status of the device when the EEPROM memory block is under the write condition

– R/$\overline{B}$ = '0': internal writing is in process,

– R/$\overline{B}$ = '1': no internal writing in in process.

It should be noted that the Ready/Busy pin does not reflect the status of Programming/Erasing in the Flash memory.

This status bit can be used when reading (or fetching opcodes) in the Flash memory block.

The Ready/Busy output uses an open drain transistor, allowing therefore the use of the M39432 in multi-memory applications with all Ready/Busy outputs connected to a single Ready/Busy line (OR-wired with an external pull-up resistor).

Table 3. Basic Operations

Operation	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read in Flash Block
	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Read in EEPROM Block
Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Write in Flash Block
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Write in EEPROM Block
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
	V_{IH}	V_{IL}	V_{IH}	X	Hi-Z
Standby	V_{IH}	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}.

OPERATIONS

The M39432 memory is addressed through 19 inputs A0-A18 and provides data on eight Data Inputs/Outputs DQ0-DQ7 with the help of four control lines: Chip Enable EEPROM ($\overline{EE}$), Chip Enable Flash ($\overline{EF}$), Output Enable ($\overline{E}$) and Write Enable ($\overline{W}$) inputs.

An operation is defined as the basic decoding of the logic level applied to the control input pins ($\overline{EF}$, $\overline{EE}$, $\overline{G}$, $\overline{W}$) and the specified voltages applied on the relevant address pins. These operations are detailed in Table 3.

Read. Both Chip Enable and Output Enable (that is $\overline{EF}$ and $\overline{G}$ or $\overline{EE}$ and $\overline{G}$) must be low in order to read the output of the memory.

Read operations are used to output the contents from the Flash or EEPROM block, the Manufacturer identifier, the Flash Sector protection Status, the Flash block Identifier, the EEPROM identifier or the OTP row content.

Notes:

– The Chip Enable input mainly provides power control and should be used for device selection. The Output Enable input should be used to gate data onto the output in combination with active $\overline{EF}$ or $\overline{EE}$ input signals.

– The data read depends on the previous instruction entered into the memory (see Table 4).

Write. A Write operation can be used for two goals:

– either write data in the EEPROM memory block

– or enter a sequence of bytes composing an instruction.

The reader should note that Programming a Flash byte is an instruction (see Instructions paragraph).

Writing data requires:

– the Chip Enable (either $\overline{EE}$ or $\overline{EF}$) to be Low

– the Write Enable ($\overline{W}$) to be Low with Output Enable (G) High.

Addresses in Flash block (or EEPROM block) are latched on the falling edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs last; the data to be written in Flash block (EEPROM block) is latched on the rising edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs first.

Specific Read and Write Operations. Device specific data is accessed through operations decoding the V_{ID} level applied on A9 (V_{ID} = 12V + 0.5V) and the logic levels applied on address inputs (A0, A1, A6). These specific operations are:

– Read the Manufacturer identifier

– Read the Device identifier

– Define the Flash Sector protection

– Read the EEPROM identifier

– Write the EEPROM identifier

Note: The OTP row (64 bytes) is accessed with a specific software sequence detailed in the paragraph "Write in OTP row".

Instructions

An instruction is defined as a sequence of specific Write operations. Each received byte is sequentially decoded (and not executed as standard Write operations) and the instruction is executed when the correct number of bytes are properly received and the time between two consecutive bytes is shorter than the time-out value.

The sequencing of any instruction must be followed exactly, any invalid combination of instruction bytes or time-out between two consecutive bytes will reset the device logic into a Read memory state (when addressing the Flash block) or directly decoded as a single operation when addressing the EEPROM block.

Table 4. Instructions (1)

Instruction	$\overline{EE}$	$\overline{EF}$	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
Read Manufacturer Identifier (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) at (0,0,0)			
Read Flash Identifier (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read identifier with (A0,A1,A6) at (1,0,0)			
Read OTP Row	0	1	AAh @5555h	55h @2AAAh	90h @5555h	Read byte 1	Read byte 2		Read byte N
Read Block Protection Status (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) at (0,1,0)			
Program a Flash Byte	1	0	AAh @5555h	55h @2AAAh	A0h @5555h	Data @address			
Erase one Flash Block	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	30h @Sector address	30h @Sector address(3)
Erase the Whole Flash	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	10h @5555h	
Suspend Block Erase	1	0	B0h @any address						
Resume Block Erase	1	0	30h @any address						
EEPROM Power Down	0	1	AAh @5555h	55h @2AAAh	30h @5555h				
Deep Power Down	1	0	20h @5555h						
SDP Enable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	A0h @5555h	Write byte 1	Write byte 2		Write byte N
SDP Disable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	20h @5555h	
Write in OTP Row	0	1	AAh @5555h	55h @2AAAh	B0h @5555h	Write byte 1	Write byte 2		Write byte N
Return (from OTP Read or EEPROM Power Down)	0	1	F0h @ any address						
Reset	1	0	AAh @5555h	55h @2AAAh	F0h @any Address				
Reset (short instruction)	1	0	F0h @any address						

Notes: 1. AAh @5555h means Write byte AAh at address 5555h.
2. This instruction can also be performed as a simple Read operation with A9=V_{ID} (refer to READ chapter).
3. Additional blocks to be erased must be entered within 80µs.

Table 5. Device Identifiers

Identifier	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Read the Manufacturer Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Read the Flash Block Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	0E3h
Read the EEPROM Block Identifier	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	V_{ID}	Don't Care	64 bytes user defined

Note: X = Don't Care.

The M39432 set of instructions includes:

– Program a byte in the Flash block
– Read a Flash sector protection status
– Erase instructions: Flash Sector Erase, Flash Block Erase, Flash Sector Erase Suspend, Flash Sector Erase Resume
– EEPROM power down
– Deep power down
– Set/Reset the EEPROM software write protection (SDP)
– OTP row access
– Reset and Return
– Read identifiers: read the manufacturer identifier, Read the Flash block identifier

These instructions are detailed in Table 4.

For efficient decoding of the instruction, the two first bytes of an instruction are the coded cycles and are followed by a command byte or a confirmation byte. The coded cycles consist of writing the data AAh at address 5555h during the first cycle and data 55h at address 2AAAh during the second cycle.

In the specific case of the Erase instruction, the instruction expects confirmation by two additional coded cycles.

POWER SUPPLY and CURRENT CONSUMPTION

EEPROM Power Down. The M39432 can be set with the EEPROM in power down with the help of the EEPROM power down instruction (see Table 4). Once the EEPROM power down instruction is decoded, the EEPROM block cannot be accessed unless a further Return instruction is decoded.

Deep Power Down. The M39432 can be set in the lowest I_{CC} consumption mode with the help of the Deep Power Down instruction (see Table 4). Once the instruction is decoded, the device is set in a sleep mode until a Reset instruction is decoded.

Power Up. The M39432 internal logic is reset upon a power-up condition to Read memory status. Any Write operation in EEPROM is inhibited during the first 5 ms following the power-up.

Either $\overline{EF}$, $\overline{EE}$ or $\overline{W}$ must be tied to V_{IH} during Power-up for the maximum security of the data contents and to remove the possibility of a byte being written on the first rising edge of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$. Any write cycle initiation is locked when Vcc is below V_{LKO}.

READ

Read operations and instructions can be used to:

– read the contents of the Memory Array (Flash block and EEPROM block)
– read the Memory Array (Flash block and EEPROM block) status and identifiers.

Read data (Flash and EEPROM blocks)

Both Chip Enable $\overline{EF}$ (or $\overline{EE}$) and Output Enable ($\overline{G}$) must be low in order to read the data from the memory.

Read the Manufacturer Identifier

The manufacturer's identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The manufacturer's identifier can be read with a Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level (V_{ID} = 12V + 0.5V) on A9 (see Table 5).

Read Instruction. The manufacturer's identifier can also be read with a single instruction composed of 4 operations: 3 specific Write operations (see Table 4) and a Read which outputs the Manufacturer identifier, the Flash block identifier or the Flash sector protection status (depending on the levels applied on A0, A1, A6, A16, A17 and A18.

Table 6. Status Bit

	$\overline{EF}$	$\overline{EE}$	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash	V_{IL}	V_{IH}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-out	X	X	X
EEPROM	V_{IH}	V_{IL}	Data Polling	Toggle Flag	X	X	X	X	X	X

Note: X = Not guaranteed value, can be read either '1' or '0'.

Read the Flash Block Identifier

The Flash block identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The Flash block identifier (E3h) can be read with a single Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (see Table 5).

Read Instruction. The Flash block identifier can also be read with an instruction composed of 4 operations: 3 specific Write operations and a Read (see Table 4).

Read the EEPROM Block Identifier

The EEPROM block identifier (64 bytes, user defined) can be read with a single Read operation with A6 = '0' and A9 = V_{ID} (see Table 5).

Read the OTP Row

The OTP row is mapped in the EEPROM block ($\overline{EE}$ = '0', $\overline{EF}$ = '1'). Read of the OTP row (64 bytes) is by an instruction (see Table 4) composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) before reading the OTP row content.

When accessing the OTP row, only the LSB addresses (A6 to A0) are decoded where A6 must be '0'.

Each Read of the OTP row has to be followed by the Return instruction (see Table 4).

Read the Flash Sector Protection Status

Reading the Flash sector protection status is by an instruction similar to the Read Manufacturer identifier instruction, the only difference being the value of the logic levels applied on A0, A1, A6, while A16, A17 and A18 define the Flash sector whose protection has to be verified. Such a read instruction will output a 01h if the Flash sector is protected and a 00h if the Flash sector is not protected.

The Flash sector protection status can also be verified with a Read operation (see chapter: Flash block specific features), with V_{ID} on A9.

Read the Status Bits

The M39432 provides several Write operation status flags which may be used to minimize the application write (or erase or program) time. These signals are available on the I/O port bits when programming (or erasing) are in progress. It should be noted that the Ready/Busy pin also reflects the status of the EEPROM Write (the Ready/Busy pin does not reflect the status of the Flash Programming/Erasing).

Data Polling flag, DQ7. When Erasing or Programming into the Flash block (or when Writing into the EEPROM block), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is performed, the true logic value is read on DQ7 (in a Read operation).

Flash memory block specific features:

– Data Polling is effective after the fourth W pulse (for programming) or after the sixth W pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.

– During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (that is a '1' after erasing).

– if the byte to be programmed is in a protected Flash sector, the instruction is ignored.

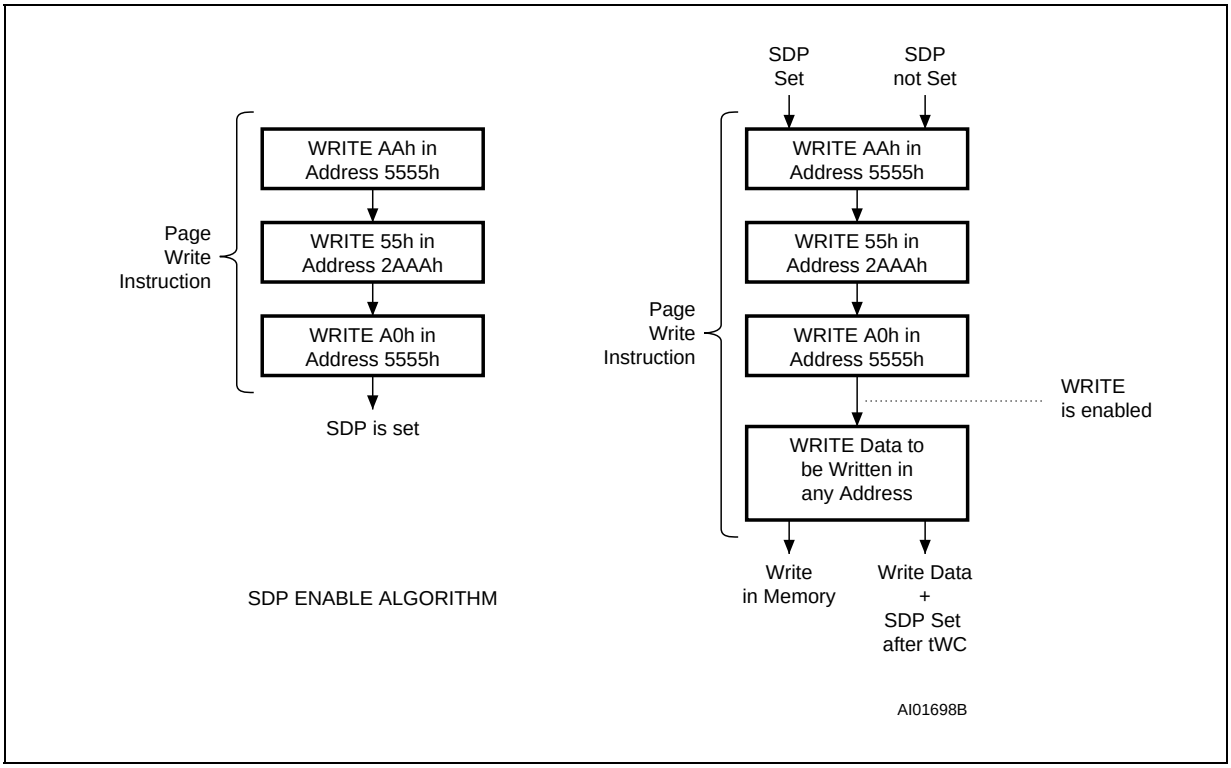
– If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed byte. No erasure will be performed.

– if all sectors are protected, a Bulk Erase instruction is ignored.

Toggle flag, DQ6. The M39432 also offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory, when either $\overline{G}$, $\overline{EE}$ or $\overline{EF}$ is low.

When the internal cycle is completed the toggling will stop and the data read on DQ0-DQ7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is completed when two successive reads yield the same output data.

Figure 4. EEPROM SDP Enable Flowcharts



Flash memory block specific features:

a. The Toggle bit is effective after the fourth $\overline{W}$ pulse (for programming) or after the sixth $\overline{W}$ pulse (for Erase).

b. If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored and:

- if all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100µs, and then return to the previous addressed byte.
- if all sectors are protected, the Bulk Erase instruction is ignored.

Error flag, DQ5 (Flash block only). This bit is set to '1' when there is a failure during either a Flash byte programming or a Sector erase or the Bulk Erase.

In case of error in Flash sector erase or byte program, the Flash sector in which the error occurred or to which the programmed byte belongs, must not be used any longer (other Flash sectors may still be used). The Error bit resets after Reset instruction.

During a correct Program or Erase, the Error bit will set to '0'.

Erase Time-out flag, DQ3 (Flash block only). The Erase Timer bit reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase timer bit is set to '0' after a Sector Erase instruction for a time period of 100µs ± 20% unless an additional Sector Erase instruction is decoded. After this time period or when the additional Sector Erase instruction is decoded, DQ3 is set to '1'.

WRITE a BYTE (or a PAGE) in EEPROM

It should be noticed that writing in the EEPROM block is an operation, it is not an instruction (as for Programming a byte in the Flash block).

Write a Byte in EEPROM Block

A write operation is initiated when Chip Enable $\overline{EE}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$, $\overline{EE}$ whichever occurs last.

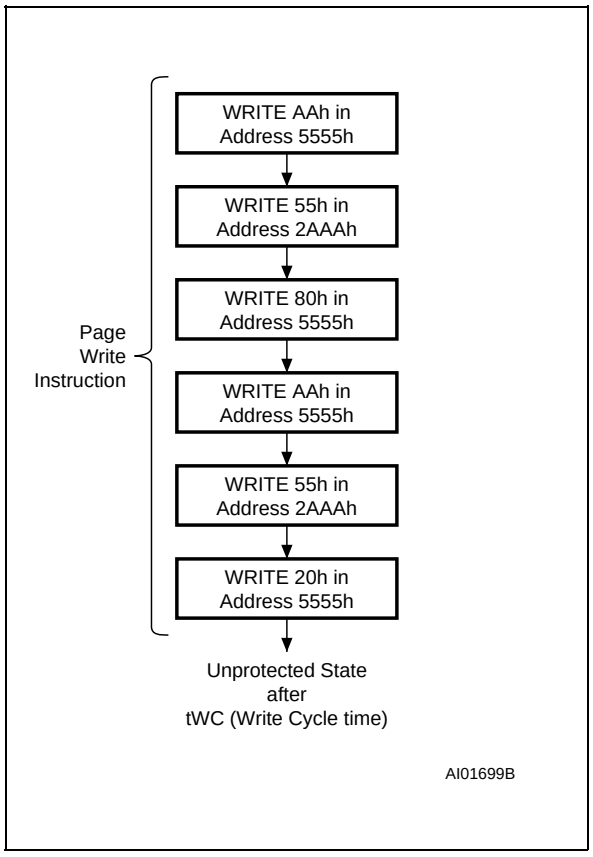
Once initiated, the write operation is internally timed until completion, that is during a time t_W.

The status of the write operation can be found by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the Ready/Busy output. This Ready/Busy output is driven low from the write of the byte being written until the completion of the internal Write sequence.

Table 7. Write the EEPROM Block Identifier

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A6	A9	Other Addresses	DQ0 - DQ7
V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	64 bytes User Defined

Figure 5. SDP disable Flowchart



Write a Page in EEPROM Block

The Page write allows up to 64 bytes within the same EEPROM page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A14 must be the same for all bytes. Once initiated, the Page write operation is internally timed until completion, that is during a time t_{WC}.

The status of the write operation can be seen by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the Ready/Busy output. This Ready/Busy output is driven low from the write of the first byte to be written until the completion of the internal Write sequence.

A Page write is composed of successive Write instructions which must be sequenced within a time period (between two consecutive Write operations) that is smaller than the t_{WLWL} value. If this period of time exceeds the t_{WLWL} value, the internal programming cycle will start.

EEPROM Block Software Data Protection

A protection instruction allows the user to inhibit all write modes to the EEPROM block: the Software Data Protection (referenced as SDP in the following). The SDP feature is useful for protecting the EEPROM memory from inadvertent write cycles that may occur during uncontrolled bus conditions.

The M39432 is shipped as standard in the unprotected state meaning that the EEPROM memory contents can be changed by the user. After the SDP enable instruction, the device enters the Protect Mode where no further write operations have any effect on the EEPROM memory contents.

The device remains in this mode until a valid SDP disable instruction is received whereby the device reverts to the unprotected state.

To enable the Software Data Protection, the device has to be written (with a Page Write) with three specific data bytes at three specific memory locations (each location in a different page) as shown in Figure 4. This sequence provides an unlock key to enable the write action, and, at the same time, SDP continues to be set. Any further Write in EEPROM when the SDP is set will use this same sequence of three specific data bytes at three specific memory locations followed by the bytes to write. The first SDP enable sequence can be directly followed by the bytes to written.

Similarly, to disable the Software Data Protection the user has to write specific data bytes into six different locations with a Page Write addressing different bytes in different pages, as shown in Figure 5.

The Software Data Protection state is non-volatile and is not changed by power on/off sequences. The SDP enable/disable instructions set/reset an internal non-volatile bit and therefore will require a write time t_{WC}, This Write operation can be monitored only on the Toggle bit (status bit DQ6) and the Ready/Busy pin. The Ready/Busy output is driven low from the first byte to be written (that is the first Write AAh, @5555h of the SDP set/reset sequence) until the completion of the internal Write sequence.

Figure 6. Data Polling Flowchart

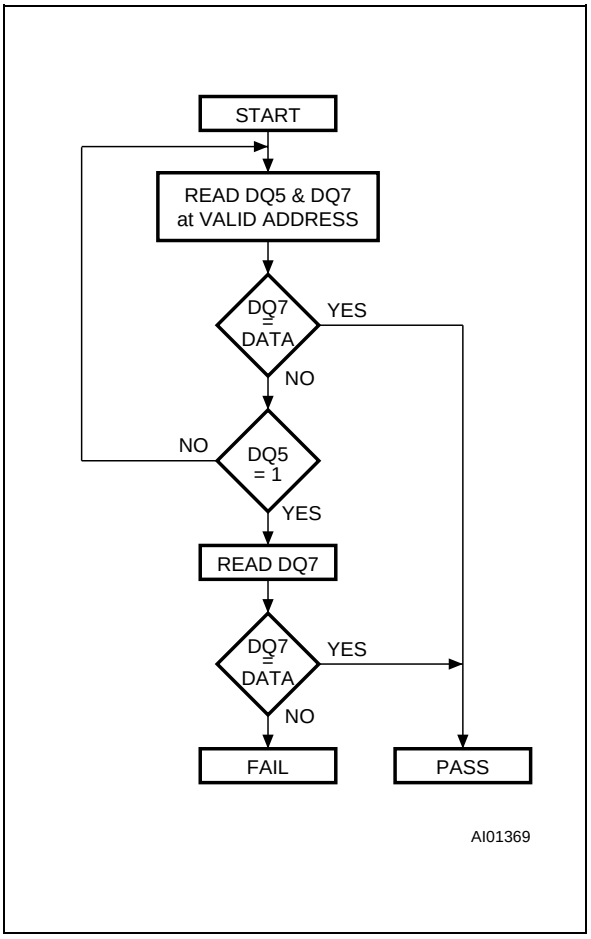
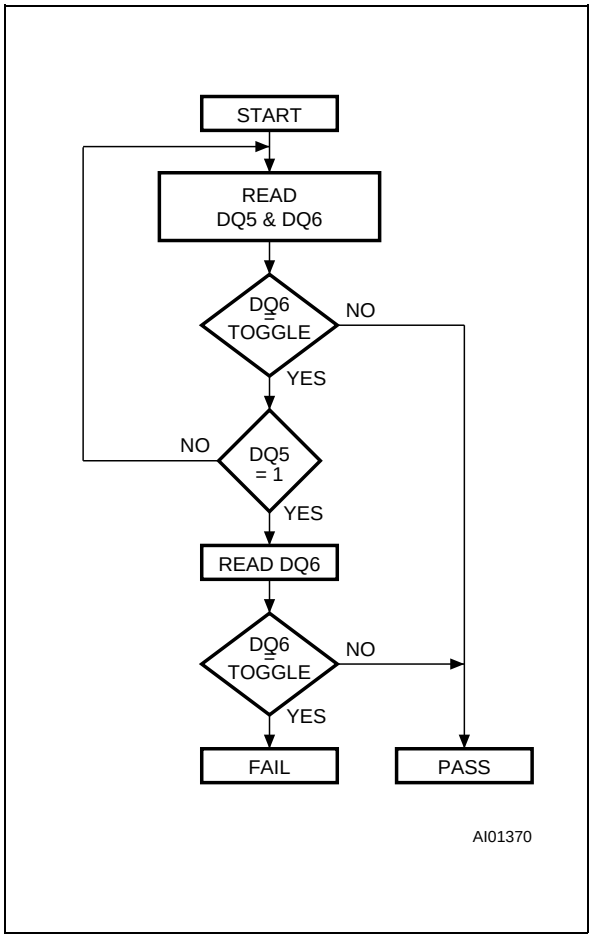


Figure 7. Data Toggle Flowchart



Write OTP Row

Writing (only one time) in the OTP row (64 bytes) is enabled by an instruction. This instruction is composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) followed by the the data to store in the OTP row (refer to Table 4).

When accessing the OTP row, the only LSB addresses (A6 to A0) are decoded, with A6 = '0'.

Write the EEPROM Block Identifier

The EEPROM block identifier can be written with a single Write operation with specific logic levels applied on A6 and the V_{ID} level on A9 (see Table 7).

PROGRAM in the Flash BLOCK

It should be noted that writing data into the EEPROM block and the Flash block is not performed in a similar way: the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s), the EEPROM memory is directly written with a simple operation (see Operation chapter).

Program Instuction. During the execution of the Program instruction, the Flash block memory will not accept any further instructions.

The Flash block memory can be programmed byte-by-byte. The program instruction is a sequence of three specific Write operations followed by writing the address and data byte to be programmed into the Flash block memory (see Table 4). The M39432 automatically starts and performs the programming after the fourth write operation.

During programming, the memory status may be checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the following sections.

Data Polling. Polling on DQ7 is a method of checking whether a Program or an Erase instruction is in progress or completed (see Figure 6). When a Program instruction is in progress, data bit DQ7 is the complement of the original data bit 7; when DQ7 is identical to the old data and the Error bit DQ5 is still '0', the instruction is complete. To determine if DQ7 is valid, each poll must store the original data for comparison, and if they are the same, it can be considered that the operation was successful. The Error bit DQ5 is checked to ensure timing limits have not exceeded.

When an Erase operation is in progress, DQ7 is always '0', and will be '1' when finished, so long as DQ5= '0'.

In all cases, when DQ5 is '1', DQ7 should be checked again, in case DQ7 changed simultaneously with DQ5. If DQ7 = true data (Program) or DQ7 = '1' (Erase), the operation is successful and execution should return to the caller. A suggested second read will provide all true data (Program) or all FFh (Erase). Otherwise, this should be flagged as an error, and the device should be Reset.

Data Toggle. Checking the Toggle bit DQ6 is an alternative method of checking if Program or Erase operations are in progress or completed (see Figure 7). When an operation is in progress, data bit DQ6 constantly toggles for successive read operations. When DQ6 no longer toggles and the Error bit DQ5 is '0', the operation is completed. To determine if DQ6 has toggled, each polling action requires 2 consecutive read operations of the data, and if the data read is the same, it can be considered that the operation was successful. The Error bit DQ5 is checked to ensure timing limits have not been exceeded. In all cases, when DQ5 is '1', DQ6 should be checked again, in case DQ6 has changed simultaneously with DQ5. If DQ6 has stopped toggling, the operation is successful and execution should return to the caller. A suggested second read will provide all true data (Program) or all FFh (Erase). Otherwise, this event should be flagged as an error, and the device should be Reset.

ERASE in the Flash BLOCK

It should be noted that:

a. Programming any byte of one Flash sector (or bulk) requires that the Flash sector (or bulk) has been previously erased (once for all bytes within the sector or bulk) with the correct instruction (see Instructions chapter).

b. Writing in the EEPROM memory is an operation triggering an automatic sequencing of byte erase followed by a byte write. Writing in EEPROM does not require a specific erase operation before writing.

Bulk Erase Instruction. The Bulk Erase instruction uses six write operations followed by Read operations of the status register bits, as described in Table 4. If any byte of the Bulk Erase instruction is wrong, the Bulk Erase instruction aborts and the device is reset to the Read Flash memory status.

During a Bulk Erase, the memory status may checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the "PROGRAM in the Flash BLOCK" chapter. The Error bit (DQ5) returns a '1' if there has been an Erase Failure (maximum number of erase cycles have been executed).

It is not necessary to program the array with 00h, the M39432 will automatically do this before erasing to FFh.

During the execution of the Bulk Erase instruction, the Flash block logic does not accept any instruction.

Sector Erase in Flash Block. The Sector Erase instruction uses six write operations, as described in Table 4. Additional Flash Sector Erase confirm commands and Flash sector addresses can written subsequently to erase other Flash sectors in parallel, without further coded cycles, if the additional instruction is transmited in a shorter time than the timeout period to end of period. The input of a new Sector Erase instruction will restart the time-out period.

The status of the internal timer can be monitored through the level of DQ3 (Erase time-out bit), if DQ3 is '0' the Sector Erase instruction has been received and the timeout is counting; if DQ3 is '1', the timeout has expired and the M39432 is erasing the Flash sector(s). Before and during Erase timeout, any instruction different than Erase suspend and Erase Resume will abort the instruction and reset the device to read array mode.
It is not necessary to program the Flash sector with 00h as the M39432 will do this automatically before erasing (byte = FFh).

During a Sector Erase, the memory status may be checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the "Program instruction" chapter. During the execution of the erase instruction, the Flash block logic accepts only the Reset and Erase Suspend instructions (erasure of one Flash sector may be suspended, in order to read data from another Flash sector, and then resumed).

Table 8. Flash Sector Protection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	A18	DQ0 - DQ7
V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	X	SA	SA	SA	Protection Activation
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	X	SA	SA	SA	Verify the protection status: when DQ0= 1, the block is protected

Notes: X = Don't care.
SA = Software Address.

Table 9. Flash Unprotection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	A18	DQ0 - DQ7
V_{ID}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	Activation of Unprotected Mode
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	X	SA	SA	SA	Verify the protection status: when 00h, the block is unprotected

Notes: X = Don't care.
SA = Software Address.

Erase Suspend Instruction. When a Flash Sector Erase operation is in progress, the Erase Suspend instruction may suspend the operation by writing B0h at any address (see Table 4). This allows reading of data from another Flash sector while erase is in progress. Erase suspend is accepted only during the Flash Sector Erase instruction execution and defaults to read array mode. An Erase Suspend instruction entered during an Erase timeout will, in addition to suspending the erase, terminates the timeout.

The Toggle bit DQ6 stops toggling when the M39432 internal logic is suspended. The Toggle bit status must be monitored at an address out of the Flash sector being erased. Toggle bit will stop toggling between 0.1µs and 15µs after the Erase Suspend instruction has been written. The M39432 will then automatically be set into Read Flash Block Memory Array mode.

When erase is suspended, Reading from Flash sectors being erased will output invalid data, a Read from Flash sector not being erased is valid. During an Erase Suspend, the Flash memory will respond only to Erase Resume and Reset instructions.

A Reset instruction will definitively abort erasure and can leave invalid data in the Flash sectors being erased.

Erase Resume Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by this instruction. The Erase Resume instruction consists of writing 30h at any address (see Table 4).

FLASH BLOCK SPECIFIC FEATURES

Flash Sector Protection. Each Flash sector can be separately protected against Program or Erase. Flash Sector Protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are set to V_{ID} (12V + 0.5V) and the Flash sector address is applied on A16, A17 and A18, as shown in Figure 8 and Table 8.

Flash sector protection is programmed with the help of a specific sequence of levels applied on $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A16, A17 and A18; this sequence includes a verification of the Protection status on DQ0 as shown in Table 8.

Any attempt to program or erase a protected Flash sector will be ignored by the device.

Remarks:

– The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status

– During the application life, the Sector protection status can be accessed with a regular Read instruction without applying a "high voltage" V_{ID} on A9. This instruction is detailed in Table 4.

Flash Sector Unprotection. Flash sectors can be unprotected to allow updating of their contents. Note that the Sector Unprotection unprotects all sectors (sector 0 up to sector 7).

Flash Sector Unprotection is activated with a specific sequence of levels applied on $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A12, A16, A17 and A18; this sequence includes a verification of the Protection status on DQ0-DQ7 as shown in Figure 9 and Table 9.

Figure 8. Block Protection Flowchart

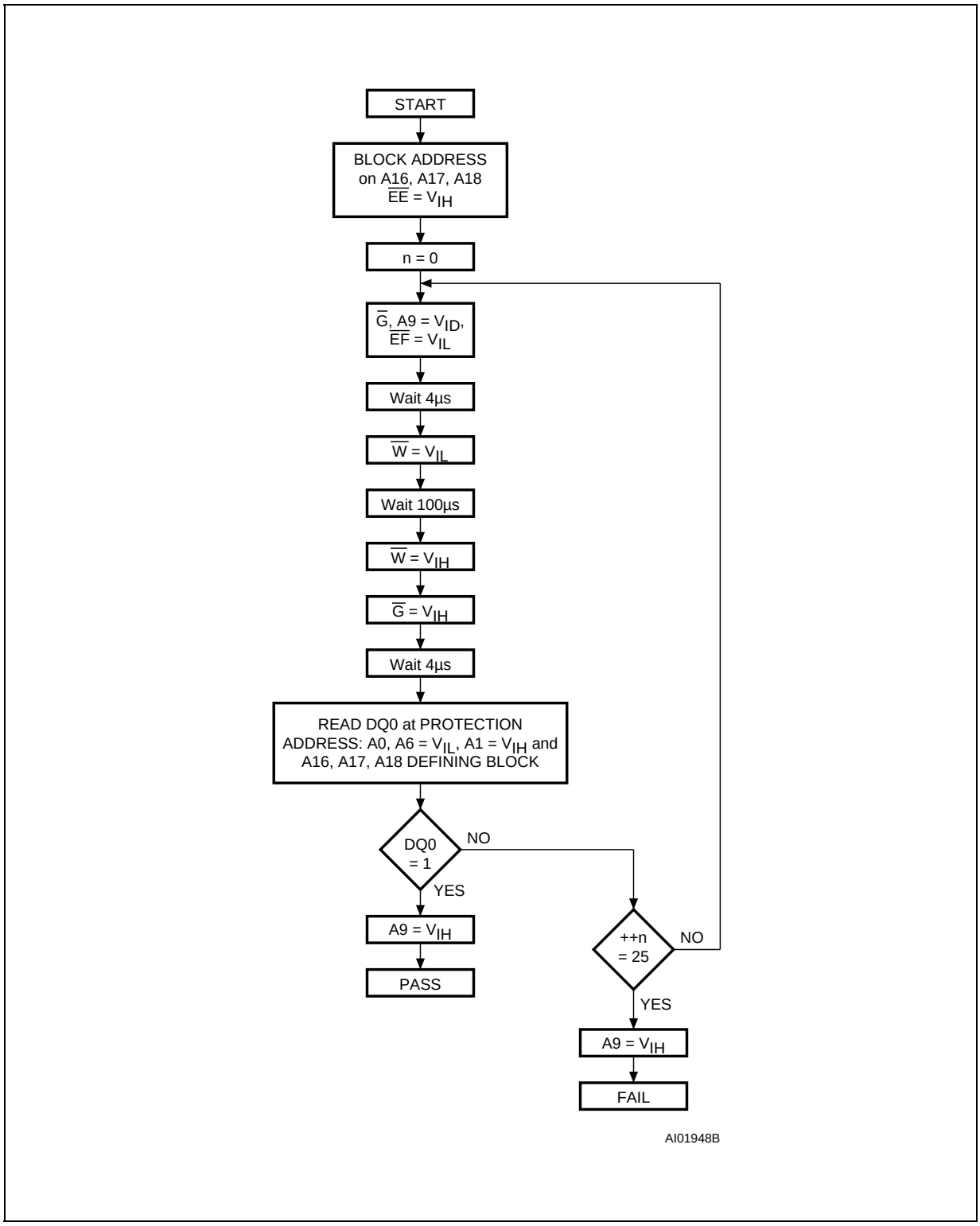
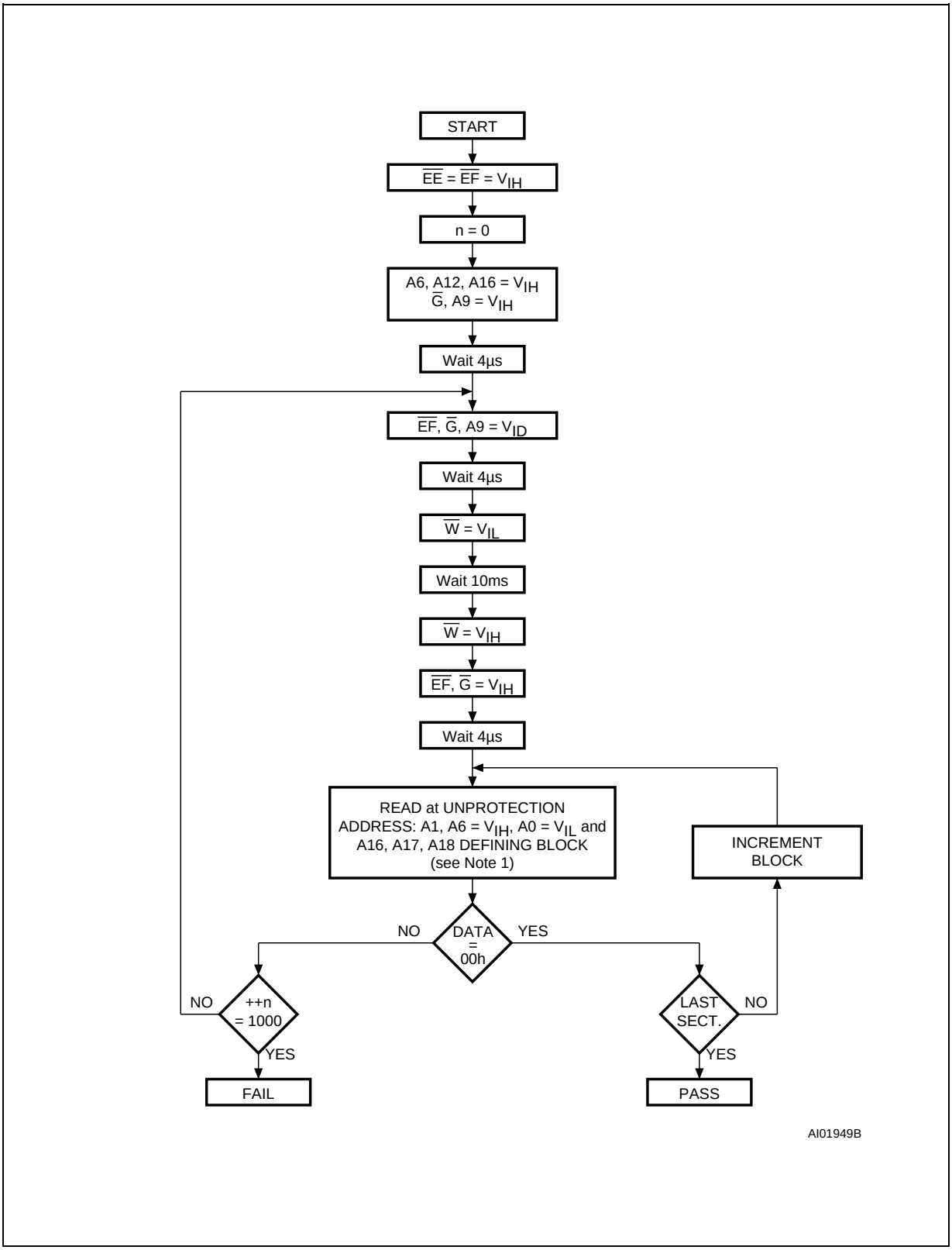


Figure 9. Block Unprotecting Flowchart



Note: 1. A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input Timing Ref. Voltages	0.8V and 2V
Output Timing Ref. Voltages	1.5V

Figure 10. AC Testing Input Output Waveform

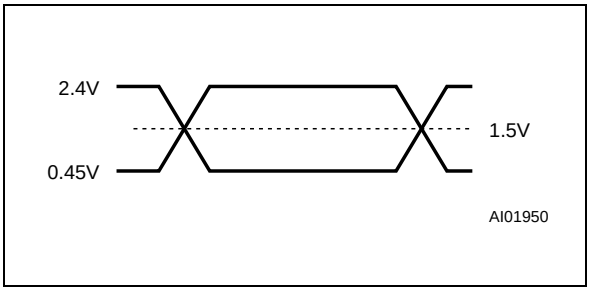


Figure 11. Output AC Testing Load Circuit

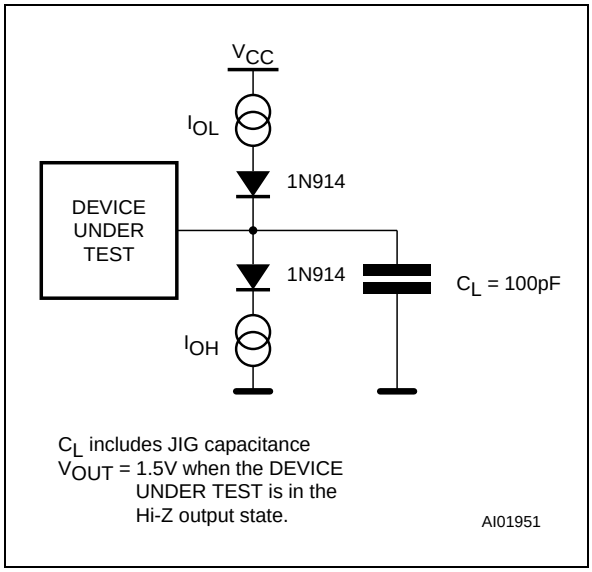


Table 11. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

FLASH BLOCK SPECIFIC FEATURES (cont' d)

This allows a guarantee of the retention of the Protection status.

Remarks:

– The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status

– During the application life, the Sector protection status can be accessed with a regular Read instruction without "high voltage" V_{ID} on A9. This instruction is detailed in Table 4.

Reset Instruction. The Reset instruction resets the device internal logic in a few µs. Reset is an instruction of either one write operation or three write operations (refer to Table 4).

Supply Rails. Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The printed circuit board trace width should be sufficient to carry the V_{CC} program and erase currents required.

GLOSSARY

Block: EEPROM block (256 Kbit) or Flash block (4Mbit)

Bulk: the whole Flash block (4Mbit)

Sector: 64 Kbyte of Flash memory

Page: 64 bytes of EEPROM

Write and Program: Writing (into the EEPROM block) and Programming (the Flash block) is not performed in a similar way:

– the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s)

– the EEPROM memory is directly written with a simple operation (see Operation chapter).

SDP: Software Data Protection. Used for protecting the EEPROM block against false Write operations (as in noisy environments).

Table 12. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} (1)	Supply Current (Read Flash) TTL	$\overline{EE} = V_{IH}$, $\overline{EF} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC2}	Supply Current (Read EEPROM) TTL	$\overline{EE} = V_{IL}$, $\overline{EF} = V_{IH}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{EF} = \overline{EE} = V_{CC} \pm 0.2V$		40	µA
I_{CC4}	Supply Current (Flash Block Program or Erase)	Byte program, Sector or Chip Erase in progress		20	mA
I_{CC5}	Supply Current (EEPROM Write)	During t_{WC}		20	mA
I_{CC6}	Supply Current in Deep Power Down Mode	After a Deep Power Down instruction (see Table 4)		2	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2mA	0.85 V_{CC}		V
V_{ID}	A9 High Voltage		11.5	12.5	V
I_{ID}	V_{ID} Current	A9 = V_{ID}		50	µA
V_{LKO}	V_{CC} Minimum for Write, Erase and Program		1.9	2.2	V

Note: 1. When reading the Flash block when an EEPROM byte(s) is under a write cycle, the supply current is I_{CC1} + I_{CC5}.

Figure 12. Read Mode AC Waveforms

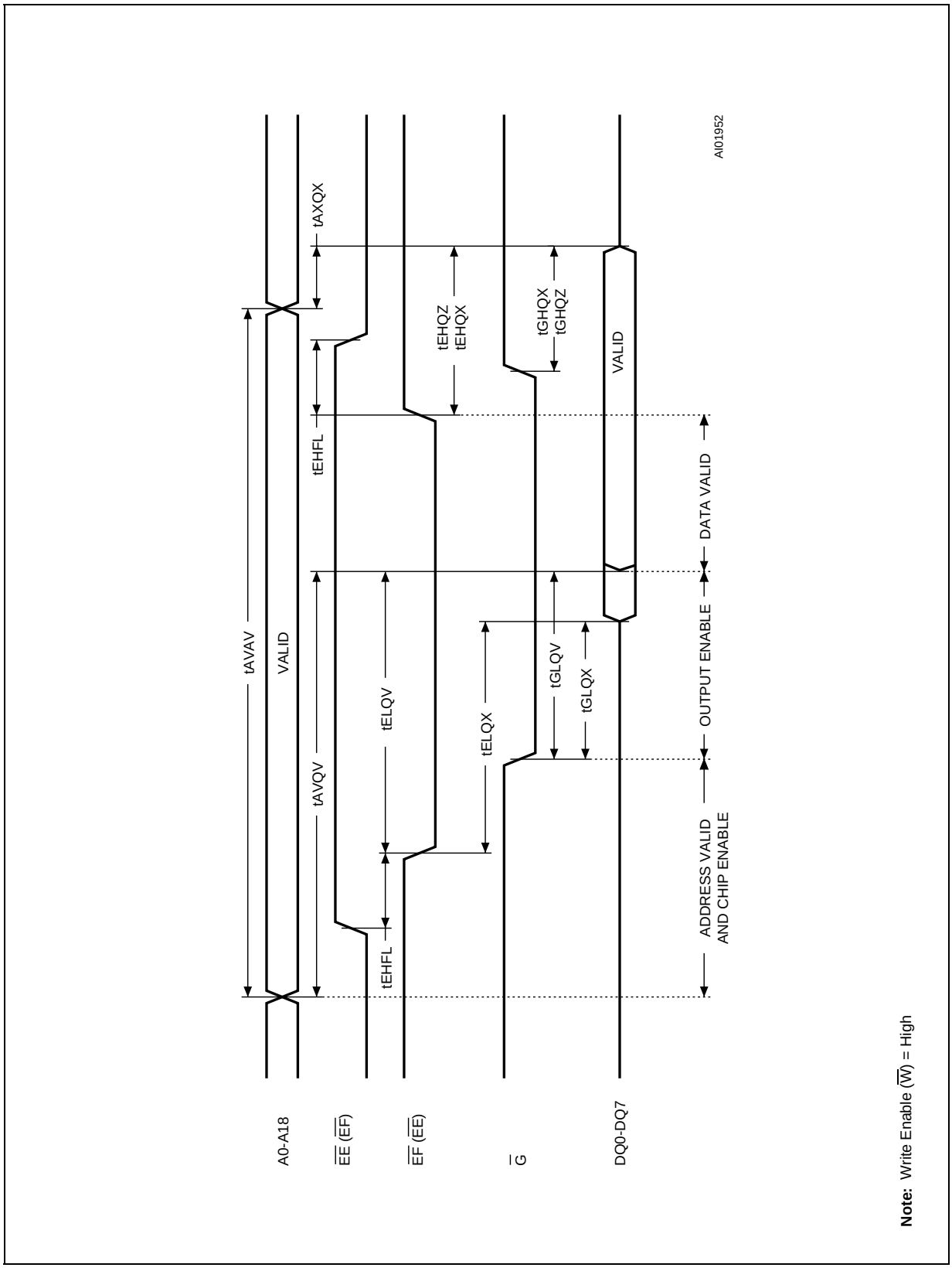


Table 13A. Read AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	M39432				Unit
				-120		-150		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, $\overline{EF}$) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, $\overline{EF}$) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})		55		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		40		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})		40		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, $\overline{EF}$) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}	0		0		ns
t_{EHFL}	t_{CED}	$\overline{EE}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{EE}$)		100		100		ns

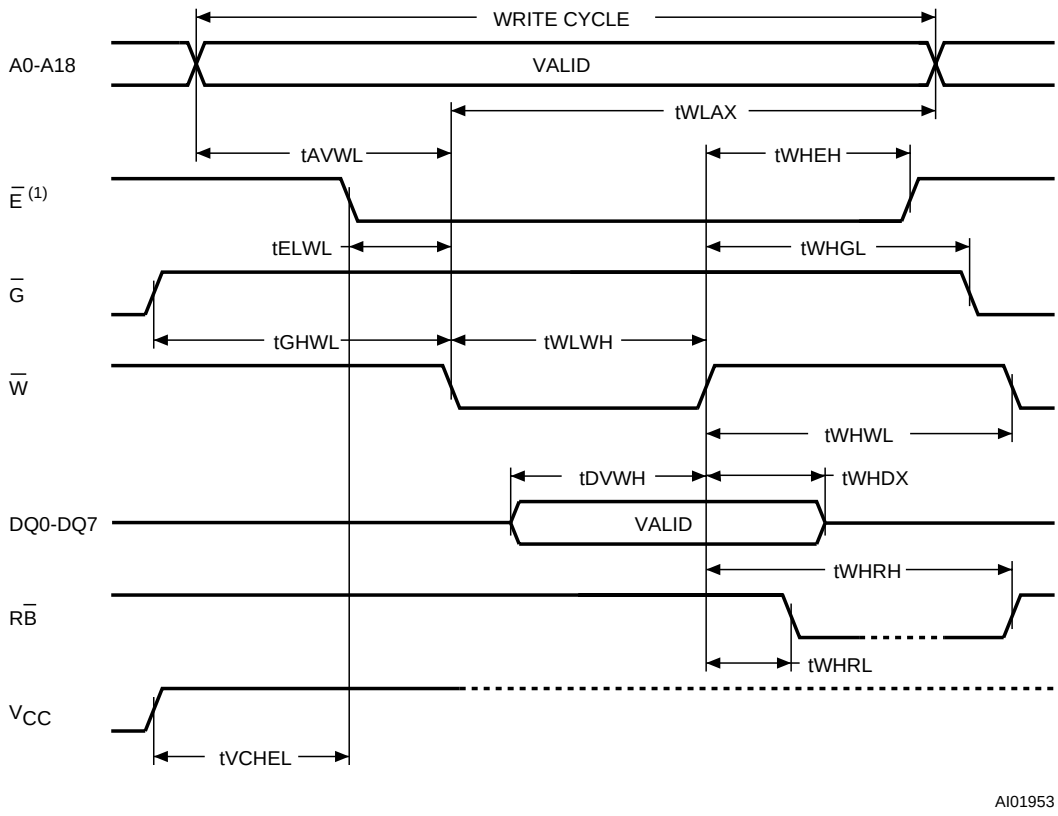
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EE}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Table 13B. Read AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	M39432				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	200		250		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$		200		250	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$		70		120	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$		50		60	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, EF) = (V_{IH}, V_{IL})$		50		60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(EE, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	0		0		ns
t_{EHFL}	t_{CED}	$\overline{EE}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{EE}$)		100		100		ns

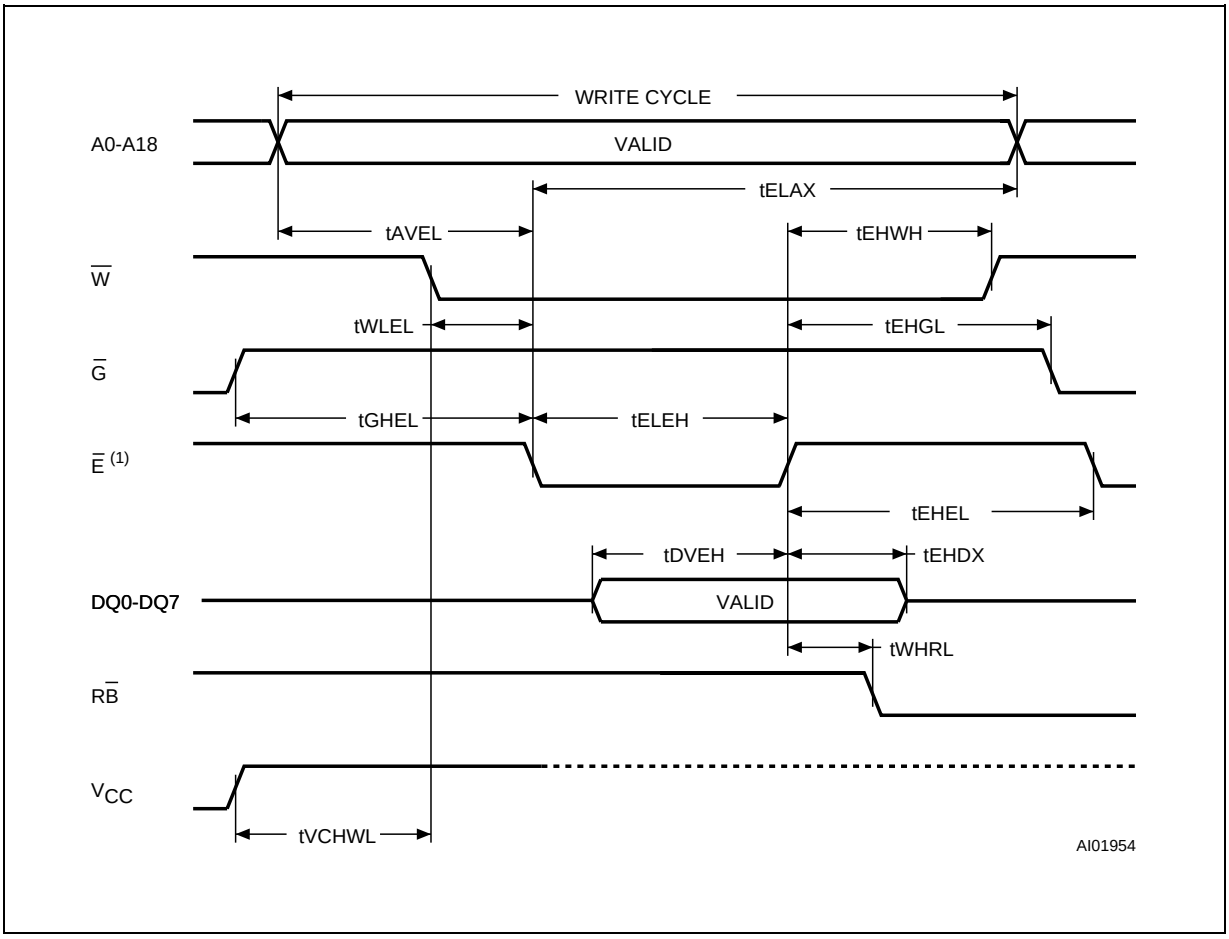
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EE}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Figure 13. Write AC Waveforms, $\overline{W}$ Controlled



Notes: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Figure 14. Write AC Waveforms, $\overline{E}$ Controlled



Notes: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Table 14. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	M39432								Unit
			-120		-150		-200		-250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		200		150		ns
t_{ELWL} (2)	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		65		80		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		65		80		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		0		ns
t_{WHEH} (2)	t_{CH}	Write Enable High to Chip Enable High	0		0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		35		35		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		65		65		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	15		15		15		10		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	2.0	30	1.0	30	sec
t_{WHWL0}		Time Out between 2 consecutive Section Erase		80		80		80		80	µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		0		0		ns
t_{WHRL} (3)	t_{DB}	Write Enable High to Ready/Busy Output Low		150		150		150		150	ns

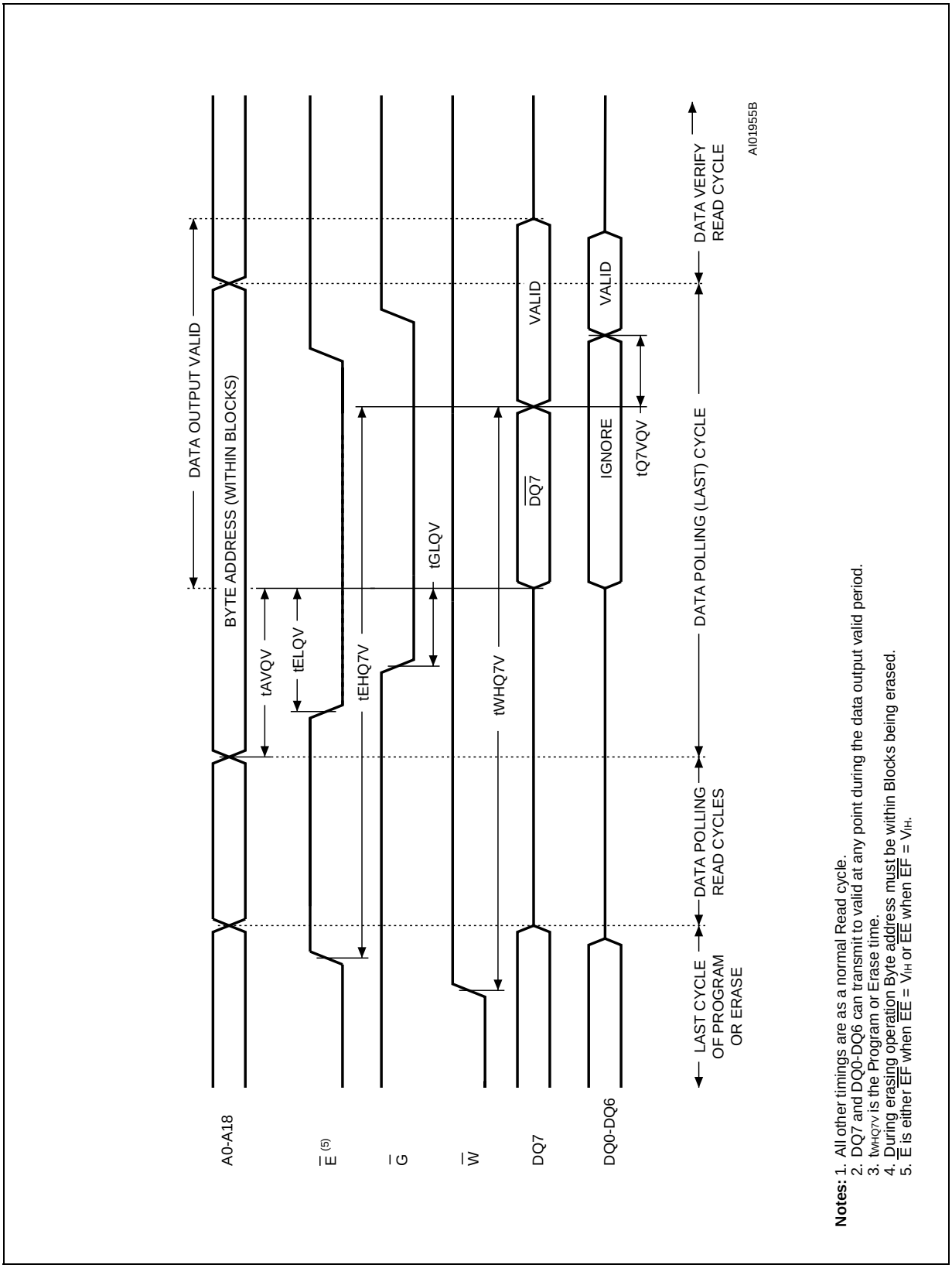
Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. Chip Enable means ($\overline{EE}$, $\overline{EF}$) = (V_{IL}, V_{IH}) or ($\overline{EE}$, $\overline{EF}$) = (V_{IH}, V_{IL}).
3. With a 3.3KΩ pull-up resistor.

Table 15. Write AC Characteristics, $\overline{EE}$ or $\overline{EF}$ Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	M39432								Unit
			-120		-150		-200		-250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{WLWL}	t_{BLC}	Byte Load Cycle (EEPROM)	0.2	150	0.2	150	0.2	150	0.2	150	µs
t_{WHRH}	t_{WC}	Write Cycle Time (EEPROM)		10		10		10		10	ms
t_{AVAV}		Address Valid to Next Address Valid	120		150		200		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Memory Block Enable Low	0		0		0		0		ns
t_{ELEH}	t_{CP}	Memory Block Enable Low to Memory Block Enable High	50		65		80		50		ns
t_{DVEH}	t_{DS}	Input Valid to Memory Block Enable High	50		65		80		50		ns
t_{EHDX}	t_{DH}	Memory Block Enable High to Input Transition	0		0		0		0		ns
t_{EHWH}	t_{WH}	Memory Block Enable High to Write Enable High	0		0		0		0		ns
t_{EHEL}	t_{CPH}	Memory Block Enable High to Memory Block Enable Low	30		35		35		20		ns
t_{AVEL}	t_{AS}	Address Valid to Memory Block Enable Low	0		0		0		0		ns
t_{ELAX}	t_{AH}	Memory Block Enable Low to Address Transition	50		65		65		50		ns
t_{GHEL}		Output Enable High to Memory Block Enable Low	0		0		0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		50		50		µs
t_{EHQV1} (1)		Memory Block Enable High to Output Valid (Program)	15		15		15		10		µs
t_{EHQV2} (1)		Memory Block Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	2.0	30	1.0	30	sec
t_{EHGL}	t_{OEH}	Memory Block Enable High to Output Enable Low	0		0		0		0		ns
t_{EHRL} (2)	t_{DB}	EEPROM Block Enable High to Ready/Busy Output Low		150		150		150		150	ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. With a 3.3KΩ pull-up resistor.

Figure 15. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Blocks being erased.
5. $\overline{E}$ is either $\overline{EF}$ when $\overline{EE} = V_{IH}$ or $\overline{EE}$ when $\overline{EF} = V_{IH}$.

Table 16. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	M39432								Unit
			-120		-150		-200		-250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program, W Controlled)	10		10		10		10		µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Sector Erase, W Controlled)	1.5	30	1.5	30	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Flash Block Enable High to DQ7 Valid (Program, EF Controlled)	10		10		10		10		µs
t_{EHQ7V2} (2)		Flash Block Enable High to DQ7 Valid (Sector Erase, EF Controlled)	1.5	30	1.5	30	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		50		55		70		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)	10		10		10		10		µs
t_{WHQV2}		Write Enable High to Output Valid (Sector Erase)	1.5	30	1.5	30	1.5	30	1.5	30	sec
t_{EHQV1}		Flash Block Enable High to Output Valid (Program)	10		10		10		10		µs
t_{EHQV2}		Flash Block Enable High to Output Valid (Sector Erase)	1.5	30	1.5	30	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Table 17. Program, Erase Times and Program, Erase Endurance Cycles (Flash Block)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Parameter	M39432			Unit
	Min	Typ	Max	
Chip Program (Byte)		8		sec
Chip Erase (Preprogrammed)		3	30	sec
Chip Erase		10		sec
Sector Erase (Preprogrammed)		1	30	sec
Sector Erase		2		sec
Byte Program	10		1200	µs
Program/Erase Cycles (per Sector)	100,000			cycles

Figure 16. Data Toggle DQ6 AC Waveforms

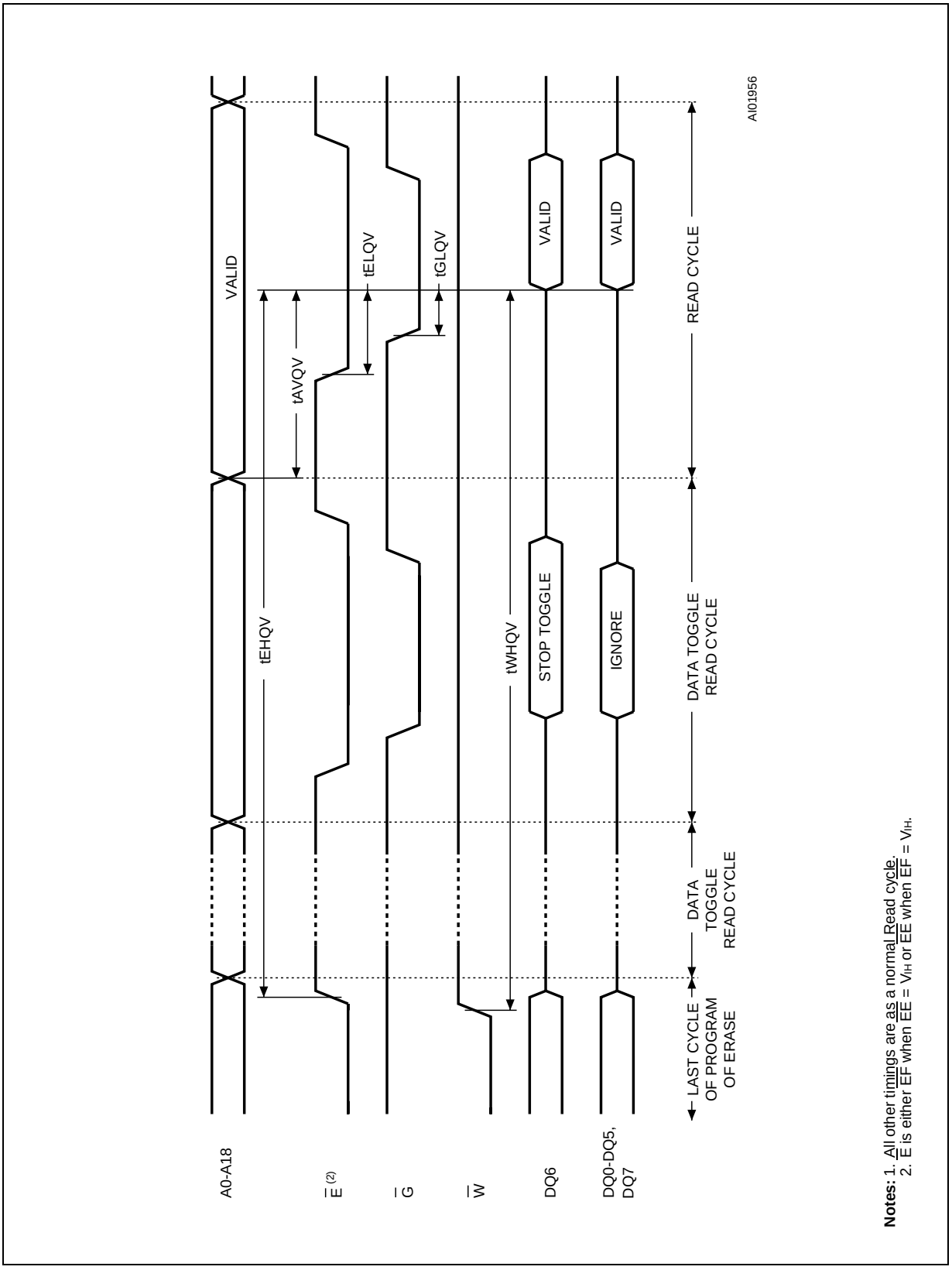
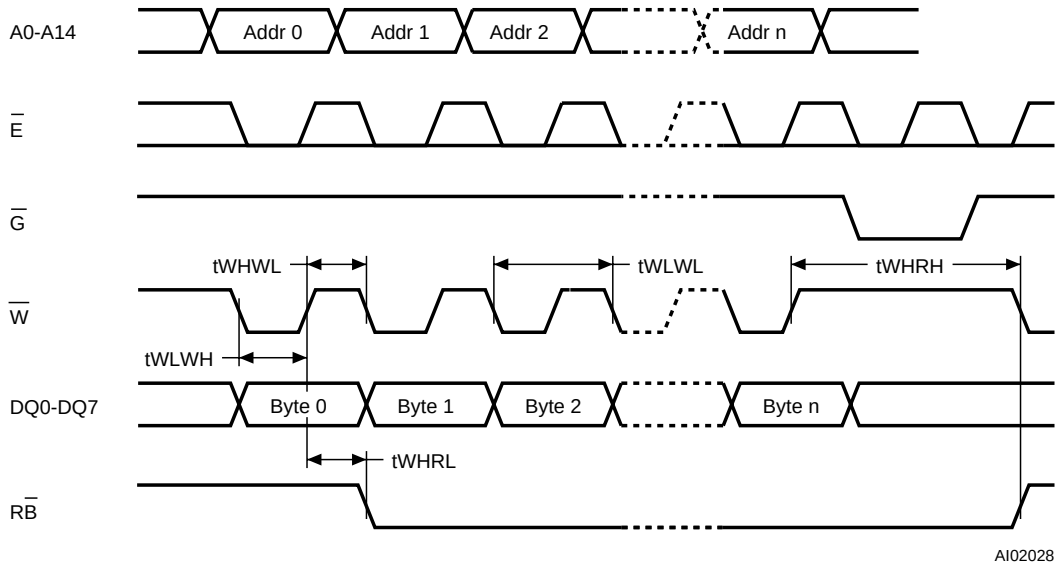
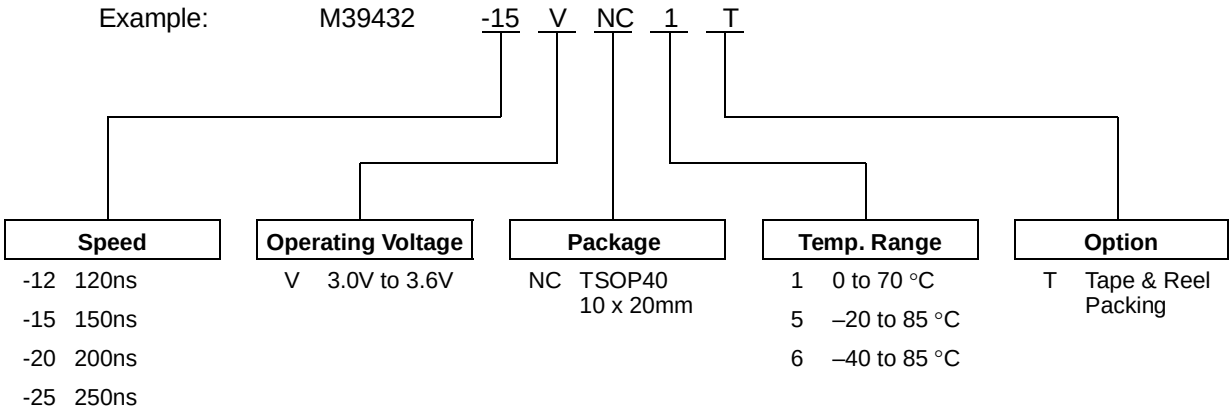


Figure 17. EEPROM Page Write Mode AC Waveforms, $\overline{W}$ Controlled



ORDERING INFORMATION SCHEME

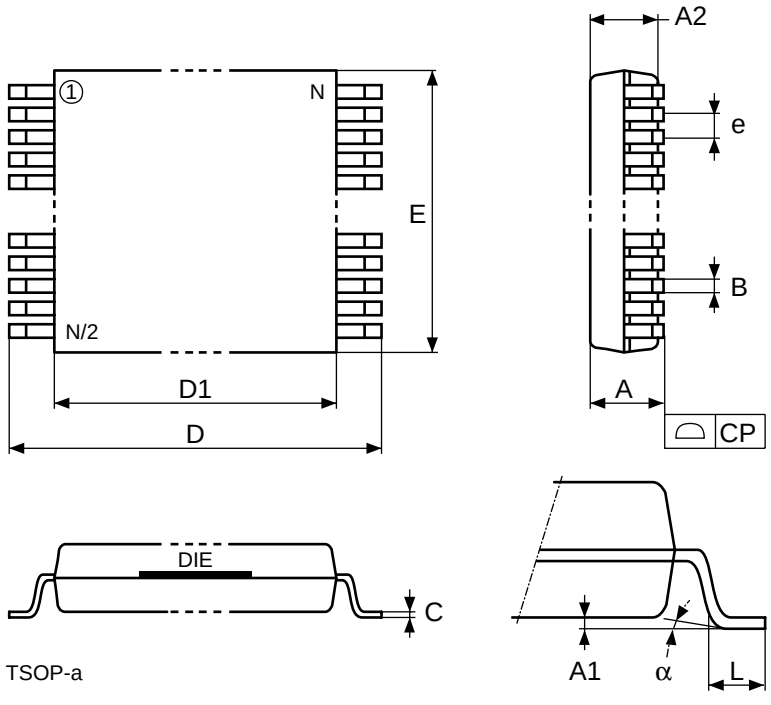


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0	5		0	5
N	40			40		
CP			0.10			0.004



TSOP-a

Drawing is not to scale.