LTC1604

High Speed, 16-Bit, 333ksps Sampling A/D Converter with Shutdown

January 1998

FEATURES

- **A Complete, 333ksps 16-Bit ADC**
- **90dB S/(N+D) and –100dB THD (Typ)**
- **Power Dissipation: 220mW (Typ)**
- No Pipeline Delay
- No Missing Codes over Temperature
- **Nap (7mW) and Sleep (10μW) Shutdown Modes**
- Operates with Internal 15ppm/°C Reference or External Reference
- True Differential Inputs Reject Common Mode Noise
- 5MHz Full Power Bandwidth
- ±2.5V Bipolar Input Range
- 36-Pin SSOP Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

DESCRIPTION

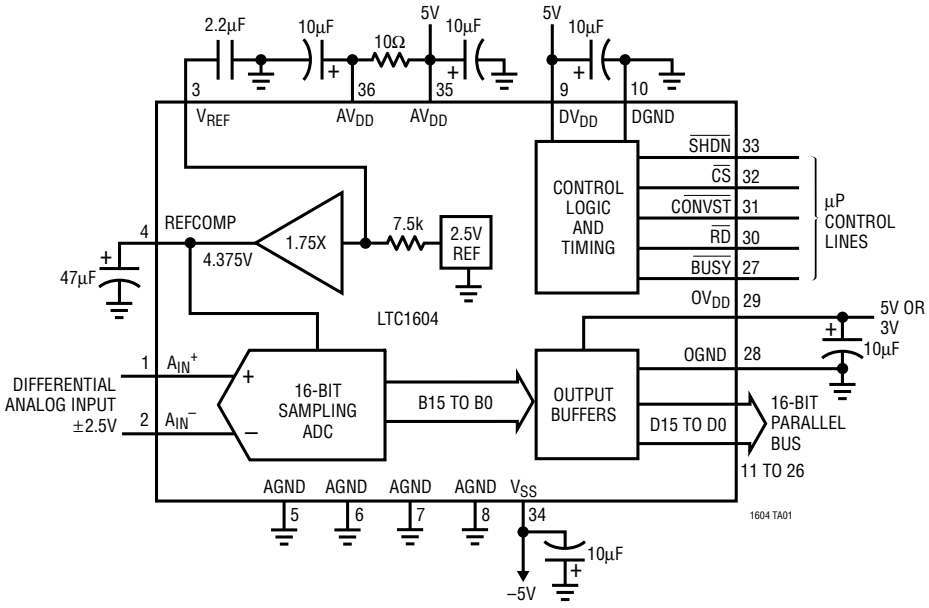
The LTC®1604 is a 333ksps, 16-bit sampling A/D converter that draws only 220mW from ±5V supplies. This high performance device includes a high dynamic range sample-and-hold, a precision reference and a high speed parallel output. Two digitally selectable power shutdown modes provide power savings for low power systems.

The LTC1604's full-scale input range is ±2.5V. Outstanding AC performance includes 90dB S/(N+D) and –100dB THD at a sample rate of 333ksps.

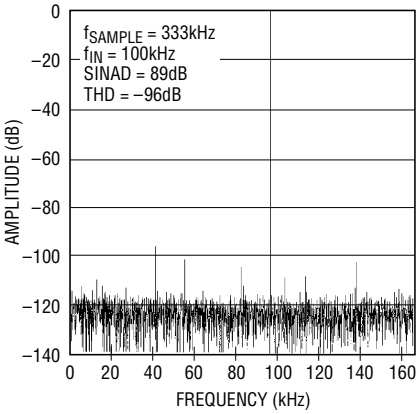
The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 5MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The ADC has μP compatible,16-bit parallel output port. There is no pipeline delay in conversion results. A separate convert start input and a data ready signal (BUSY) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION



LTC1604 4096 Point FFT

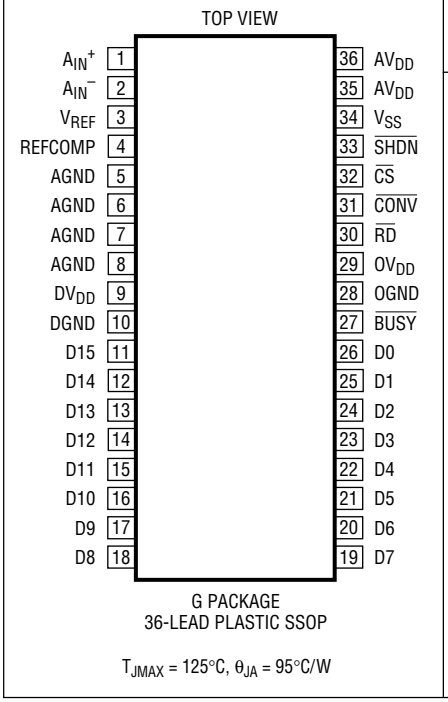


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = DV_{DD} = OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) .....–0.3V to 10V
Digital Output Voltage .....–0.3V to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1604CG

Consult factory for A grade, Industrial and Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	15	16		Bits
Integral Linearity Error	(Note 7)	●		±1	±4	LSB
Offset Error	(Note 8)	●		±0.05	±0.125	%
Full-Scale Error	Internal Reference External Reference			±0.125	±0.25 ±0.25	% %
Full-Scale Tempco	I_{OUT}(Reference) = 0			±10	±45	ppm/°C

ANALOG INPUT

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 2)	4.75 ≤ V_{DD} ≤ 5.25V, –5.25 ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			43 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time				380		ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Acquisition Delay Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (A_{IN}^- = A_{IN}^+) < 2.5V			60		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	5kHz Input Signal 100kHz Input Signal			90 89		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	5kHz Input Signal 100kHz Input Signal			–100 –94		dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal			96		dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			82		dB
	Full Power Bandwidth				5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 84dB				350		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.475	2.500	2.515	V
V_{REF} Output Tempco	I_{OUT} = 0			±15	±45	ppm/°C
V_{REF} Line Regulation	4.75 ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	0 ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			7.5		kΩ
REFCOMP Output Voltage	I_{OUT} = 0			4.375		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_{OUT} = –10µA V_{DD} = 4.75V, I_{OUT} = –400µA	 ●	 4.0	4.5		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_{OUT} = 160µA V_{DD} = 4.75V, I_{OUT} = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D15 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D15 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 10, 11)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current	$\overline{CS}$ = $\overline{RD}$ = 0V	●		18	27	mA
	Nap Mode	$\overline{CS}$ = 0V, $\overline{SHDN}$ = 0V			1.5	2.4	mA
	Sleep Mode	$\overline{CS}$ = 5V, $\overline{SHDN}$ = 0V			1	100	µA
I_{SS}	Negative Supply Current	$\overline{CS}$ = $\overline{RD}$ = 0V	●		26	37	mA
	Nap Mode	$\overline{CS}$ = 0V, $\overline{SHDN}$ = 0V			1	100	µA
	Sleep Mode	$\overline{CS}$ = 5V, $\overline{SHDN}$ = 0V			1	100	µA
P_D	Power Dissipation	$\overline{CS}$ = $\overline{RD}$ = 0V	●		220	320	mW
	Nap Mode	$\overline{CS}$ = 0V, $\overline{SHDN}$ = 0V			7.5	12	mW
	Sleep Mode	$\overline{CS}$ = 5V, $\overline{SHDN}$ = 0V			0.01	1	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	333			kHz
t_{CONV}	Conversion Time		●	1.5	2.45	2.8	µs
t_{ACQ}	Acquisition Time	(Note 9)	●			480	ns
$t_{ACQ+CONV}$	Throughput Time (Acquisition + Conversion)		●			3	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	$\overline{SHDN}\downarrow$ to $\overline{CS}\uparrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	$\overline{CS}$ = Low (Note 10)			400		ns
t_5	$\overline{CONVST}$ Low Time	(Note 10)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			36		ns
			●			80	ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$				60		ns
			●	32			ns
t_8	Delay Between Conversions	(Note 10)	●	200			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	(Note 10)	●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF			40	50	ns
			●			60	ns
		C_L = 100pF			45	60	ns
			●			75	ns
t_{11}	Bus Relinquish Time				50	60	ns
		LTC1604C	●			70	ns
		LTC1604I	●			75	ns
t_{12}	$\overline{RD}$ Low Time	(Note 10)	●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time	(Note 10)	●	40			ns
t_{14}	Aperture Delay of Sample-and-Hold				2		ns

TIMING CHARACTERISTICS (Note 5)

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, OGND and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SMPL} = 333kHz, and $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specification apply for a single-ended A_{IN}^+ input with A_{IN}^- grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a critical point during the conversion it can create small errors. For best performance ensure that $\overline{\text{CONVST}}$ returns high either within 250ns after conversion start or after $\overline{\text{BUSY}}$ rises.

PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input. The ADC converts the difference voltage between A_{IN}^+ and A_{IN}^- with a differential range of ±2.5V. A_{IN}^+ has a ±2.5V input range when A_{IN}^- is grounded.

A_{IN}^- (Pin 2): Negative Analog Input. Can be grounded, tied to a DC voltage or driven differentially with A_{IN}^+.

V_{REF} (Pin 3): 2.5V Reference Output. Bypass to AGND with 2.2µF tantalum in parallel with 0.1µF ceramic.

REFCOMP (Pin 4): 4.375 Reference Compensation Pin. Bypass to AGND with 47µF tantalum in parallel with 0.1µF ceramic.

AGND (Pins 5 to 8): Analog Grounds. Tie to analog ground plane.

DV_{DD} (Pin 9): 5V Digital Power Supply. Bypass to DGND with 10µF tantalum in parallel with 0.1µF ceramic.

DGND (Pin 10): Digital Ground for Internal Logic. Tie to analog ground plane.

D15 to D0 (Pins 11 to 26): Three-State Data Outputs. D15 is the Most Significant Bit.

$\overline{\text{BUSY}}$ (Pin 27): The $\overline{\text{BUSY}}$ output shows the converter status. It is low when a conversion is in progress. Data is valid on the rising edge of $\overline{\text{BUSY}}$.

OGND (Pin 28): Digital Ground for Output Drivers.

OV_{DD} (Pin 29): Digital Power Supply for Output Drivers. Bypass to OGND with 10µF tantalum in parallel with 0.1µF ceramic.

$\overline{\text{RD}}$ (Pin 30): Read Input. A logic low enables the output drivers when $\overline{\text{CS}}$ is low.

$\overline{\text{CONVST}}$ (Pin 31): Conversion Start Signal. This active low signal starts a conversion on its falling edge when $\overline{\text{CS}}$ is low.

$\overline{\text{CS}}$ (Pin 32): The Chip Select Input. Must be low for the ADC to recognize $\overline{\text{CONVST}}$ and $\overline{\text{RD}}$ inputs.

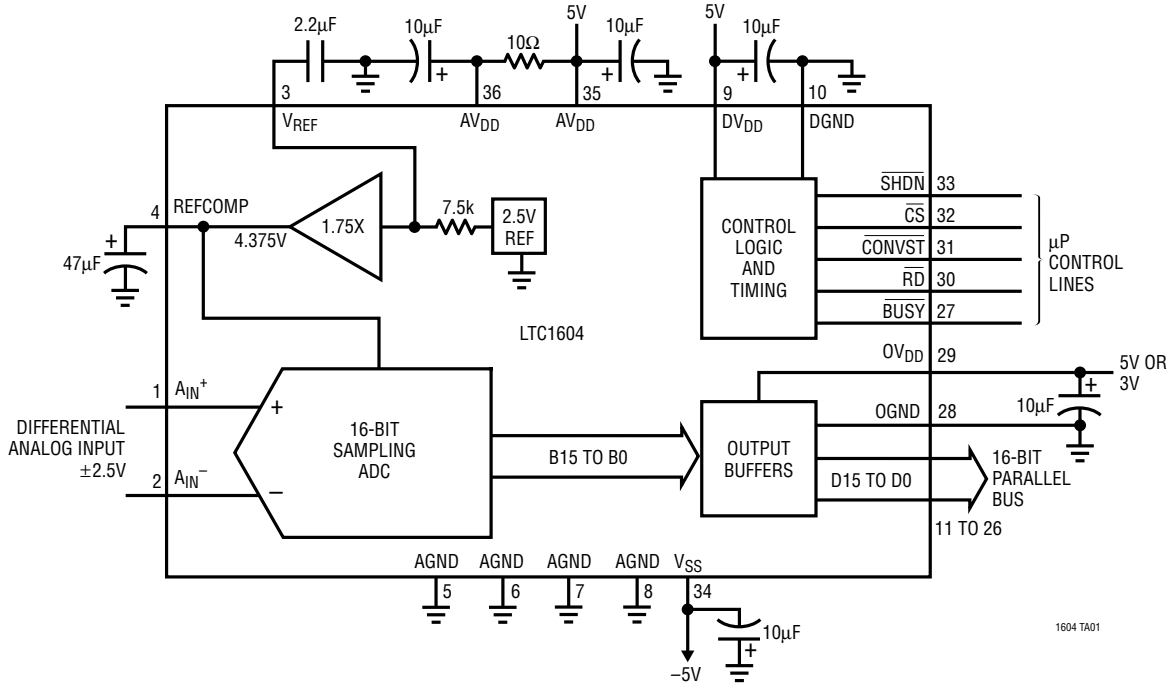
$\overline{\text{SHDN}}$ (Pin 33): Power Shutdown. Drive this pin low with $\overline{\text{CS}}$ low for nap mode. Drive this pin low with $\overline{\text{CS}}$ high for sleep mode.

V_{SS} (Pin 34): –5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

AV_{DD} (Pin 35): 5V Analog Power Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

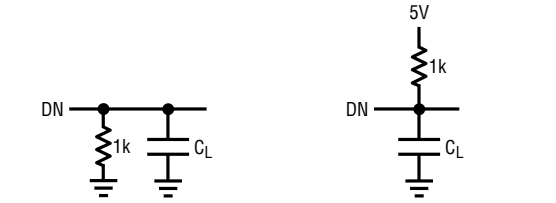
AV_{DD} (Pin 36): 5V Analog Power Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic and connect this pin to Pin 35 with a 10Ω resistor.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

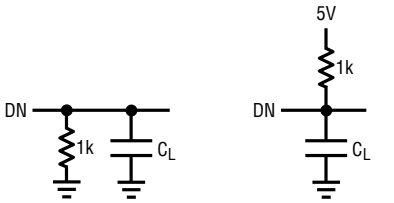
Load Circuits for Access Timing



(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH} (B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

1604 TC01

Load Circuits for Output Float Delay



(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

1604 TC02

APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1604 uses a successive approximation algorithm and internal sample-and-hold circuit to convert an analog signal to a 16-bit parallel output. The ADC is complete with a sample-and-hold, a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion the successive approximation register (SAR) resets. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 16-bit capacitive DAC output is sequenced by the SAR from the Most Significant Bit (MSB) to the Least Significant Bit (LSB). Referring to Figure 1, the A_{IN}^+ and A_{IN}^- inputs are acquired during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a duration of 480ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches connect the C_{SMPL} capacitors to ground, transferring the differential analog input charge onto the summing junctions. This input charge is successively compared with the binarily weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the A_{IN}^+ and A_{IN}^- input charges. The SAR contents (a 16-bit data word) which represent the difference of A_{IN}^+ and A_{IN}^- are loaded into the 16-bit output latches.

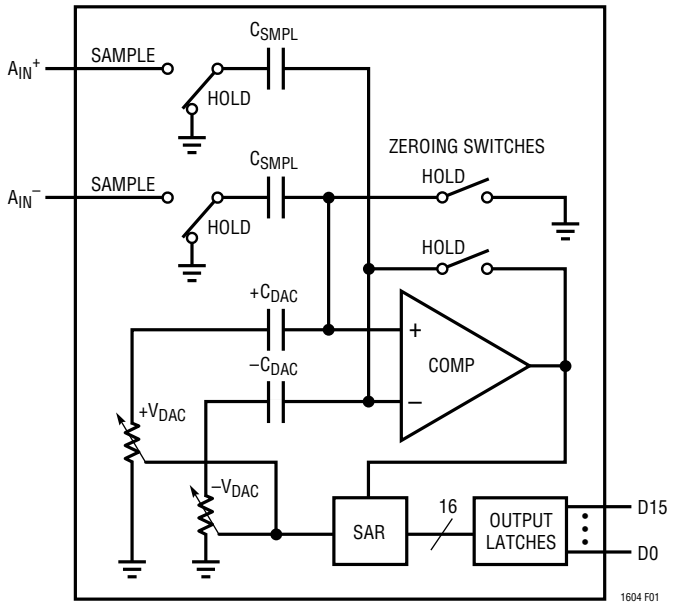


Figure 1. Simplified Block Diagram

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that runs the A/D conversion. The internal clock is factory trimmed to achieve a typical conversion time of 2.45µs and a maximum conversion time of 2.8µs over the full temperature range. No external adjustments are required. The guaranteed maximum acquisition time is 480ns. In addition, a throughput time (acquisition + conversion) of 3µs and a minimum sampling rate of 333ksps are guaranteed.

APPLICATIONS INFORMATION

Power Shutdown

The LTC1604 provides two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from Nap to active is 200ns. In Sleep mode all bias currents are shut down and only leakage current remains m (about 1µA). Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 160ms with the recommended 47µF capacitor.

Shutdown is controlled by Pin 33 ($\overline{SHDN}$). The ADC is in shutdown when $\overline{SHDN}$ is low. The shutdown mode is selected with Pin 32 ($\overline{CS}$). When $\overline{SHDN}$ is low, $\overline{CS}$ low selects nap and $\overline{CS}$ high selects sleep.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. A falling edge applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

We recommend using a narrow logic low or narrow logic high $\overline{CONVST}$ pulse to start a conversion as shown in Figures 5 and 6. A narrow low or high $\overline{CONVST}$ pulse prevents the rising edge of the $\overline{CONVST}$ pulse from upsetting the critical bit decisions during the conversion time. Figure 4 shows the change of the differential nonlinearity error versus the low time of the $\overline{CONVST}$ pulse. As shown, if $\overline{CONVST}$ returns high early in the conversion (e.g., $\overline{CONVST}$ low time <500ns), accuracy is unaffected. Similarly, if $\overline{CONVST}$ returns high after the conversion is over (e.g., $\overline{CONVST}$ low time >t_{CONV}), accuracy is unaffected. For best results, keep t_5 less than 500ns or greater than t_{CONV}.

Figures 5 through 9 show several different modes of operation. In modes 1a and 1b (Figures 5 and 6), $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the

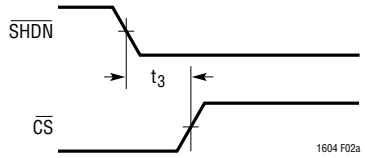


Figure 2a. Nap Mode to Sleep Mode Timing

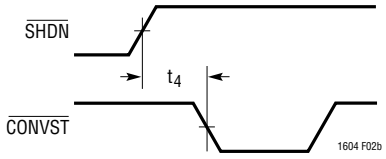


Figure 2b. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

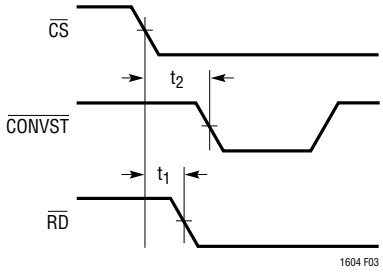


Figure 3. $\overline{CS}$ top $\overline{CONVST}$ Setup Timing

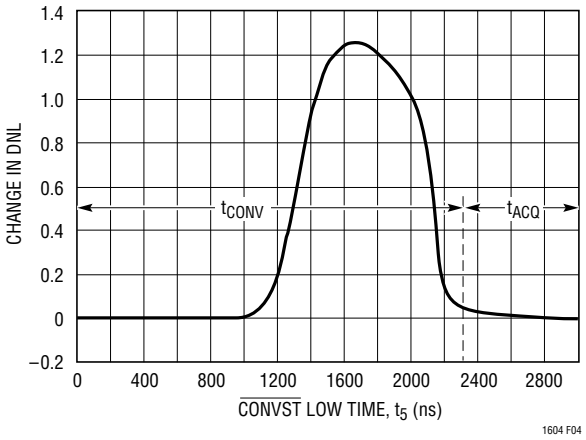


Figure 4. Change in DNL vs $\overline{CONVST}$ Low Time. Be Sure the $\overline{CONVST}$ Pulse Returns High Early in the Conversion or After the End of Conversion

APPLICATIONS INFORMATION

conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 7) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared data bus.

In slow memory and ROM modes (Figures 8 and 9) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the combined $\overline{CONVST}$-$\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock is needed).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high, releasing the processor and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

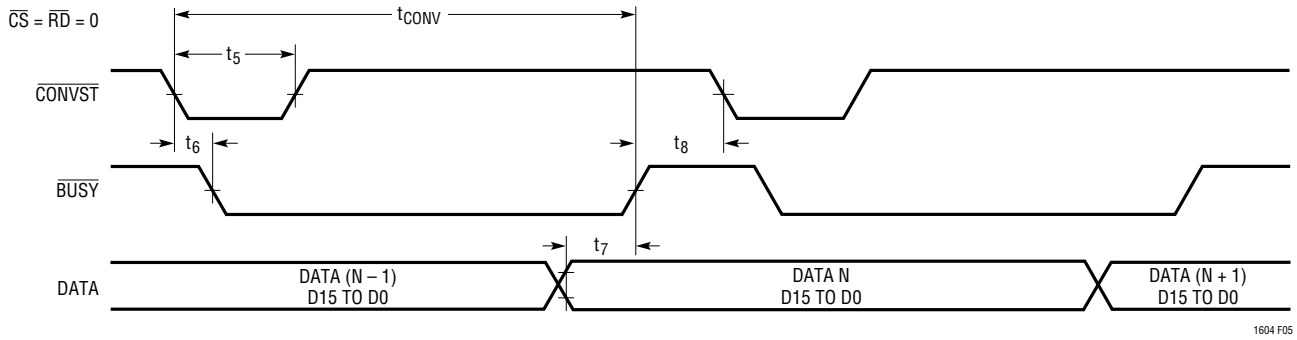


Figure 5. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⎍⎍⎍)

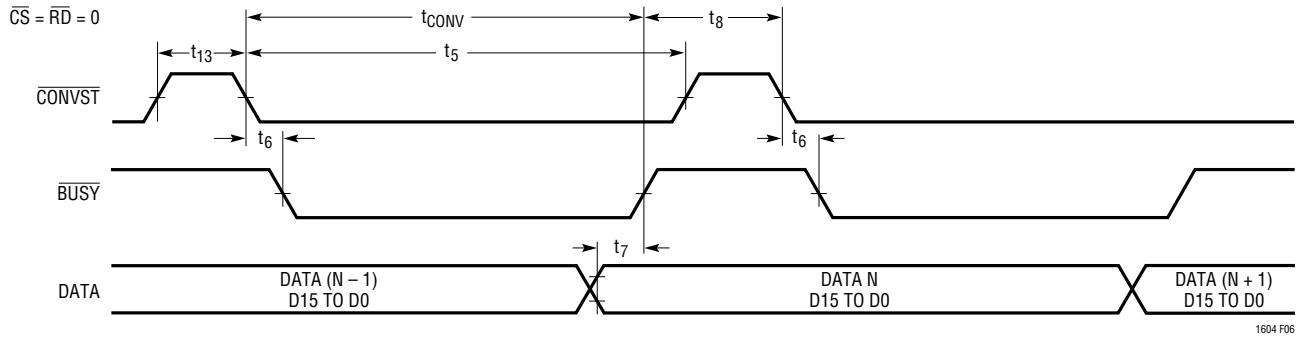


Figure 6. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⎍⎍⎍)

APPLICATIONS INFORMATION

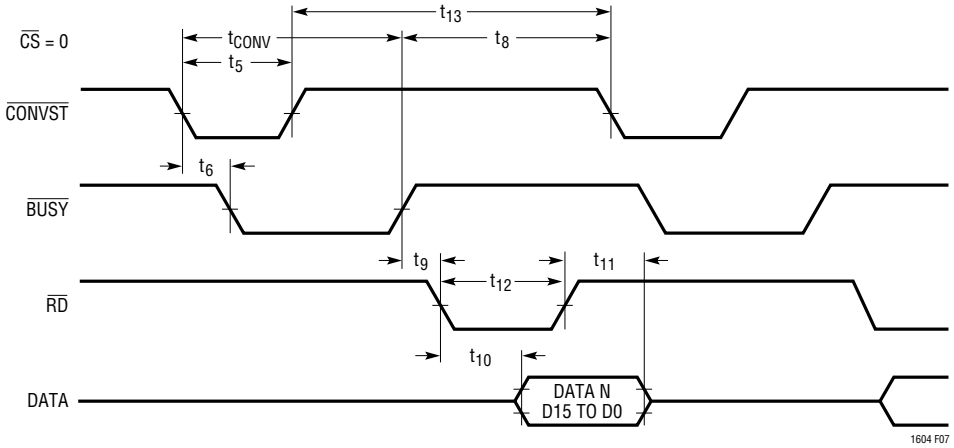


Figure 7. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

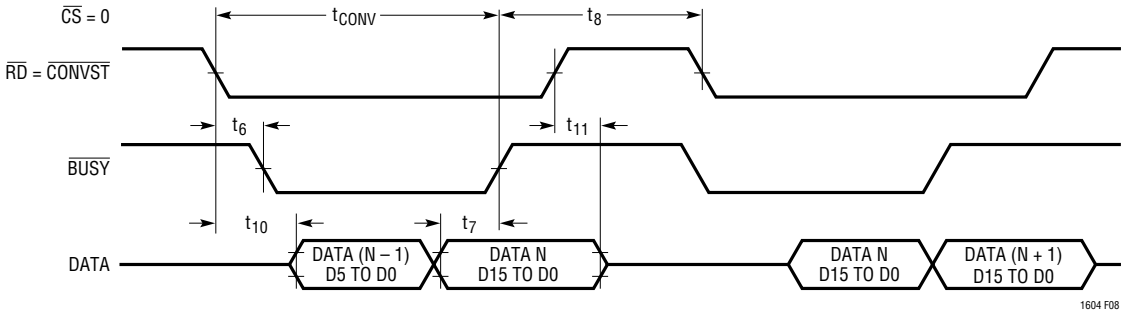


Figure 8. Mode 2. Slow Memory Mode Timing

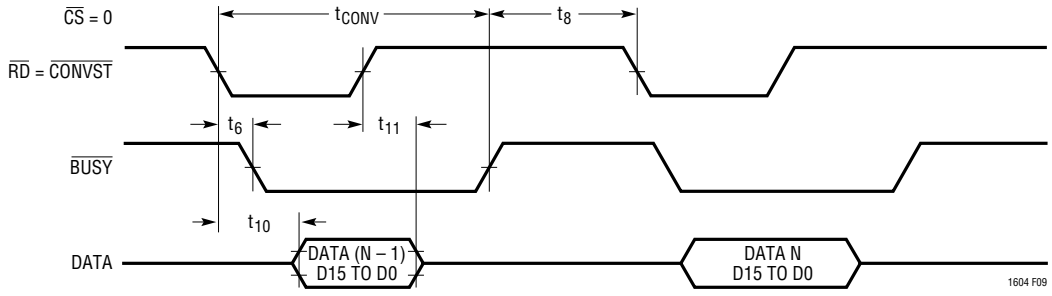
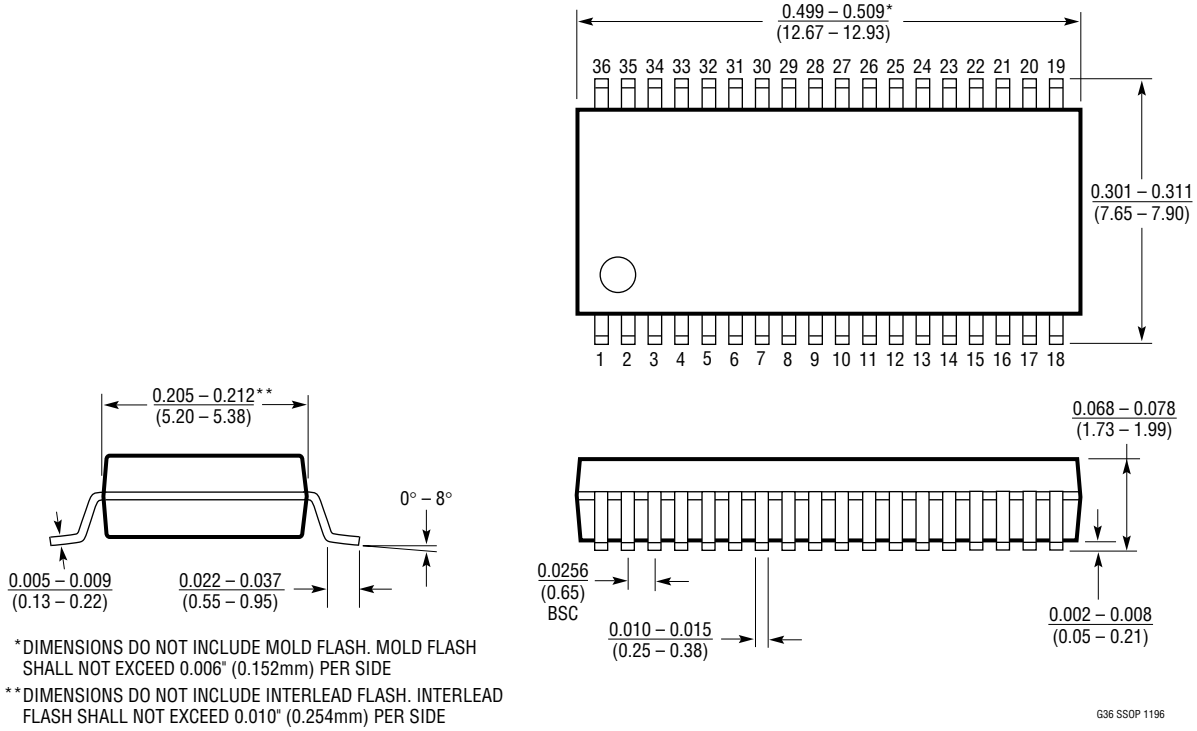


Figure 9. ROM Mode Timing

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
36-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

SAMPLING ADCs

PART NUMBER	DESCRIPTION	COMMENTS
LTC1410	12-Bit, 1.25Msps, ±5V ADC	71.5dB SINAD at Nyquist, 150mW Dissipation
LTC1415	12-Bit, 1.25Msps, Single 5V ADC	55mW Power Dissipation, 72dB SINAD
LTC1419	Low Power 14-Bit, 800ksps ADC	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation
LTC1605	16-Bit, 100ksps, Single 5V ADC	±10V Inputs, 55mW, Byte or Parallel I/O

DACs

PART NUMBER	DESCRIPTION	COMMENTS
LTC1595	16-Bit Multiplying I_{OUT} DAC in SO-8	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1596	16-Bit Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, AD7543/DAC8143 16-Bit Upgrade

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417• (408)432-1900
FAX: (408) 434-0507•TELEX: 499-3977 • www.linear-tech.com
1604i LT/TP 0198 4K • PRINTED IN USA