LTC1414

14-Bit, 2.2Msps, Sampling A/D Converter

August 1998

FEATURES

- **Sample Rate: 2.2Msps**
- **80dB S/(N + D) and 95dB SFDR at 100kHz**
- **78dB S/(N + D) and 86dB SFDR at Nyquist**
- Power Dissipation: 175mW on ±5V Supplies
- External or Internal Reference Operation
- No Pipeline Delay
- True Differential Inputs Reject Common Mode Noise
- ±2.5V Bipolar Input Range
- 40MHz Full Power Bandwidth Sampling
- 28-Pin Narrow SSOP Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

DESCRIPTION

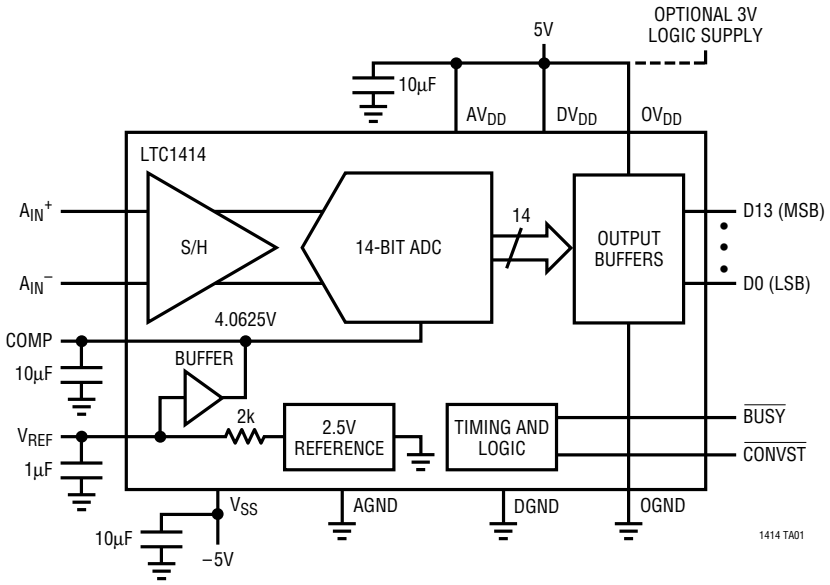
The LTC®1414 is a 14-bit, 2.2Msps, sampling A/D converter which draws only 175mW from ±5V supplies. This high performance ADC includes a high dynamic range sample-and-hold, a precision reference and requires no external components.

The LTC1414's high performance sample-and-hold has a full-scale input range of ±2.5V. Outstanding AC performance includes 80dB S/(N + D) and 95dB SFDR with a 100kHz input. The performance remains high at the Nyquist input frequency of 1.1MHz with 78dB S/(N + D) and 86dB SFDR.

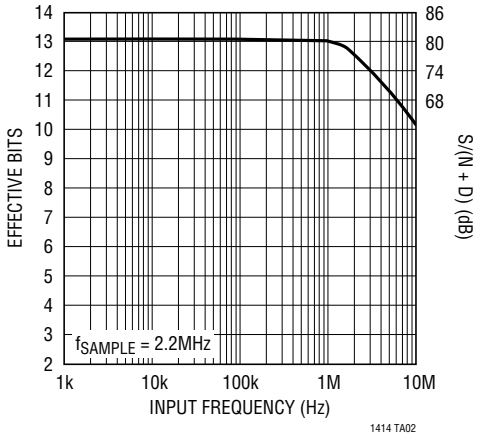
The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 40MHz bandwidth. The 70dB common mode rejection can eliminate ground loops and common mode noise by measuring signal differentially from the source

The ADC has a microprocessor compatible, 14-bit parallel output port. There is no pipline delay in the conversion results.

TYPICAL APPLICATION



Effective Bits and Signal-to-Noise + Distortion vs Input Frequency

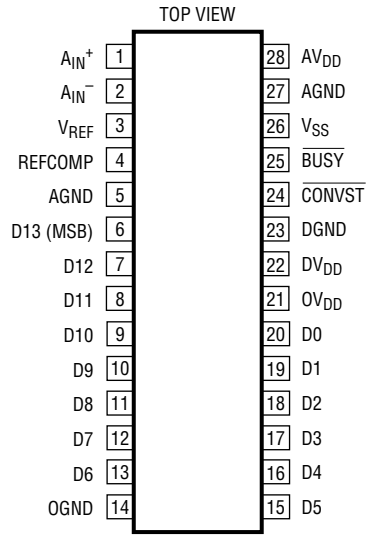


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = OV_{DD} = DV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) ..... (V_{SS} – 0.3V) to 10V
Digital Output Voltage ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 110°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1414CGN

Consult factory for Industrial, Military and A grade parts.

CONVERTER CHARACTERISTICS

With internal reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1414 MIN	LTC1414 TYP	LTC1414 MAX	UNITS
Resolution (No Missing Codes)		●	13			Bits
Integral Linearity Error	(Note 7)	●		±0.75	±2.0	LSB
Differential Linearity Error		●		±0.75	±1.75	LSB
Offset Error	(Note 8)	 ●		±5	±20 ±24	LSB LSB
Full-Scale Error	Internal Reference External Reference = 2.5V			±10 ±5	±60 ±25	LSB LSB
Full-Scale Tempco	Internal Reference External Reference = 2.5V			±15 ±1		ppm/°C ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current		●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			8 4		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		40	100	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–1		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				3		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (A_{IN}^- = A_{IN}^+) < 2.5V			70		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 1.1MHz Input Signal			80 78		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics 1.1MHz Input Signal, First 5 Harmonics			–95 –84		dB dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal 1.1MHz Input Signal, First 5 Harmonics			95 86		dB dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–86		dB
	Full Power Bandwidth				40		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 74dB			1.8		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	$\lvert I_{OUT} \rvert$ ≤ 0.1mA			2		kΩ
COMP Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				1.2		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA V_{DD} = 4.75V, I_O = –200µA	 ●	 4.0	4.74		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA V_{DD} = 4.75V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D13 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D13 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 10)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current	$\overline{CS}$ High	●		12	16	mA
I_{SS}	Negative Supply Current	$\overline{CS}$ High	●		23	30	mA
P_D	Power Dissipation				175	230	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	2.2			MHz
t_{CONV}	Conversion Time		●	220	330	400	ns
t_{ACQ}	Acquisition Time		●		40	100	ns
$t_{THROUGHPUT}$	Throughput Time (Acquisition + Conversion)		●		370	454	ns
t_1	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			10		ns
t_2	Data Ready Before $\overline{BUSY}\uparrow$				±20		ns
t_3	Delay Between Conversions	(Note 10)	●	100			ns
t_4	$\overline{CONVST}$ Low Time	(Note 11)	●	40			ns
t_5	$\overline{CONVST}$ High Time	(Note 11)	●	40			ns
t_6	Aperture Delay of Sample-and-Hold				–1		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SAMPLE} = 2.2MHz and $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN}^+ input with A_{IN}^- grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

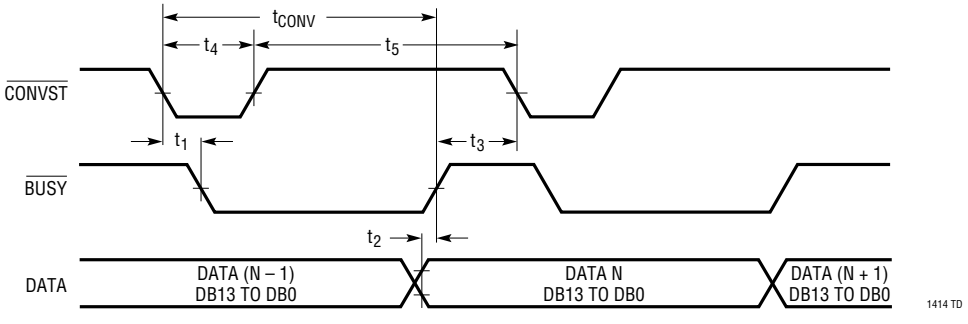
Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that $\overline{CONVST}$ returns high either within 225ns after the start of the conversion or after $\overline{BUSY}$ rises.

TIMING DIAGRAM



PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input. ±2.5V input range when A_{IN}^- is grounded. ±2.5V differential if A_{IN}^- is driven differentially with A_{IN}^+.

A_{IN}^- (Pin 2): Negative Analog Input. Can be grounded or driven differentially with A_{IN}^+.

V_{REF} (Pin 3): 2.5V Reference Output.

REFCOMP (Pin 4): 4.06V Reference Bypass Pin. Bypass to AGND with 10µF ceramic or 10µF tantalum in parallel with 0.1µF ceramic.

AGND (Pin 5): Analog Ground.

D13 to D6 (Pins 6 to 13): Data Outputs.

OGND (Pin 14): Digital Ground for the Output Drivers. Tie to AGND

D5 to D0 (Pins 15 to 20): Data Outputs.

OV_{DD} (Pin 21): Positive Supply for the Output Drivers. Tie to Pin 28 when driving 5V logic. For 3V logic, tie to supply of the logic being driven.

DV_{DD} (Pin 22): 5V Positive Supply. Tie to Pin 28.

DGND (Pin 23): Digital Ground. Tie to AGND.

$\overline{\text{CONVST}}$ (Pin 24): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

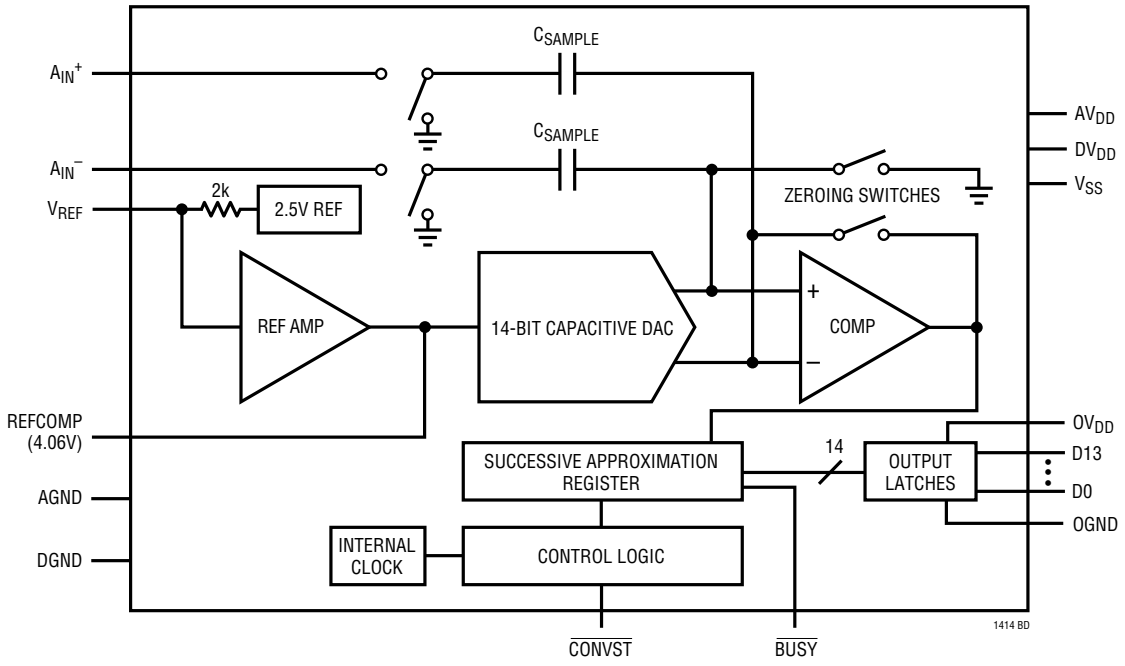
$\overline{\text{BUSY}}$ (Pin 25): The $\overline{\text{BUSY}}$ Output Shows the Converter Status. It is low when a conversion is in progress.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND with 10µF ceramic or 10µF tantalum in parallel with 0.1µF ceramic.

AGND (Pin 27): Analog Ground.

AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF ceramic or 10µF tantalum in parallel with 0.1µF ceramic.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

Driving the Analog Input

The differential analog inputs of the LTC1414 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1414 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 1). For minimum acquisition time, with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 80ns for full throughput rate).

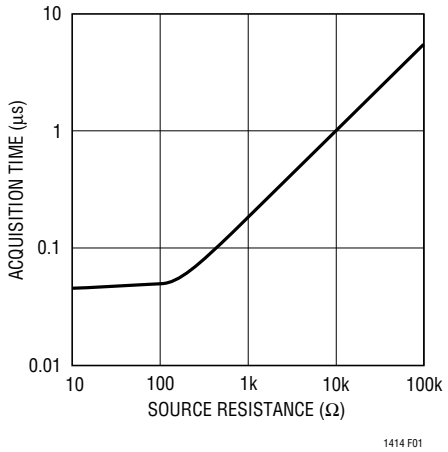


Figure 1. Acquisition Time vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1414 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1414. More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.

LT®1223: 100MHz Video Current Feedback Amplifier. 6mA supply current. ±5V to ±15V supplies. Low noise. Good for AC applications.

LT1227: 140MHz Video Current Feedback Amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise. Best for AC applications.

LT1229/LT1230: Dual and Quad 100MHz Current Feedback Amplifiers. ±2V to ±15V supplies. Low noise. Good AC specifications, 6mA supply current each amplifier.

LT1360: 50MHz Voltage Feedback Amplifier. 3.8mA supply current. Good AC and DC specs. ±5V to ±15V supplies. 70ns settling to 0.5LSB.

LT1363: 70MHz, 1000V/µs Op Amps. 6.3mA supply current. Good AC and DC specifications. 60ns settling to 0.5LSB.

LT1364/LT1365: Dual and Quad 70MHz, 1000V/µs Op Amps. 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1414 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 40MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input

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circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

For example, Figure 2 shows a 500pF capacitor from A_{IN}^+ to ground and a 100Ω source resistor to limit the input bandwidth to 3.2MHz. The 500pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch-sensitive circuitry. High quality capacitors and resistors should be used since poor quality components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Range

The ±2.5V input range of the LTC1414 is optimized for low noise and low distortion. Most op amps also perform best over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1414 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The LTC1414 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3), see Figure 3. A 2k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry. The reference amplifier multiplies the voltage at the V_{REF} pin by 1.625 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin, REFCOMP (Pin 4) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or 10µF tantalum in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means shown in Figure 4. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1414 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed after a reference adjustment.

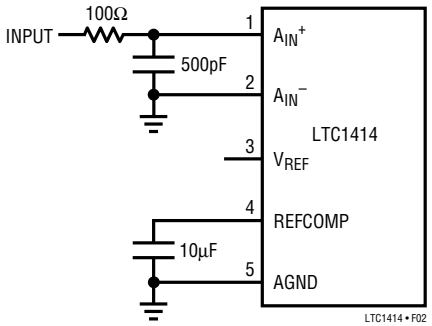

Figure 2. An RC Filter Reduces the ADC's 40MHz Bandwidth to 3.2MHz and Filters Out Wideband Noise Which May Be Present in the Input Signal

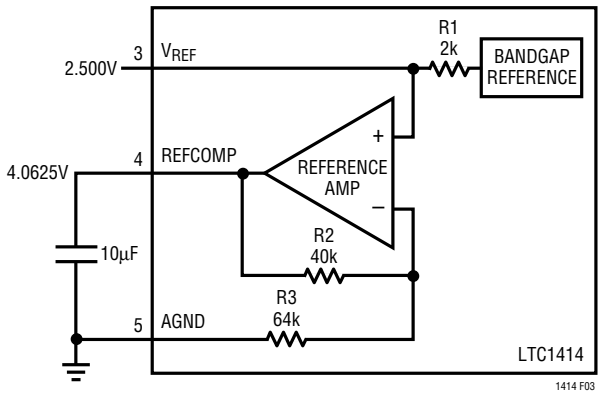

Figure 3. LTC1414 Reference Circuit

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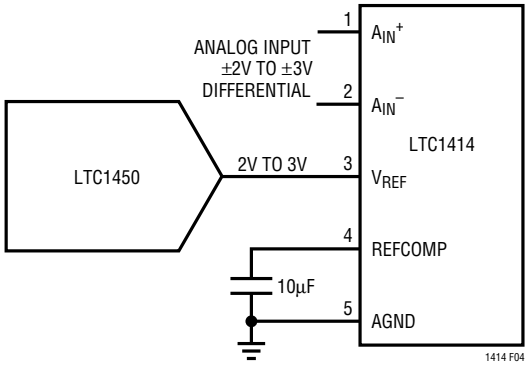

Figure 4. Driving V_{REF} with a DAC

Differential Inputs

The LTC1414 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $A_{IN}^+ - (A_{IN}^-)$ independent of the common mode voltage. The common mode rejection holds up to extremely high frequencies, see Figure 5. The only requirement is that neither input can exceed the AV_{DD} or AV_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common mode voltage. THD will degrade as the inputs approach either power supply rail, from –86dB with a common mode of 0V to –75dB with a common mode of 2.5V or –2.5V.

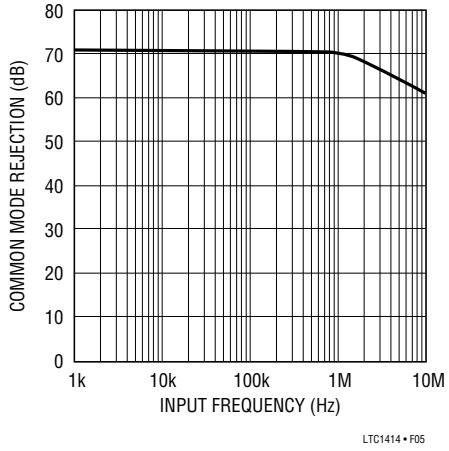

Figure 5. CMRR vs Input Frequency

Full-Scale and Offset Adjustment

Figure 6 shows the ideal input/output characteristics for the LTC1414. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB,...FS – 2.5LSB, FS – 1.5LSB). The output is two's complement binary with 1LSB = FS – (–FS)/16384 = 5V/16384 = 305.2µV.

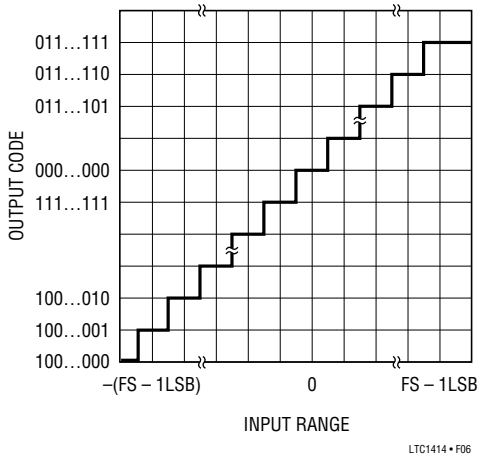

Figure 6. LTC1414 Transfer Characteristics

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 7 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply –152µV (i.e., –0.5LSB) at A_{IN}^+ and adjust the offset at the A_{IN}^- input until the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 2.499544V (FS – 1.5LSBs) is applied to A_{IN}^+ and R2 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.

Board Layout and Bypassing

To obtain the best performance from the LTC1414, a printed circuit board with a ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as

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possible. In particular, care should be taken not to run any digital line alongside an analog signal line or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD}, V_{SS} and V_{REF} pins. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1414 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- inputs will be reflected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1414 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 1) and A_{IN}^- (Pin 2) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at AGND (Pin 5, 27) or as close as possible to the ADC (see Figure 8). The ADC's DGND (Pin 23) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and these traces should be as wide as possible. Excessive capacitive loading on the ADC's data output lines can generate large transient currents on the ADC supplies which may affect conversion results. In these cases, the use of digital buffers is recommended to isolate the ADC from the excessive loading.

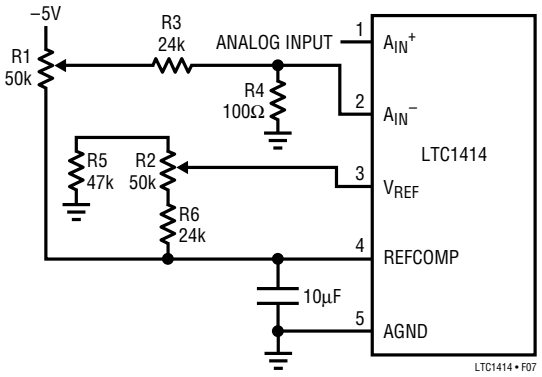

Figure 7. Offset and Full-Scale Adjust Circuit

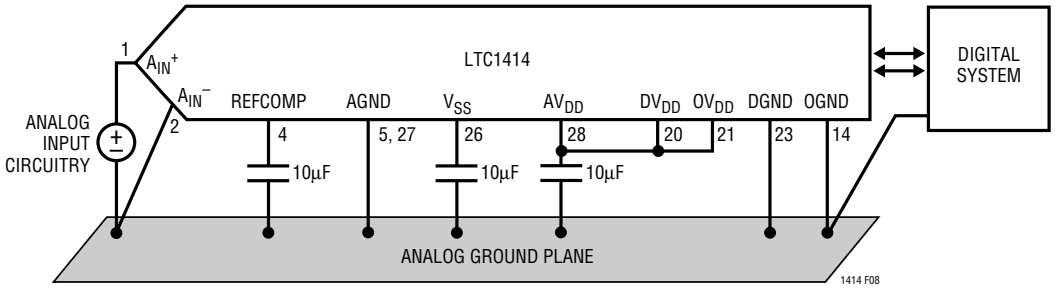

Figure 8. Power Supply Grounding Practice

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Digital Interface

The A/D converter has just one control input $\overline{\text{CONVST}}$. Data is output on 14-bit parallel bus. An additional output $\overline{\text{BUSY}}$ indicates the converter status.

Internal Clock

The internal clock is factory trimmed to achieve a typical conversion time of 330ns and a maximum conversion time over the full operating temperature range of 400ns. No external adjustments are required. The guaranteed maximum acquisition time is 100ns. In addition, a throughput time (acquisition + conversion) of 454ns and a minimum sampling rate of 2.2Msps is guaranteed.

Timing and Control

The conversion start is controlled by the $\overline{\text{CONVST}}$ input. The falling edge of $\overline{\text{CONVST}}$ will start a conversion. Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{\text{BUSY}}$ output. $\overline{\text{BUSY}}$ is low during a conversion.

The output data is updated at the end of the conversion as $\overline{\text{BUSY}}$ rises. Output data is updated coincident with the rising edge of $\overline{\text{BUSY}}$. Data will be valid, and can be latched, 20ns after the rising edge of $\overline{\text{BUSY}}$. Valid data can also be latched with the falling edge of $\overline{\text{BUSY}}$ or with the rising edge of $\overline{\text{CONVST}}$. In the latter two cases the data latched will be for the previous conversion.

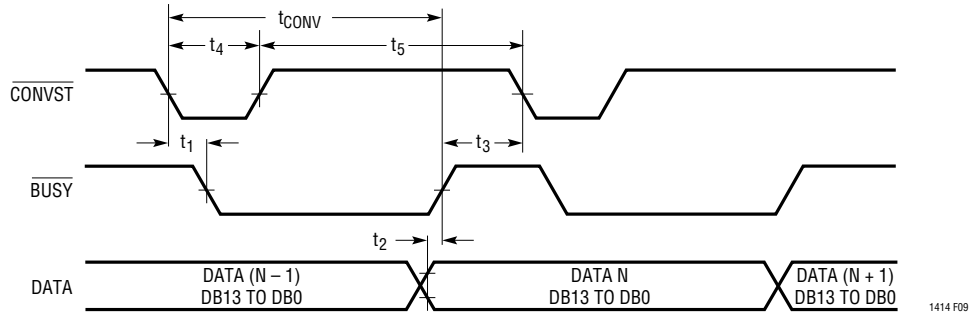
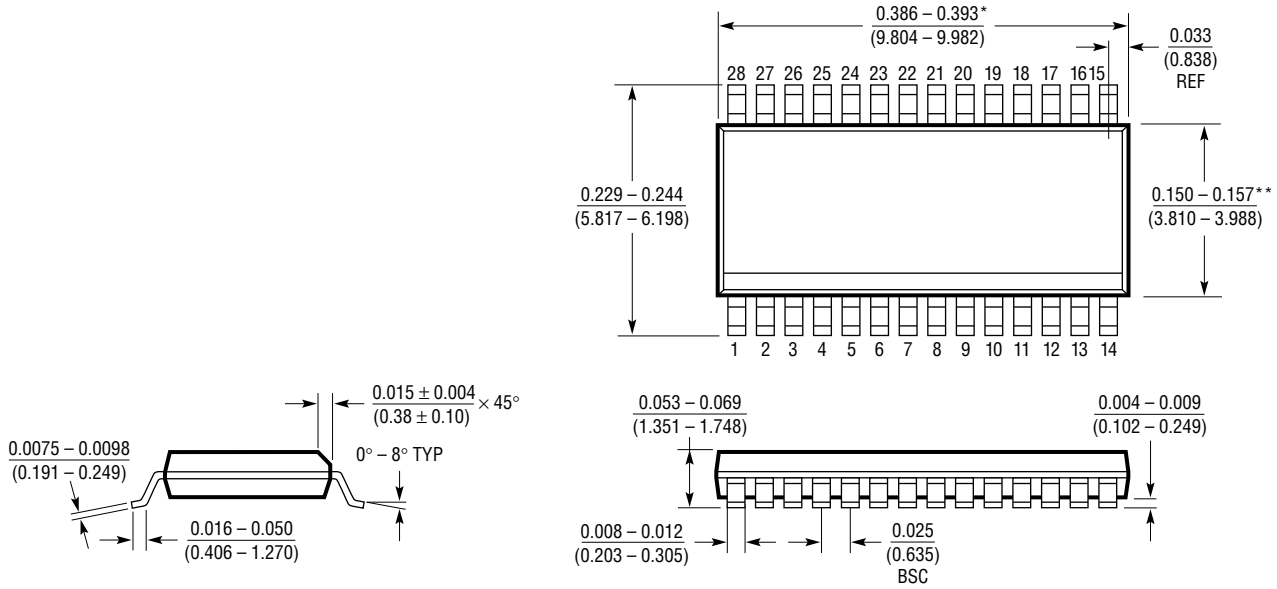


Figure 9. Timing Diagram

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
28-Lead Plastic SSOP Narrow (0.150)
(LTC DWG # 05-08-1641)



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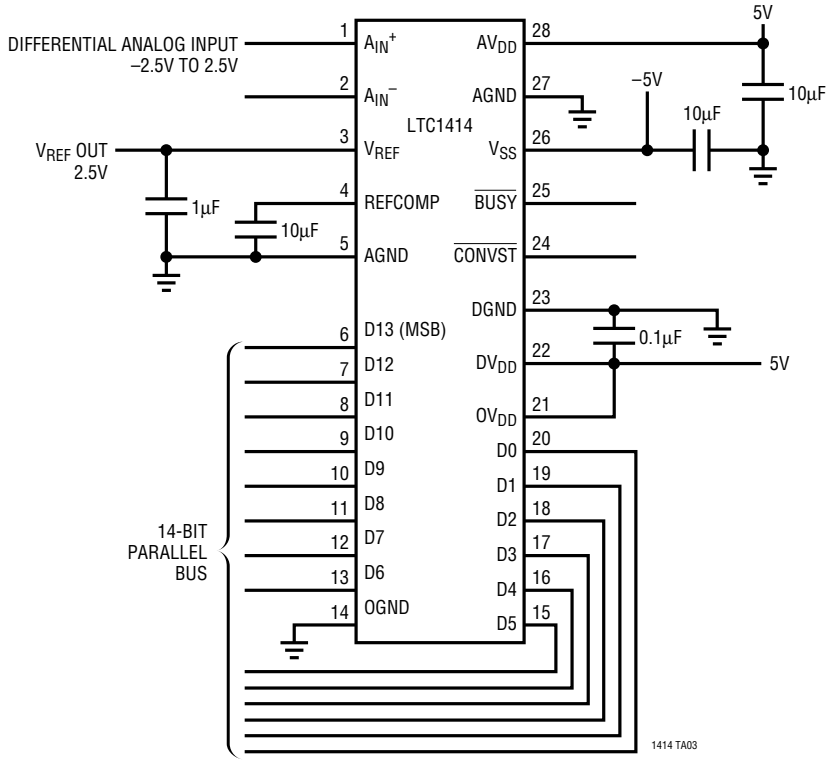
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

2.2MHz, 14-Bit Sampling ADC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1412	Low Power, 12-Bit 3Msps ADC	Nyquist Sampling, 150mW, 72dB SINAD
LTC1415	Single 5V, 12-Bit 1.25Msps ADC	Single Supply, 55mW Dissipation
LTC1416	Low Power, 14-Bit 400ksps ADC	±5V Supplies, 75mW Dissipation
LTC1418	Very Low Power 14-Bit, 200ksps ADC	15mW, 5V Supply, Serial or Parallel I/O
LTC1419	Low Power 14-Bit, 800ksps ADC	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation

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