GENERAL DESCRIPTION

The part is a high performance BICMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 67 to 212 Mbps.

Functional blocks include a serial port, an automatic gain control amplifier, a programmable filter, an offset canceller, a peak detecting pulse qualifier, an adaptive transversal filter, a Viterbi qualifier, a 8/9 GCR ENDEC, a data synchronizer, a time base generator, an integrating servo demodulator, as shown in figure 1.

The part requires a single +5V power supply. The part utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which results in a high performance device with low power consumption.

FEATURES

GENERAL

- Register programmable data rates from 67 to 212 Mbit/s
- Sampled data read channel with Viterbi qualification
- Programmable filter for PR4 equalization
- Five tap transversal filter with adaptive PR4 equalization
- 8/9 GCR ENDEC
- Data Scrambler / Descrambler
- Presettable Precoder state
- Programmable write precompensation
- Low operating power - 1000mW maximum at 5.5V to allow use of TOFP packages. Active power management is applied to achieve this target
- Register programmable power management (<5 mW power down mode)
- 4-bit nibble and byte wide bi-directional NRZ data interface
- 8 bit direct write mode automatically configured for CLK=VCO/8
- Serial Interface port for access to internal program storage registers
- Single power supply (5V ± 10%)
- Small package footprint: 100 lead TOFP

AUTOMATIC GAIN CONTROL

- Dual mode AGC, continuous time during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery in continuous time mode
- Programmable, symmetric, charge pump currents for data reads in sampled mode
- Charge pump currents track programmable data rate during data reads
- Low drift AGC hold circuitry
- Low-Z circuitry at AGC input provides for rapid external coupling capacitor recovery
- AGC Amplifier squelch during Low-Z
- Wide bandwidth amplitude feedback circuit to allow improved stability of AGC level vs. frequency
- Programmable AGC controls
  - Separate external input pins for AGC hold, fast recovery, and Low-Z control or
  - Internal Low-Z and fast recovery timing for rapid transient recovery and AGC acquisition. Timing set with external resistors (2). Ultra fast decay current set with external resistor.

FILTER / EQUALIZER

- Programmable, 7-pole, continuous time filter with asymmetrical zeros
- Channel filter and pulse slimming equalization for coarse equalization to PR4
- Programmable cutoff frequency from 10 to 56 MHz
- Programmable boost/equalization of 0 to 13 dB
- Programmable “zeros” equalization provides asymmetry compensation
- ±30% group delay variation from 0.3Fc to Fc with Fc=56 MHz
- Low-Z switch for fast offset recovery at the filter output
- No external coupling capacitors required
- DC offset compensation provided at the filter output
- Three or Five tap transversal filter for fine equalization to PR4.
- Self adapting symmetric Inner taps
- Programmable symmetric outer taps with 4 bits of resolution
    - Equalization hold input
    - Asymmetry factor output and “zeros” channel quality output

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register programmable hysteresis or window qualification peak detector for servo reads, with programmable thresholds
- Selectable RDS pulse width for servo grey code reads
- RDS and PPOL outputs are disabled during burst capture to reduce noise generation

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 225 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and *8/9* GCR ENDEC
- Register programmable to 212 Mbps
- Fast Acquisition, sampled data phase locked loop
- Decision directed clock recovery from data samples
- Adaptive clock recovery thresholds
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler / descrambler to reduce fixed pattern effects
- Byte wide NRZ data interface and 4 bits nibble interface
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Surface defect scan mode
- Direct Write modes

SERVO

- 6-burst servo capture with A-B, C-D, E-F outputs
- Internal hold capacitors
- Separate, automatically selected, registers for servo fc, boost, and threshold
- Wide bandwidth, high precision full-wave rectifier is optimized for low-level linearity
- “Soft Landing” charge pump architecture
- Programmable selection of normal or differentiated filter output to servo-capture block
- Programmable gain with 2 external inputs

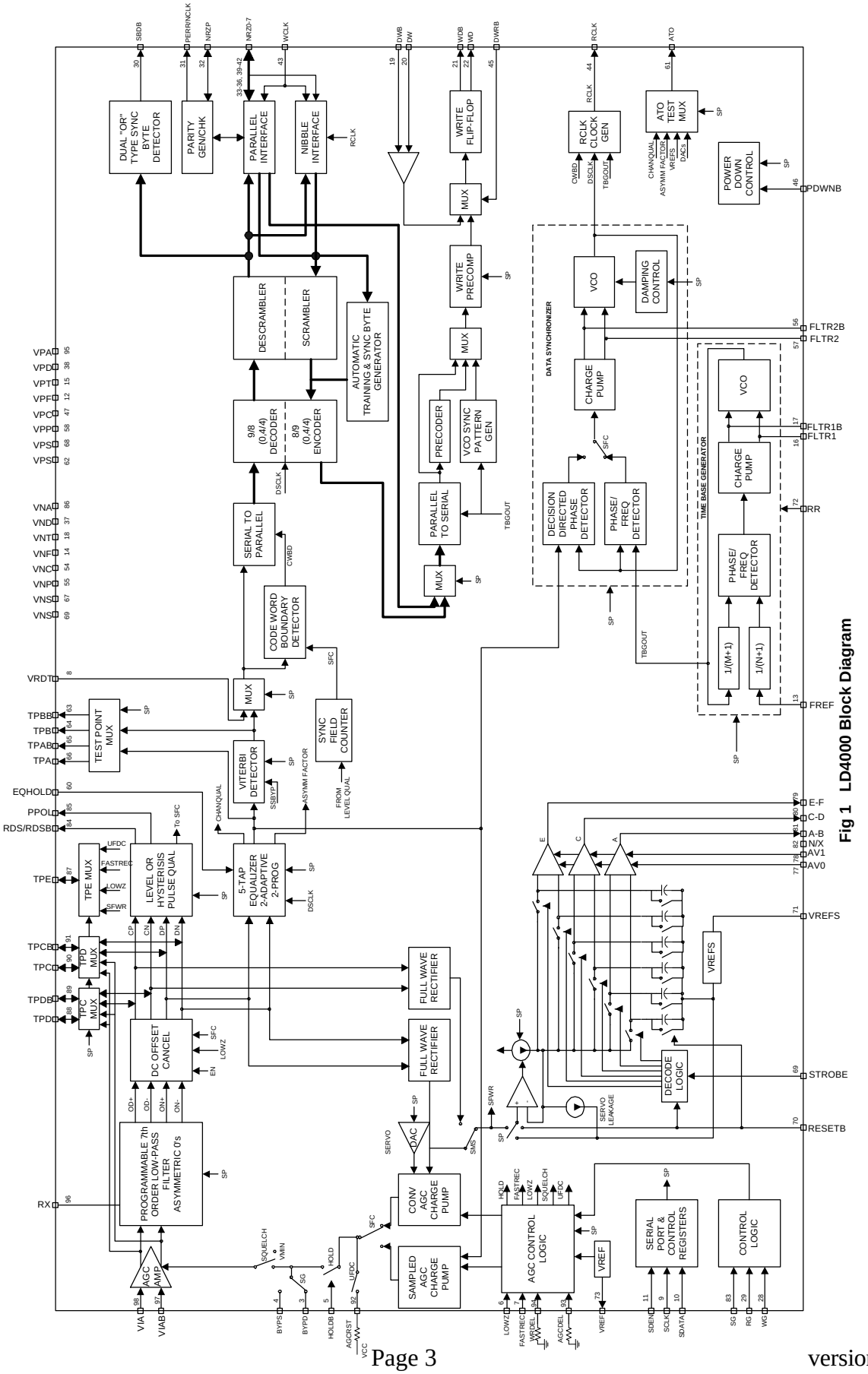
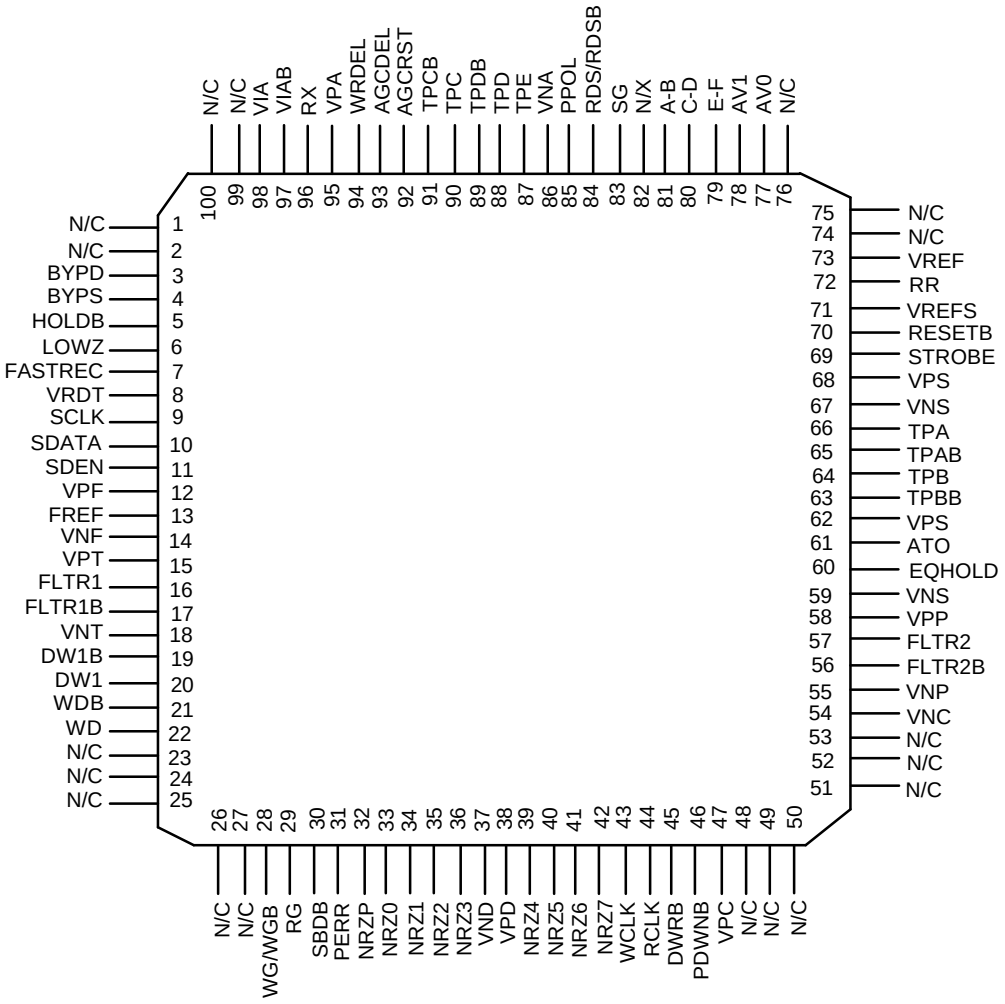


Fig 1 LD4000 Block Diagram



LD4000
100-Lead TQFP