

LA5317M

Variable Divided Voltage Generator for LCD Use

Overview

The LA5317M is a variable divided voltage generator IC for multiple drive of LCD matrix.

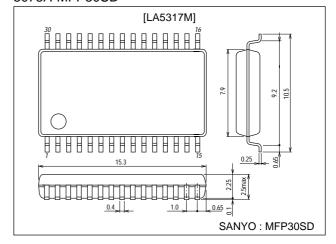
Features

- Power supply for variable bias LCD drive (1/5 to 1/20 bias available by on-chip resistances).
- 5 operational amplifiers to deliver 5 voltage outputs.
- Low current drain (1.6mA typ).
- Miniflat package.

Package Dimensions

unit:mm

3073A-MFP30SD



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{EE} max	VCC-VEE	-38 to 0	V
Maximum output current	I _{OUT} max	V ₁ to V ₅	*±25	mA
Allowable power dissipation	Pd max		800	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-30 to +125	°C

Note 1) Continuous operation (nonbreakdown) is guaranteed when operated at the maximum ratings shown above.

Note 2)* The maximum output current is a value specified under the conditions otherwise specified separately.

Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VEE	VCC-VEE	−35 to −10	V
Output current	I _{OUT1}	V ₁	-0.5 to +10	mA
	I _{OUT2, 3}	V_2, V_3	-10 to +10	mA
	I _{OUT4, 5}	V_4, V_5	-15 to +0.5	mA

Note 3) Set V_{CC} , V_{EE} so that $|V_1|$, $|V_5-V_4|$ become 1V or greater.

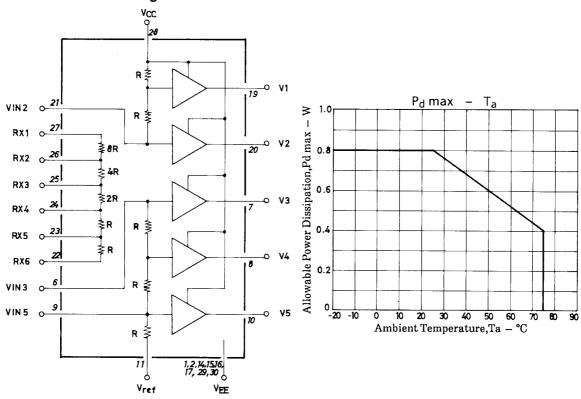
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Operating Characteristics at Ta = 25 $^{\circ}$ C, V $_{CC}$ –V $_{EE}$ =20 V, V $_{REF}$ =V $_{EE}$, R $_{X}$ =8 R

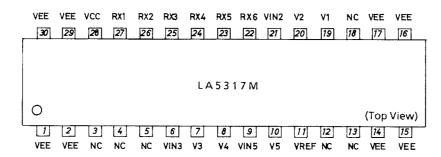
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	Onit
Current drain	ICC, IEE	V _{CC} , V _{EE} : V _{CC} =V _{EE} =20V, R _X =8R		1.6	3	mA
Output voltage ratio 1	Ra1	V ₂ /V ₁	1.96	2.00	2.04	
Output voltage ratio 2	Ra2	(V ₅ -V ₃)/(V ₅ -V ₄)	1.96	2.00	2.04	
Output voltage ratio 3	Rb1	V ₅ /V ₁	11.64	12.00	12.36	
Output voltage ratio 4	Rb2	V ₅ /V ₂	5.82	6.00	6.18	
Output voltage ratio 5	Rb3	V ₅ /(V ₅ -V ₃)	5.82	6.00	6.18	
Output voltage ratio 6	Rb4	V ₅ /(V ₅ -V ₄)	11.64	12.00	12.36	
Internal resistance ratio 1	8R	$R_X^{1-R}_{X^2}$, Resistance ratio referenced to R across R_X^{5} and R_X^{6}		8		
Internal resistance ratio 2	12R	R_X 1- R_X 3, Resistance ratio referenced to R across R_X 5 and R_X 6		12		
Internal resistance ratio 3	14R	$R_X^{1-}R_X^{4}$, Resistance ratio referenced to R across R_X^{5} and R_X^{6}		14		
Internal resistance ratio 4	15R	R_{χ}^{1-R} , Resistance ratio referenced to R across R_{χ}^{5} and R_{χ}^{6}		15		
Internal resistance ratio 5	16R	R_{X} 1- R_{X} 6, Resistance ratio referenced to R across R_{X} 5 and R_{X} 6		16		
Resistance	R	R value when 0.5V is applied across R χ 5 and R χ 6		20		kΩ
Load regulation 1	ΔV1	V ₁ : -0.2mA <i<sub>OUT1<+10.0mA</i<sub>			±20	mV
Load regulation 2	ΔV ₂	V ₂ : -0.2mA <i<sub>OUT2<+10.0mA</i<sub>			±20	mV
Load regulation 3	ΔV ₃	V ₃ : -0.2mA <i<sub>OUT3<+10.0mA</i<sub>			±20	mV
Load regulation –2	<i>-</i> ΔV ₂	V ₂ : -10.0mA <i<sub>OUT2<+0.2mA</i<sub>			±20	mV
Load regulation –3	-ΔV ₃	V ₃ : -10.0mA <i<sub>OUT3<+0.2mA</i<sub>			±20	mV
Load regulation -4	-ΔV ₄	V ₄ : -10.0mA <i<sub>OUT4<+0.2mA</i<sub>			±20	mV
Load regulation –5	-ΔV ₅	V ₅ : -10.0mA <i<sub>OUT5<+0.2mA</i<sub>			±20	mV

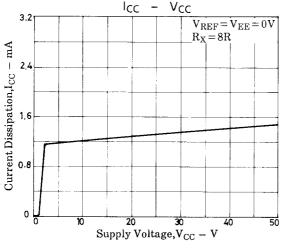
Equivalent Circuit Block Diagram

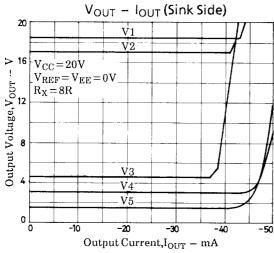


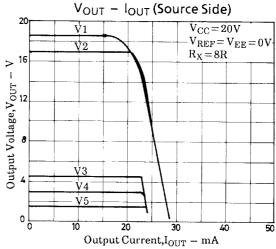
Note : Use the IC so that $V_{RX1} \!\!\ge\!\! V_{RX2} \!\!\ge\!\! V_{RX3} \!\!\ge\!\! V_{RX4} \!\!\ge\!\! V_{RX5} \!\!\ge\!\! V_{RX6}$ is obtained.

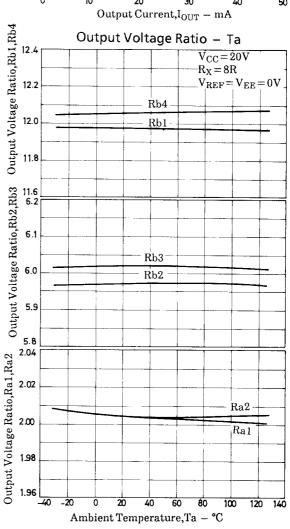
Pin Assingment











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