

COS/MOS
INTEGRATED
CIRCUITS

S G S-THOMSON 07C D
7929237 0014964 7

T-45-23-09



41C 08978 D

7929225 S G S SEMICONDUCTOR CORP

PRESETTABLE UP/DOWN COUNTERS

- MEDIUM SPEED OPERATION $f_{CL} = 8$ MHz TYP. AT 10V
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- RESET AND PRESET CAPABILITY
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4510B**, **HCC 4516B** (extended temperature range) and the **HCF 4510B**, **HCF 4516B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4510B** Presettable BCD Up/Down Counter and the **HCC/HCF 4516B** Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the **RESET** line, and can be preset to any binary number present on the jam inputs by a high level on the **PRESET ENABLE** line. The **HCC/HCF 4510B** will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the **CARRY-IN** input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the **CARRY-OUT** of a less significant stage to the **CARRY-IN** of a more significant stage. The **HCC/HCF 4510B** and **HCC/HCF 4516B** can be cascaded in the ripple mode by connecting the **CARRY-OUT** to the clock of the next stage. If the **UP/DOWN** input changes during a terminal count, the **CARRY-OUT** must be gated with the clock, and the **UP/DOWN** input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20	V
		-0.5 to 18	V
V_I	Input voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for $T_{op} =$ full package-temperature range	100	mW
T_{op}	Operating temperature: HCC types HCF types	-55 to 125	°C
		-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

- HCC 45XX BD for dual in-line ceramic package
- HCC 45XX BF for dual in-line ceramic package, frit seal
- HCC 45XX BK for ceramic flat package
- HCF 45XX BE for dual in-line plastic package
- HCF 45XX BF for dual in-line ceramic package, frit seal

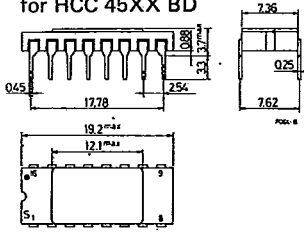


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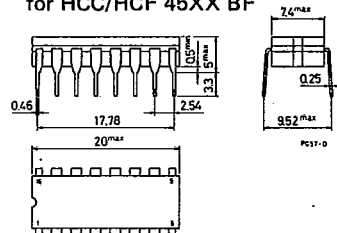
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MECHANICAL DATA (dimensions in mm)

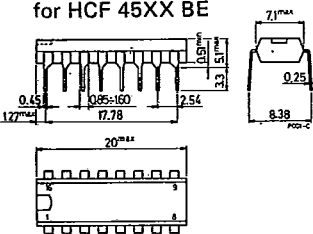
Dual in-line ceramic package for HCC 45XX BD



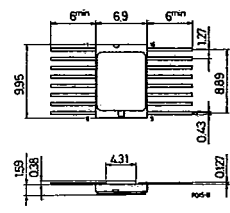
Dual in-line ceramic package for HCC/HCF 45XX BF



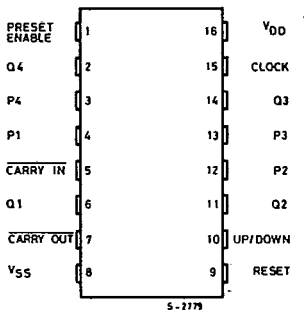
Dual in-line plastic package for HCF 45XX BE



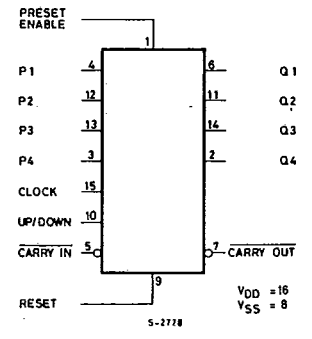
Ceramic flat package for HCC 45XX BK



CONNECTION DIAGRAMS



FUNCTIONAL DIAGRAM



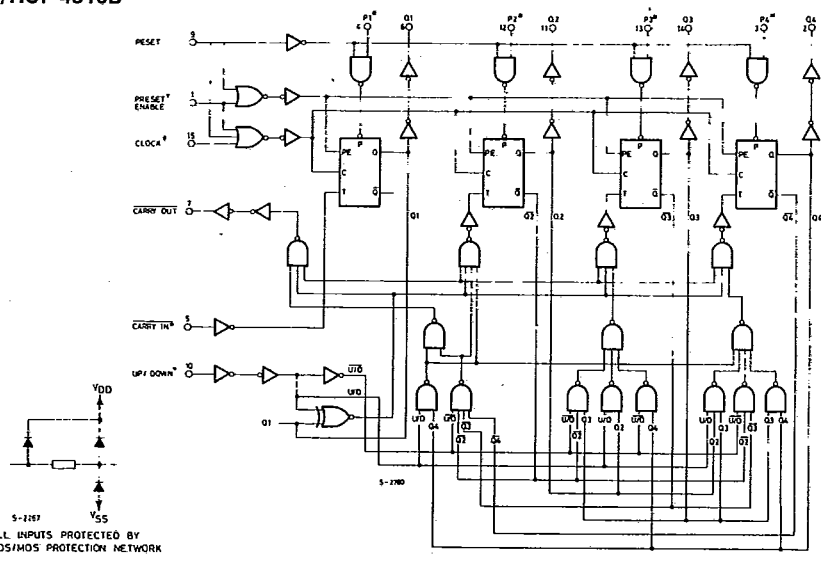
RECOMMENDED OPERATING CONDITIONS

V _{DD}	Supply voltage: HCC types	3 to 18	V
	HCF types	3 to 15	V
V _I	Input voltage	0 to V _{DD}	V
T _{op}	Operating temperature: HCC types	-55 to 125	°C
	HCF types	-40 to 85	°C



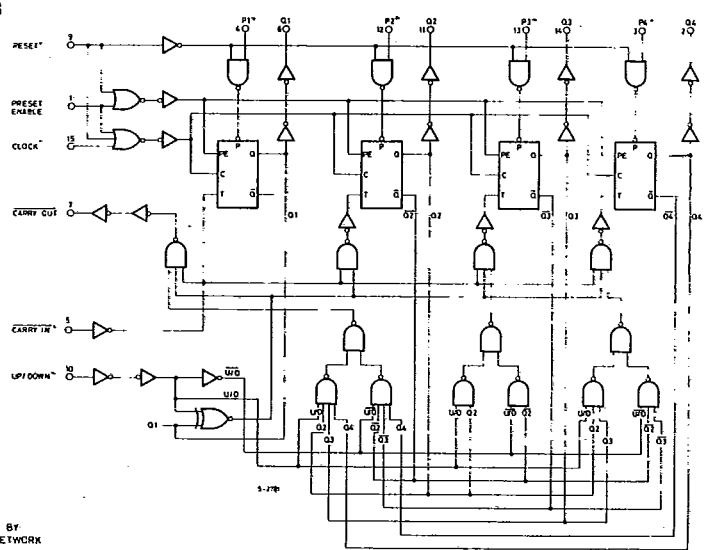
41C 08980 D

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LOGIC DIAGRAMS
for HCC/HCF 4510B



VDD
VSS
5-2187
ALL INPUTS PROTECTED BY
COS/MOS PROTECTION NETWORK

for HCC/HCF 4516B



VDD
VSS
5-2187
ALL INPUTS PROTECTED BY
COS/MOS PROTECTION NETWORK

T-45-23-09

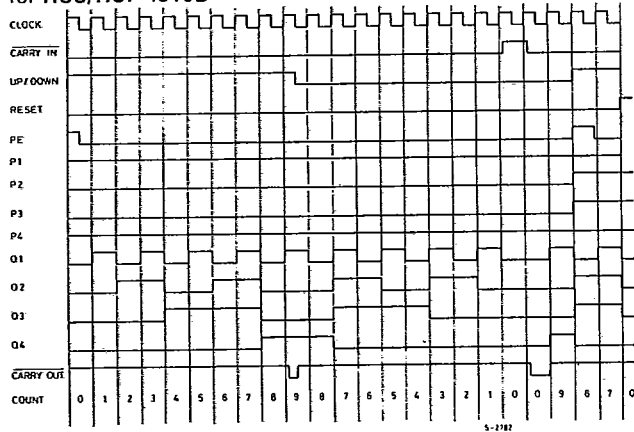
HCC/HCF 4510B
HCC/HCF 4516B

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TIMING DIAGRAMS AND TRUTH TABLE

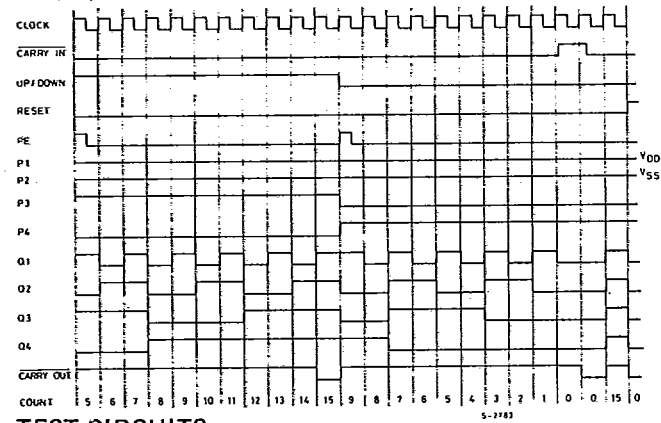
for HCC/HCF 4510B



CL	CT	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
0	0	1	0	0	COUNT UP
0	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

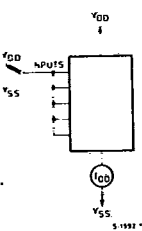
X = Don't care

for HCC/HCF 4516B

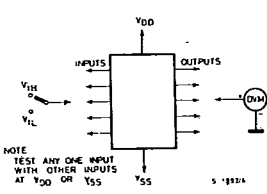


TEST CIRCUITS

Quiescent device current

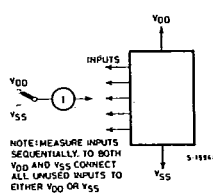


Noise immunity



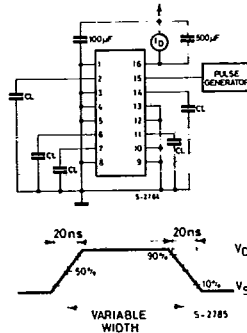
NOTE: TEST ANY ONE INPUT WITH OTHER INPUTS AT VDD OR VSS

Input leakage current



NOTE: MEASURE INPUTS SEQUENTIALLY TO BOTH VDD AND VSS. CONNECT ALL UNUSED INPUTS TO EITHER VDD OR VSS

Power dissipation and input waveform





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STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter	Test conditions				Values						Unit		
	V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *			
					Min.	Max.	Min.	Typ.	Max.	Min.		Max.	
I _L Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
	HCF types	0/20			20		100		0.08	100		3000	
		0/ 5			5		20		0.04	20		150	
		0/10			10		40		0.04	40		300	
V _{OH} Output high voltage		0/15			15		80		0.04	80		600	V
		0/ 5		< 1	5	4.95		4.95			4.95		
		0/10		< 1	10	9.95		9.95			9.95		
V _{OL} Output low voltage		0/15		< 1	15	14.95		14.95			14.95		V
		5/0		< 1	5		0.05			0.05		0.05	
		10/0		< 1	10		0.05			0.05		0.05	
V _{IH} Input high voltage		15/0		< 1	15		0.05			0.05		0.05	V
			0.5/4.5	< 1	5	3.5		3.5			3.5		
			1/9	< 1	10	7		7			7		
V _{IL} Input low voltage			1.5/13.5	< 1	15	11		11			11		V
			4.5/0.5	< 1	5		1.5			1.5		1.5	
			9/1	< 1	10		3			3		3	
I _{OH} Output drive current	HCC types		13.5/1.5	< 1	15		4			4		4	mA
		0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		
		0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
	HCF types	0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
I _{OL} Output sink current	HCC types	0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
	HCF types	0/ 5	0.4		5	0.64		0.51	1		0.36		
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
I _{IH} , I _{IL} Input leakage current	HCC types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
C _I Input capacitance	HCF types	0/18		Any input	18		±0.1		±10 ⁻⁵	±0.1		± 1	
		0/15		Any input	15		±0.3		±10 ⁻⁵	±0.3		± 1	

* T_{Low} = - 55°C for HCC device; -40°C for HCF device.
 * T_{High} = +125°C for HCC device; +85°C for HCF device.
 The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
 2V min. with V_{DD} = 10V
 2.5V min. with V_{DD} = 15V

T-45-23-09

S G S-THOMSON D7C D 7929237 0014969 6

HCC/DCF 4510B
HCC/DCF 4516B

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DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$, $C_L = 50$ pF, $R_L = 200$ k Ω , typical temperature coefficient for all V_{DD} values is 0.3%/ $^{\circ}C$, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit	
		V_{DD} (V)	Min.	Typ.		Max.
t_{PHL} , t_{PLH} Propagation delay time clock to Q output		5		200	400	ns
		10		100	200	
		15		75	150	
t_{PHL} , t_{PLH} Propagation delay time preset or reset to Q output		5		210	420	ns
		10		105	210	
		15		80	160	
t_{PHL} , t_{PLH} Propagation delay time clock to carry out		5		240	480	ns
		10		120	240	
		15		90	180	
t_{PHL} , t_{PLH} Propagation delay time carry in to carry out		5		125	250	ns
		10		60	120	
		15		50	100	
t_{PHL} , t_{PLH} Propagation delay time preset or reset to carry out		5		320	640	ns
		10		160	320	
		15		125	250	
t_{THL} , t_{TLH} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	
f_{max} Max. clock frequency		5	2	4		MHz
		10	4	8		
		15	5.5	11		
t_w Clock pulse width		5	150			ns
		10	75			
		15	60			
* Preset enable or reset removal time		5	150			ns
		10	80			
		15	60			
t_r , t_f * Clock rise and fall time		5			15	μs
		10			5	
		15			5	
t_{setup} Carry in setup time		5	130			ns
		10	60			
		15	45			
t_{setup} Up-down setup time		5	360			ns
		10	160			
		15	110			
t_w Preset enable or reset pulse width		5	220			ns
		10	100			
		15	75			

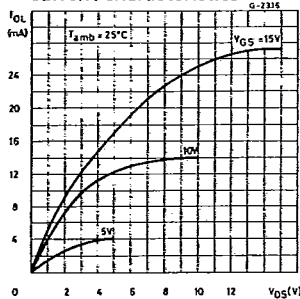
* Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

* If more than unit is cascaded in the parallel clocked application, $t_{r,CL}$ should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

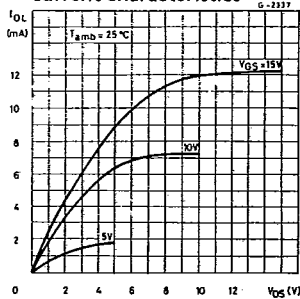


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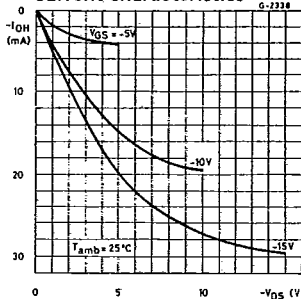
Typical output low (sink) current characteristics



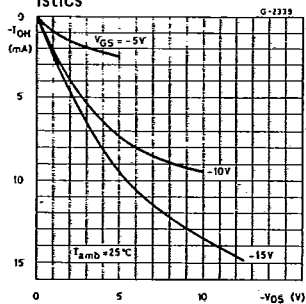
Minimum output low (sink) current characteristics



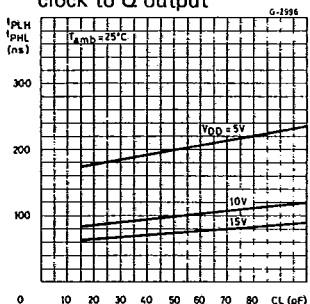
Typical output high (source) current characteristics



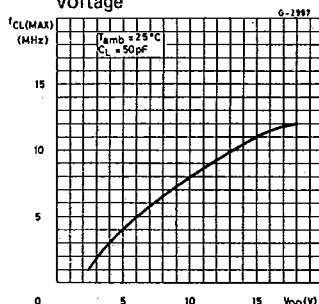
Minimum output high (source) current characteristics



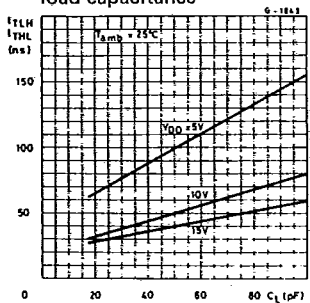
Typical propagation delay time vs. load capacitance for clock to Q output



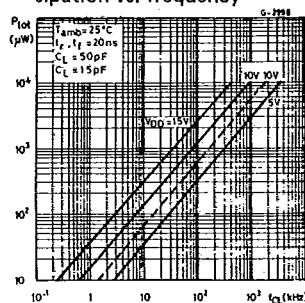
Typical maximum clock input frequency vs. supply voltage



Typical transition time vs. load capacitance



Typical dynamic power dissipation vs. frequency

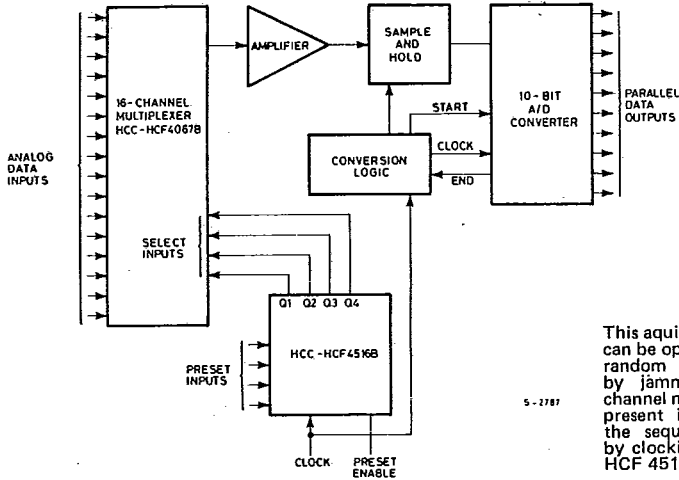


HCC/HCF 4510B
HCC/HCF 4516B

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TYPICAL APPLICATIONS

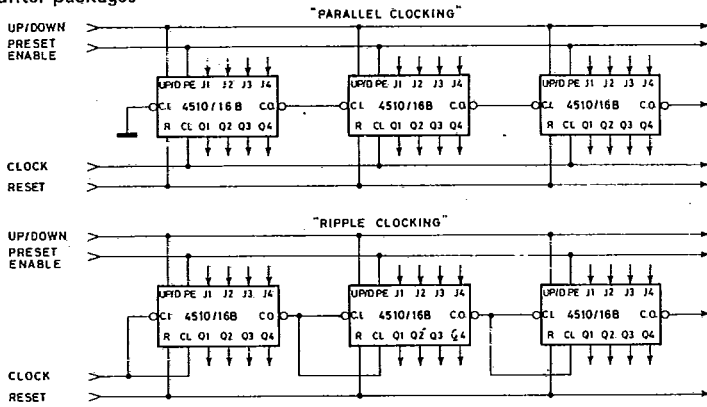
Typical 16-channel, 10 bit data acquisition system



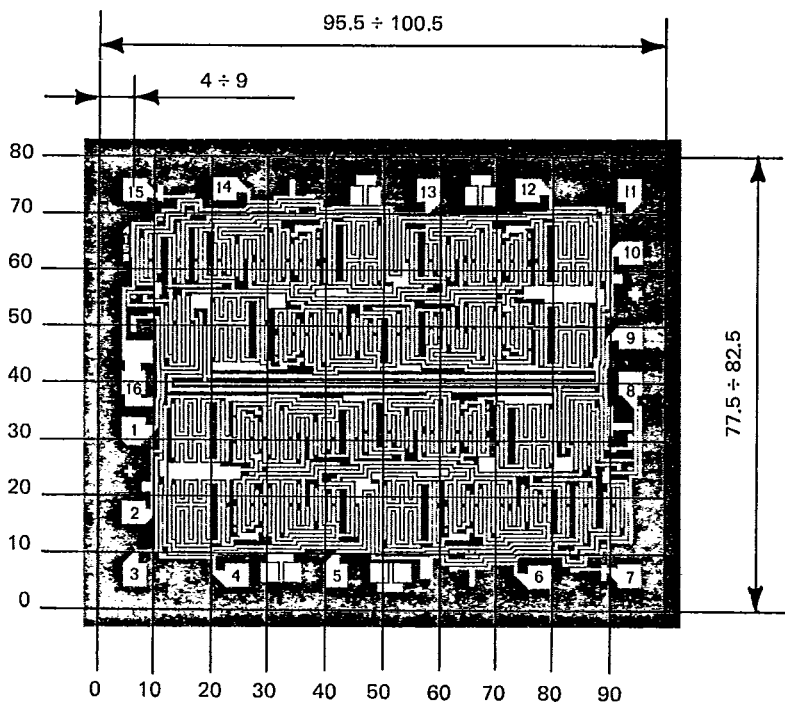
This acquisition system can be operated in the random access mode by jamming in the channel number at the preset inputs, or in the sequential mode by clocking the HCC/HCF 4516B.

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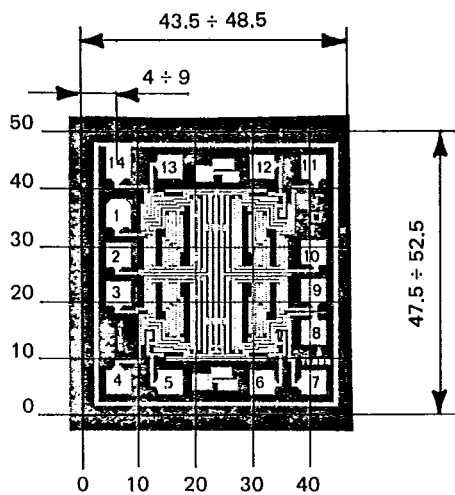
Cascading counter packages



5-2786



4015B



4016B