NEC

User's Manual

# How to Use IC for RS-232 Line Driver/Receivers

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μPD4711B
μPD4712C/4712D
μPD4713A
μPD4714A
μPD4715A
μPD4721
μPD4722
μPD4723
μPD4724
μPD4726

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**[MEMO]**

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M7D 98.12

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## CONTENTS

## 1. INTRODUCTION

The serial communication standard EIA/TIA-232-E (generally called “RS-232”), established by EIA and TIA, has been used for industrial devices. However, today it is widely used as a communication means between office automation equipment that equips serial interface, and PCs and PC peripheral devices or home appliances.

NEC lines up six μPD471X Series products and five μPD472X Series products so that they can be widely applied to various devices for industrial equipment and appliances as ICs for RS-232 line driver/receivers.

This document summarizes usage of the products, technical data, and notes for using these ICs.

Your necessary information is found as follows:

- For overview of RS-232 standard: → Refer to Chapter **9**. **RS-232 STANDARD**.
- For overview and list of NEC’s products: → Refer to Chapter **2. FEATURES OF ICS FOR RS-232 LINE DRIVER/RECEIVERS** and Chapter **3. SERIES LINEUP**.
- For details on functions of NEC’s products: → Refer to Chapter **6**. **INTERNAL BLOCK DIAGRAMS**.
- For characteristics and performance of NEC’s products: → Refer to Chapter **8**. **TYPICAL CHARACTERISTICS**.
- For answers to common questions and how-to: → Refer to Chapter **12**. **Q&A**.

## 2. FEATURES OF ICS FOR RS-232 LINE DRIVER/RECEIVERS

There are two types of product series of ICs for RS-232 Line Driver/Receiver, and each type has following features:

○ μPD471X Series

- Compliant with EIA/TIA-232-E standard.
- Operated by single power supply with voltage of +5 V
- Positive and negative outputs by four external capacitors and on-chip DC/DC converter
- On-chip driver output control functions
- Function for selecting receiver input threshold voltage
- Low current dissipation mode by standby function
- Two types of packages: DIP and SOP

○ μPD472X Series

- Complied with EIA/TIA-232-E Standard
- Operated by single power supply with either voltage of +5 V or +3.3 V
- Positive and negative outputs by four or five external capacitors and on-chip DC/DC converter
- Low current dissipation mode by standby function
- On-chip receiver functions which can be operated during standby
- SSOP package for space saving

## 3. SERIES LINEUP

### 3.1 Selection Guide

The list of ICs for RS-232 line driver/receivers is shown below.

| Part Number | Driver | Receiver | Power Supply Voltage | Standby | Driver Output Control | Low Current Dissipation Receiver Operation Mode |
|---|---|---|---|---|---|---|
| μPD4711B | 2 | 2 | 5 V | ○ | ○ | × |
| μPD4712C | 4 | 4 | 5 V | ○ | ○ | × |
| μPD4712D | 4 | 4 | 5 V | ○ | ○ | × |
| μPD4713A | 3 | 3 | 5 V | ○ | ○ | × |
| μPD4714A | 3 | 5 | 5 V | ○ | ○ | × |
| μPD4715A | 5 | 3 | 5 V | ○ | ○ | × |
| μPD4721 | 2 | 2 | 3.3/5 V | ○ | × | × |
| μPD4722 | 4 | 4 | 3.3/5 V | ○ | × | ○ |
| μPD4723 | 3 | 3 | 3.3/5 V | ○ | × | ○ |
| μPD4724 | 3 | 5 | 3.3/5 V | ○ | × | ○ |
| μPD4726 | 4 | 7 | 5 V | ○ | × | ○ |

○: Available ×: Not available

### 3.2 Ordering Information

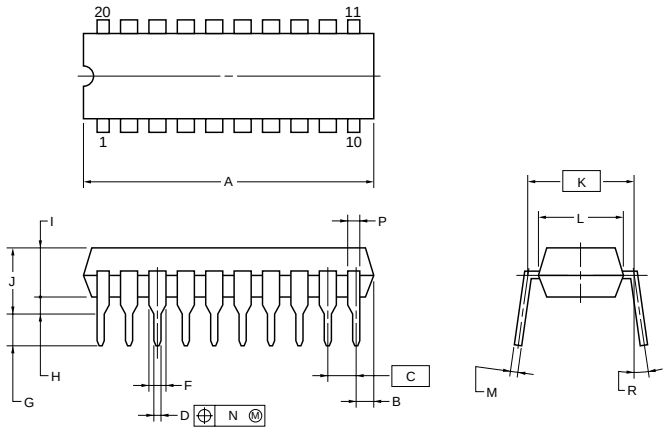
Ordering information and the package list of ICs for RS-232 line driver/receivers are shown below.

| Part Number | Ordering Information | Package |
|---|---|---|
| μPD4711B | μPD4711BCX | 20-pin DIP (300 mil) |
| | μPD4711BGS | 20-pin SOP (300 mil) |
| μPD4712C | μPD4712CCY | 28-pin DIP (400 mil) |
| | μPD4712CGT | 28-pin SOP (375 mil) |
| μPD4712D | μPD4712DCY | 28-pin DIP (400 mil) |
| | μPD4712DGT | 28-pin SOP (375 mil) |
| μPD4713A | μPD4713ACX | 24-pin DIP (300 mil) |
| | μPD4713AGT | 24-pin SOP (375 mil) |
| μPD4714A | μPD4714ACY | 28-pin DIP (400 mil) |
| | μPD4714AGT | 28-pin SOP (375 mil) |
| μPD4715A | μPD4715ACY | 28-pin DIP (400 mil) |
| | μPD4715AGT | 28-pin SOP (375 mil) |
| μPD4721 | μPD4721GS-GJG | 20-pin SSOP (300 mil) |
| μPD4722 | μPD4722GS-GJG | 30-pin SSOP (300 mil) |
| μPD4723 | μPD4723GS-GJG | 30-pin SSOP (300 mil) |
| μPD4724 | μPD4724GS-GJG | 30-pin SSOP (300 mil) |
| μPD4726 | μPD4726GS-BAF | 36-pin SSOP (300 mil) |

# 4. PACKAGE DRAWINGS, PIN CONFIGURATIONS, AND FUNCTIONAL BLOCK DIAGRAMS

## 4.1 Package Drawings

**20PIN PLASTIC DIP (300 mil)**




**NOTES**

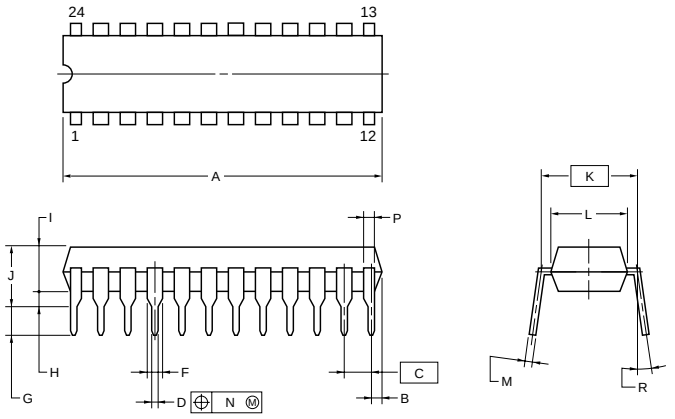
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 25.40 MAX. | 1.000 MAX. |
| B | 1.27 MAX. | 0.050 MAX. |
| C | 2.54 (T.P.) | 0.100 (T.P.) |
| D | $0.50\pm0.10$ | $0.020^{+0.004}_{-0.005}$ |
| F | 1.1 MIN. | 0.043 MIN. |
| G | 3.5±0.3 | 0.138±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 7.62 (T.P.) | 0.300 (T.P.) |
| L | 6.4 | 0.252 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.25 | 0.01 |
| P | 0.9 MIN. | 0.035 MIN. |
| R | 0–15° | 0–15° |

**P20C-100-300A,C-1**

**24PIN PLASTIC DIP (300 mil)**




**NOTES**

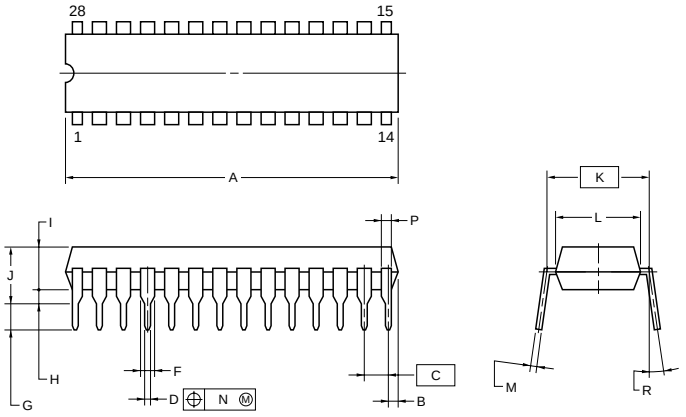
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 33.02 MAX. | 1.300 MAX. |
| B | 2.54 MAX. | 0.100 MAX. |
| C | 2.54 (T.P.) | 0.100 (T.P.) |
| D | $0.50\pm0.10$ | $0.020^{+0.004}_{-0.005}$ |
| F | 1.2 MIN. | 0.047 MIN. |
| G | 3.5±0.3 | 0.138±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 7.62 (T.P.) | 0.300 (T.P.) |
| L | 6.4 | 0.252 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.25 | 0.01 |
| P | 1.0 MIN. | 0.039 MIN. |
| R | 0–15° | 0–15° |

**P24C-100-300A-1**

### 28PIN PLASTIC DIP (400 mil)




**NOTES**

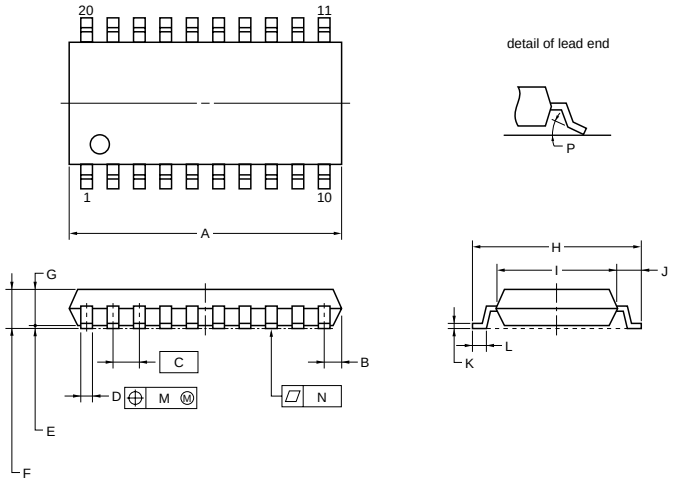
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 35.56 MAX. | 1.400 MAX. |
| B | 1.27 MAX. | 0.050 MAX. |
| C | 2.54 (T.P.) | 0.100 (T.P.) |
| D | $0.50\pm0.10$ | $0.020^{+0.004}_{-0.005}$ |
| F | 1.1 MIN. | 0.043 MIN. |
| G | $3.5\pm0.3$ | $0.138\pm0.012$ |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.72 MAX. | 0.226 MAX. |
| K | 10.16 (T.P.) | 0.400 (T.P.) |
| L | 8.6 | 0.339 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.25 | 0.01 |
| P | 0.9 MIN. | 0.035 MIN. |
| R | 0–15° | 0–15° |

**P28C-100-400-1**

### 20 PIN PLASTIC SOP (300 mil)



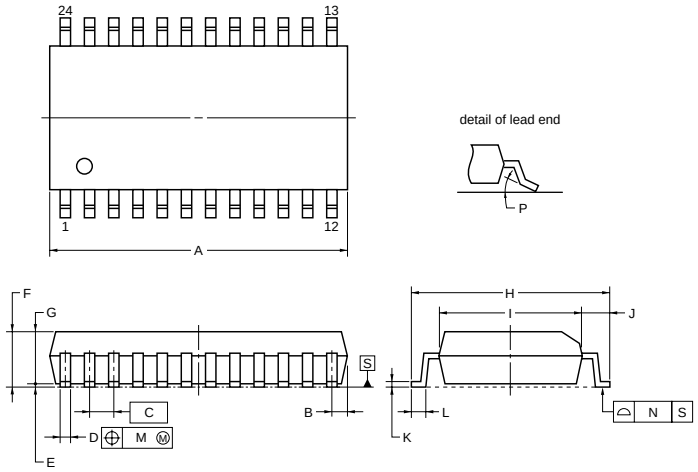

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | $12.7\pm0.3$ | $0.500\pm0.012$ |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | $0.42^{+0.08}_{-0.07}$ | $0.017^{+0.003}_{-0.004}$ |
| E | $0.1\pm0.1$ | $0.004\pm0.004$ |
| F | 1.8 MAX. | 0.071 MAX. |
| G | $1.55\pm0.05$ | $0.061\pm0.002$ |
| H | $7.7\pm0.3$ | $0.303\pm0.012$ |
| I | $5.6\pm0.2$ | $0.220^{+0.009}_{-0.008}$ |
| J | 1.1 | 0.043 |
| K | $0.22^{+0.08}_{-0.07}$ | $0.009^{+0.003}_{-0.004}$ |
| L | $0.6\pm0.2$ | $0.024^{+0.008}_{-0.009}$ |
| M | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ+7^{\circ}}_{-3^{\circ}}$ |

**P20GM-50-300B, C-5**

**24 PIN PLASTIC SOP (375 mil)**



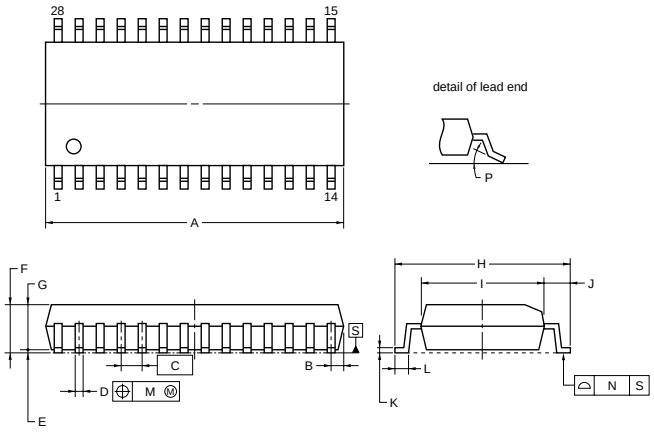

**NOTES**

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 15.4±0.14 | 0.606±0.006 |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | $0.42^{+0.08}_{-0.07}$ | $0.017^{+0.003}_{-0.004}$ |
| E | 0.125±0.075 | $0.005^{+0.003}_{-0.004}$ |
| F | 2.77 MAX. | 0.110 MAX. |
| G | 2.47±0.1 | $0.097^{+0.005}_{-0.004}$ |
| H | 10.3±0.3 | $0.406^{+0.012}_{-0.013}$ |
| I | 7.2 | 0.283 |
| J | 1.6 | 0.063 |
| K | $0.17^{+0.08}_{-0.07}$ | $0.007^{+0.003}_{-0.004}$ |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | 0.12 | 0.005 |
| N | 0.15 | 0.006 |
| P | $3^{\circ+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ+7^{\circ}}_{-3^{\circ}}$ |

**P24GM-50-375B-4**

**28-PIN PLASTIC SOP (375 mil)**



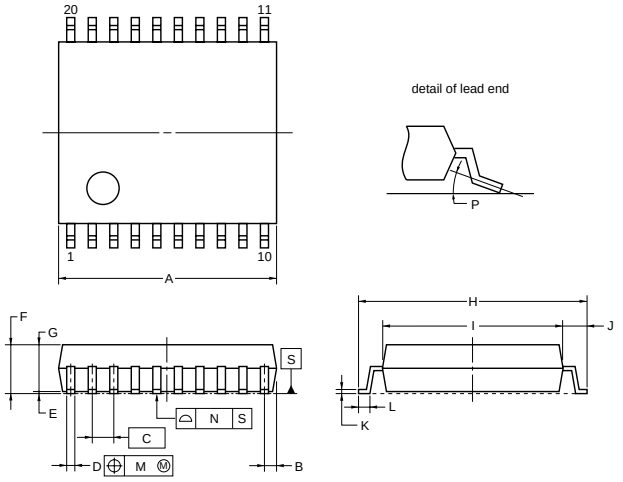

**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 17.9±0.17 |
| B | 0.78 MAX. |
| C | 1.27 (T.P.) |
| D | $0.42^{+0.08}_{-0.07}$ |
| E | 0.1±0.1 |
| F | 2.6±0.2 |
| G | 2.50 |
| H | 10.3±0.3 |
| I | 7.2±0.2 |
| J | 1.6±0.2 |
| K | $0.17^{+0.08}_{-0.07}$ |
| L | 0.8±0.2 |
| M | 0.12 |
| N | 0.15 |
| P | $3^{\circ+7^{\circ}}_{-3^{\circ}}$ |

**P28GM-50-375B-4**

**20 PIN PLASTIC SHRINK SOP (300 mil)**



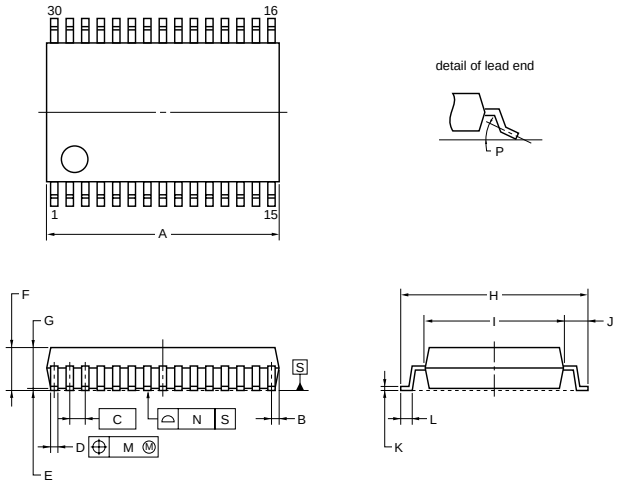

**NOTE**

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 6.7±0.3 | $0.264^{+0.012}_{-0.013}$ |
| B | 0.575 MAX. | 0.023 MAX. |
| C | 0.65 (T.P.) | 0.026 (T.P.) |
| D | $0.32^{+0.08}_{-0.07}$ | $0.013^{+0.003}_{-0.004}$ |
| E | 0.125±0.075 | 0.005±0.003 |
| F | 2.0 MAX. | 0.079 MAX. |
| G | 1.7±0.1 | $0.067^{+0.004}_{-0.005}$ |
| H | 8.1±0.3 | 0.319±0.012 |
| I | 6.1±0.2 | 0.240±0.008 |
| J | $1.0^{\pm}0.2$ | $0.039^{+0.009}_{-0.008}$ |
| K | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.002}$ |
| L | 0.5±0.2 | $0.020^{+0.008}_{-0.009}$ |
| M | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3°^{+7°}_{-3°}$ | $3°^{+7°}_{-3°}$ |

**P20GM-65-300B-3**

**30 PIN PLASTIC SHRINK SOP (300 mil)**



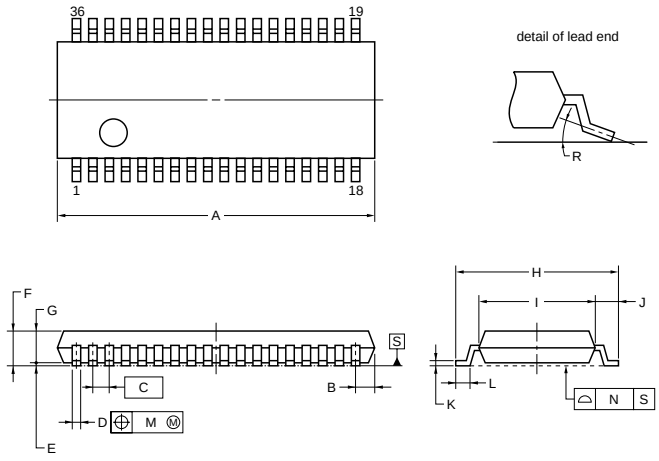

**NOTES**

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 9.85±0.26 | 0.388±0.011 |
| B | 0.51 MAX. | 0.020 MAX. |
| C | 0.65 (T.P.) | 0.026 (T.P.) |
| D | $0.32^{+0.08}_{-0.07}$ | $0.013^{+0.003}_{-0.004}$ |
| E | 0.125±0.075 | 0.005±0.003 |
| F | 2.0 MAX. | 0.079 MAX. |
| G | 1.7±0.1 | 0.067±0.004 |
| H | 8.1±0.2 | 0.319±0.008 |
| I | 6.1±0.2 | 0.240±0.008 |
| J | 1.0±0.2 | $0.039^{+0.009}_{-0.008}$ |
| K | $0.17^{+0.08}_{-0.07}$ | $0.007^{+0.003}_{-0.004}$ |
| L | 0.5±0.2 | $0.020^{+0.008}_{-0.009}$ |
| M | 0.10 | 0.004 |
| N | 0.10 | 0.004 |
| P | $3°^{+7°}_{-3°}$ | $3°^{+7°}_{-3°}$ |

**P30GS-65-300B-2**

**36 PIN PLASTIC SSOP (300 mil)**




**NOTE**

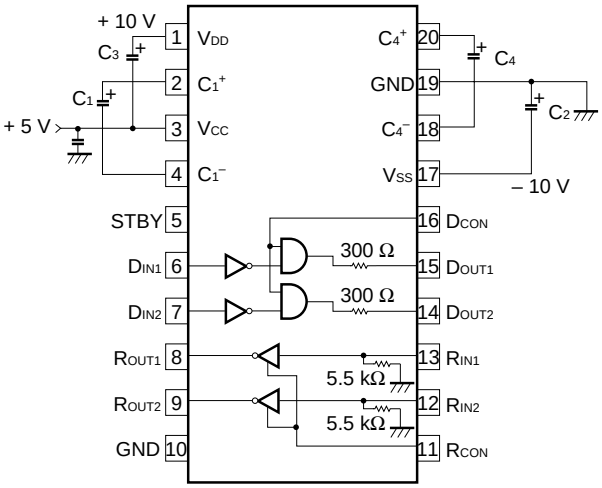
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 15.3±0.24 |
| B | 0.97 MAX. |
| C | 0.8 (T.P.) |
| D | $0.37^{+0.08}_{-0.07}$ |
| E | 0.125±0.075 |
| F | $1.675^{+0.125}_{-0.175}$ |
| G | 1.55 |
| H | 7.7±0.3 |
| I | 5.6±0.15 |
| J | 1.05±0.2 |
| K | $0.22^{+0.08}_{-0.07}$ |
| L | 0.6±0.2 |
| M | 0.10 |
| N | 0.10 |
| R | 5°±5° |

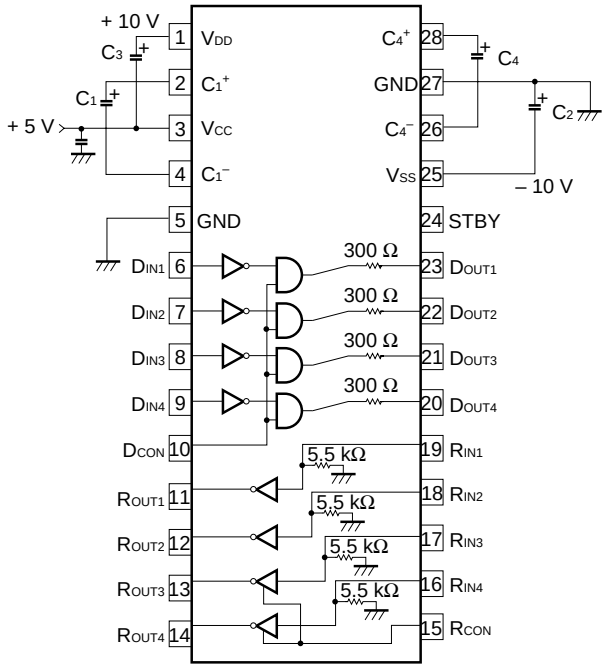
**P36GM-80-300B-4**

## 4.2 Pin Configurations

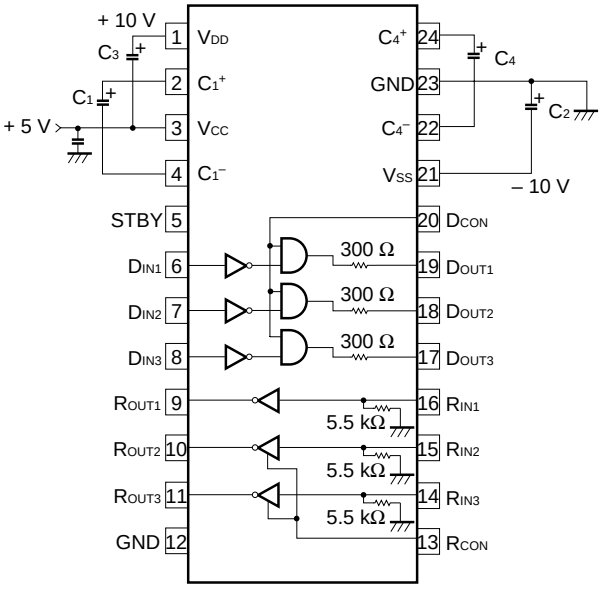
**μPD4711B**



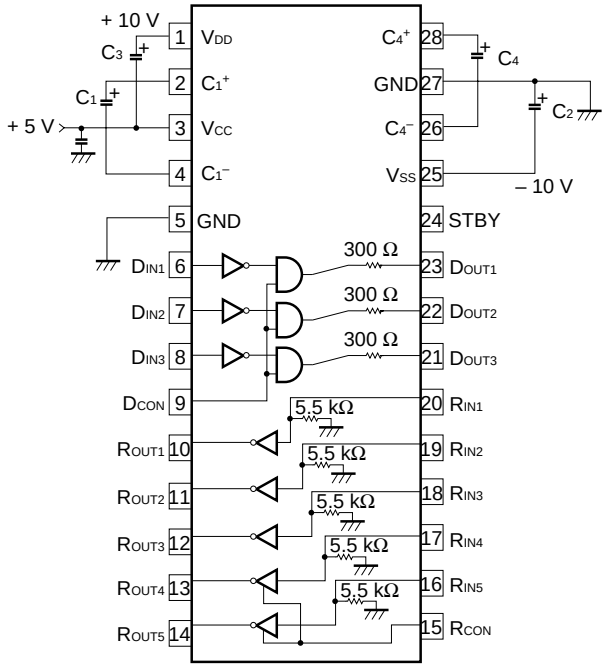

**μPD4712C/D**



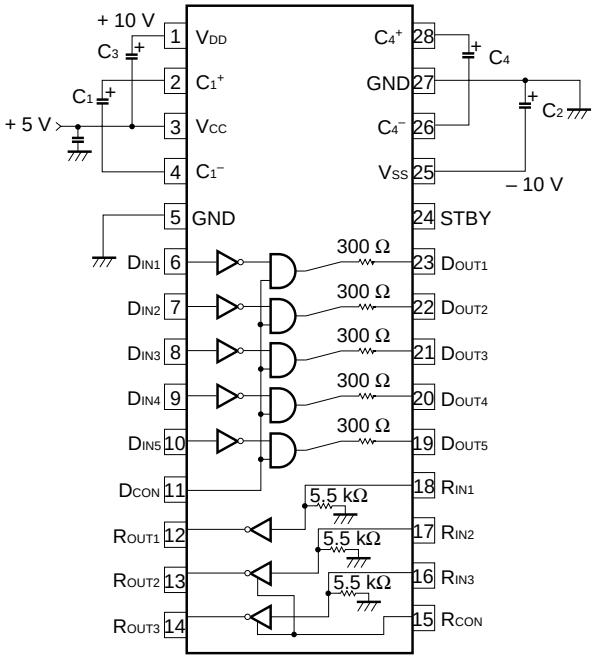

**μPD4713A**



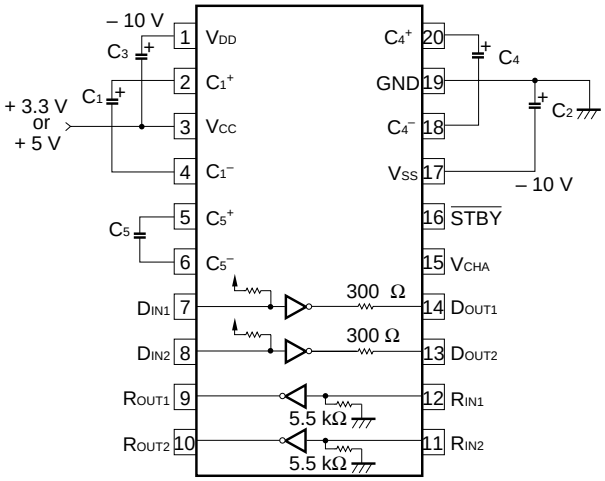

**μPD4714A**



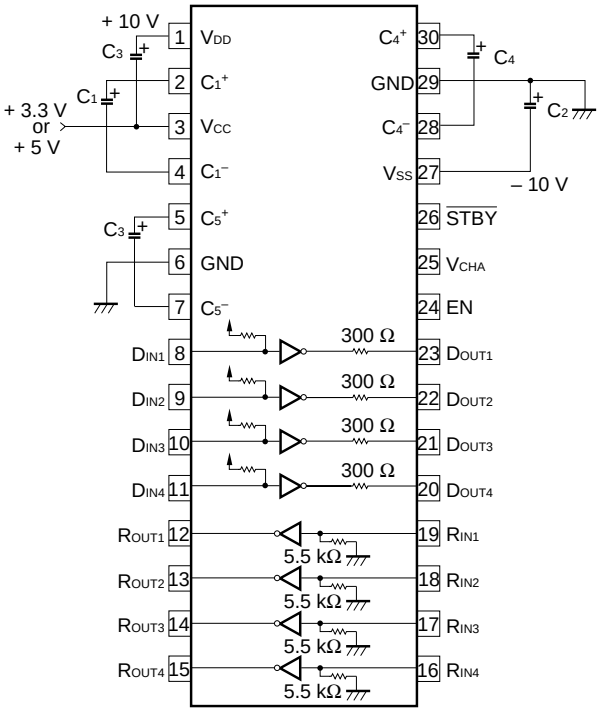
**μPD4715A**



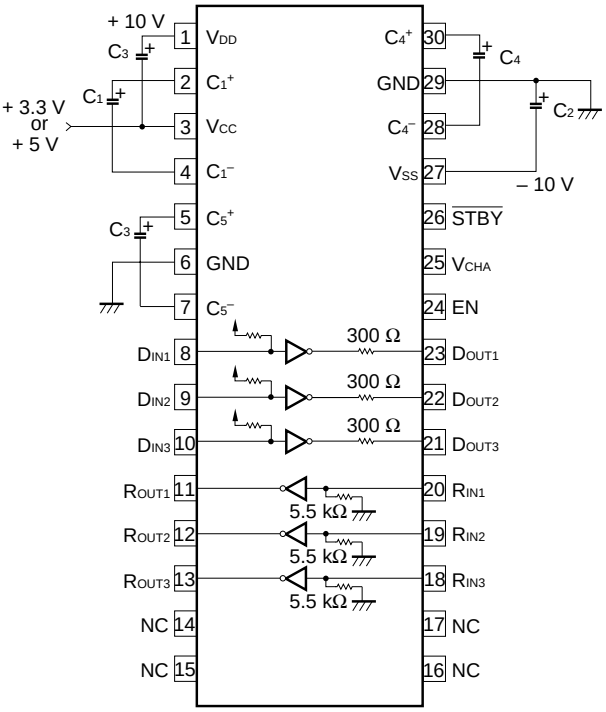

**μPD4721**



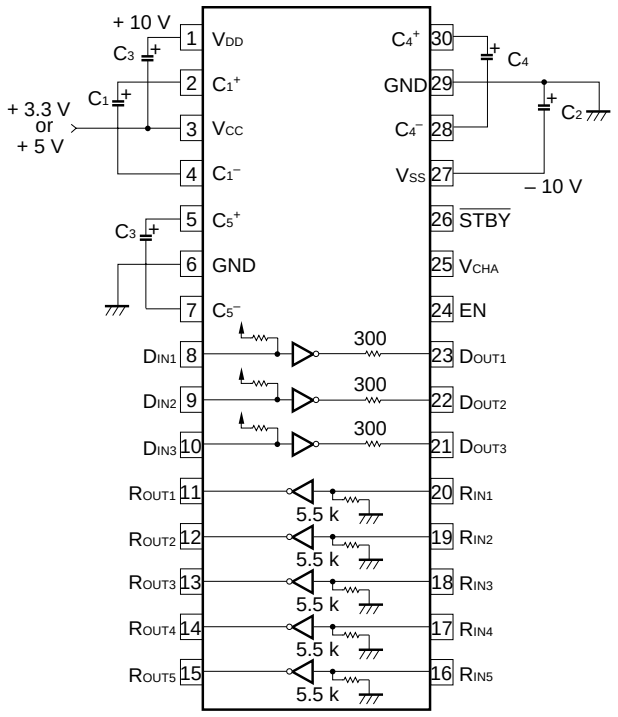

**μPD4722**



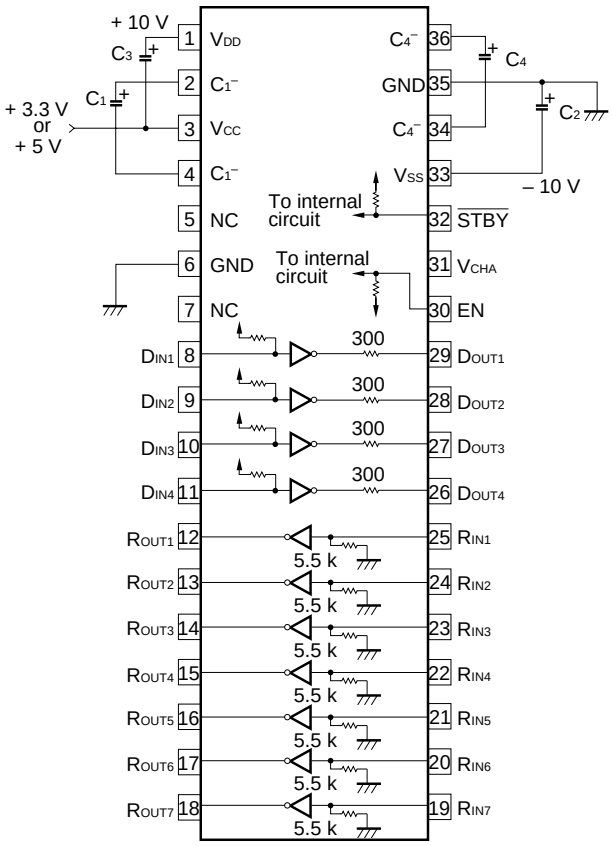

**μPD4723**



**μPD4724**

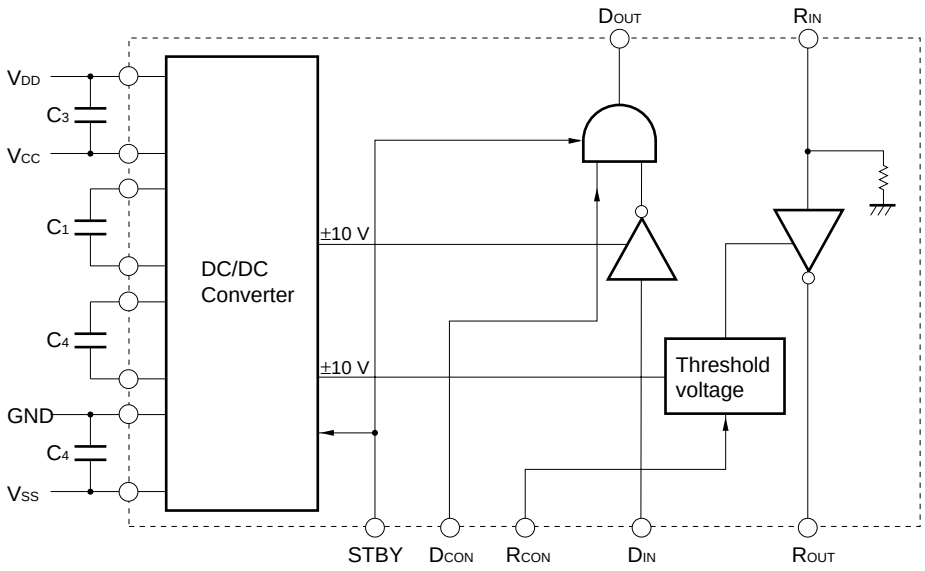



**μPD4726**

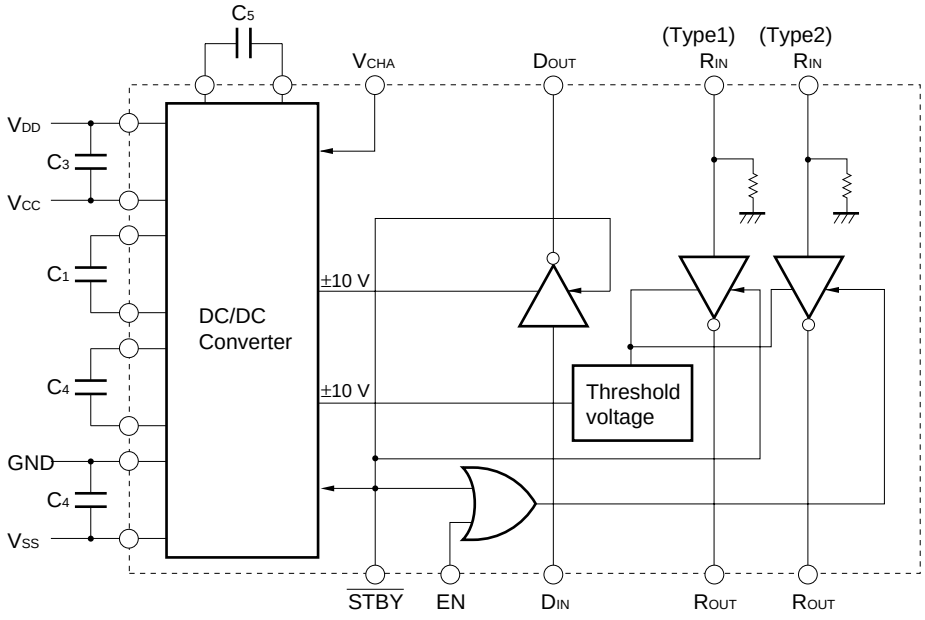


## 4.3 Functional Block Diagrams

### μPD471X Series



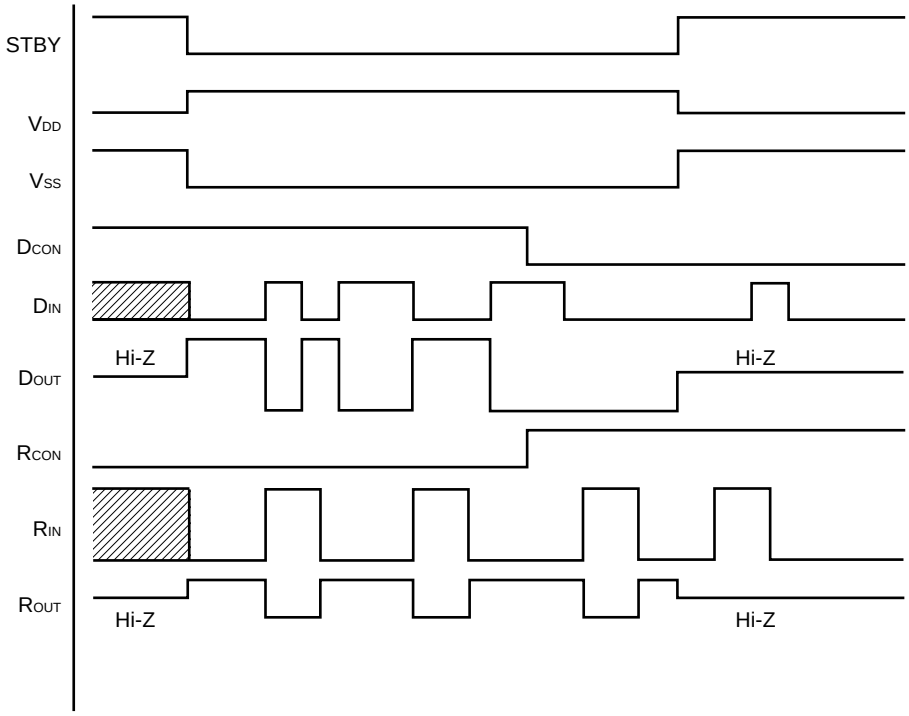

### μPD472X Series



# 5. BASIC OPERATIONS

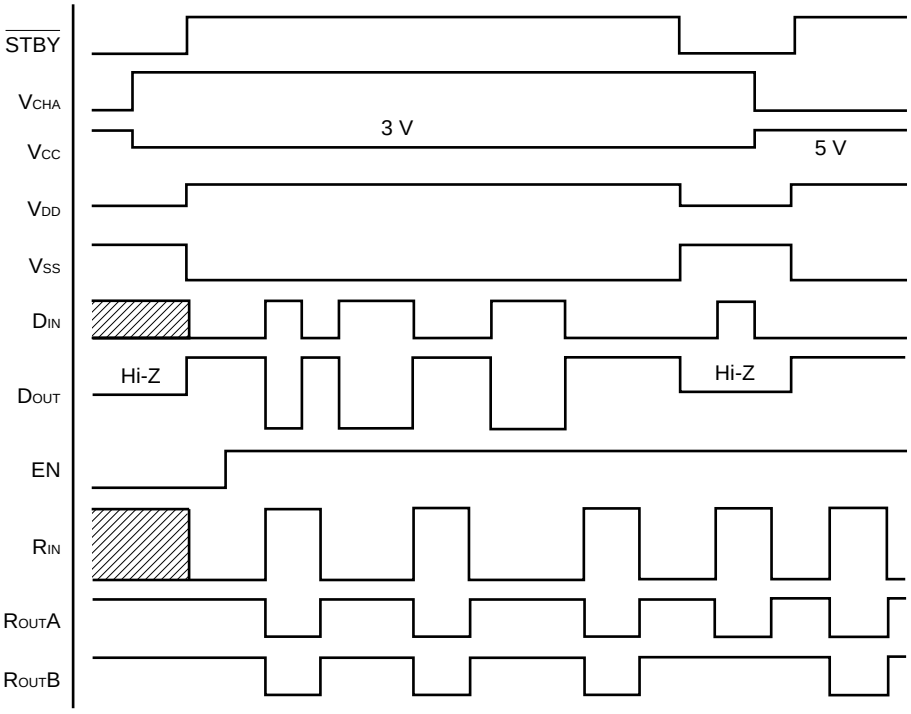
## 5.1 Basic Operation of μPD471X Series

The basic operation of the μPD471X Series is shown in the figure below.




## 5.2 Basic Operation of μPD472X Series

The basic operation of the μPD472X Series is shown in the figure below.



# 6. INTERNAL BLOCK DIAGRAM

## 6.1 μPD471X Series

### 6.1.1 DC/DC converter block

The μPD471X Series incorporate a DC/DC converter block. A DC/DC converter is a circuit to boost $V_{CC}$ to $V_{DD}/V_{SS}$ to generate the necessary voltage level for RS-232 communication by fast switching with external capacitors.

RS-232 communication, which requires positive and negative power supplies even with a single voltage of 5 V, can be achieved by integrating this circuit with a RS-232 line driver/receiver.

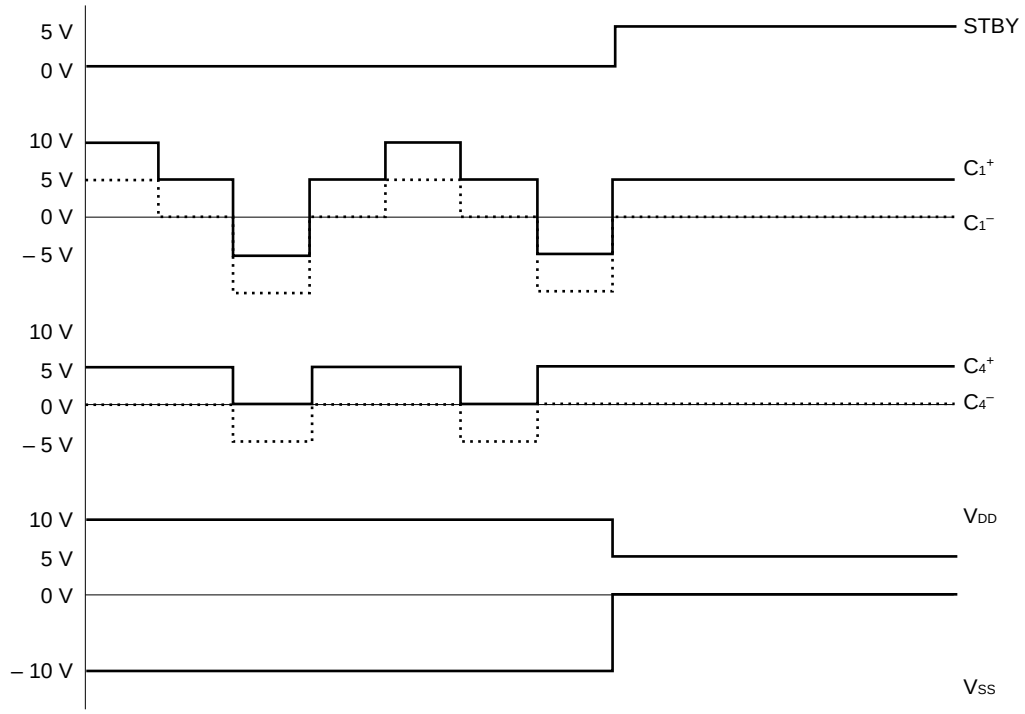
The maximum voltage of electric potential difference applied at the both ends of each capacitor having characteristics of DC/DC converter circuit is shown in the table below, and the theoretical operating waveform of each pin is shown in the figure below.

Also, DC/DC converter circuit is stopped when STBY is at H. At this moment, $V_{DD} = V_{CC}$ and $V_{SS}$ = GND.

**The electric potential difference applied to each capacitor when $V_{CC}$ = 5 V**

| Capacitor | Voltage (V) |
|---|---|
| $C_1^+ – C_1^-$ | 5 |
| $C_2^+ – C_2^-$ | 10 |
| $C_3^+ – C_3^-$ | 5 |
| $C_4^+ – C_4^-$ | 5 |

**Operating waveform at capacitors**



### 6.1.2 Driver output logic

STBY is the Standby Control Signal.

When STBY is at H, $D_{OUT}$ becomes high impedance regardless of the status of $D_{CON}$ and $D_{IN}$. While STBY is at L, driver output depends on input signals from $D_{CON}$ and $D_{IN}$.

$D_{CON}$ is driver output control signal and active at high.

When $D_{CON}$ is H, $D_{IN}$ (TTL level) is reversed and output from $D_{OUT}$ (RS-232 level). While $D_{CON}$ is L, $D_{OUT}$ is fixed at L regardless of the status of $D_{IN}$.

Truth table of driver output logic is shown below (refer to **12.1 Internal Circuit Functions** in **12. Q&A LIST** for actual usage of $D_{CON}$).

| STBY | $D_{CON}$ | $D_{IN}$ | $D_{OUT}$ | Remarks |
|---|---|---|---|---|
| H | X | X | Hi-Z | Standby mode (DC/DC Converter stopped) |
| L | L | X | L | Mark level output |
| L | H | L | H | Space level output |
| L | H | H | L | Mark level output |

### 6.1.3 Receiver output logic

When STBY is at H, $R_{OUT}$ becomes High Impedance state regardless of the status of $R_{IN}$. While STBY is at L, $R_{IN}$ (RS-232 level) is reversed and output from $R_{OUT}$ (TTL level).

Truth table of receiver output logic is shown below.

| STBY | $R_{IN}$ | $R_{OUT}$ | Remarks |
|---|---|---|---|
| H | X | Hi-Z | Standby Mode (DC/DC converter stopped) |
| L | L | H | Mark level output |
| L | H | L | Space level output |

### 6.1.4 Receiver input threshold voltage

The $\mu$PD471X Series has a function to switch receiver input threshold voltage as its specific function. Refer to individual data sheet for characteristics of threshold voltage.

When $R_{CON}$ is at L, $R_{OUT}$ always operates in A Mode. When $R_{CON}$ is at H, $R_{IN}$A operates in A Mode and $R_{IN}$B operates in B Mode as the table below.

The truth table and pin list of each part number are shown below (refer to **12.1 Internal Circuit Functions** in **12. Q&A** for actual usage of $R_{CON}$)

**The truth table of receiver input threshold**

| $R_{CON}$ | $R_{IN}$A | $R_{IN}$B |
|---|---|---|
| L | A Mode | A Mode |
| H | A Mode | B Mode (C Mode only in $\mu$PD4712D) |

**The pin list of each product in A Mode and B Mode**

| Part Number | $R_{IN}A$ | $R_{IN}B$ |
|---|---|---|
| μPD4711B | – | $R_{IN1}$, $R_{IN2}$ |
| μPD4712C/4712D | $R_{IN1}$, $R_{IN2}$ | $R_{IN3}$, $R_{IN4}$ |
| μPD4713A | $R_{IN1}$ | $R_{IN2}$, $R_{IN3}$ |
| μPD4714A | $R_{IN1}$, $R_{IN2}$, $R_{IN3}$ | $R_{IN4}$, $R_{IN5}$ |
| μPD4715A | $R_{IN1}$ | $R_{IN2}$, $R_{IN3}$ |

### 6.1.5 Input pin treatment

The internal configuration of input pins of the μPD471X Series is shown in the table below. If an input pin is opened, through current flows as CMOS-specific characteristics. Therefore, open pins should be treated as follows:

| Pin Name | Pull-up or Pull-down Resistor | Handling of Open Pins |
|---|---|---|
| STBY | Pull-down resistor | Even if the input is open, the input becomes “L” and the operation-mode is active. |
| $D_{CON}$ | None | Be sure to fix it at “H” or “L” level before using. |
| $D_{IN}$ | | |
| $R_{CON}$ | | |
| $R_{IN}$ | Pull-down resistor (5.5 kΩ) | Even if the input is open, the input becomes “L” and the output becomes “H.” |

## 6.2 μPD472X Series

### 6.2.1 DC/DC Converter Block

The μPD472X Series incorporates a DC/DC converter block. A DC/DC converter Block is a circuit to boost $V_{CC}$ to $V_{DD}/V_{SS}$ to generate the necessary voltage level for RS-232 communication by fast switching with external capacitors. It has a Double Boosting Mode and Triple Boosting Mode to use single power supply either voltage with 5 V or 3.3 V as specific function of μPD472X Series.

RS-232 communication, which requires positive and negative power supplies even with a single voltage of 5 V or 3.3 V, can be achieved by integrating this circuit with an RS-232 line driver/receiver.

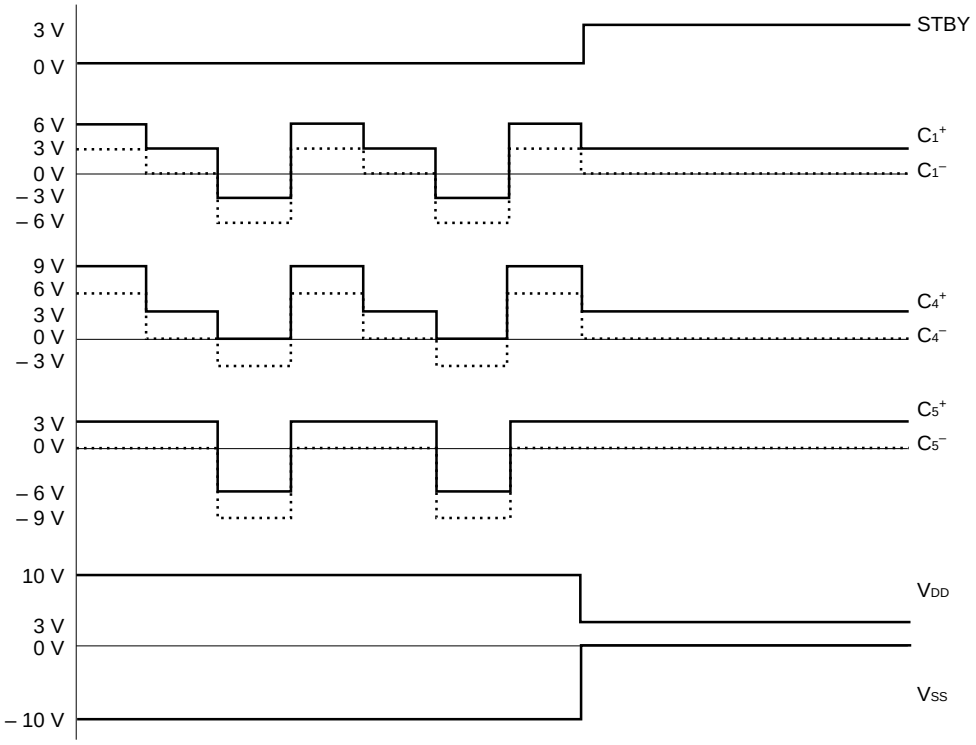
The maximum voltage of electric potential difference applied at both ends of each capacitor having characteristics of DC/DC converter circuit is shown in the table below, and theoretical operating waveform of each pin (Only in 3-V mode. The waveform in 5-V mode is the same as the one of the μPD471X Series.) is shown in the figure below.

Also, DC/DC Converter circuit is stopped when $\overline{STBY}$ is at L. At this moment, $V_{DD} = V_{CC}$ and $V_{SS}$ = GND.

**Electric potential difference applied to each capacitor when $V_{CC}$ = 5 V (5-V Mode) or 3 V (3-V Mode)**

| Capacitor | Voltage (V) | |
|---|---|---|
| | 5-V Mode | 3-V Mode |
| $C_1^+ – C_1^-$ | 5.0 | 3.0 |
| $C_2^+ – C_2^-$ | 10.0 | 9.0 |
| $C_3^+ – C_3^-$ | 5.0 | 6.0 |
| $C_4^+ – C_4^-$ | 5.0 | 3.0 |
| $C_5^+ – C_5^-$ | 5.0 | 3.0 |

**Operating waveform at capacitors**



### 6.2.2 Driver output logic

When $\overline{\text{STBY}}$ is at L, $D_{OUT}$ becomes high impedance regardless of the status of $D_{CON}$ and $D_{IN}$.

When $\overline{\text{STBY}}$ is H, $D_{IN}$ (TTL level) is reversed and output from $D_{OUT}$ (RS-232 level).

The truth table of driver output logic is shown below.

| $\overline{\text{STBY}}$ | $D_{IN}$ | $D_{OUT}$ | Remarks |
|---|---|---|---|
| L | X | Hi-Z | Standby Mode (DC/DC converter stopped) |
| H | L | H | Space level output |
| H | H | L | Mark level output |

### 6.2.3 Receiver output logic

When $\overline{\text{STBY}}$ is at L, two types of standby modes can be selected depending on the EN logic. When EN is L, regardless of the status of $R_{IN}$ (RS-232 level), H is output for $R_{OUT}$ (TTL level). When EN is H, $R_{OUT}$A (TTL level) is output by an inverter without hysteresis for the input of $R_{IN}$A (RS-232 level). Regardless of $R_{IN}$B (RS-232 level), H is output for $R_{OUT}$B (TTL level).

When $\overline{\text{STBY}}$ is H, $R_{IN}$ (RS-232 level) is reversed and output from $R_{OUT}$ (TTL level) regardless of the EN state.

The truth table of the receiver output logic is shown below (refer to **12.1 Internal Circuit Functions** in **12. Q&A** for actual sample usage of EN pin).

**Truth table of receiver output logic**

| $\overline{\text{STBY}}$ | EN | $R_{IN}$ | | $R_{OUT}$ | | Remarks |
|---|---|---|---|---|---|---|
| | | $R_{IN}$A | $R_{IN}$B | $R_{OUT}$A | $R_{OUT}$B | |
| L | L | X | X | H | H | Standby Mode 1 (DC/DC converter stopped) |
| L | H | L | X | H | H | Standby Mode 2 (DC/DC converter stopped) |
| L | H | H | X | L | H | Standby Mode 2 (DC/DC converter stopped) |
| H | X | L | | H | | Mark level output |
| H | X | H | | L | | Space level output |

**Pin list of each product in A Mode and B Mode**

| Part Number | $R_{IN}$A | $R_{IN}$B |
|---|---|---|
| $\mu$PD4721 | – | $R_{IN1}$, $R_{IN2}$ |
| $\mu$PD4722 | $R_{IN3}$, $R_{IN4}$ | $R_{IN1}$, $R_{IN2}$ |
| $\mu$PD4723 | $R_{IN2}$, $R_{IN3}$ | $R_{IN1}$ |
| $\mu$PD4724 | $R_{IN4}$, $R_{IN5}$ | $R_{IN1}$, $R_{IN2}$, $R_{IN3}$ |
| $\mu$PD4726 | $R_{IN6}$, $R_{IN7}$ | $R_{IN1}$, $R_{IN2}$, $R_{IN3}$, $R_{IN4}$, $R_{IN5}$ |

### 6.2.4 Switching voltage boosting mode

Voltage boosting mode of internal DC/DC converter can be switched by $V_{CHA}$. When the voltage of the power supply used is lowered (5 V → 3 V), it can be switched even when the power is turned on.

When you switch the voltage boosting mode, the operation mode must be Standby Mode ($\overline{\text{STBY}}$ = L).

| $V_{CHA}$ | Operating Mode |
|---|---|
| L | 5-V Mode (double boost) |
| H | 3-V Mode (triple boost) |

### 6.2.5 Input pin treatment

The internal configuration of input pins of the $\mu$PD472X Series is shown in the table below. If an input pin is left open, through current flows due to CMOS-specific characteristics. Therefore, open pins should be treated as follows.

| Pin Name | Pull-up or Pull-down Resistor | Handling of Open Pin |
|---|---|---|
| $\overline{\text{STBY}}$ | None | Fix to "H" or "L" level. |
| $V_{CHA}$ | | |
| EN | | |
| $D_{IN}$ | Active pull-up resistor (up to 300 kΩ) | Even if the input is open, the input becomes "H" and the output becomes "L." |
| $R_{IN}$ | Pull-down resistor (5.5 kΩ) | Even if the input is open, the input becomes "L" and the output becomes "H." |

A pull-up resistor is connected to the $D_{IN}$ pin so that the input potential is fixed even it is opened. This pull-up resistor is an active resistor whose resistance becomes higher when the input potential is low and becomes lower when the input potential is high (refer to **8. TYPICAL CHARACTERISTICS**).

Therefore, when the input voltage is L, the current passed through the pull-up resistor is 25 $\mu$A MAX., and the power dissipation due to the input current is negligibly low.

Also, fix the $D_{IN}$ pin open or to H to minimize the power dissipation in Standby ($\overline{\text{STBY}}$ = L).

At this time, the input current is 1 $\mu$A or lower, and the power dissipation due to the input current through pull-up resistor is minimized.

## 7. NOTES FOR USE

The following items are general notes for using ICs for RS-232 line driver/receivers. They are common between the μPD471X Series and the μPD472X Series unless otherwise specified.

Power block

- If $V_{CC}$ is unstable, the on-chip DC/DC converter circuit may not properly operate. Therefore, it is recommended to connect a bypass capacitor (approximately 0.1 to 1 μF) between $V_{CC}$ and GND.
- Since $V_{DD}$ and $V_{SS}$ are output pins and their voltages are boosted up by the internal DC/DC converter circuit, do not feed or take out current to/from these pins (such as connecting any load). If any load is connected to these pins, the on-chip DC/DC converter circuit may not properly operate (refer to **12.2 Characteristics of Voltage Boosting Circuit** in **12. Q&A** for typical characteristics).

Pin treatment

- Fix all pins for control input (such as $D_{CON}$, $R_{CON}$, and STBY pins) to High or Low, if no pull-down resistor is connected to them.
- If a driver input pin is open, through current may flow. Fix all unconnected driver input pins to High or Low (for μPD471X Series).
- Ensure that voltage over rated voltage such as surge is not impressed to receiver input pins. If there is a possibility that the voltage higher than rated voltage is applied, it is recommended to connect an external protection circuit (refer to **12.5 Reliability** in **12. Q&A** for a typical application).

Selection of external capacitors

- Tantalum, aluminum electrolytic, and ceramic capacitors can be used for external capacitors for on-chip DC/DC converters. Since they are repeatedly charged and discharged by internal switching, use capacitors with better frequency characteristics.
- It is recommended to apply capacitors with a capacitance range of 4.7 to 47 μF (for the μPD471X Series, excepting the μPD4711B with capacitance range of 1 to 47 μF) and 0.33 to 4.7 μF (for the μPD472X Series, excepting μPD4722 with capacitance range of 0.47 to 4.7 μF). Determine appropriate capacitance within these ranges after evaluating with the actual product circuit. Note that the capacitance of electrolytic capacitors is lowered in low temperatures. Therefore, determine the capacitance of such capacitors with some margin taking into account the operating temperature.
- If only 5-V Mode ($V_{CHA}$ ="L" and $V_{CC}$ = 5 V) is used, it is not necessary to connect the $C_5$ capacitor. In this case, the $C_5$ pin should be left open (for μPD472X Series).

## 8. TYPICAL CHARACTERISTICS

The main characteristics of the μPD4722 as a representative product for RS-232 line driver/receivers are shown below.

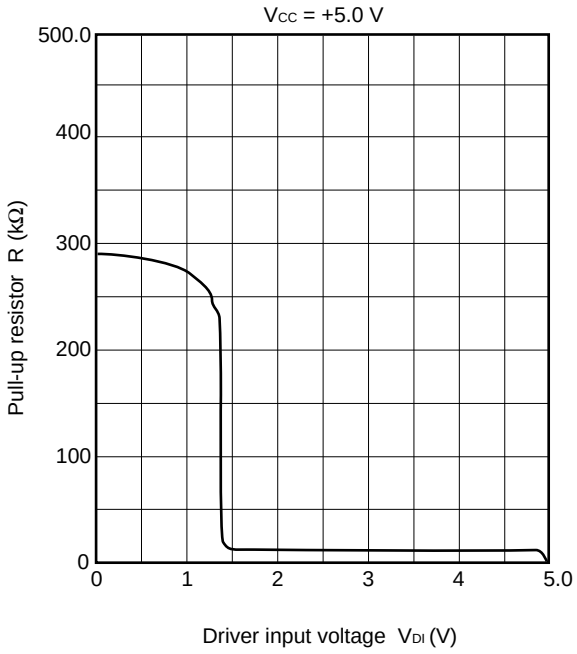
- Driver Input Characteristics
  The characteristics of a pull-up resistor (active resistor) at a driver input pin are shown below.
  (1) In 5-V Mode operation
  (2) In 3.3-V Mode operation

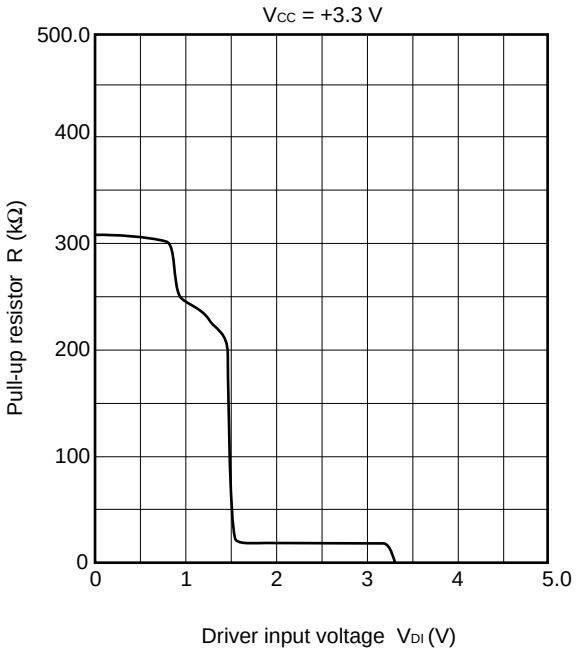
- Characteristics of Driver Output slew rate vs. load capacitance
  The slew rate characteristics when a load capacitance is connected to driver output 1 are shown below.
  Conditions: $V_{CC}$ = 5 V and 3.3 V
  External capacitor = 1.0 μF (Tantalum)
  $R_L$ = 3 kΩ (only at one output)
  Note that the slew rate characteristics are lower than the curve shown here if simultaneous switching for all outputs is performed.

- Characteristics of driver output voltage vs. output current
  The output characteristics with current at driver output are shown below.
  Conditions: $V_{CC}$ = 4.5 to 5.5 V and 3.0 to 3.6 V
  External capacitor = 0.47 μF
  With all driver outputs
  (1) Ceramic capacitors are used.
  (2) Tantalum capacitors are used.
  (3) Aluminum electrolytic capacitors are used.

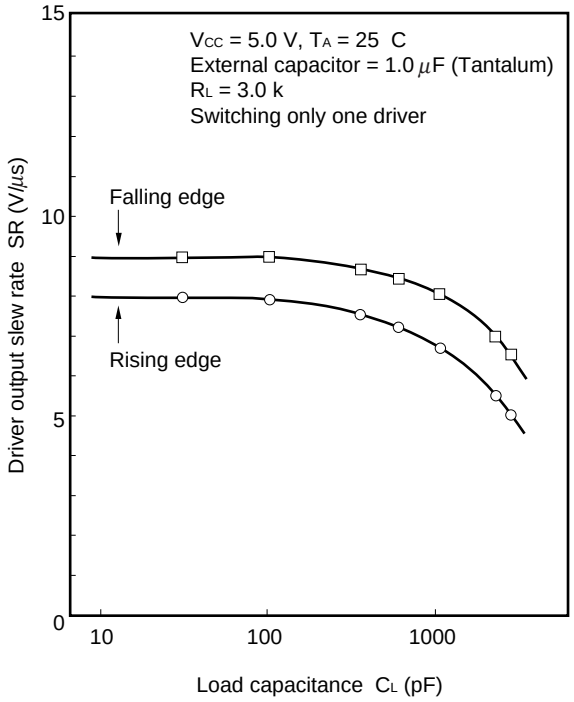
- Characteristics of driver output voltage vs. external capacitors
  The driver output characteristics when the capacitance of external capacitor is changed are shown below.
  Conditons: $V_{CC}$ = 4.5 V and 3.0 V
  Load 3 kΩ
  With all driver outputs

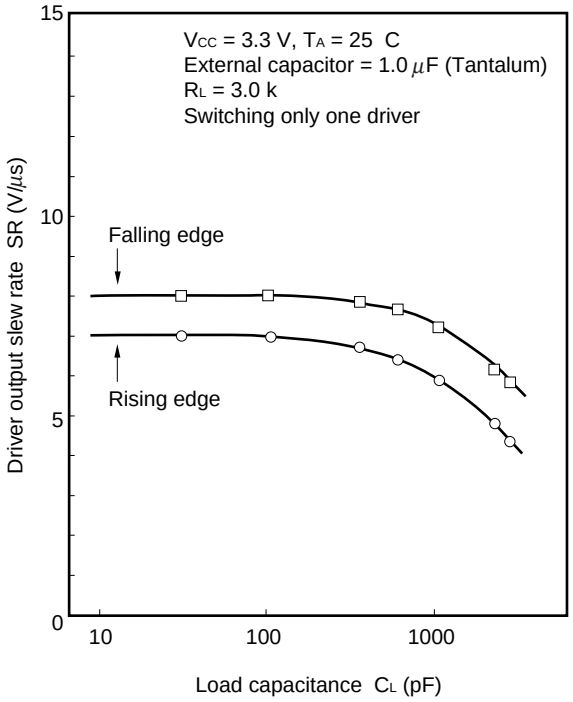
- Driver input characteristics




- Characteristics of driver output slew rate vs. load capacitance

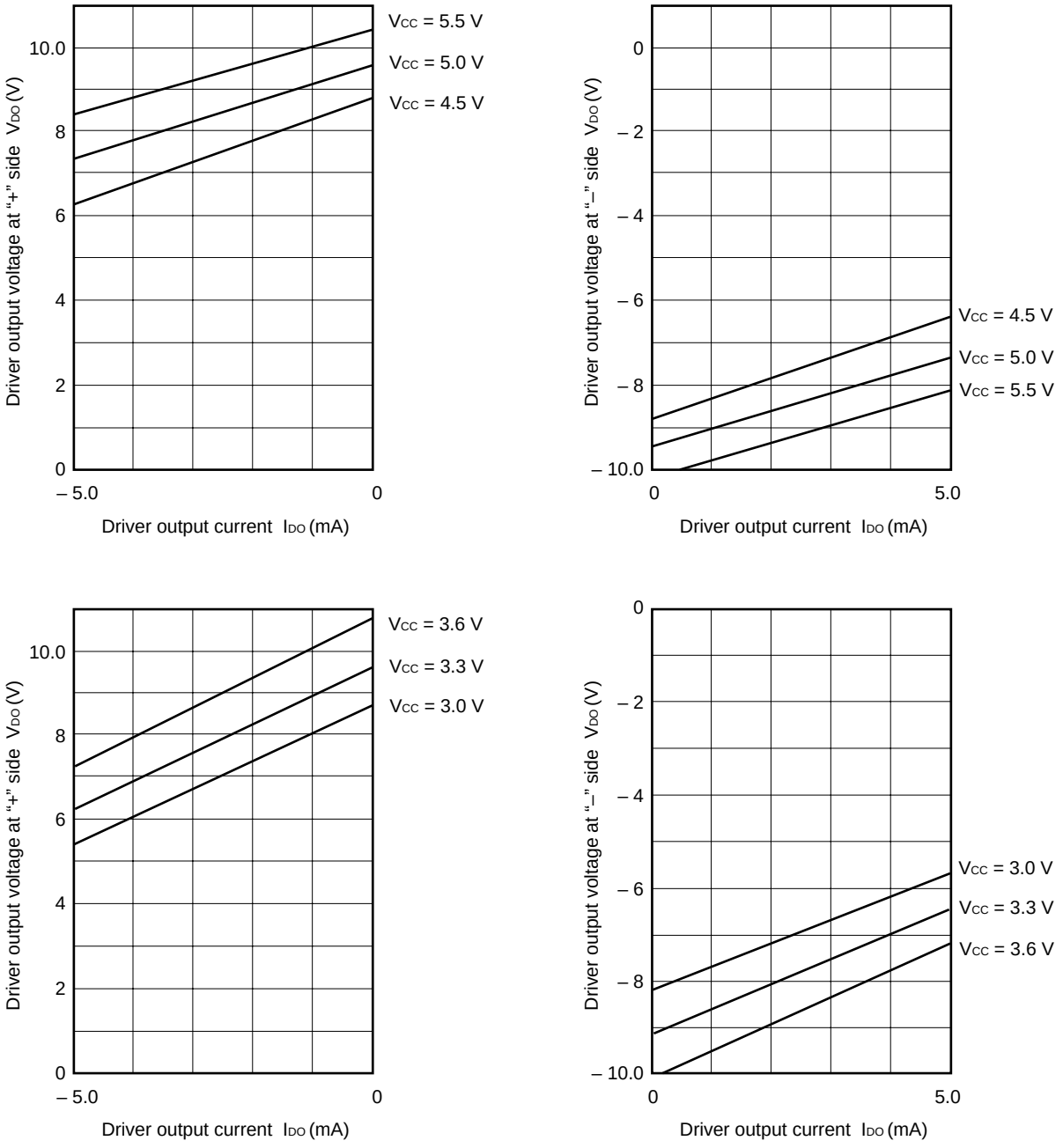


- Characteristics of driver output voltage vs. output current

(Ceramic capacitors used)

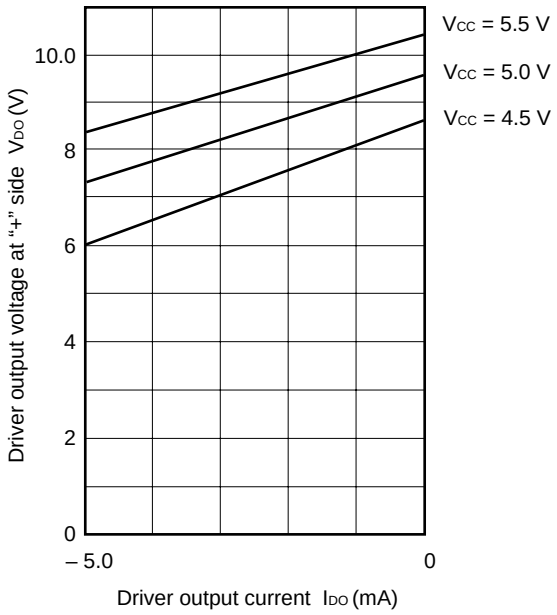
$C_1$ to $C_5$ = 0.47 $\mu$F: RPE123R474K50 manufactured by Murata Manufacturing Co., Ltd.

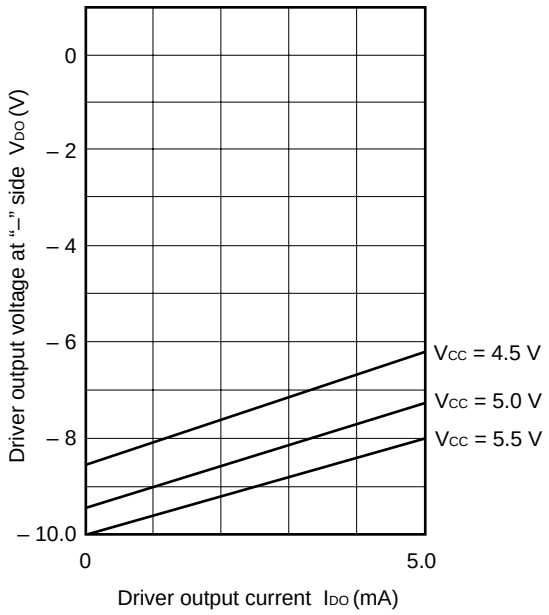


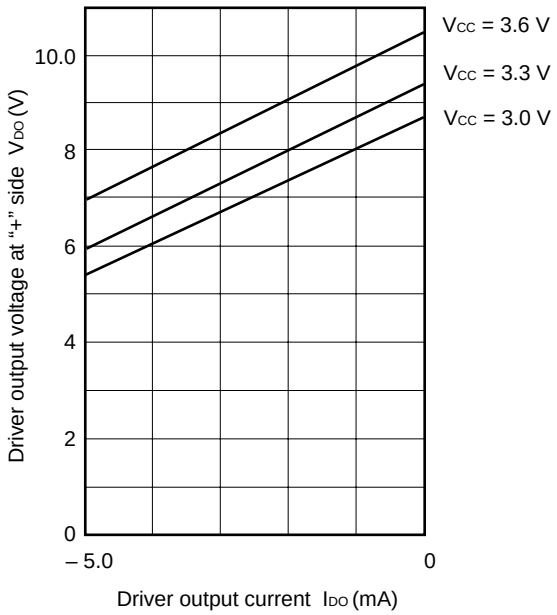
- Characteristics of driver output voltage vs. output current

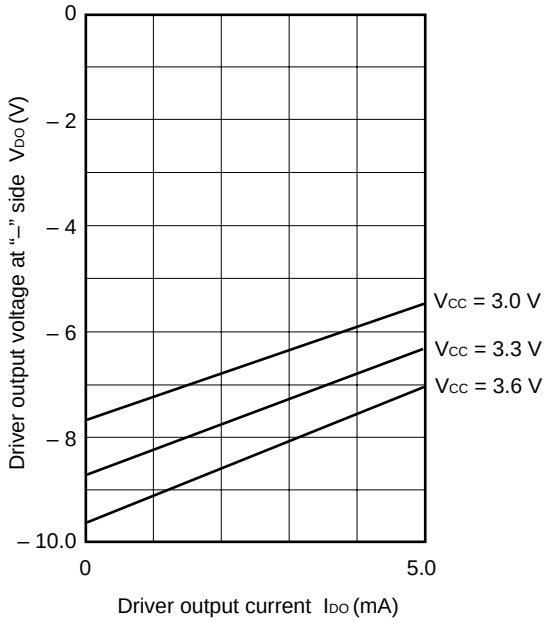
(Tantalum capacitors used)

$C_1$ to $C_5$ = 0.47 $\mu$F: S981V474MB1 manufactured by Nichicon



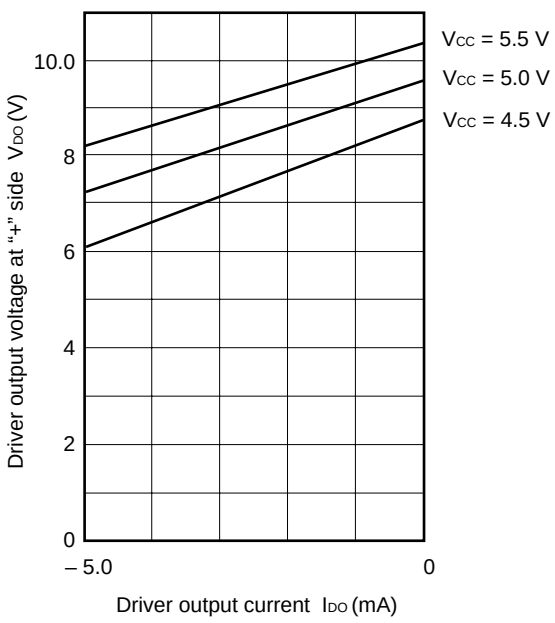



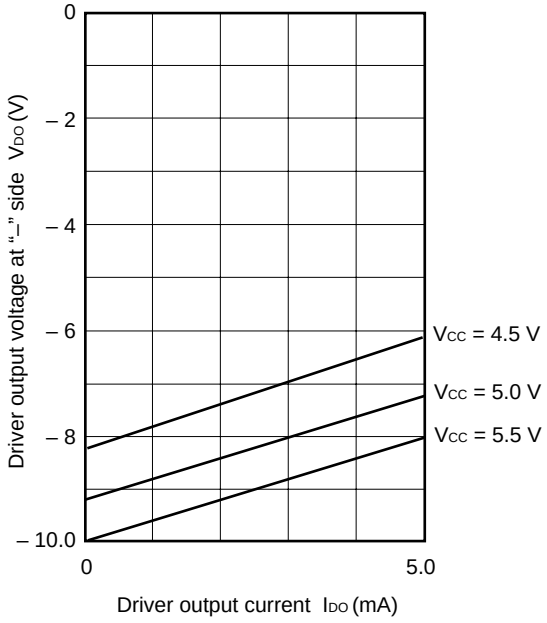



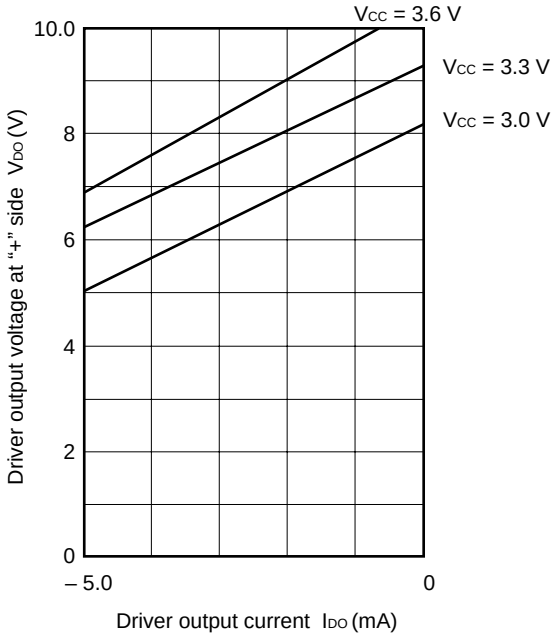
- Characteristics of driver output voltage vs. output current

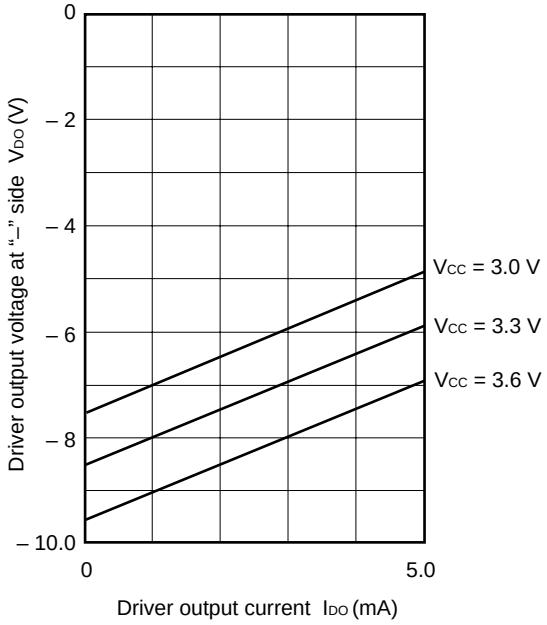
(Aluminum electrolytic capacitors used)

$C_1$ to $C_5$ = 0.47 $\mu$F: UVZ1HR47MDH manufactured by Nichicon



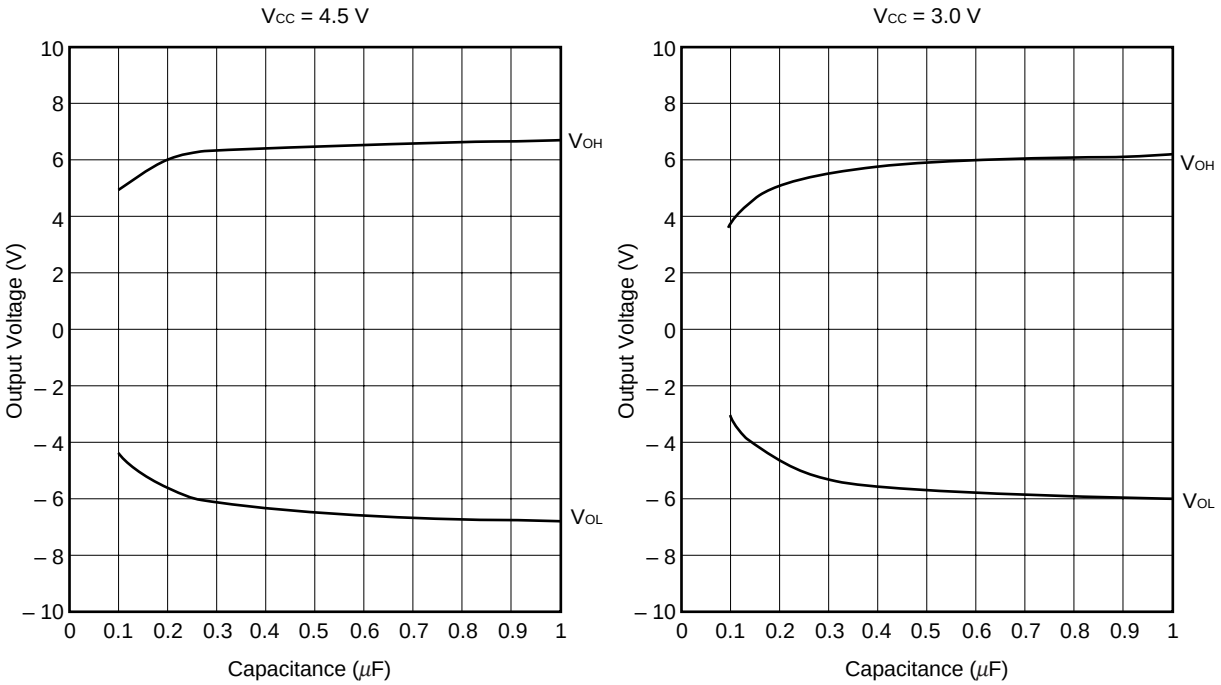



- Characteristics of driver output voltage vs. external capacitors

(Tantalum capacitors used)
$R_L$ = 3 kΩ, $T_A$ = 25°C
(With all driver outputs)



# 9. RS-232 STANDARD

## 9.1 What is the RS-232 Standard?

RS-232 is a standardized serial interface that defines the mechanical and electrical characteristics for connecting DTE (Data Terminal Equipment) and DCE (Data Communication Equipment) devices, and was developed by the EIA (Electrical Industries Association) in the U.S.A. This standard is generally called RS-232-C.

The official name of the standard is now “EIA/TIA-232-E”, but “RS-232-C” is used in this document, as this term is widely used.

RS-232-C specifies electrical specifications, types of signal cables and connector specifications, and is originally referred as an interface standard to connect modems and data pins (such as PC) to each other.

The main characteristics of RS-232-C are shown below.

**Characteristics of driver block**

| Item | Standard Value | Unit |
|---|---|---|
| Data transfer rate | Max.: 20 | kbps |
| Output voltage | Max.: ±15 (Unloaded) | V |
| Output voltage | Max.: ±5 (3 kΩ) | V |
| Slew rate | Max.: 30 | V/ns |

**Characteristics of receiver block**

| Item | Standard Value | Unit |
|---|---|---|
| Load capacitance | Max.: 2500[Note] | pF |
| Threshold voltage | Max.: ±3 | V |
| Input resistance | 3 to 7 | kΩ |
| Input voltage | Max.: ±25 | V |

**Note** Load capacitance is determined by type and length of signal cable and others, however, cable length is not specified in the standard.

## 9.2 Signal Level

Signal levels are specified in the RS-232-C standard.

| Status | Low | | High | |
|---|---|---|---|---|
| | Driver output | Receiver input | Driver output | Receiver input |
| Voltage level | –5 to –15 V | –3 to –25 V | +5 to +15 V | +3 to +25 V |
| Logical level | “1” (Mark level) | | “0” (Space level) | |

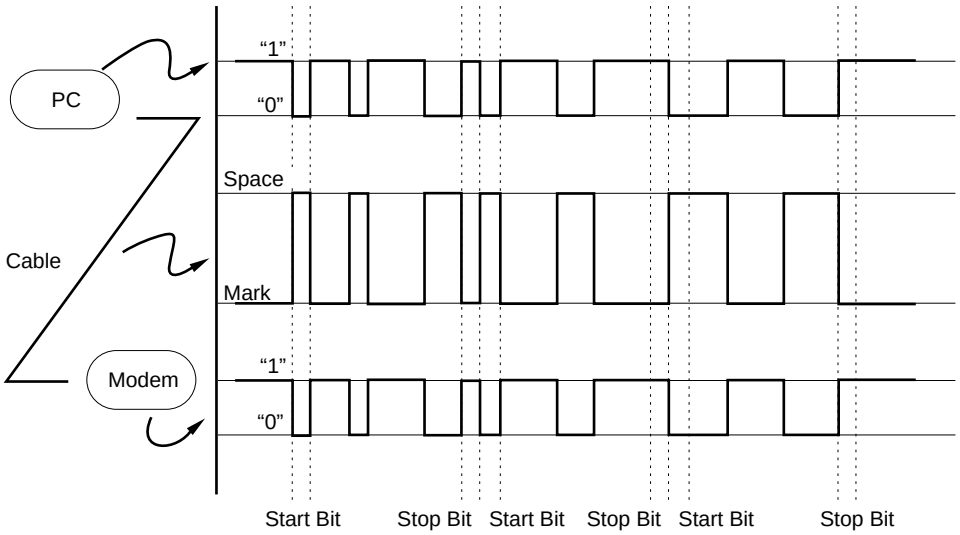
The signal levels in the cable are in negative logic, reversed from logical level, in the table above.

Therefore, an inverter must be inserted for a driver to output signals to the cable and a receiver must be inserted to input signals from the cable to match the internal logic (this is the role of ICs for RS-232 line driver/receivers).

Since there is a potential difference (2 V) between the driver output voltage and receiver input voltage, a noise margin or magnitude drop of up to 2 V is allowed.

## 9.3 Basics of RS-232-C Communication

The typical waveforms of 8-bit data transfer are shown below.




The following is defined in RS-232C communication.

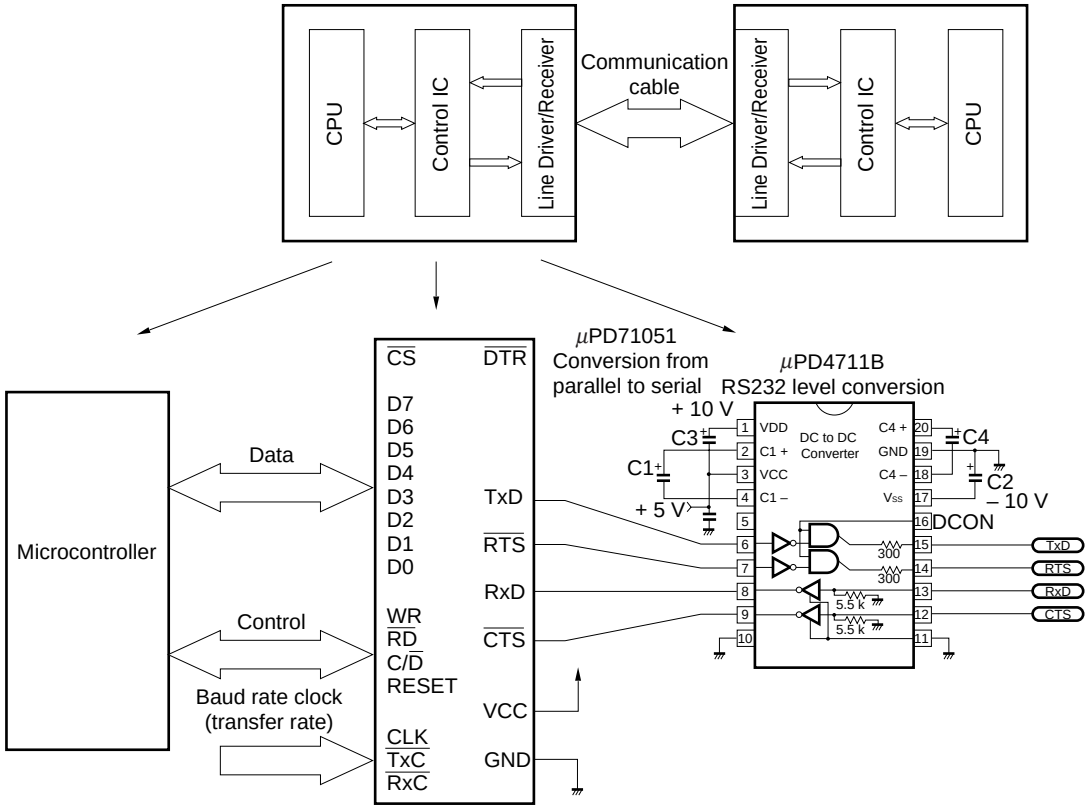
No Transfer (Idle) : Mark ("1")
Transfer Start (Start Bit) : Space ("0")
Transfer Stop (Stop Bit) : Mark ("1")

Transfer steps are as follows:

(1) In the Idle state, send Start Bit to start transfer.
(2) After data transfer is completed, send Stop Bit to stop transfer.
(3) If succeeding data is transferred, send Start Bit after Stop Bit again to transfer the data. The Idle state must be set for periods during which no data is transferred.

## 10. TYPICAL APPLICATION

A typical application for PC to modem communication or PC to PC communication is shown below.




The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

## 11. REVISION HISTORY OF PRODUCTS

The revision history of the μPD471X Series is shown below. Current part numbers are equivalent to discontinued part numbers on package, pin configurations, and characteristics. Therefore, customers who have been using discontinued part numbers of the μPD471X Series can use current products without modification of board circuits etc. However, operation checks for actual applications are necessary, because actual characteristics may differ.

| Part Number | Ordering Information (Discontinued) | Ordering Information (Current) | Reason of Modification |
|---|---|---|---|
| μPD4711 | μPD4711<br>μPD4711ACX/4711AGS | μPD4711B | Process integration due to standardization of design. |
| μPD4712 | μPD4712<br>μPD4712ACY/4712AGT<br>μPD4712BCY/4712BGT | μPD4712CCY/4712CGT<br>μPD4712DCY/4712DGT | |
| μPD4713 | μPD4713CX/4713GT | μPD4713ACX/4713AGT | |
| μPD4714 | μPD4714CY/4714GT | μPD4714ACY/4714AGT | |
| μPD4715 | μPD4715CY/4715GT | μPD4715ACY/4715AGT | |

The revision history of the μPD472X Series is shown below.

Current products are designed so as to raise the driven output performance, and as a result, the min. capacitance value for external capacitors is smaller. This reduction in capacitor capacitance may enable reduction of the circuit set size.

| Part Number | Production Category (Previous Standard) | Capacitance of External Capacitor | Production Category (Current Standard) | Capacitance of External Capacitor | Reason of Modification |
|---|---|---|---|---|---|
| μPD4721 | E | 1.0 to 4.7 μF | P | 0.33 to 4.7 μF | Capacitance of external capacitors is lowered due to improvement of driver output capability. |
| μPD4722 | | 1.0 to 4.7 μF | | 0.47 to 4.7 μF | |
| μPD4723 | | 1.0 to 4.7 μF | | 0.33 to 4.7 μF | |
| μPD4724 | | 1.0 to 4.7 μF | | 0.33 to 4.7 μF | |
| μPD4725 | – | – | E | 1.0 to 4.7 μF | (No modification) |

The term “current product” as used here refers to products as of May 1998.

## 12. Q&A

### 12.1 Internal Circuit Functions

Q. How is the $D_{CON}$ pin actually used? ($\mu$PD471X Series)

A. Idle state (No Transfer) is defined as Mark Level ("L" Output) in the RS-232 Standard. If driver input of the $\mu$PD471X may be unstable even if it is in Normal Operation Mode (not Standby), it can be fixed to Idle state making driver output level at Mark Level, using the $D_{CON}$ pin. This function can prevent output of abnormal signal (such as mis-recognition of the signal as Start Bit). (Refer to **6.1.2 Driver output logic**.)

Q. How is the $R_{CON}$ pin actually used? ($\mu$PD471X Series)

A. The space level voltage range is specified from –25 V to –3 V and the mark level voltage range is specified from +3 V to +25 V in the RS-232 Standard. Therefore, strictly speaking, the logic level is undefined when the cable signal is 0 V.

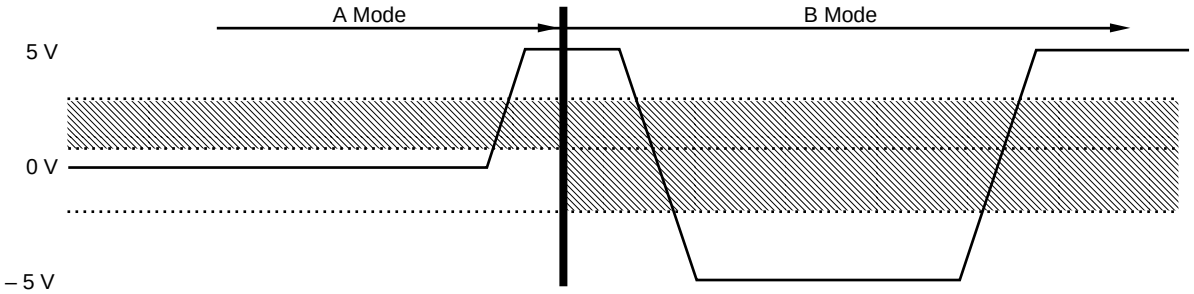
The input threshold voltage of the $\mu$PD471X Series can be switched using the $R_{CON}$ pin. The product has an A Mode, whereby the threshold voltage is set in positive, and a B Mode, whereby the threshold voltage is set in negative in order to prevent erroneous operations even if a 0-V signal is input.

If a signal with higher noise is input, a malfunction due to the smaller hysteresis width of A Mode occurs. In this case, B Mode must be used.

However, if a DC signal is output in a case such as when a control signal is transferred, signals of TTL level (0 to +5 V) may be easily handled. In this case, set the threshold voltage to the A mode so that signals can be recognized.

As described above, various signals can be flexibly handled by switching input threshold voltage depending on the purpose. The threshold voltage range is shown below. (Refer to **6.1.4 Receiver input threshold voltage**.)

**Receiver input threshold voltage range**




Shaded part indicates range of threshold voltage.

Q. How is the EN pin actually used? ($\mu$PD472X Series)

A. The products of the $\mu$PD472X Series (except for the $\mu$PD4721) have a mode by which receiver input can be accepted even if it is in the Standby state. This function allows the device to use the Wake-up function, which enables operation by receiving signals from the cable.

However, the receiver with the EN pin enabled has no hysteresis width in the Standby mode (the threshold voltage is typically 1.5 V). In this case, it is recommended to apply a filter circuit to prevent erroneous operation due to noise. (Refer to **6.2.3 Receiver output logic**.)

## 12.2 Characteristics of Boosting Circuit

Q. Receiver input threshold voltage exceeds the rated value.

A. $V_{DD}$ and $V_{SS}$ boosted by the internal DC/DC converter circuit are used for the receiver input threshold voltage. Therefore, the cause of abnormal receiver input threshold voltage may be erroneous operation of the DC/DC converter circuit. Refer to **Q. Voltage not boosted** in **12.2 Characteristics of Boosting Circuit** for measures to address improper operation of the DC/DC converter circuit.

Q. How long does it take for the DC/DC converter to switch?

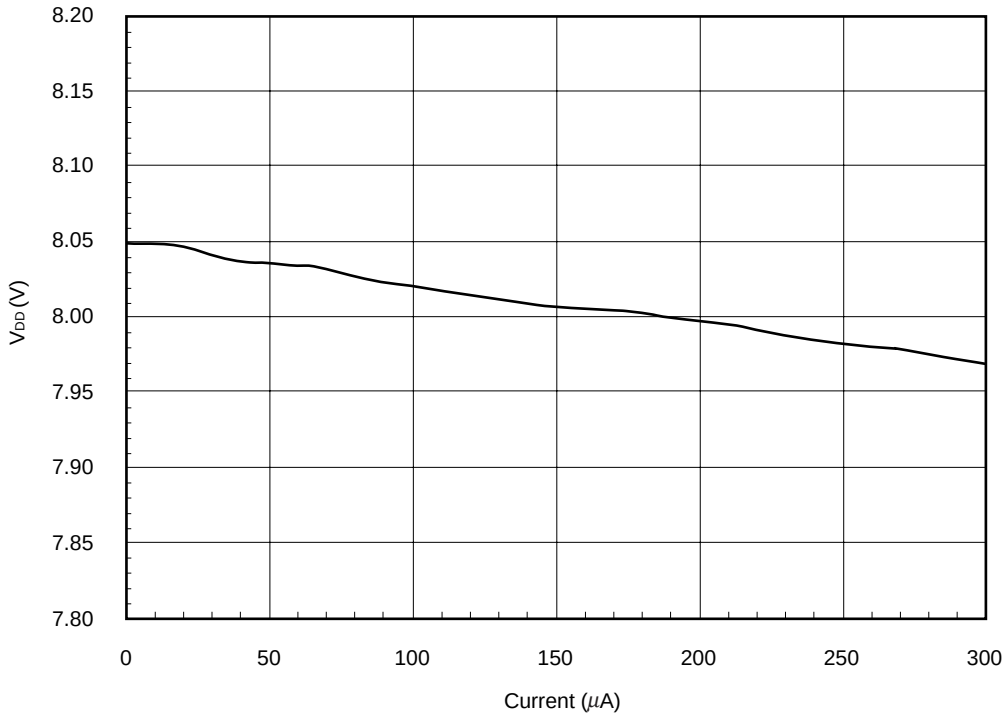
A. Switching time can be determined by measuring $C_1^+$, $C_1^-$, $C_4^+$, and $C_4^-$ with an oscilloscope or other device. It is designed so that the switching time is approximately 5 $\mu$s. However, the switching time is fairly changed depending on dispersions of internal Cs and Rs which determine the time constant. Dispersion of approximately half to double of the designed value should be taken into account.

Q. Can any current be taken out from the boosted power pins ($V_{DD}$ and $V_{SS}$)?

A. The boosted power pins are voltage output pins with voltages internally boosted. They are used for driver output, setting of receiver input threshold voltage or others. Therefore, do not directly connect any loads to these pins. Just for reference, a typical characteristic when current is taken out from the $V_{DD}$ pin of the $\mu$PD4721 is shown in the figure below. (Refer to **7. NOTE FOR USING**.)

**A typical characteristic of $V_{DD}$ vs. Takeout Current when current is taken out from $V_{DD}$**

(Conditions: $T_A$ = 25°C, $V_{CC}$ = 3.3 V, $C_1$ to $C_5$ = 0.33 $\mu$F, $D_{OUT}$ Full Load $R_L$ = 3 kΩ)



Q. Are there any problems if two ICs are used with one common capacitor?

A. DC/DC converters in the μPD471X Series and μPD472X Series are not designed expecting that two circuits are used with one common capacitor. In addition, because switching timings of capacitors cannot be externally synchronized, expected boosting operation cannot be achieved. Always use one capacitor for a single IC.

Q. Voltage not boosted.

A. There are several causes. Refer to the following measures.

1. Noise is superposed on the power supply pin.
   → Connect a bypass capacitor between $V_{CC}$ and GND for stabilizing. Locate the capacitor in the vicinity of the $V_{CC}$ pin to minimize the wiring length.
2. External voltage is applied to the driver output pin before the power is turned on.
   → Internal DC/DC converter circuit may not boost the voltage, if other voltage is applied to the driver output pin from external circuit before the power is turned on.
   Even if a different voltage within the rated value range is applied to the driver output pins, there is no operational problem if the IC is in operation. However, for functionality purposes, this IC is not designed expecting that another voltage will be applied to the driver output pins from an external circuit. Therefore, ensure that any other voltage is not applied to driver output pins from an external circuit.

### 12.3 External Capacitors

Q. What is the withstand voltage of external capacitors?

A. As specified in the data sheet, the following capacitors with specified withstand voltages are recommended.

| Series | Withstand Voltage of External Capacitor |
|---|---|
| μPD471X | 16 V |
| μPD472X | 20 V |

A maximum of 10 V is theoretically applied to an external capacitor as specified in the table in **DC/DC converter block** in Sections 6.1.1 and 6.2.1. However, since noise may be generated at switching, voltages with some margins (16 V or 20 V) are recommended.

Q. What kind of capacitor is recommended?

A. We have already confirmed that there are no problems in operation with the following capacitors after evaluation. As they are repeatedly charged and discharged by switching operation, use capacitors with better frequency characteristics.

| Capacitor Type | Model |
|---|---|
| Ceramic capacitor | RPE123R474K50<br>(Murata Manufacturing Co., Ltd.) |
| Tantalum capacitor | S981V474MB1 (Nichicon) |
| Aluminum electrolytic capacitors | UVZ1HR47MDH (Nichicon) |

(Refer to **8. TYPICAL CHARACTERISTICS** for capacitor characteristics.)

Q. What will happen if capacitors with polarity such as Tantalum capacitor are connected in reversed polarity?

A. If a capacitor with polarity is connected in the opposite direction from the connection diagram, the capacitor may be shorted.
Connect capacitors based on the connection diagram when connecting capacitors with polarity.
If the capacitor is shorted, refer to the next item “Q. Is the IC damaged if the capacitor is shorted?”

Q. Is the IC damaged if the capacitor is shorted?

A. High current may flow between $V_{DD}$ and $V_{CC}$ or between $V_{CC}$ and GND if the capacitor is shorted. This high current may destroy the capacitor. Absolute maximum rating of the input current on each pin of the μPD472X Series is specified as ±20 mA. Therefore, excessive current over this value may destroy capacitors.

### 12.4 Transfer Rate

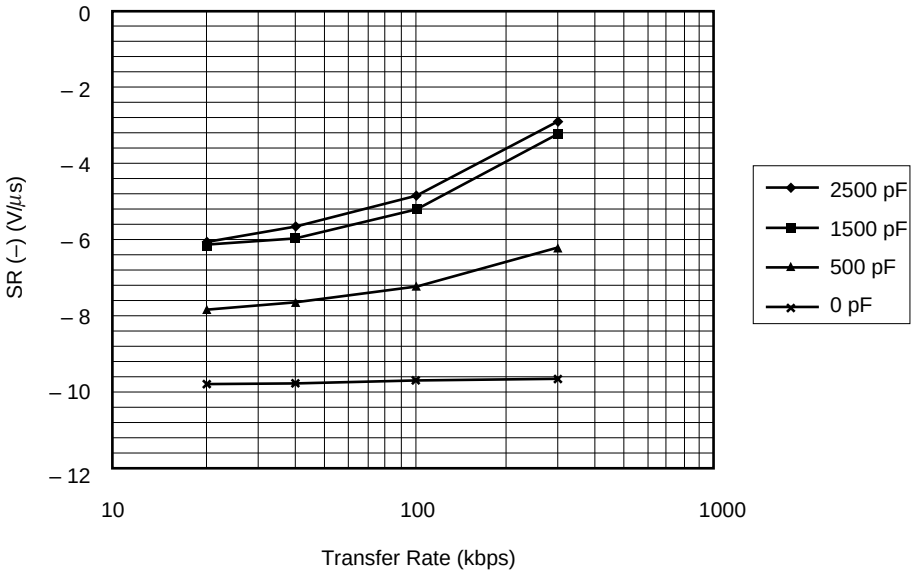
Q. Is the operation guaranteed when using a maximum transfer rate of 115 kbps?

A. The maximum transfer rate of the μPD471X Series and μPD472X Series is specified as 20 kbps. Therefore, their operation is not guaranteed with a transfer rate over 20 kbps.
The actual transfer rate depends on the driver output load (such as signal cable length). If they are used for applications with a lower load, such as when the cable length is extremely short, transfer with rate of over 20 kbps is potentially possible.
For your reference, actually measured values of slew rate and driver output voltage vs. transfer rate are shown on the following pages.

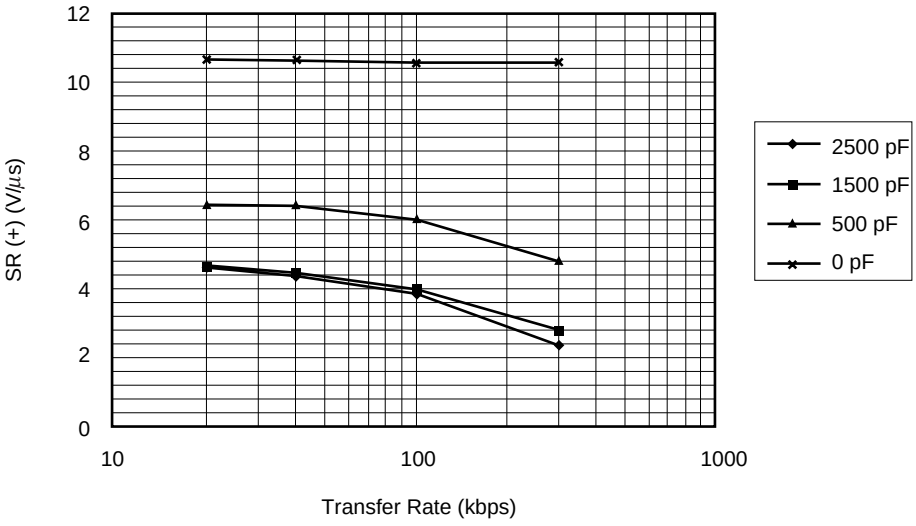
Measured on : $\mu$PD4722

Measuring conditions : $T_A$ = 25°C, $V_{CC}$ = 3 V, $C_1$ – $C_5$ = 1$\mu$F, $R_L$ = 3 k$\Omega$, with all drivers output

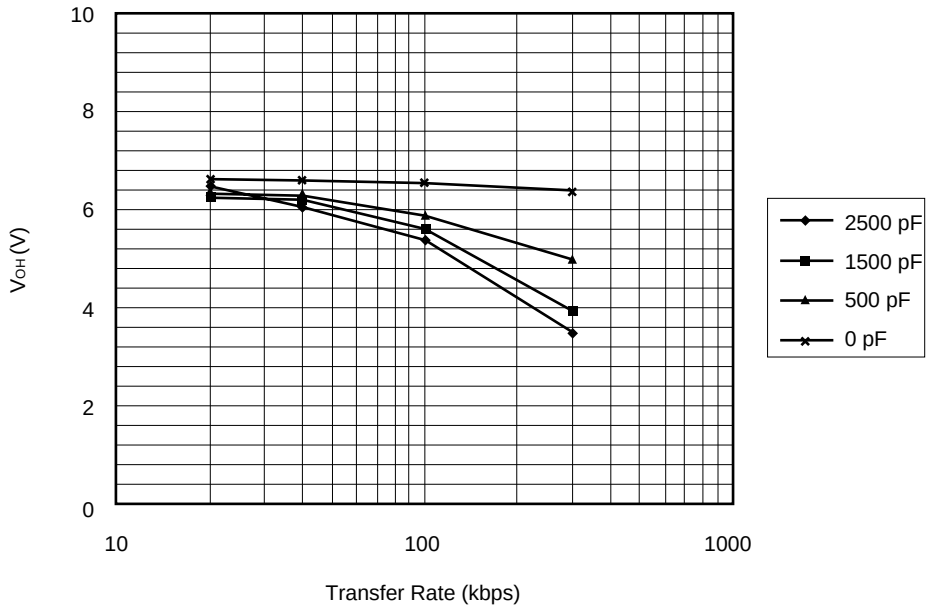
**Transfer rate - slew rate (at rising edge)**



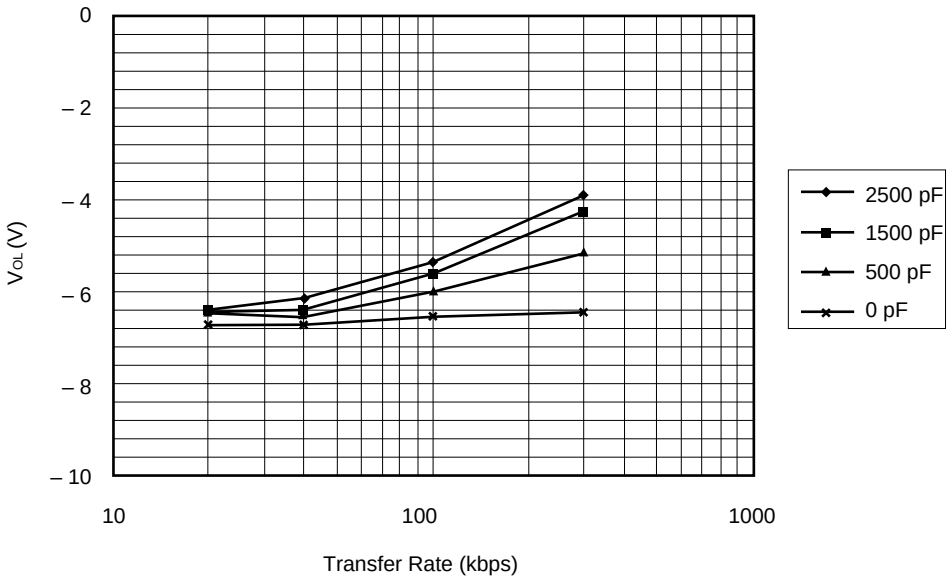

**Transfer rate - slew rate (at falling edge)**



**Transfer rate - driver output voltage (with output “H”)**




**Transfer rate - driver output voltage (with output “L”)**



## 12.5 Reliability

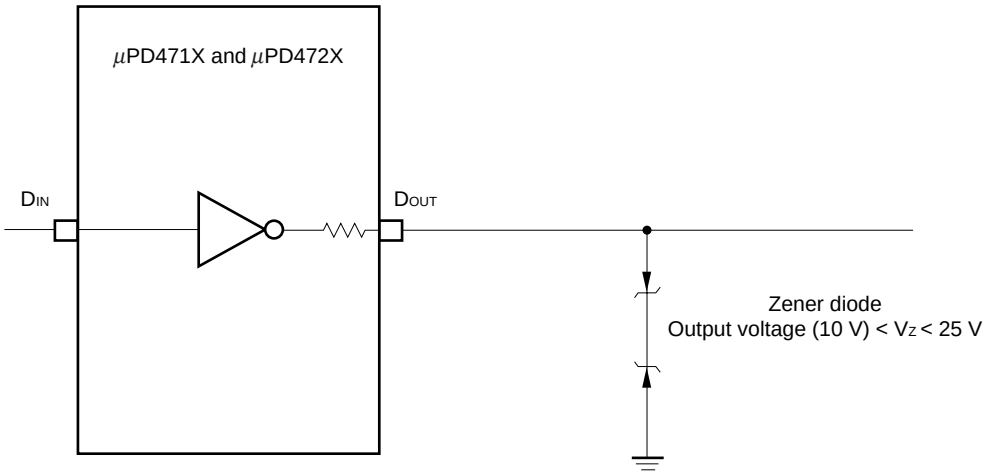
Q. What is ESD withstand voltage?

A. These series have passed the ESD (Electrostatic Discharge) test (MIL Method, ESD Test by EIAJ Method) defined by NEC. Confirm the measured values in the ESD test by obtaining the Result Report of Reliability Testing. Request it from Reliability and Quality Control Dept. through your NEC sales representative.

Q. How are ESD protection circuits configured?

A. A protection circuit for the driver output block can be configured with a combination of Zener diodes. A sample circuit for protection is shown below. $V_Z$ of the Zener diodes should be lower than the rated voltage of the driver output (25 V) and higher than the output voltage (up to 10 V).
(Refer to **7. NOTES FOR USING**.)

**Example of ESD Protection Circuit**




Q. What will happen if driver outputs of the transfer source and the transfer destination conflict with each other?

A. Over current between outputs may flow depending on the status of their driver outputs. For example, if the output of source is “H” and the output of destination is “L”, a high current flows from the source driver to the destination driver.
In this case, the internal DC/DC converter may not be able to properly boost the voltage, and erroneous operation may result.
Therefore, do not connect driver output pins to each other.

## 12.6 Equivalent Products of Other Companies

Q. Give me information on equivalent products of other companies.

A. Tables of products from other companies are shown below. Refer to those tables to find equivalent NEC products starting from the part number of products of other companies.

**Products operated with 5-V single power supply**

| Features | | NEC | Maxim | National Semiconductor | Harris | Linear Technology |
|---|---|---|---|---|---|---|
| Driver | Receiver | | | | | |
| 2 | 2 | μPD4711B | MAX202<br>MAX220<br>MAX222<br>MAX232/232A<br>MAX242 | | HIN202<br>HIN232 | LT1080<br>LT1081<br>LT1180<br>LT1181<br>LT1280<br>LT1281 |
| 3 | 3 | μPD4713A | | | | |
| 3 | 5 | μPD4714A | | DS14185<br>DS14C535 | | LT1327<br>LT1337<br>LT1338<br>LT1341 |
| 4 | 3 | | MAX206<br>MAX236 | | HIN206<br>HIN236 | |
| 4 | 4 | μPD4712C/D | MAX208<br>MAX238 | DS14C238 | HIN208<br>HIN238 | LT1134 |
| 4 | 5 | | MAX211<br>MAX213<br>MAX241 | DS14C241 | HIN211<br>HIN213 | LT1136 |
| 5 | 3 | μPD4715A | MAX207<br>MAX237 | DS14196 | HIN207<br>HIN237 | LT1132<br>LT1138 |
| 5 | 5 | | MAX240 | | HIN205 | LT1130 |

**Products operated with 3-V single power supply**

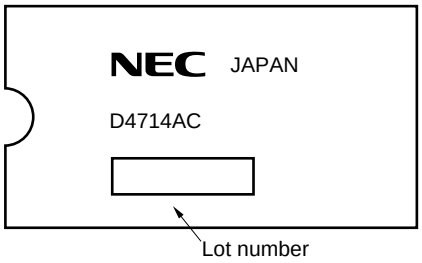
| Features | | NEC | Maxim | National Semiconductor | Harris | Linear Technology |
|---|---|---|---|---|---|---|
| Driver | Receiver | | | | | |
| 2 | 2 | μPD4721 | MAX563<br>MAX3222<br>MAX3232<br>MAX3223 | DS14C232 | | LTC1385<br>LTC1386 |
| 3 | 3 | μPD4723 | | | | |
| 3 | 5 | μPD4724 | MAX3212<br>MAX3243 | DS14C335 | | LT1331<br>LTC1348 |
| 4 | 4 | μPD4722 | | | | |
| 4 | 5 | | MAX560<br>MAX561 | | | |
| 4 | 7 | μPD4726 | | | | |

## 12.7 Marking, Packages and Others

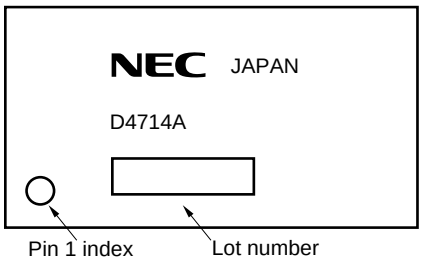
Q. Give me information on current marking.

A. The markings of the μPD4714A and μPD4722 (on May 1998) are shown below.

**DIP package (μPD4714ACY: μPD471X Series)**

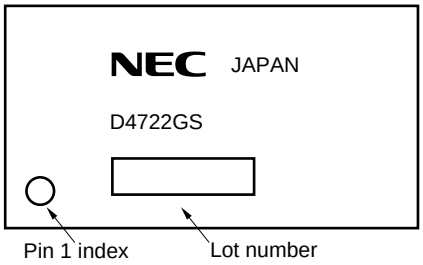



**SOP package (μPD4714AGT: μPD471X Series)**




Only μPD4711BGX has different marking for part number.
Part number: D4711BG

**SSOP package (μPD4722GS-GJG: μPD472X Series)**




Only marking of product name of μPD4721GX-GJG is different from others.
Part number: D4721

Q. Give me information on the packaged quantity in a magazine and a reel

A. Refer to the **SEMICONDUCTORS SELECTION GUIDE** (X13769X) for details on magazines and reels. The packaged quantities of each part number and package type is shown in the table below.

**DIP package (magazine)**

| Part Number | Packaged Quantity |
|---|---|
| μPD4711BCX | 18 |
| μPD4712CCY/DCY | 13 |
| μPD4713ACX | 15 |
| μPD4714ACY | 13 |
| μPD4715ACY | 13 |

**SOP package (adhesive taping)**

| Part Number | Packaged Quantity |
|---|---|
| μPD4711BGS | 1500 |
| μPD4712CGT/DGT | |
| μPD4713AGT | |
| μPD4714AGT | |
| μPD4715AGT | |

**SOP package (embossed taping)**

| Part Number | Packaged Quantity | Taping Specification |
|---|---|---|
| μPD4711BGS | 2500 | 24 mm width tape |
| μPD4712CGT/DGT | 1500 | |
| μPD4713AGT | | |
| μPD4714AGT | | |
| μPD4715AGT | | |

**SSOP package**

| Part Number | Packaged Quantity | Taping Specification |
|---|---|---|
| μPD4721GS-GJG | 2500 | 16 mm width tape |
| μPD4722GS-GJG | | |
| μPD4723GS-GJG | | |
| μPD4724GS-GJG | | |
| μPD4726GS-GJG | | 24 mm width tape |

## APPENDIX ELECTRICAL SPECIFICATIONS

The typical electrical specifications of the μPD471X Series and μPD472X Series are shown in the tables below. Refer to the relevant document for details.

### Appendix 1. Main Characteristics of μPD471X Series (Ex.: μPD4714A)

**Electrical specifications (common)** (Unless otherwise specified, $V_{CC}$ = +5 V ± 10%, $T_A$ = –20 to +80°C, $C_1$ to $C_5$ = 22 μF)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Circuit current | $I_{CC1}$ | $V_{CC}$ = +5 V, No load, $R_{IN}$ pin open, (STBY pin open) | | 7.0 | 18.0 | mA |
| Circuit current | $I_{CC2}$ | $V_{CC}$ = +5 V, $R_L$ = 3 kΩ ($D_{OUT}$), $D_{IN}$ = GND, $R_{IN}$, $R_{OUT}$ pin open (STBY pin open) | | 23.0 | 40.0 | mA |
| Circuit current at standby | $I_{CC}$ (Standby) | $V_{CC}$ = +5 V, No load, $R_{IN}$ pin open (STBY pin high) | | 50 | 120 | μA |
| Standby high level input voltage | $V_{IH}$ (Standby) | | 2.0 | | | V |
| Standby low level input voltage | $V_{IL}$ (Standby) | | | | 0.8 | V |

**Electrical specifications (driver)** (Unless otherwise specified, $V_{CC}$ = +5 V ± 10%, $T_A$ = –20 to +80°C, $C_1$ to $C_5$ = 22 μF)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low-level input voltage | $V_{IL}$ | | | | 0.8 | V |
| High-level input voltage | $V_{IH}$ | | 2.0 | | | V |
| Low-level input current | $I_{IL}$ | | 0 | | –1.0 | μA |
| High-level input current | $I_{IH}$ | | 0 | | 1.0 | μA |
| Output voltage | $V_{DO}$ | $V_{CC}$ = +5.0 V, $R_L$ = ∞, $T_A$ = 25°C | | ±9.7 | | V |
| | | $V_{CC}$ = +5.0 V, $R_L$ = 3 kΩ | ±5.5 | | | V |
| | | $V_{CC}$ = +4.5 V, $R_L$ = 3 kΩ | ±5.0 | | | V |
| Output short-circuit current | $I_{SC}$ | $V_{CC}$ = +5.0 V, from GND | | ±15 | ±40 | mA |
| Slew rate | SR | $C_L$ = 10 pF, $R_L$ = 3 to 7 kΩ | 1.5 | 9 | 30 | V/μs |
| | | $C_L$ = 2500 pF, $R_L$ = 3 to 7 kΩ | 1.5 | 5 | 30 | V/μs |
| Transfer delay time | $t_{PHL}$ $t_{PLH}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 0.8 | | μs |
| Output resistance | $R_O$ | $V_{CC}$ = $V_{DD}$ = $V_{SS}$ = 0 V, $V_{OUT}$ = ±2 V | 300 | 500 | | Ω |
| Standby output transition time | $t_{DAZ}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 4 | 10 | μs |
| Standby output transition time | $t_{DZA}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 25 | 50 | ms |

**Electrical specifications (receiver)** (Unless otherwise specified, $V_{CC}$ = +5 V ± 10%, $T_A$ = –20 to +80°C, $C_1$ to $C_5$ = 22 μF)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low-level output voltage | $V_{OL}$ | $I_{OUT}$ = 4 mA | | | 0.4 | V |
| High-level output voltage | $V_{OH}$ | $I_{OUT}$ = –4 mA | $V_{CC}$ – 0.8 | | | V |
| Low-level input voltage | $V_{OL}$ | $R_{CON}$ pin | | | 0.8 | V |
| High-level input voltage | $V_{OH}$ | $R_{CON}$ pin | 2.0 | | | V |
| Propagation delay time | $t_{PHL}$<br>$t_{PLH}$ | $R_L$ = 1 kΩ, $C_L$ = 150 pF | | 0.13 | | μs |
| Input resistance | $R_I$ | | 3 | 5 | 7 | kΩ |
| Input open circuit voltage | $V_{IO}$ | Input threshold A mode only. | | | 0.5 | V |
| Threshold A mode ($R_{CON}$ pin Low) | $V_{IH}$ | $V_{CC}$ = +5 V | 1.7 | 2.3 | 2.7 | V |
| | $V_{IL}$ | $V_{CC}$ = +5 V | 0.7 | 1.1 | 1.7 | V |
| | $V_H$ | $V_{CC}$ = +5 V (Hysteresis width) | 0.5 | 1.2 | 1.8 | V |
| Threshold B mode ($R_{CON}$ pin High) | $V_{IH}$ | $V_{CC}$ = +5 V | 1.6 | 2.2 | 2.6 | V |
| | $V_{IL}$ | $V_{CC}$ = +5 V | –0.4 | –1.8 | –3.0 | V |
| | $V_H$ | $V_{CC}$ = +5 V (Hysteresis width) | 2.6 | 4.0 | 5.4 | V |
| Standby output transition time | $t_{DAZ}$ | | | 0.4 | 1 | μs |
| Standby output transition time | $t_{DZA}$ | | | 1.0 | 10 | ms |

## Appendix 2. Main Characteristics of μPD472X Series (Ex.: μPD4724)

**Electrical specifications (common)** (Unless otherwise specified, $T_A$ = –40 to +85°C, $C_1$ to $C_5$ = 1 μF)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Circuit current | $I_{CC1}$ | $V_{CC}$ = +3.3 V, No load, $R_{IN}$ pin open, $\overline{STBY}$ = H | | 7.5 | 15 | mA |
| | | $V_{CC}$ = +5.0 V, No load, $R_{IN}$ pin open, $\overline{STBY}$ = H | | 5.5 | 11 | mA |
| Circuit current | $I_{CC2}$ | $V_{CC}$ = +3.3 V, $R_L$ = 3 kΩ ($D_{OUT}$), $D_{IN}$ = GND, $R_{IN}$, $R_{OUT}$ pin open, $\overline{STBY}$ = H | | 25 | 35 | mA |
| | | $V_{CC}$ = +5.0 V, $R_L$ = 3 kΩ ($D_{OUT}$), $D_{IN}$ = GND, $R_{IN}$, $R_{OUT}$ pin open, $\overline{STBY}$ = H | | 19 | 28 | mA |
| Circuit current at standby (Standby mode 1) | $I_{CC3}$ | $V_{CC}$ = +3.3 V, No load, $D_{IN}$, $R_{IN}$ pin open $\overline{STBY}$ = L, EN = L, $T_A$ = 25°C | | 1 | 3 | μA |
| | | $V_{CC}$ = +5.0 V, No load, $D_{IN}$, $R_{IN}$ pin open $\overline{STBY}$ = L, EN = L, $T_A$ = 25°C | | 2 | 5 | μA |
| Circuit current at standby (Standby mode 2) | $I_{CC4}$ | $V_{CC}$ = +3.3 V, No load, $D_{IN}$, $R_{IN}$ pin open $\overline{STBY}$ = L, EN = H, $T_A$ = 25°C | | 1 | 3 | μA |
| | | $V_{CC}$ = +5.0 V, No load, $D_{IN}$, $R_{IN}$ pin open $\overline{STBY}$ = L, EN = H, $T_A$ = 25°C | | 2 | 5 | μA |
| High-level input voltage | $V_{IH}$ | $V_{CC}$ = +3.0 to +5.5 V, $\overline{STBY}$, $V_{CHA}$, EN pin | 2.4 | | | V |
| Low-level input voltage | $V_{IL}$ | $V_{CC}$ = +3.0 to +5.5 V, $\overline{STBY}$, $V_{CHA}$, EN pin | | | 0.6 | V |

**Electrical specifications (driver)** (Unless otherwise specified, $T_A$ = –40 to +85°C, $C_1$ to $C_5$ = 1 μF)

**3-V mode** (Unless otherwise specified, $V_{CHA}$ = H, $V_{CC}$ = 3.0 to 3.6 V)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low-level input voltage | $V_{IL}$ | | | | 0.8 | V |
| High-level input voltage | $V_{IH}$ | | 2.0 | | | V |
| Low-level input current | $I_{IL}$ | $V_{CC}$ = +3.6 V, $V_I$ = 0 V | | | –25 | μA |
| High-level input current | $I_{IH}$ | $V_{CC}$ = +3.6 V, $V_I$ = +3.6 V | | | 1.0 | μA |
| Output voltage | $V_{DO}$ | $V_{CC}$ = +3.3 V, $R_L$ = ∞, $T_A$ = 25°C | | ±9.5 | | V |
| | | $V_{CC}$ = +3.3 V, $R_L$ = 3 kΩ | ±5.0 | ±6.0 | | V |
| | | $V_{CC}$ = +3.0 V, $R_L$ = 3 kΩ, $T_A$ = 25°C | ±5.0 | | | V |
| Output short-circuit current | $I_{SC}$ | $V_{CC}$ = +3.3 V, from GND | | | ±40 | mA |
| Slew rate | SR | $C_L$ = 10 pF, $R_L$ = 3 to 7 kΩ | 3.0 | | 30 | V/μs |
| | | $C_L$ = 2500 pF, $R_L$ = 3 to 7 kΩ | 3.0 | | 30 | V/μs |
| Transfer delay time | $t_{PHL}$ $t_{PLH}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 2.5 | | μs |
| Output resistance | $R_O$ | $V_{CC}$ = $V_{DD}$ = $V_{SS}$ = 0 V, $V_{OUT}$ = ±2 V | 300 | | | Ω |
| Standby output transition time | $t_{DAZ}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 4 | 10 | μs |
| Standby output transition time | $t_{DZA}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 1 | 3 | ms |
| Power on output transition time | $t_{PRA}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 1 | 3 | ms |

**Electrical specifications (driver)** (Unless otherwise specified, $T_A$ = –40 to +85°C, $C_1$ to $C_5$ = 1 μF)

**5-V mode** (Unless otherwise specified, $V_{CHA}$ = L, $V_{CC}$ = 5.0 V ±10%)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low-level input voltage | $V_{IL}$ | | | | 0.8 | V |
| High-level input voltage | $V_{IH}$ | | 2.0 | | | V |
| Low-level input current | $I_{IL}$ | $V_{CC}$ = +5.5 V, $V_I$ = 0 V | | | –40 | μA |
| High-level input current | $I_{IH}$ | $V_{CC}$ = +5.5 V, $V_I$ = +5.5 V | | | 1.0 | μA |
| Output voltage | $V_{DO}$ | $V_{CC}$ = +5.0 V, $R_L$ = ∞, $T_A$ = 25°C | | ±9.7 | | V |
| | | $V_{CC}$ = +5.0 V, $R_L$ = 3 kΩ | ±6.0 | | | V |
| | | $V_{CC}$ = +4.5 V, $R_L$ = 3 kΩ | ±5.0 | | | V |
| Output short-circuit current | $I_{SC}$ | $V_{CC}$ = +5.0 V, from GND | | | ±40 | mA |
| Slew rate | SR | $C_L$ = 10 pF, $R_L$ = 3 to 7 kΩ | 4.0 | | 30 | V/μs |
| | | $C_L$ = 2500 pF, $R_L$ = 3 to 7 kΩ | 4.0 | | 30 | V/μs |
| Transfer delay time | $t_{PHL}$<br>$t_{PLH}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 2 | | μs |
| Output resistance | $R_O$ | $V_{CC}$ = $V_{DD}$ = $V_{SS}$ = 0 V, $V_{OUT}$ = ±2 V | 300 | | | Ω |
| Standby output transition time | $t_{DAZ}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 4 | 10 | μs |
| Standby output transition time | $t_{DZA}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 0.5 | 1 | ms |
| Power on output transition time | $t_{PRA}$ | $R_L$ = 3 kΩ, $C_L$ = 2500 pF | | 0.5 | 1 | ms |

**Electrical specifications (receiver)** (Unless otherwise specified, $V_{CC}$ = 3.0 to 5.5 V, $T_A$ = –40 to +85°C, $C_1$ to $C_5$ = 1 μF)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low level-output voltage | $V_{OL1}$ | $I_{OUT}$ = 4 mA, $\overline{STBY}$ = H | | | 0.4 | V |
| High level-output voltage | $V_{OH1}$ | $I_{OUT}$ = –4 mA, $\overline{STBY}$ = H | $V_{CC}$ – 0.4 | | | V |
| Low level-output voltage | $V_{OL2}$ | $I_{OUT}$ = 4 mA, $\overline{STBY}$ = L | | | 0.5 | V |
| High level-output voltage | $V_{OH2}$ | $I_{OUT}$ = –4 mA, $\overline{STBY}$ = L | $V_{CC}$ – 0.5 | | | V |
| Transfer delay time ($\overline{STBY}$ = H) | $t_{PHL}$<br>$t_{PLH}$ | $R_{IN}$ → $R_{OUT}$, $C_L$ = 150 pF, $V_{CC}$ = +3.0 V | | 0.2 | | μs |
| Transfer delay time ($\overline{STBY}$ = L) | $t_{PHL}$<br>$t_{PLH}$ | $R_{IN}$ → $R_{OUT}$, $C_L$ = 150 pF, $V_{CC}$ = +3.0 V | | 0.1 | | μs |
| Transfer delay time ($\overline{STBY}$ = L) | $t_{PHA}$<br>$t_{PAH}$ | $R_{IN}$ → $R_{OUT}$, $C_L$ = 150 pF, $V_{CC}$ = +3.0 V | | 100 | 300 | ns |
| Input resistance | $R_I$ | | 3 | 5.5 | 7 | kΩ |
| Input open circuit voltage | $V_{IO}$ | | | | 0.5 | V |
| Threshold ($\overline{STBY}$ = H) | $V_{IH}$ | $V_{CC}$ = +3.0 to +5.5 V | 1.7 | 2.3 | 2.7 | V |
| | $V_{IL}$ | $V_{CC}$ = +3.0 to +5.5 V | 0.7 | 1.1 | 1.7 | V |
| | $V_H$ | $V_{CC}$ = +3.0 to +5.5 V (Hysteresis width) | 0.5 | 1.2 | 1.8 | V |
| Threshold ($\overline{STBY}$ = L, EN = H) | $V_{IH}$ | $V_{CC}$ = +3.0 to +5.5 V, $R_{IN4}$, $R_{IN5}$ | 2.7 | 1.5 | | V |
| | $V_{IL}$ | $V_{CC}$ = +3.0 to +5.5 V, $R_{IN4}$, $R_{IN5}$ | | 1.5 | 0.7 | V |
| Standby output transition time | $t_{DAH}$ | | | 0.2 | 3 | μs |
| Standby output transition time | $t_{DHA}$ | $V_{CHA}$ = H (3-V mode) | | 0.6 | 3 | ms |
| | | $V_{CHA}$ = L (5-V mode) | | 0.3 | 1 | ms |
| Power on reset release time | $t_{PRA}$ | $V_{CHA}$ = H (3-V mode) | | 1 | 3 | ms |
| | | $V_{CHA}$ = L (5-V mode) | | 0.5 | 1 | ms |

**[MEMO]**

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