DATA SHEET

TDA8004T
IC card interface

Product specification
Supersedes data of 1997 Nov 21
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

IC card interface TDA8004T

FEATURES

- 3 or 5 V supply for the IC (GND and V_{DD})
- Step-up converter for V_{CC} generation (separately powered with a 5 V ±10% supply, V_{DDP} and PGND)
- 3 specific protected half duplex bidirectional buffered I/O lines (C4, C7 and C8)
- V_{CC} regulation 5 V ±5% on 2 × 100 nF or 1 × 100 nF and 1 × 220 nF multilayer ceramic capacitors with low ESR, I_{CC} < 65 mA at 4.5 V < V_{DDP} < 6.5 V, current spikes of 40 nAs up to 20 MHz, with controlled rise and fall times, filtered overload detection approximately 90 mA)
- Thermal and short-circuit protections on all card contacts
- Automatic activation and deactivation sequences (initiated by software or by hardware in the event of a short-circuit, card take-off, overheating or supply drop-out)
- Enhanced ESD protection on card side (>6 kV)
- 26 MHz integrated crystal oscillator
- Clock generation for the card up to 20 MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals)
- Non-inverted control of RST via pin RSTIN
- ISO 7816, GSM11.11 and EMV (payment systems) compatibility
- Supply supervisor for spikes killing during power-on and power-off
- One multiplexed status signal $\overline{OFF}$.

APPLICATIONS

- IC card readers for banking
- Electronic payment
- Identification
- Pay TV.

GENERAL DESCRIPTION

The TDA8004T is a complete low cost analog interface for asynchronous smart cards. It can be placed betw the card and the microcontroller with very few external components to perform all supply protection and control functions.

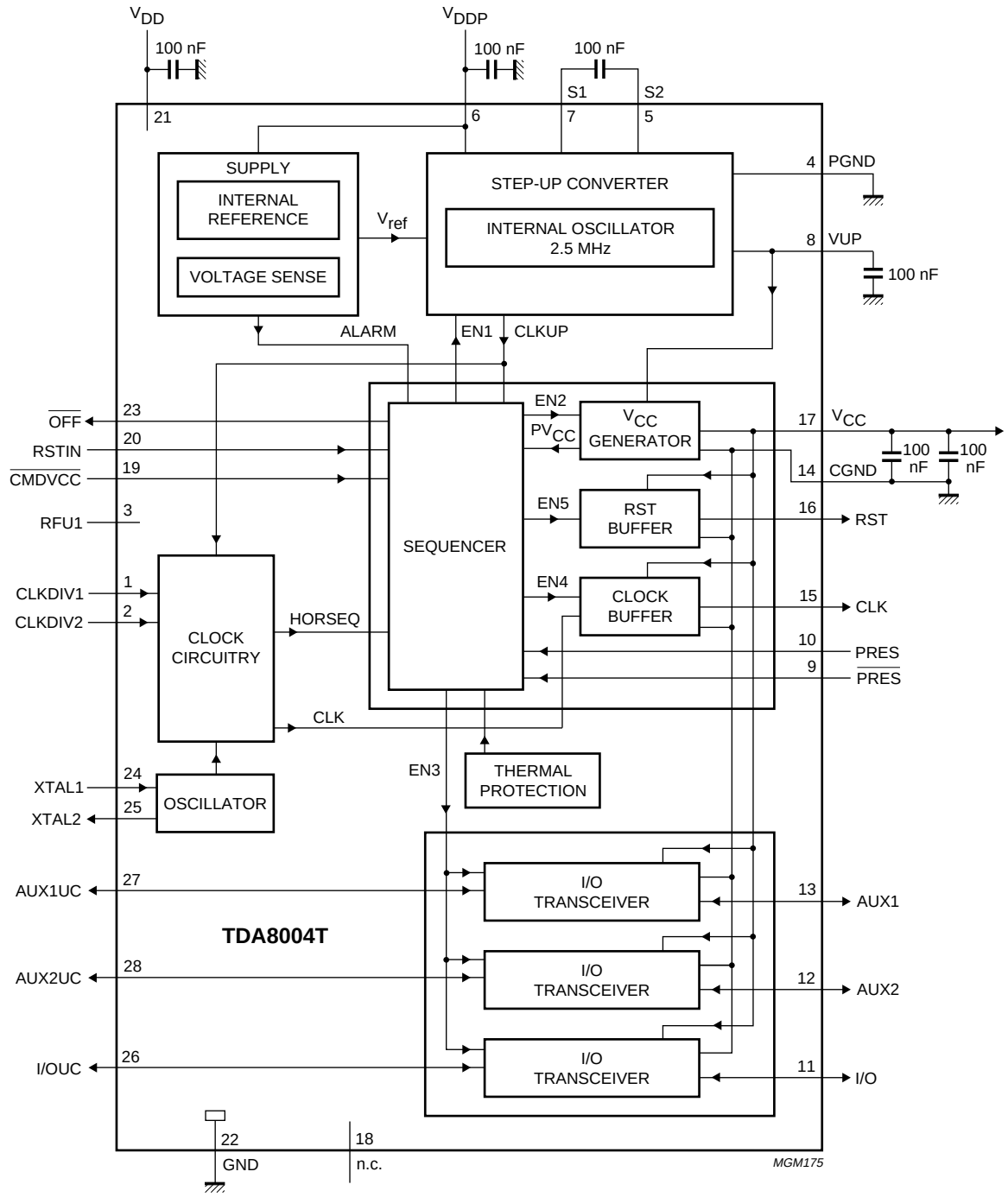
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8004T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.7	–	6.5	V
V_{DDP}	step-up supply voltage		4.5	5	6.5	V
I_{DD}	supply current	inactive mode; V_{DD} = 3.3 V; f_{XTAL} = 10 MHz	–	–	1.2	mA
		active mode; V_{DD} = 3.3 V; f_{XTAL} = 10 MHz; no load	–	–	1.5	mA
I_{DDP}	step-up supply current	inactive mode; V_{DDP} = 5 V; f_{XTAL} = 10 MHz	–	–	0.1	mA
		active mode; V_{DDP} = 5 V; f_{XTAL} = 10 MHz; no load	–	–	18	mA
Card supply						
V_{CC}	card supply voltage including ripple	DC $\lvert I_{CC}\rvert$ < 65 mA	4.75	–	5.25	V
		AC current spikes of 40 nAs	4.65	–	5.25	V
$V_{i(ripple)(p-p)}$	ripple voltage on V_{CC} (peak-to-peak value)	20 kHz ≤ f ≤ 200 MHz	–	–	350	mV
$\lvert I_{CC}\rvert$	card supply current	V_{CC} from 0 to 5 V	–	–	65	mA
General						
f_{CLK}	card clock frequency		0	–	20	MHz
t_{de}	deactivation cycle duration		60	80	100	µs
P_{tot}	continuous total power dissipation	T_{amb} = –25 to +85 °C	–	–	0.56	W
T_{amb}	ambient temperature		–25	–	+85	°C

BLOCK DIAGRAM



All capacitors are mandatory.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLKDIV1	1	I	control with CLKDIV2 for choosing CLK frequency
CLKDIV2	2	I	control with CLKDIV1 for choosing CLK frequency
RFU1	3	I	reserved for future use (to be connected to V_{DD} or microcontroller I/O; active HIGH)
PGND	4	supply	power ground for step-up converter
S2	5	I/O	capacitance connection for step-up converter (a 100 nF capacitor with ESR < 100 mΩ must be connected between pins S1 and S2)
V_{DDP}	6	supply	power supply voltage for step-up converter
S1	7	I/O	capacitance connection for step-up converter (a 100 nF capacitor with ESR < 100 mΩ must be connected between pins S1 and S2)
VUP	8	I/O	output of step-up converter (a 100 nF capacitor with ESR < 100 mΩ must be connected to PGND)
$\overline{PRES}$	9	I	card presence contact input (active LOW); if PRES or $\overline{PRES}$ is true, then the card is considered as present
PRES	10	I	card presence contact input (active HIGH); if PRES or $\overline{PRES}$ is true, then the card is considered as present
I/O	11	I/O	data line to and from card (C7) (internal 10 kΩ pull-up resistor connected to V_{CC})
AUX2	12	I/O	auxiliary line to and from card (C8) (internal 10 kΩ pull-up resistor connected to V_{CC})
AUX1	13	I/O	auxiliary line to and from card (C4) (internal 10 kΩ pull-up resistor connected to V_{CC})
CGND	14	supply	ground for card signals
CLK	15	O	clock to card (C3)
RST	16	O	card reset (C2)
V_{CC}	17	O	Supply for card (C1); decouple to CGND with 2 × 100 nF or 1 × 100 nF and 1 × 220 nF capacitors with ESR < 100 mΩ (with 220 nF, the noise margin on V_{CC} will be higher).
n.c.	18	–	not connected
$\overline{CMDVCC}$	19	I	start activation sequence input from microcontroller (active LOW)
RSTIN	20	I	card reset input from microcontroller (active HIGH)
V_{DD}	21	supply	supply voltage
GND	22	supply	ground
$\overline{OFF}$	23	O	NMOS interrupt to microcontroller (active LOW) with 20 kΩ internal pull-up resistor connected to V_{DD} (refer section “Fault detection”)
XTAL1	24	I	crystal connection or input for external clock
XTAL2	25	O	crystal connection (leave open if an external clock source is used)
I/OUC	26	I/O	microcontroller data I/O line (internal 10 kΩ pull-up resistor connected to V_{DD})
AUX1UC	27	I/O	auxiliary line to and from microcontroller (internal 10 kΩ pull-up resistor connected to V_{DD})
AUX2UC	28	I/O	auxiliary line to and from microcontroller (internal 10 kΩ pull-up resistor connected to V_{DD})

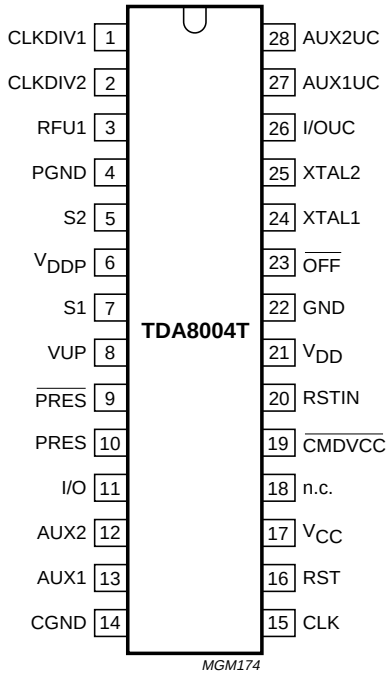


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Throughout this document, it is assumed that the reader is familiar with ISO 7816 norm terminology.

Power supply

The supply pins for the IC are V_{DD} and GND. V_{DD} should be in the range from 2.7 to 6.5 V. All interface signals with the system controller are referenced to V_{DD}; so, be sure the supply voltage of the system controller is also V_{DD}. All card contacts remain inactive during powering up or powering down. The sequencer is not activated until V_{DD} reaches $V_{th2} + V_{hys(th2)}$ (see Fig.3). When V_{DD} falls below V_{th2}, an automatic deactivation of the contacts is performed.

For generating a 5 V ±5% V_{CC} supply to the card, an integrated voltage doubler is incorporated. This step-up converter should be separately supplied by V_{DDP} and PGND (from 4.5 to 6.5 V). Due to large transient currents, the 2×100 nF capacitors of the step-up converter should have an ESR less than 100 mΩ and be located as near as possible to the IC.

The supply voltages V_{DD} and V_{DDP} may be applied to the IC in any time sequence.

If a voltage between 7 and 9 V is available within the application, this voltage may be tied to pin VUP, thus blocking the step-up converter. In this case, V_{DDP} must be tied to V_{DD} and the capacitor between pins S1 and S2 may be omitted.

Voltage supervisor

This block surveys the V_{DD} supply. A defined reset pulse of approximately 10 ms (t_W) is used internally for maintaining the IC in the inactive mode during powering up or powering down of V_{DD} (see Fig.3).

As long as V_{DD} is less than $V_{th2} + V_{hys(th2)}$, the IC will remain inactive whatever the levels on the command lines. This also lasts for the duration of t_W after V_{DD} has reached a level higher than $V_{th2} + V_{hys(th2)}$.

The system controller should not try to start an activation during this time.

When V_{DD} falls below V_{th2}, a deactivation sequence of the contacts is performed.

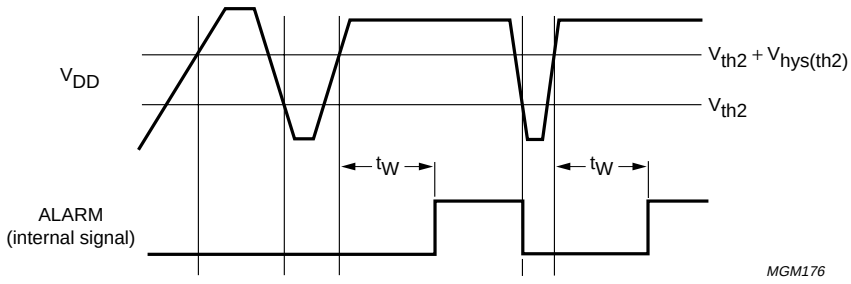


Fig.3 ALARM as a function of V_{DD} (t_W = 10 ms).

Clock circuitry

The clock signal (CLK) to the card is either derived from a clock signal input on pin XTAL1 or from a crystal up to 26 MHz connected between pins XTAL1 and XTAL2.

The frequency may be chosen at f_{XTAL}, $\frac{1}{2}f_{XTAL}$, $\frac{1}{4}f_{XTAL}$ or $\frac{1}{8}f_{XTAL}$ via pins CLKDIV1 and CLKDIV2.

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45% of the smallest period and that the first and last clock pulse around the change has the correct width.

In the case of f_{XTAL}, the duty factors are dependent on the signal at XTAL1.

In order to reach a 45% to 55% duty factor on pin CLK the input signal on XTAL1 should have a duty factor of 48% to 52% and transition times of less than 5% of the input signal period.

If a crystal is used with f_{XTAL}, the duty factor on pin CLK may be 45% to 55% depending on the layout and on the crystal characteristics and frequency.

In the other cases, it is guaranteed between 45% and 55% of the period.

The crystal oscillator runs as soon as the IC is powered up. If the crystal oscillator is used, or if the clock pulse on XTAL1 is permanent, then the clock pulse will be applied to the card according to the timing diagram of the activation sequence (see Fig.5).

If the signal applied to XTAL1 is controlled by the system controller, then the clock pulse will be applied to the card when the system controller will send it (after completion of the activation sequence).

Table 1 Clock circuitry definition

CLKDIV1	CLKDIV2	CLK
0	0	$\frac{1}{8}f_{XTAL}$
0	1	$\frac{1}{4}f_{XTAL}$
1	1	$\frac{1}{2}f_{XTAL}$
1	0	f_{XTAL}

I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

The Idle state is realized by both lines (I/O and I/OUC) being pulled HIGH via a 10 kΩ resistor (I/O to V_{CC} and I/OUC to V_{DD}).

I/O is referenced to V_{CC} and I/OUC to V_{DD}, thus allowing operation with $V_{CC} \neq V_{DD}$.

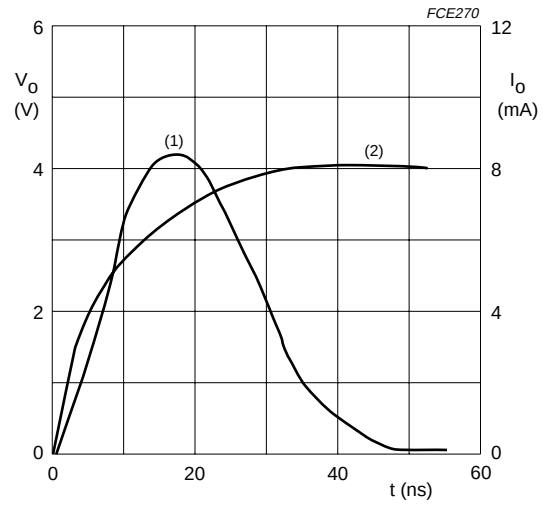
The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes a slave.

After a time delay $t_{d(edge)}$ (approximately 200 ns), the N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side returns to logic 1, the P transistor on the slave side is turned on during the time delay $t_{d(edge)}$ and then both sides return to their Idle states.

This active pull-up feature ensures fast LOW-to-HIGH transitions; it is able to deliver more than 1 mA up to an output voltage of $0.9V_{CC}$ on a 80 pF load. At the end of the active pull-up pulse, the output voltage only depends on the internal pull-up resistor and on the load current (see Fig.4).

The maximum frequency on these lines is 1 MHz.



(1) Current.
(2) Voltage.

Fig.4 I/O, AUX1, and AUX2 output voltage and current as a function of time during a LOW-to-HIGH transition.

Inactive state

After power-on reset, the circuit enters the inactive state. A minimum number of circuits are active while waiting for the microcontroller to start a session.

- All card contacts are inactive (approximately 200 Ω to GND)
- I/OUC, AUX1UC and AUX2UC are high impedance (10 kΩ pull-up resistor connected to V_{DD})
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active.

Activation sequence

After power-on and after the internal pulse width delay, the system controller may check the presence of the card with the signal $\overline{OFF}$ ($\overline{OFF}$ = HIGH while $\overline{CMDVCC}$ is HIGH means that the card is present; $\overline{OFF}$ = LOW while $\overline{CMDVCC}$ is HIGH means that no card is present).

If the card is in the reader (which is the case if $\overline{PRES}$ or PRES is true), the system controller may start a card session by pulling $\overline{CMDVCC}$ LOW.

The following sequence then occurs (see Fig.5):

- $\overline{CMDVCC}$ is pulled LOW (t_0)
- The voltage doubler is started ($t_1 \sim t_0$)
- V_{CC} rises from 0 to 5 V with a controlled slope ($t_2 = t_1 + \frac{1}{2}3T$) (I/O, AUX1 and AUX2 follow V_{CC} with a slight delay)
- I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 4T$)
- CLK is applied to the C3 contact (t_4)
- RST is enabled ($t_5 = t_1 + 7T$).

In the timing informations above and below, T is 64 times the period of the internal oscillator, about 25 μs.

The clock may be applied to the card in the following way:

- Set RSTIN HIGH before setting $\overline{CMDVCC}$ LOW and reset it LOW between t_3 and t_5; CLK will start at this moment. RST will remain LOW until t_5, where RST is enabled to be the copy of RSTIN. After t_5, RSTIN has no further action on CLK. This is to allow a precise count of CLK pulses before toggling RST.

If this feature is not needed, then $\overline{CMDVCC}$ may be set LOW with RSTIN LOW. In this case, CLK will start at t_3 and after t_5, RSTIN may be set HIGH in order to get the Answer To Request (ATR) from the card.

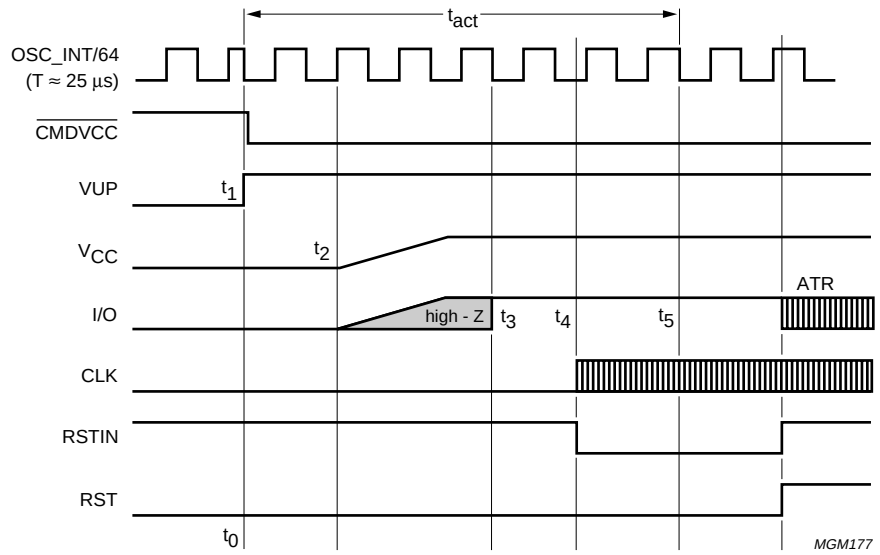


Fig.5 Activation sequence.

Active state

When the activation sequence is completed, the TDA8004T will be in the active state. Data is exchanged between the card and the microcontroller via the I/O lines. The TDA8004T is designed for cards without V_{PP} (this is the voltage required to program or erase the internal non-volatile memory).

Depending on the layout and on the application test conditions (for example with an additional 1 pF cross capacitance between C2/C3 and C2/C7) it is possible that C2 is polluted with high frequency noise from C3. In this case, it will be necessary to connect a 220 pF capacitance between C2 and CGND.

It is recommended to:

1. Keep track C3 as far as possible from other tracks
2. Have straight connection between CGND and C5 (the 2 capacitors on C1 should be connected to this ground track)
3. Avoid ground loops between CGND, PGND and GND
4. Decouple V_{DDP} and V_{DD} separately; if the 2 supplies are the same in the application, then they should be connected in star on the main track.

With all these layout precautions, noise should be at an acceptable level and jitter on C3 should be less than 100 ps. Refer to *Application Note AN97036* for specimen layouts

Deactivation sequence

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see Fig.6):

- RST goes LOW → ($t_{11} = t_{10}$)
- CLK is stopped LOW → ($t_{12} = t_{11} + ½T$)
- I/O, AUX1 and AUX2 are output into high-impedance state → ($t_{13} = t_{11} + T$); 10 kΩ pull-up resistor connected to V_{CC}
- V_{CC} falls to zero → ($t_{14} = t_{11} + ½3T$); the deactivation sequence is completed when V_{CC} reaches its inactive state
- VUP falls to zero → ($t_{15} = t_{11} + 5T$) and all card contacts become low-impedance to GND; I/OUC, AUX1UC and AUX2UC remain pulled up to V_{DD} via a 10 kΩ resistor.

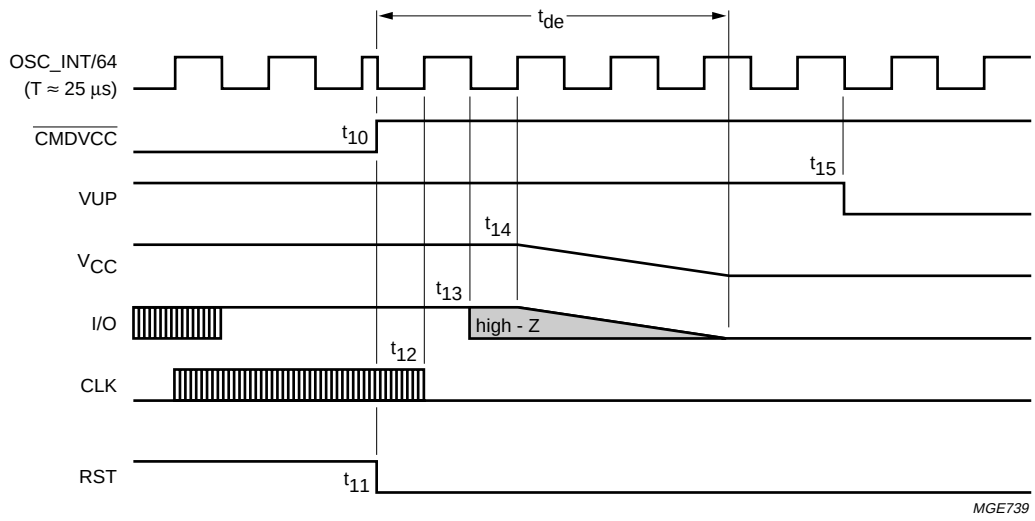


Fig.6 Deactivation sequence.

Fault detection

The following fault conditions are monitored by the circuit:

- Short-circuit or high current on V_{CC}
- Removing card during transaction
- V_{DD} dropping
- Overheating.

There are two different cases (see Fig.7):

1. $\overline{\text{CMDVCC}}$ HIGH: (outside a card session) then, $\overline{\text{OFF}}$ is LOW if the card is not in the reader and HIGH if the card is in the reader. A supply voltage drop on V_{DD} is detected by the supply supervisor, generates an internal power-on reset pulse, but don't act upon $\overline{\text{OFF}}$. The card is not powered-up, so no short-circuit or overheating is detected.
2. $\overline{\text{CMDVCC}}$ LOW: (within a card session) then, $\overline{\text{OFF}}$ falls LOW if the card is extracted, or if a short-circuit has occurred on V_{CC}, or if the temperature on the IC has become too high. As soon as the fault is detected, an emergency deactivation is automatically performed (see Fig.8).

   When the system controller sets $\overline{\text{CMDVCC}}$ back to HIGH, it may sense $\overline{\text{OFF}}$ again in order to distinguish between a hardware problem or a card extraction. If a supply voltage drop on V_{DD} is detected whilst the card is activated, then an emergency deactivation will be performed, but $\overline{\text{OFF}}$ remains HIGH.

Depending on the type of card presence switch within the connector (normally closed or normally open) and on the mechanical characteristics of the switch, a bouncing may occur on presence signals at card insertion or withdrawal.

There is no debounce feature in the device, so the software has to take it into account; however, the detection of card take off during active phase, which initiates an automatic deactivation sequence is done on the first true/false transition on PRES or $\overline{\text{PRES}}$ and is memorized until the system controller sets $\overline{\text{CMDVCC}}$ HIGH.

So, the software may take some time waiting for presence switches to be stabilized without causing any delay on the necessary fast and normalized deactivation sequence.

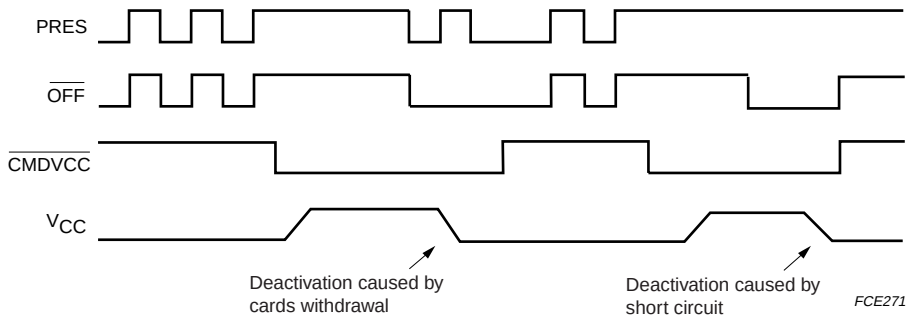


Fig.7 Behaviour of $\overline{OFF}$, $\overline{CMDVCC}$, PRES and V_{CC}.

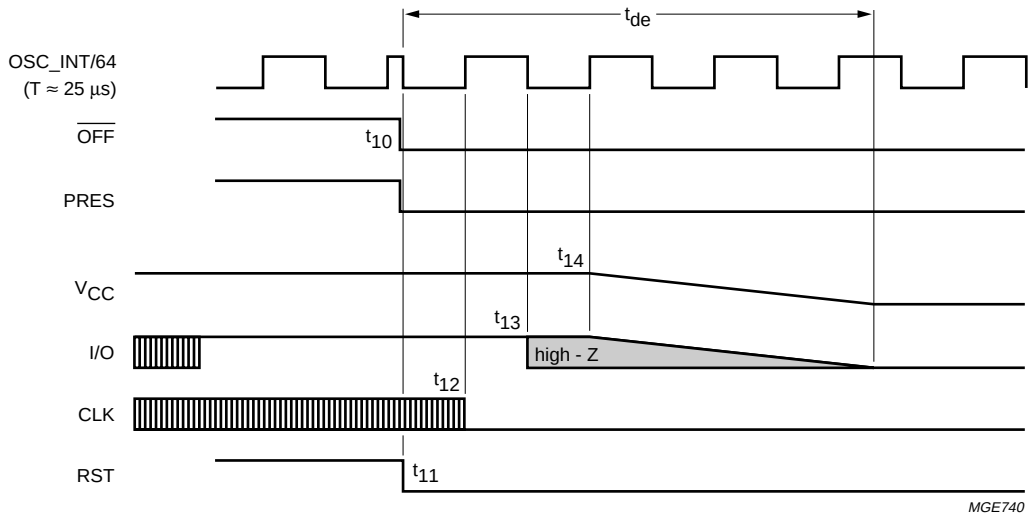


Fig.8 Emergency deactivation sequence.

V_{CC} regulator

V_{CC} buffer is able to deliver up to 65 mA continuously. It has an internal overload detection at approximately 90 mA.

This detection is internally filtered, allowing spurious current pulses up to 200 mA to be drawn by the card without causing a deactivation (the average current value must stay below 65 mA).

For V_{CC} accuracy reasons, a 100 nF capacitor with ESR < 100 mΩ should be tied to CGND near pin 17 and a 100 nF (or better 220 nF) with same ESR should be tied to CGND near C1 contact.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}, V_{DDP}	supply voltage		–0.3	+7	V
V_{n1}	voltage on pins: XTAL1, XTAL2, RFU1, RSTIN, AUX2UC, AUX1UC, I/OUC, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$ and $\overline{\text{OFF}}$		–0.3	+7	V
V_{n2}	voltage on card contact pins PRES, $\overline{\text{PRES}}$, I/O, RST, AUX1, AUX2 and CLK		–0.3	+7	V
V_{n3}	voltage on pin VUP, S1 and S2		–	9	V
T_{stg}	IC storage temperature		–55	+125	°C
P_{tot}	continuous total power dissipation	T_{amb} = –25 to +85 °C	–	0.56	W
T_j	junction temperature		–	150	°C
V_{es1}	electrostatic voltage on pins: I/O, RST, V_{CC}, AUX1, CLK, AUX2, PRES and $\overline{\text{PRES}}$		–6	+6	kV
V_{es2}	electrostatic voltage on all other pins		–2	+2	kV

Notes

1. All card contacts are protected against any short with any other card contact.
2. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM; 1500 Ω; 100 pF) 3 pulses positive and 3 pulses negative on each pin referenced to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

CHARACTERISTICS

V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25 °C; all parameters remain within limits but are only statistically tested for the temperature range; f_{XTAL} = 10 MHz; unless otherwise specified; all currents flowing into the IC are positive. When a parameter is specified as a function of V_{DD} or V_{CC}, it means their actual value at the moment of measurement.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature						
T_{amb}	ambient temperature		–25	–	+85	°C
Supplies						
V_{DD}	supply voltage		2.7	–	6.5	V
V_{DDP}	supply voltage for the voltage doubler		4.5	5	6.5	V
$V_{o(VUP)}$	output voltage on pin VUP from step-up converter		–	5.5	–	V
$V_{i(VUP)}$	input voltage to be applied on VUP in order to block the step-up converter		7	–	9	V
I_{DD}	supply current	inactive mode	–	–	1.2	mA
		active mode; $f_{CLK} = f_{XTAL}$; C_L = 30 pF	–	–	1.5	mA
I_P	supply current for the step-up converter	inactive mode	–	–	0.1	mA
		active mode; $f_{CLK} = f_{XTAL}$; C_L = 30 pF				
		I_{CC} = 0	–	–	18	mA
		I_{CC} = 65 mA	–	–	150	mA
V_{th2}	threshold voltage on V_{DD} (falling)		2.2	–	2.4	V
$V_{hys(th2)}$	hysteresis on V_{th2}		50	–	150	mV
t_W	width of the internal ALARM pulse		6	–	20	ms
Card supply voltage (V_{CC}); note 1						
V_{CC}	output voltage including ripple	inactive mode	–0.1	–	+0.1	V
		inactive mode; I_{CC} = 1 mA	–0.1	–	+0.4	V
		active mode; $\lvert I_{CC} \rvert$ < 65 mA DC	4.75	–	5.25	V
		active mode; single current pulse of –100 mA; 2 µs	4.65	–	5.25	V
		active mode; current pulses of 40 nAs with $\lvert I_{CC} \rvert$ < 200 mA; t < 400 ns;	4.65	–	5.25	V
$V_{i(ripple)(p-p)}$	peak-to-peak ripple voltage on V_{CC}	20 kHz ≤ f ≤ 200 MHz	–	–	350	mV
$\lvert I_{CC} \rvert$	output current	from 0 to 5 V;	–	–	65	mA
		V_{CC} short-circuit to ground	–	–	120	mA
SR	slew rate	up and down	0.11	0.17	0.22	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal connections (XTAL1 and XTAL2)						
C_{ext}	external capacitance on XTAL1 and XTAL2	depending on specification of crystal or resonator used	–	–	15	pF
$f_{i(XTAL)}$	crystal input frequency		2	–	26	MHz
$V_{IH(XTAL)}$	HIGH-level input voltage on XTAL1		$0.8V_{DD}$	–	V_{DD} + 0.2	V
$V_{IL(XTAL)}$	LOW-level input voltage on XTAL1		–0.3	–	$0.2V_{DD}$	V
Data lines (I/O, I/OUC, AUX1, AUX2, AUXUC1 and AUXUC2)						
GENERAL						
$t_{d(edge)}$	delay between falling edge on pins I/OUC and I/O (or I/O and I/OUC) and width of active pull-up pulse		–	200	–	ns
$f_{I/O(max)}$	maximum frequency on data lines		–	–	1	MHz
C_i	input capacitance on data lines		–	–	10	pF
DATA LINES; I/O, AUX1 AND AUX2 (WITH 10 kΩ PULL-UP RESISTOR CONNECTED TO V_{CC})						
V_{OH}	HIGH-level output voltage on data lines	no DC load	$0.9V_{CC}$	–	V_{CC} + 0.1	V
		I_{OH} = –40 μA	$0.75V_{CC}$	–	V_{CC} + 0.1	V
V_{OL}	LOW-level output voltage on data lines	I = 1 mA	–	–	300	mV
V_{IH}	HIGH-level input voltage on data lines		1.8	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage on data lines		–0.3	–	+0.8	V
$V_{inactive}$	voltage on data lines outside a session	no load	–	–	0.1	V
		$I_{I/O}$ = 1 mA	–	–	0.3	V
I_{edge}	current from data lines when active pull-up active	$V_{OH} = 0.9V_{CC}$; C_o = 80 pF	–1	–	–	mA
$\|I_{LIH}\|$	input leakage current HIGH on data lines	$V_{IH} = V_{CC}$	–	–	10	μA
I_{IL}	LOW-level input current on data lines	V_{IL} = 0 V	–	–	600	μA
$R_{pu(int)}$	internal pull-up resistance between data lines and V_{CC}		9	11	13	kΩ
t_r, t_f	input transition times on data lines	from $V_{IL(max)}$ to $V_{IH(min)}$	–	–	1	μs
	output transition times on data lines	C_o = 80 pF, no DC load; 10% to 90% of V_{CC} (see Fig.9)	–	–	0.1	μs
DATA LINES; I/OUC, AUX1UC AND AUX2UC (WITH 10 kΩ PULL-UP RESISTOR CONNECTED TO V_{DD})						
V_{OH}	HIGH-level output voltage on data lines	no DC load	$0.9V_{DD}$	–	V_{DD} + 0.2	V
		I_{OH} = –40 μA	$0.75V_{DD}$	–	V_{DD} + 0.2	
V_{OL}	LOW-level output voltage on data lines	I_{OL} = 1 mA	–	–	300	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage on data lines		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage on data lines		0	–	$0.3V_{DD}$	V
$\|I_{LIH}\|$	input leakage current HIGH on data lines	$V_{IH} = V_{DD}$	–	–	10	µA
I_{IL}	LOW-level input on data lines	V_{IL} = 0 V	–	–	600	µA
$R_{pu(int)}$	internal pull-up resistance between data lines and V_{DD}		9	11	13	kΩ
t_r, t_f	input transition times on data lines	from $V_{IL(max)}$ to $V_{IH(min)}$	–	–	1	µs
	output transition times on data lines	C_o = 30 pF; 10% to 90% of V_{DD} (see Fig.9)	–	–	0.1	µs
Internal oscillator						
$f_{osc(int)}$	frequency of internal oscillator		2.2	–	3.2	MHz
Reset output to the card (RST)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		I_o = 1 mA	0	–	0.3	V
$t_{d(RSTIN-RST)}$	delay between pins RSTIN and RST	RST enabled	–	–	2	µs
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	$0.9V_{CC}$	–	V_{CC}	V
t_r, t_f	rise and fall times	C_o = 250 pF	–	–	0.1	µs
Clock output to the card (CLK)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		I_o = 1 mA	0	–	0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	$0.9V_{CC}$	–	V_{CC}	V
t_r, t_f	rise and fall times	C_L = 35 pF; note 2	–	–	8	ns
δ	duty factor (except for f_{XTAL})	C_L = 35 pF; note 2	45	–	55	%
SR	slew rate (rise and fall)	C_L = 35 pF	0.2	–	–	V/ns
Logic inputs (CLKDIV1, CLKDIV2, PRES, $\overline{\text{PRES}}$, $\overline{\text{CMDVCC}}$, RSTIN and RFU1); note 3						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
$\|I_{LIL}\|$	input leakage current LOW	$0 < V_{IL} < V_{DD}$	–	–	5	µA
$\|I_{LIH}\|$	input leakage current HIGH	$0 < V_{IH} < V_{DD}$	–	–	5	µA
$\overline{\text{OFF}}$ output ($\overline{\text{OFF}}$ is an open drain with an internal 20 kΩ pull-up resistor to V_{DD})						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –15 µA	$0.75V_{DD}$	–	–	V
Protections						
T_{sd}	shut-down temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–	–	110	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
t_{act}	activation sequence duration	see Fig.5	–	180	220	µs
t_{de}	deactivation sequence duration	see Fig.6	60	80	100	µs
t_3	start of the window for sending CLK to the card	see Fig.5	–	–	130	µs
t_5	end of the window for sending CLK to the card	see Fig.5	140	–	–	µs

Notes

1. To meet these specifications V_{CC} should be decoupled to CGND using two ceramic multilayer capacitors of low ESR with values of either 100 nF or one 100 nF and one 220 nF.
2. The transition times and duty factor definitions are shown in Fig.9; $\delta = \frac{t_1}{(t_1 + t_2)}$
3. $\overline{PRES}$ and $\overline{CMDVCC}$ are active LOW; RSTIN and PRES are active HIGH; for CLKDIV1 and CLKDIV2 see Table 1; RFU1 must be tied HIGH.

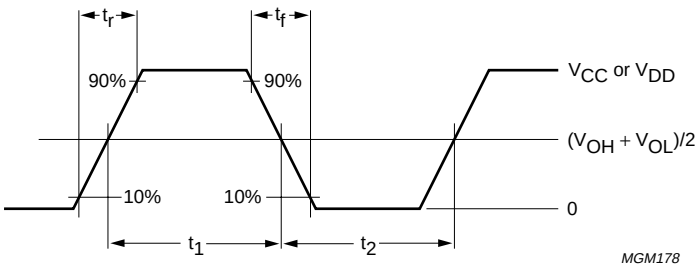


Fig.9 Definition of output transition times.

APPLICATION INFORMATION

V_{DD} for the TDA8004T must be the same as for the microcontroller and CLKDIV1, CLKDIV2, RSTIN, PRES, $\overline{PRES}$, AUX1UC, AUX2UC, I/OUC, RFU1, $\overline{CMDVCC}$ and $\overline{OFF}$ should be referenced to V_{DD} and XTAL1 also when driven by an external clock.

For optimum layout be sure that there is enough ground area around the TDA8004T and the connector. Place the TDA8004T very near to the connector, ideally under the connector, and decouple V_{DD} and V_{DDP} properly.

Refer to *AN97036* for further application information for proper implementation of the TDA8004T.

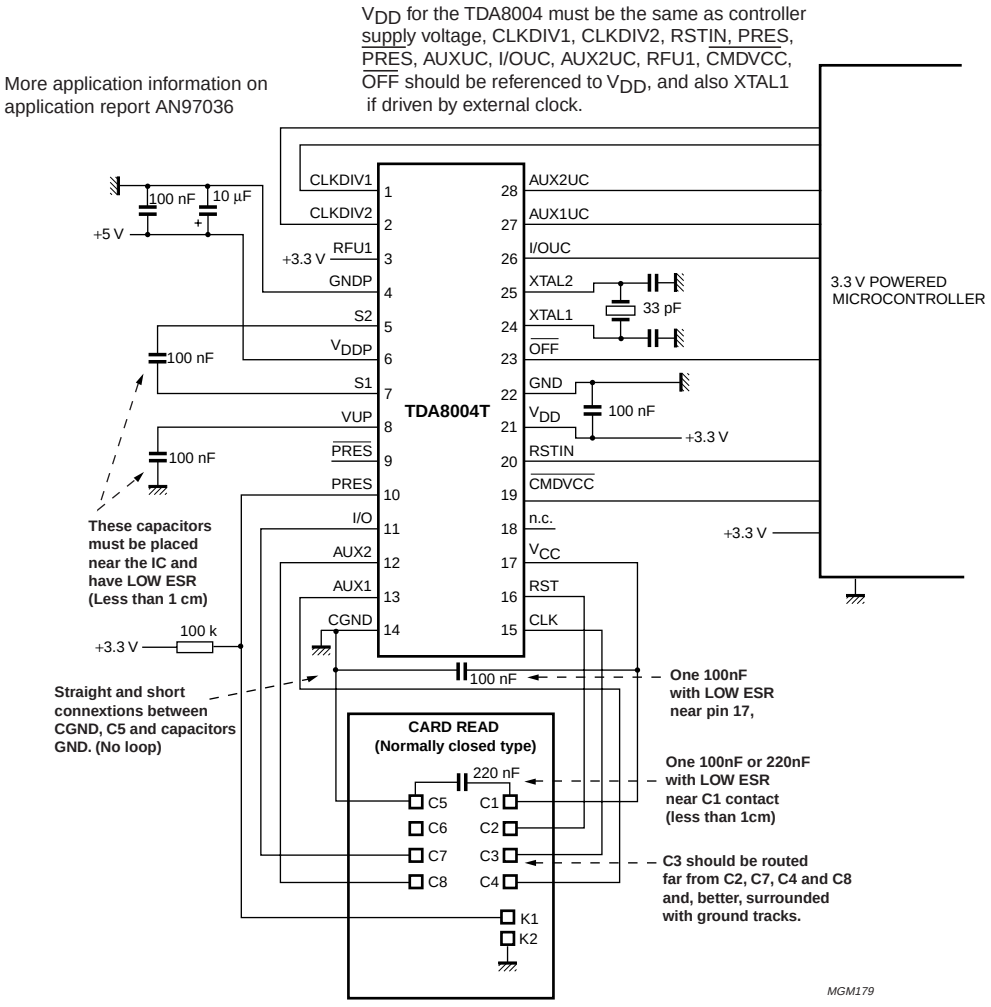
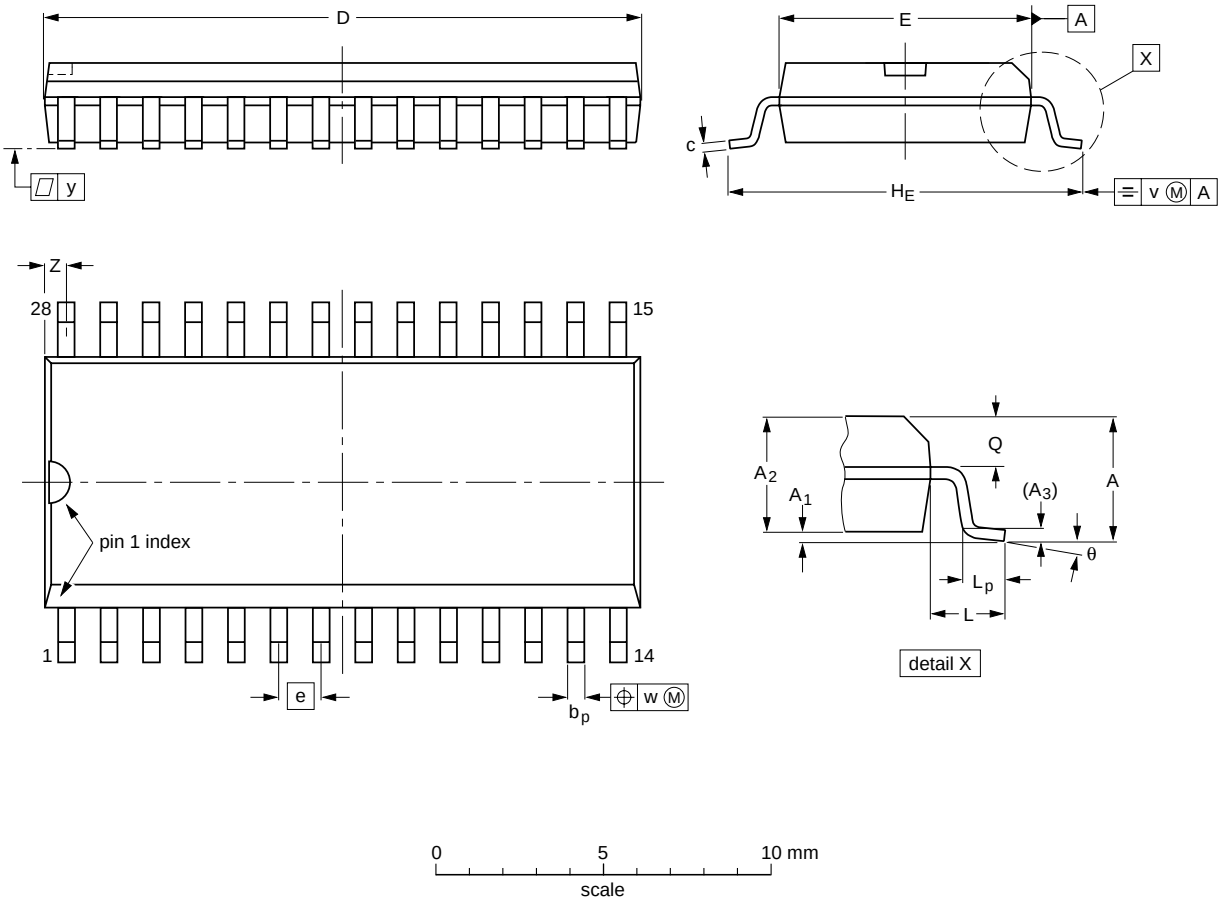


Fig.10 Application diagram.

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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