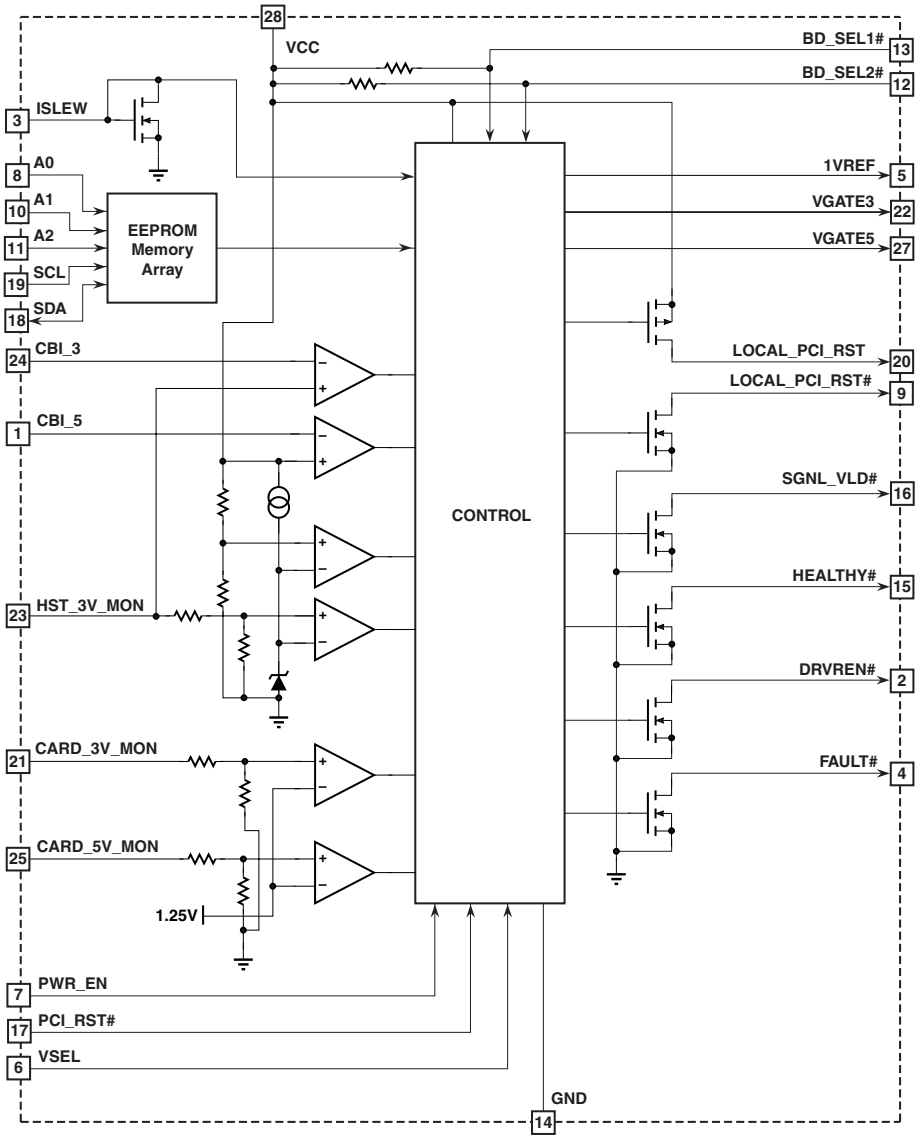
Distributed Power Hot-Swap Controller for *CompactPCI*®

Preliminary

FEATURES

- Full Voltage Control for Hot Swap Applications
  - 15V High Side Driver Generation Allows use of Low On Resistance N-Channel FETs
  - Under-Voltage Lockout
  - Electronic Circuit Breakers
  - Card Insertion Detection
  - Host V_{CC} Detection
  - Card Voltage Sequencing
- Flexible Reset Control
  - Low Voltage Resets
  - Host Reset Filtering
  - Soft Reset
- Adjustable Power On Slew Rate
- Suppoprts Mixed Voltage Cards
- Two Wire I^2C Serial Data Interface
  - 4k-Bit E^2PROM Memory

FUNCTIONAL BLOCK DIAGRAM



PCI INDUSTRIAL PICMG® COMPUTERS

ASSOCIATE MEMBER

DESCRIPTION

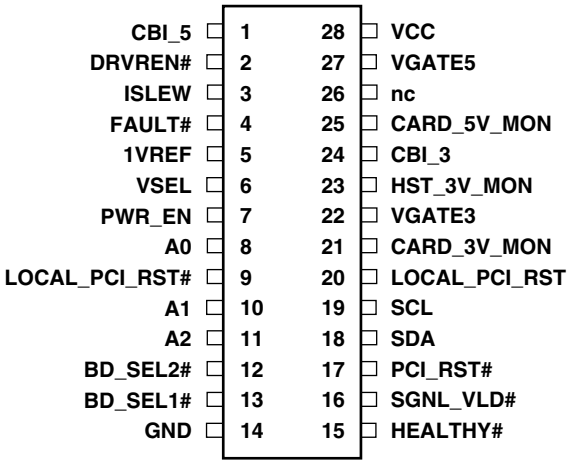
The SMH4042A is a fully integrated hot swap controller that provides complete power control for add-in cards ranging in use for basic hot swap systems to high availability *CompactPCI*® systems. It detects proper insertion of the card and senses valid supply voltage levels at the backplane. Utilizing external low on-resistance N-channel MOSFETs, card power is ramped by two high-side driver outputs that are slew-rate limited at 250V/s.

The SMH4042A continuously monitors the host supplies, the add-in card supplies and the add-in card current. If the SMH4042A detects the current is higher than the programmed value it will shut down the MOSFETs and issue a fault status back to the host.

The internal 512×8 E^2PROM can be used as configuration memory for the individual card or as general purpose memory. The proprietary Data Download mode provides a more direct interface to the E^2PROM, simplifying access by the add-in card's controller or ASIC.

Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

PIN CONFIGURATION



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PIN DESCRIPTIONS

A0 (8)

Address 0 is not used by the memory array. It can be connected to ground or left floating. It must not be connected V_{CC}.

A1, A2 (10, 11)

Address inputs 1 and 2 are used to set the two-bit device address of the memory array. The state of these inputs will determine the device address for the memory if it is on a two-wire bus with multiple memories with the same device type identifier.

SCL (19)

The SCL input is used to clock data into and out of the memory array. In the write mode, data must remain stable while SCL is HIGH. In the read mode, data is clocked out on the falling edge of SCL.

SDA (18)

The SDA pin is a bidirectional pin used to transfer data into and out of the memory array. Data changing from one state to the other may occur only when SCL is LOW, except when generating START or STOP conditions. SDA is an open-drain output and may be wire-ORed with any number of open-drain outputs.

CARD_3V_MON (21)

This input monitors the card-side 3.3V supply. If the input falls below V_{TRIP} then the HEALTHY# and SGNL_VLD# outputs are de-asserted and the reset outputs are driven active.

CARD_5V_MON (25)

This input monitors the card-side 5V supply. If the input falls below V_{TRIP} then the HEALTHY# and SGNL_VLD# outputs are de-asserted and the reset outputs are driven active.

CBI_3 (24)

CBI_3 is the circuit breaker input for the low supply. With a series resistor placed in the supply path between VCC3 and CBI_3, the circuit breaker will trip whenever the voltage across the resistor exceeds 50mV.

CBI_5 (1)

CBI_5 is the circuit breaker input for the supply voltage. With a series resistor placed in the supply path between the 5V early power and CBI_5, the circuit breaker will trip whenever the voltage across the resistor exceeds 50mV.

HST_3V_MON (23)

This input monitors the host 3.3V supply and it is used as a reference for the circuit breaker comparator. If VCC3 falls below V_{TRIP} then SGNL_VLD# is de-asserted, the high side drivers are disabled, and LOCAL_PCI_RST# is asserted.

ISLEW (3)

A Diode-connected NFET input. It may be used to adjust the 250V/s default slew rate of the high-side driver outputs.

PCI_RST# (17)

A TTL level reset input signal from the host interface. A high to low transition (held low longer than 40ns) will initiate a reset sequence. The LOCAL_PCI_RST# and LOCAL_PCI_RST outputs will be driven active for a minimum period of t_{PURST}. If the PCI_RST# input is still held low after t_{PURST} times out the reset outputs will continue to be driven until PCI_RST# is released.

PWR_EN (7)

A TTL level input that allows the host to enable or disable the power to the individual card. During initial power up this signal would start in a low state, and then be driven high during software initialization. If this signal is driven low then the power supply control outputs will be driven into the inactive state and the reset signals asserted. In a “non-High Availability” system this input can be tied high. The PWR_EN input is also used to reset the SMH4042A circuit breakers. After an over-current condition is detected the VGATE outputs can be turned back on by first taking PWR_EN low then returning it high.

VSEL (6)

A TTL level input used to determine which of the host power supply inputs will be monitored for valid voltage and reset generation. This is a static input and the pin should be tied to V_{CC} or ground through a resistor. VSEL is high for 3.3V power. VSEL is low for 5V or mixed mode power.

V_{CC} (28)

The power supply input. It is monitored for power integrity. If it falls below the 5V sense threshold (V_{TRIP}) and the VSEL input is low then the SGNL_VLD# and HEALTHY# signals are de-asserted, the high side drivers disabled, and reset outputs asserted. On a ***CompactPCI*** board this must be connected to early power.

GND (14)

Power supply return line. Ground should be applied at the same time as early power.

BD_SEL1#, BD_SEL2# (13, 12)

These are active low TTL level inputs with internal pull-ups to V_{CC}. When pulled low they indicate full board insertion. On the host side the signals should be directly tied to ground. In a "High Availability" application these inputs can be the last pins to mate with the backplane. Alternatively, they can be actively driven by the host, or be connected to switches interfaced to the board ejectors, or any combination. Regardless, both inputs must be low before the SMH4042A will begin to turn on the backend voltage.

DRVREN# (2)

An open-drain, active-low output that indicates the status of the 3 volt and 5 volt high side driver outputs (VGATE5 and VGATE3). This signal may also be used as a switching signal for the 12 volt supply.

FAULT# (4)

An open-drain, active-low output. It will be driven low whenever an over-current condition is detected. It will be reset at the same time that the VGATE outputs are turned back on after a reset from the host on the PWR_EN signal.

HEALTHY# (15)

An open-drain, active-low output indicating card side power inputs are above their reset trip levels.

LOCAL_PCI_RST# (9)

An open-drain active-low output. It is used to reset the backend circuitry on the add-in card. It is active whenever the card-side monitor inputs are below their respective V_{TRIP} levels. It may also be driven low by a low input on the PCI_RST# pin.

LOCAL_PCI_RST (20)

An open-drain (PFET) active-high output. It operates in parallel with LOCAL_PCI_RST#, providing an active high reset signal which is required by many 8051 style MCUs. It is active whenever the card-side monitor inputs are below their respective V_{TRIP} levels. It may also be driven active by a low input on the PCI_RST# pin.

SGNL_VLD# (16)

An open-drain, active-low output that indicates card side power is valid and the internal card side PCI_RST# timer has timed out.

VGATE3 (22)

A slew rate limited high side driver output for the 3.3V external power FET gate. The output-voltage is generated by an on-board charge pump.

VGATE5 (27)

A slew rate limited high side driver output for the 5V external power FET gate. The output voltage is generated by an on-board charge pump.

$1V_{REF}$ (5)

This output provides a 1V reference for pre-charging the bus signal pins. Implementing a simple unity-gain amplifier circuit will allow pre-charging a large number of pins.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300 °C
Terminal Voltage with Respect to GND:
CARD_3V_MON, CARD_5V_MON, HST_3V_MON, SGNL_VLD#, HEALTHY#, LOCAL_PCI_RET#, V_{CC} 7V
VGATE3, VGATE5, DRVREN# 16V
RESET ..... V_{CC} + 0.7V
All Others ..... V_{CC} + 0.7V
Junction Temperature.....150°C
ESD Rating per JEDEC.....2000V
Latch-Up testing per JEDEC.....+/- 100mA

RECOMMENDED OPERATING CONDITIONS*

Temperature Range (Industrial).....-40° C to +85°C
(Commercial).....-5° C to +70°C
Supply Voltage.....2.7V to 5.5V
Package Thermal Resistance (θ JA)
28 Lead SOIC/SSOP.....80°C/W
Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention.....100 Years
Endurance.....100,000 Cycles

Note * - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Conditions (2)	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage	(1)	1			V
I_{CC1}	Power Supply Current	Operating			500	µA
I_{CC2}		Writing			3	mA
V_{TRIP} (2)	Threshold Levels	V_{CC}5 ***A***	4.250	4.375	4.500	V
		V_{CC}5 ***B***	4.500	4.625	4.750	V
		HST_3V_MON ***G***	2.57	2.65	2.72	V
		HST_3V_MON ***H***	2.72	2.80	2.87	V
		HST_3V_MON ***K***	2.87	2.95	3.00	V
		HST_3V_MON ***L***	3.00	3.10	3.17	V
		CARD_5V_MON ***M***		V_{CC}5 + 50mV		V
		CARD_5V_MON ***N***		V_{CC}5 – 50mV		V
		CARD_3V_MON ***M***		HST_3V_MON + 50mV		V
		CARD_3V_MON ***N***		HST_3V_MON – 50mV		V
V_{TRHYST}	Trip Point Hysteresis			7		mV
I_{LI}	Input Leakage Current				2	µA
I_{LO}	Output Leakage Current				10	µA
V_{IL}	Input Low Voltage		–0.1		0.8	V
V_{IH}	Input High Voltage		2		V_{CC} + 1V	V
V_{OL}	Output Low Voltage	V_{CC} = 5.0V, I_{OL} = 2.1mA			0.4	V
V_{OH}	Output High Voltage	V_{CC} = 5.0V, I_{OH} = –400µA	2.4			V
V_{OLRS}	LOCAL_PCI_RST# Low	I_{OL} = 3.2mA			0.4	V
V_{OHRS}	RESET High	I_{OH} = –800µA	V_{CC} – 0.75V			V
V_{OHVG3}	VGATE3 High	I_{OH} = 5µA	12	13	15	V
V_{OHVG5}	VGATE5 High	I_{OH} = 5µA	13	14	15	V
V_{REF}	Reference Output Voltage	No Load	0.95	1.00	1.05	V
V_{CB}	Circuit Breaker Trip Voltage	(3)	40	50	60	mV

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Notes: (1) The SMH4042A will drive the Reset outputs and voltage control signals throughout the operating range of 1V to 5.5V. The balance of the logic will not be guaranteed operational unless V_{CC} is greater than 2.7V.

(2) A, B,G, H, K. L, M, & N refer to the Part Number Suffix.

(3) For T_A = –10ºC to 85ºC.

DEVICE OPERATION

Power-Up Sequence

The SMH4042A is an integrated power controller for any hot swappable add-in card. It provides all the signals and control functions to be compatible with ***CompactPCI*** Hot Swap requirements for basic hot swap systems, full hot swap boards, and high availability systems.

Insertion Process

As the add-in board is inserted into the backplane, physical connections are made with the chassis in order to properly discharge any voltage potentials to ground. The board will first contact the long pins on the backplane that provide early power (5V, 3.3V and ground). Depending upon the board configuration, early power should be routed to the V_{CC} pin of the SMH4042A. As soon as power is applied the SMH4042A will assert the reset outputs to the backend circuits, turn off the VGATE3 and VGATE5 outputs (disabling the external power FETs) and assert 1VREF. This signal can be used to pre-charge the I/O pins before they begin to mate with the bus signals. The open collector HEALTHY# output will be de-asserted. It should be actively pulled high by an external pull-up resistor (minimum 10kΩ).

The next pins to mate are the I/Os, and the balance of the power pins if they are not already mated. The I/Os will have been pre-charged by the 1VREF output.

The BD_SEL# pins are the last inputs to be driven to their true state. In most systems these will most likely be driven to ground when the short pins are mated. This would indicate the card is fully inserted and the power-up sequence can begin. If, however, the design is based on high availability requirements, the two pins can be actively driven by the host or combined with a switch input indicating the ejector handles are fully engaged.

Sequencing

Once the proper card insertion has been assured the SMH4042A will check the status of the Power Enable signal from the host. This input can be used to power down individual cards on the bus via software control. It must by held high in order for the SMH4042A to enable power sequencing to the card.

When these conditions have been met, the SMH4042A will drive the VGATE3 and VGATE5 outputs to turn on the external 3 volt and 5 volt power FETs. The slew rate of these outputs is controlled to a slew rate of 250V/s. Different slew rates can be accommodated by either adding an additional capacitor between the MOSFET gate and ground or by injecting current into the ISLEW input. All circuitry on the card is held in a reset condition until the 5V (or 3.3V) supply is stable and the reset interval timer has timed out the 150ms reset time. At this point, the reset signals are de-asserted, and proper operation of the card commences. See Figure 1, Table 1, and Flow Chart 1.

The SMH4042A will monitor the card's backend voltages. Once they are at or above the card V_{TRIP} levels the SMH4042A will drive the HEALTHY# output.

Card Removal Process

The card removal process operates in the opposite sequence. For non-high-availability cards the action of card removal disconnects the BD_SEL# (short pins) from ground and the SMH4042A will instantly shutdown the VGATE outputs, change the HEALTHY# status, and assert the LOCAL_PCI_RST# output.

Because connectors to the host backplane employ staggered pins, power will still be applied to the SMH4042A and the I/O interface circuits. The LOCAL_PCI_RST# signal will place the interface circuits into a high impedance condition. The pre-charge voltage will be applied to the I/Os enabling a graceful disengagement from the active bus. Once the I/O pins are free of the backplane, power can be removed from the SMH4042A and other early power devices by releasing the long pins.

The removal process is slightly different for a high-availability system. As the ejector handle is rotated the ejector switch will open, causing a change of state that will activate the ENUM# signal to the host. In response to this notification the host will de-assert a hardware controlled BD_SEL# signal. This action will turn on an indicator LED on the card, notifying the operator it is now safe to proceed with the removal of the card. The sequence will then follow that outlined for the non-high-availability removal process.

Power Configurations

The SMH4042A can be used in 5V-only, 3.3V-only and mixed voltage systems. For systems with a single power supply, connect V_{CC} and HST_3V_MON together to the bus power line. Also connect CARD_3V_MON and CARD_5V_MON together to the card side power. Now the state of VSEL determines the reset level that will be used to signal valid power. For 3.3V systems tie VSEL to V_{CC}, for 5V systems tie VSEL to ground.

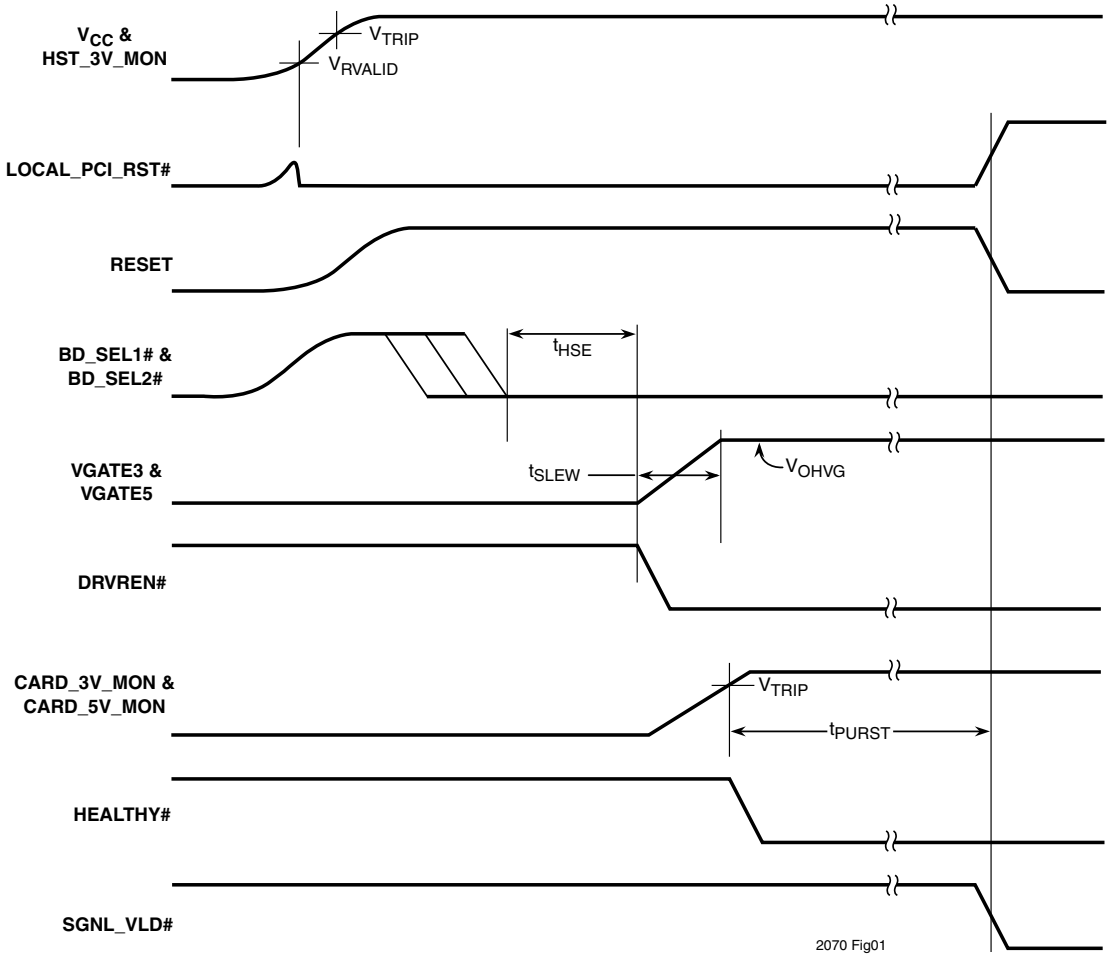
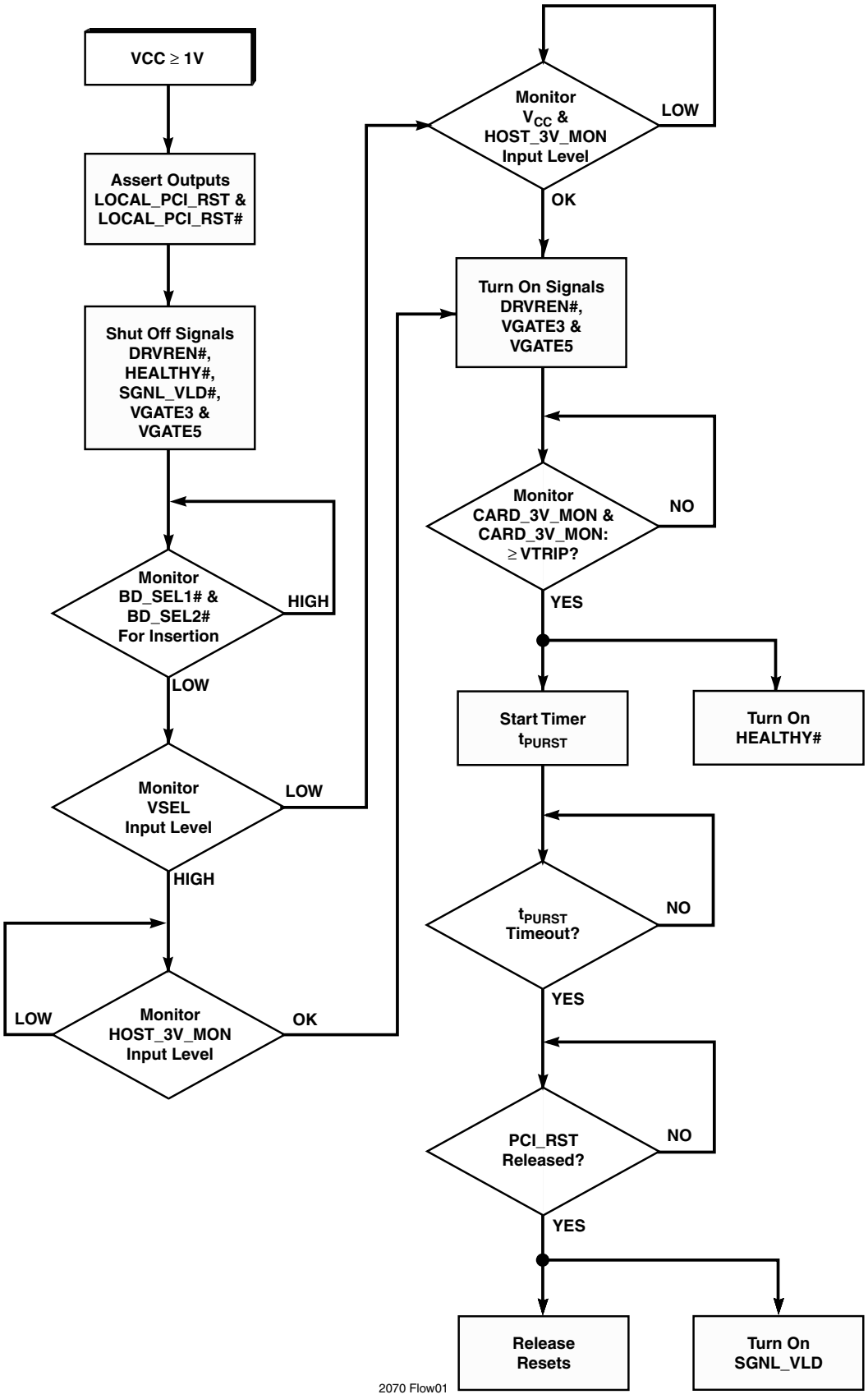


Figure 1. Card Insertion Timing Diagram

Symbol	Description	Min.	Typ.	Max.	Units
t_{VTPD}	V_{TRIP} to Power Down Delay, Host Voltage Input		1	5	µs
t_{VTR}	V_{TRIP} to Reset Output Delay, Card Voltage Input		1	5	µs
t_{PRLPR}	PCI_RST# to LOCAL_PCI_RST#		0.1	1	µs
V_{RVALID}	Local Reset Output Valid	1			V
t_{SLEW}	Slew Rate			250	V/s
t_{HSE}	BD_SEL# to Power On Delay, BD_SEL Noise Filter	100	150	200	ms
t_{PURST}	Reset Timeout	100	150	200	ms
t_{GLITCH}	Glitch Reject Pulse Width			40	ns
t_{OCF}	Over-Current to Fault#		1		µs
t_{OCVG}	Over-Current to VGATE Off		1		µs
t_{CBTC}	Circuit Breaker Time Constant, Power up		4		µs
	Circuit Breaker Time Constant, Operating		16		µs

2037 Table01 2.0

Table 1. Card Insertion Timing



Flow Chart 1. Sequence Diagram

MONITORING POWER SUPPLY HEALTH

MONITOR INPUTS

The SMH4042A has a total of six comparators that are used to monitor the health of the host platform supplies and the card-side (backend) voltages. In hot swap applications each supply going to the backend logic needs to be monitored at three points.

The first point is at the source on the host connector, V_{CC} and HST_3V_MON. If this voltage is not within specification, then the down stream sequencing of powering-on the backend logic will not proceed.

The next stage (the CBI inputs) is one step closer to the backend logic to monitor the current flowing into the backend logic. This can not exceed the specification; however, If it does, then the SMH4042A must turn off the source to the backend logic.

The CARD_5V_MON and CARD_3V_MON inputs are used to sense the actual voltage level in the backend logic. If either comparator detects a low voltage condition the backend logic will be placed in a reset condition (LOCAL_PCI_RST# asserted), but the VGATE outputs will remain active so long as the host voltage and current sense are valid.

V_{CC} vs. HST_3V_MON

The V_{CC} input is the supply input and in a ***CompactPCI*** application this pin must connect to an early power pin on the host connector. The HST_3V_MON input is strictly a voltage monitoring input, it is not a supply input. The operating supply voltage range on the V_{CC} pin is 2.7V to 5.5V, but it will only monitor a 5V supply. This is not an issue with a dual supply application. But in a single supply application these two pins must be shorted and VSEL conditioned.

Programmable V_{TRIP} Thresholds

The host voltage monitors and the backend voltage monitors are programmable (by the factory) and provide a number of options to the end user. The V_{CC} monitor V_{TRIP} level can be selected for either a 5% or 10% supply with default values of 4.25V or 4.625V. The HST_3V_MON V_{TRIP} level can be programmed to 2.65V, 2.8V, 2.95V and 3.1V.

The CARD_5V_MON and CARD_3V_MON thresholds are set in relation to their corresponding host voltage monitor thresholds. Their offset can be either +50mV or –50mV. This allows the designer to select +50mV if they want a collapse in the backend voltage to trigger a local reset condition prior to the host supply collapsing and powering down the board without warning. Alternatively they can choose –50mV to trigger a board shutdown based on the host power supply falling out of spec.

Also see Figure 2

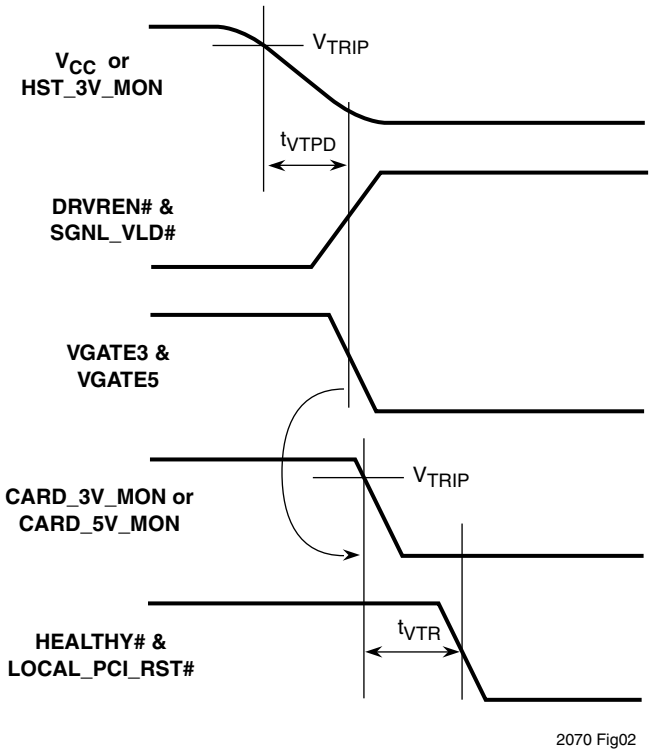


Figure 2. Loss-of-Voltage Timing Sequence

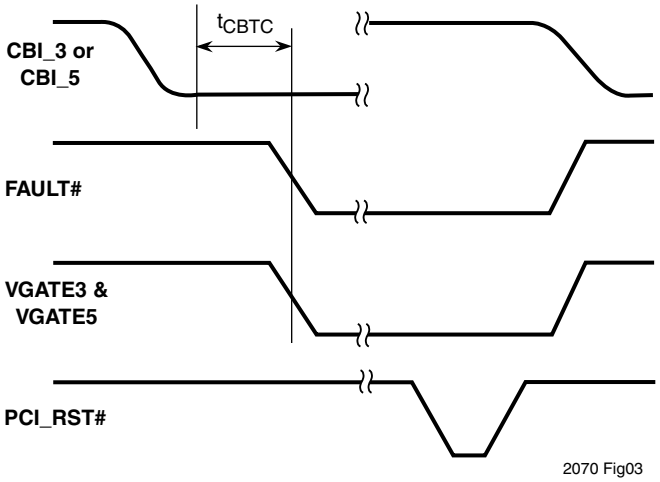


Figure 3. Circuit Breaker Timing Sequence

Over-current Circuit Breaker

The SMH4042A provides a circuit breaker function to protect against short circuit conditions or exceeding the supply limits. By placing a series resistor between the host supply and the CBI pins, the breakers will trip whenever the voltage drop across the series resistor is greater than 50mV for more than 16µs.

The over-current detection circuit was designed to maximize protection while minimizing false alarms. The most critical period of time is during the power-on sequence when the backend circuits are first being energized. If the card has a faulty component or shorted traces, the time to shut off should be minimal. However, if the board has been operational for a long period of time the likelihood of a catastrophic failure occurring is quite low. Therefore, the SMH4042A employs two different sampling schemes. During power-up the device will sample the current every 500ns. If eight consecutive over-current conditions are detected the VGATE outputs will immediately be shut down. This provides an effective response time of 4µs. During normal operation, after the FETs have been turned on, the sampling rate will be adjusted to 2µs, thus providing an effective response time of 16µs.

Also see Figure 3.

RESET CONTROL

While in the power sequencing mode, the reset outputs are the last to be released. When they are released all conditions of a successful power-up sequence must have been met:

1) VCC and HST_3V_MON are at or above their respective VTRIP levels;

2) BD_SEL# inputs are low;

3) CARD_3V_MON and CARD_5V_MON are at or above their respective trip levels;

4) PWR_EN is high; and

5) PCI_RST is high.

The PCI-RST# input must be high for the reset outputs to be released. Assuming all of the conditions listed above have been met and PCI_RST# is high and t_{PURST} has expired, a low input of greater than 40ns duration on the PCI_RST# input will initiate a reset cycle. The duration of the reset cycle will be determined by the PCI_RST# input. If PCI_RST# low is shorter than t_{PURST}, the reset outputs will be driven active for t_{PURST}. If PCI_RST# is longer than t_{PURST} the reset outputs will remain active until PCI_RST# is released.

Also see Figure 4.

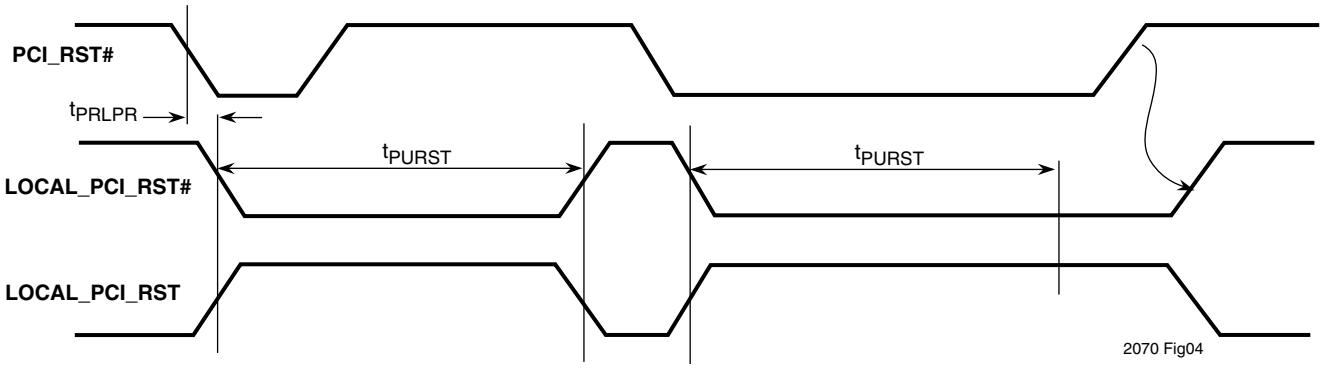


Figure 4. Host-Initiated Reset Timing

BUS INTERFACE

GENERAL DESCRIPTION

The I²C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial Data line (SDA) and a serial Clock line (SCL). All Summit Microelectronics parts support a 100kHz clock rate, and some support the alternative 400kHz clock. Check Table 2 for the value of f_{SCL}. The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. Summit parts have a Schmitt input on both lines. See Figure 5 and Table 2 for waveforms and timing on the bus. One bit of Data is transferred during each Clock pulse. The Data must remain stable when the Clock is high.

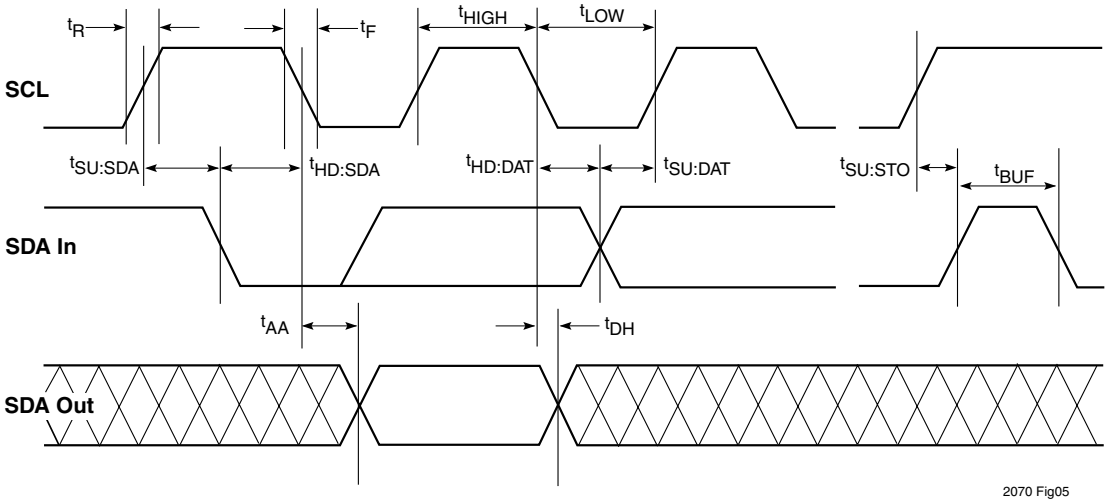


Figure 5. I²C Timing Diagram

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency		0		100	kHz
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4.0			µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7			µs
$t_{SU:STA}$	Start condition setup time		4.7			µs
$t_{HD:STA}$	Start condition hold time		4.0			µs
$t_{SU:STO}$	Stop condition setup time		4.7			µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA rise time (1)				1000	ns
t_F	SCL and SDA fall time (1)				300	ns
$t_{SU:DAT}$	Data In setup time		250			ns
$t_{HD:DAT}$	Data In hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		100		ns
t_{WR}	Write cycle time				5	ms

Note 1 - Guaranteed by Design

2037 Table02 2.0

Table 2. I²C AC Operating Characteristics

Start and Stop Conditions

Both Data and Clock lines remain high when the bus is not busy. Data transfer between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the Data line while the Clock line is high is defined as a Start condition. A low-to-high transition of the Data line while the Clock line is high is defined as a Stop condition. See Figure 6.

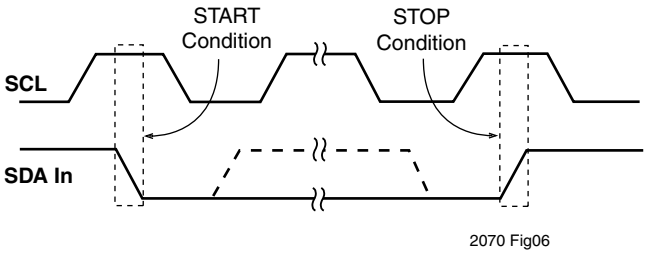


Figure 6. I²C Start and Stop Timing

Protocol

The protocol defines any device that sends data onto the bus as a Transmitter, and any device that receives data as a Receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the Summit Microelectronic devices are Slave devices, since they never initiate any data transfers.

Acknowledge

Data is always transferred in 8-Bit bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The Transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the Receiver will pull the SDA line low to Acknowledge that it received the eight bits of data (See Figure 7). The termination of a Master Read sequence is indicated by a non-Acknowledge (NACK), where the Master will leave the Data line high.

In the case of a Read from a Summit part, when the last byte has been transferred to the Master, the Master will leave the Data line high for a NACK. This will cause the Summit part to stop sending data, and the Master will issue a Stop on the clock pulse following the NACK.

In the case of a Write to a Summit part the Master will send a Stop on the clock pulse after the last Acknowledge. This will indicate to the Summit part that it should begin its internal non-volatile write cycle.

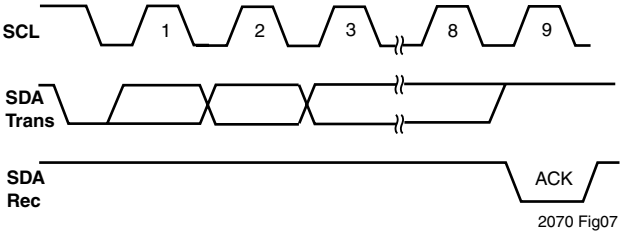


Figure 7. Acknowledge Timing

Basic Read and Write

The first byte from a Master is always made up of a seven bit Slave address and the Read/Write bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SMH4042A is 1010_{BIN}. The next two bits are used to select one-of-four possible devices on the bus. The next bit is the block select bit. The SMH4042A will issue an Acknowledge after recognizing a Start condition and its DTI.

In the Read mode the SMH4042A transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4042A will continue to transmit data. If an Acknowledge is not detected (NACK), the SMH4042A will terminate further data transmission. See Figure 9.

In the Write mode the SMH4042A receives eight bits of data, then generates an Acknowledge signal. It will continue to generate ACKs until a Stop condition is generated by the Master. See Figure 10.

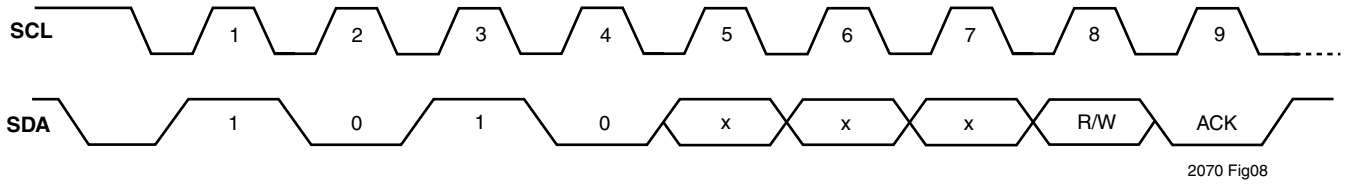


Figure 8. Typical Master Address Byte Transmission

Random Address Read

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a write command which includes the start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4042A to the desired address. After the word address Acknowledge is received by the Master, it immediately reissues a start condition followed by another Slave address field with the R/W bit set to Read. The SMH4042A will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the Master sets SDA high (NACK) and generates a Stop condition. The SMH4042A discontinues data transmission and reverts to its standby power mode.

Sequential Read

Sequential Reads can be initiated as either a current address Read or a random access Read. The first word is transmitted as with the other byte read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4042A. The SMH4042A continues to output data for each Acknowledge received. The Master terminates the sequential Read operation with a NACK and issues a Stop condition. During a sequential read operation the internal address counter is automatically incremented with each Acknowledge signal. For read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will roll-over and the memory will continue to output data.

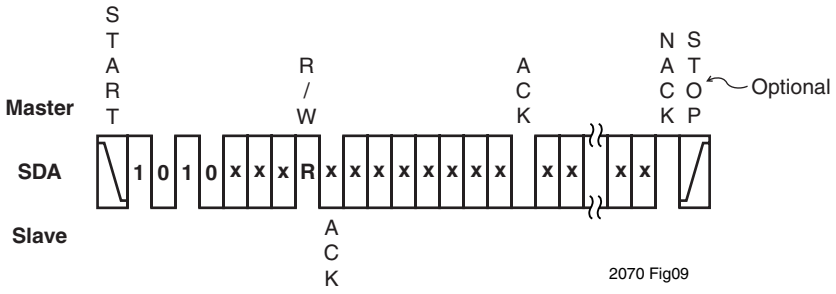


Figure 9. Basic Read

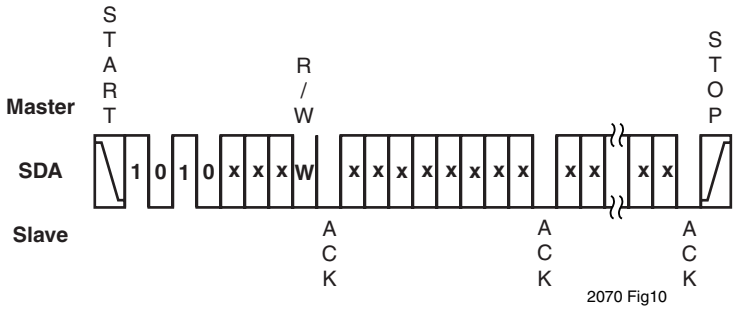


Figure 10. Basic Write

MEMORY OPERATION

WRITE OPERATIONS

The SMH4042A allows two types of Write operations to its a 512 x 8 array: byte Write and page Write. A byte Write operation writes a single byte during the nonvolatile Write period (t_{WR}). The page Write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte Write

After the slave address is sent (to identify the slave device, and a Read or Write operation), a second byte is transmitted which contains the 8 bit address of any one of the 512 words in the array. Upon receipt of the word address the SMH4042A responds with an Acknowledge. After receiving the next byte of data, it again responds with an Acknowledge. The master then terminates the transfer by generating a Stop condition, at which time the SMH4042A begins the internal write cycle. The SMH4042A inputs are disabled while the internal write cycle is in progress, and the device will not respond to any requests from the Master.

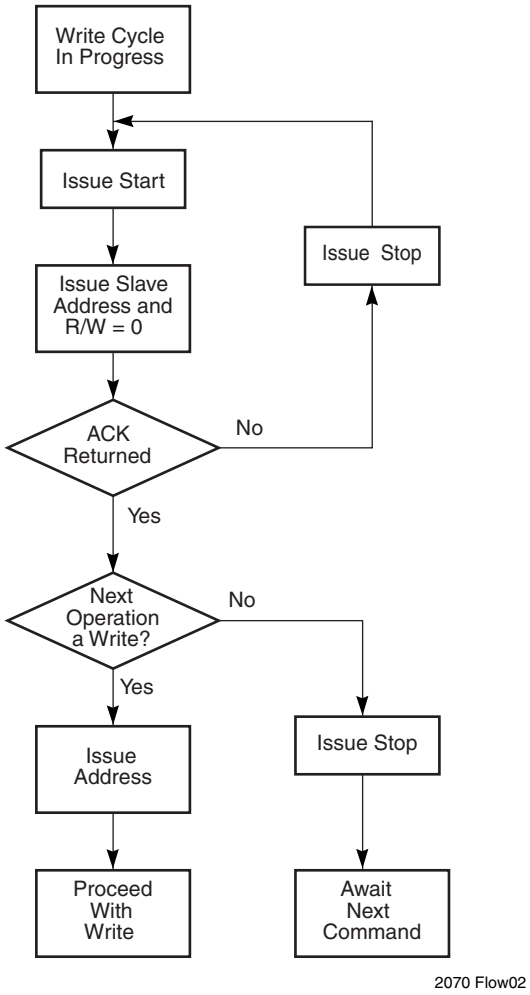
Page Write

The SMH4042A is capable of a 16-byte page Write operation. It is initiated in the same manner as the byte-Write operation, but, instead of terminating the Write cycle after the first data word, the Master can transmit up to 15 more bytes of data. After the receipt of each byte the SMH4042A will respond with an Acknowledge.

The SMH4042A automatically increments the address for subsequent data words. After the receipt of each word the low order address bits are internally incremented by one. The high order bits of the address byte remain constant. Should the Master transmit more than 16 bytes, prior to generating the Stop condition, the address counter will roll over and the previously written data will be overwritten. As with the byte-Write operation, all inputs are disabled during the internal write cycle. Refer to Figure 5 for the address, Acknowledge and data transfer sequence.

Acknowledge Polling

When the SMH4042A is performing an internal Write operation it will ignore any new Start conditions. Since the device will only return an acknowledge after it accepts the Start, the part can be continuously queried until an acknowledge is issued, indicating that the internal write cycle is complete. See Flow Chart 2 for the proper sequence of operations for polling.



Flow Chart 2. Polling

READ OPERATIONS

There are two different read options:

1. Current Address Byte Read
2. Random Address Byte Read

Current Address Read

The SMH4042A contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a Read or Write) was to address location *n*, the next Read operation would access data from address location *n+1* and increment the current address pointer. When the SMH4042A receives the Slave address field with the R/W

bit set to "1" it issues an acknowledge and transmits the 8-Bit word stored at address location *n+1*. The current address byte Read operation only accesses a single byte of data. The Master holds the SDA line high (NACK) and generates a Stop condition. At this point the SMH4042A discontinues data transmission.

Random Address Read

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4042A to the desired address. After the word address acknowledge is received by the Master, the Master immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4042A will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the Master issues a NACK and generates the Stop condition. The SMH4042A discontinues data transmission and reverts to its standby power mode.

Sequential Read

Sequential Reads can be initiated as either a current address Read or a random access Read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read); however, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4042A. The SMH4042A continues to output data for each Acknowledge received. The Master terminates the sequential Read operation with a NACK and a Stop. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will roll over and the memory will continue to output data.

Data Download

The SMH4042A supports a proprietary mode of operation specifically for the Hot Swap environment. After a power on reset the internal address pointer is reset to 00. The host or ASIC then only needs to issue a Read command and then sequentially clock out data starting at address 00.

APPLICATIONS

DESIGN CONSIDERATIONS FOR A *COMPACTPCI* BOARD

Figure 11 is a generic representation of a ***CompactPCI*** board and it illustrates how the SMH4042A is the key component in the board insertion/removal process. The illustrations that follow show in more detail how the various blocks interface to the SMH4042A.

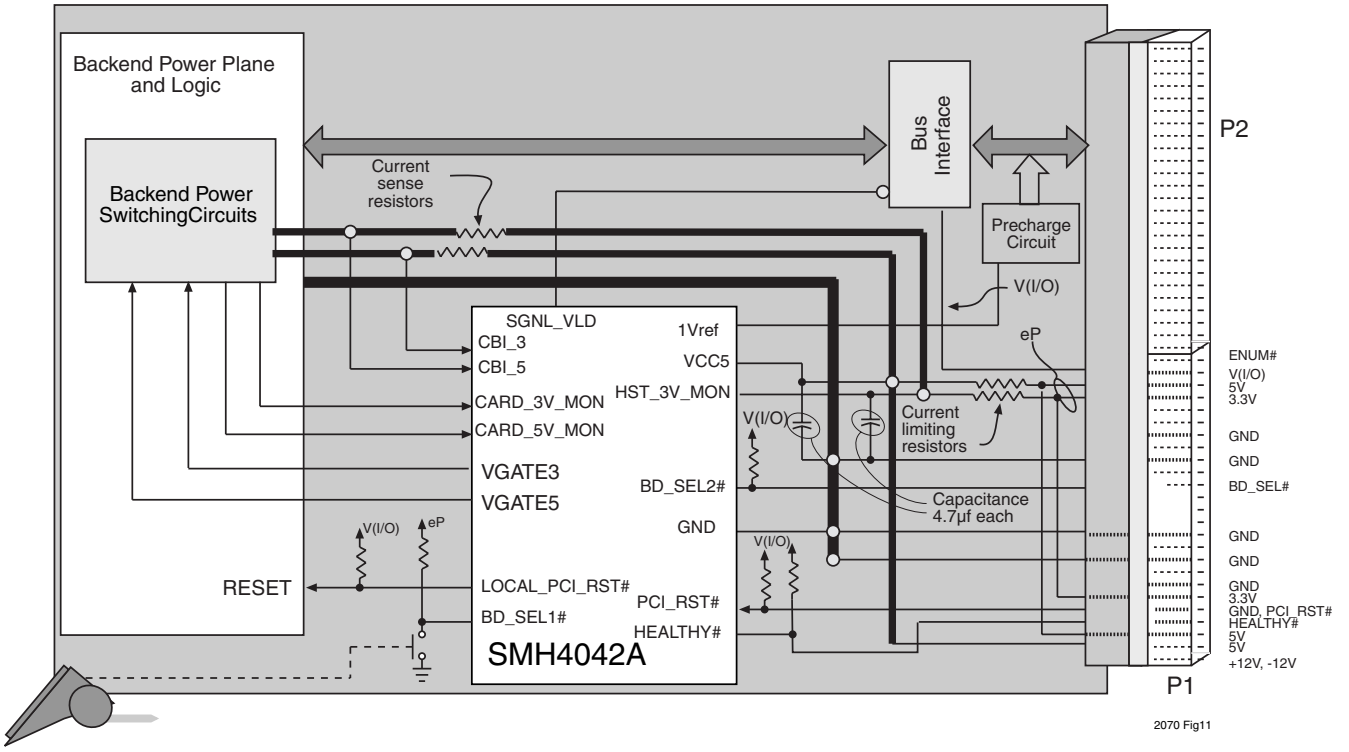


Figure 11. Diagram of Typical *CompactPCI* Board

Power Busses

It is important in the design of the board to ensure the backend logic is isolated from the power control circuits and other early power circuits such as FPGAs and the I/O interface circuits. In Figure 12 the early power busses for 5V and 3V have series current limiting resistors. These values should be calculated so as to limit the in-rush current that will initially charge the capacitive load of the early power circuits. As the card is inserted further, the medium length pins engage and short out the current limiting resistors. Note the placement of the sense (shunt) resistors. They are in series with the power FETs and no voltage drop will be detected across the resistor until VGATE is applied to the power FETs. The sense resistor values are determined by dividing 50mV by the current specification for that supply.

It should be noted that there is an inherent delay from VGATE5 turning on to VGATE3 turning on. The typical delay is illustrated in Figure 13.

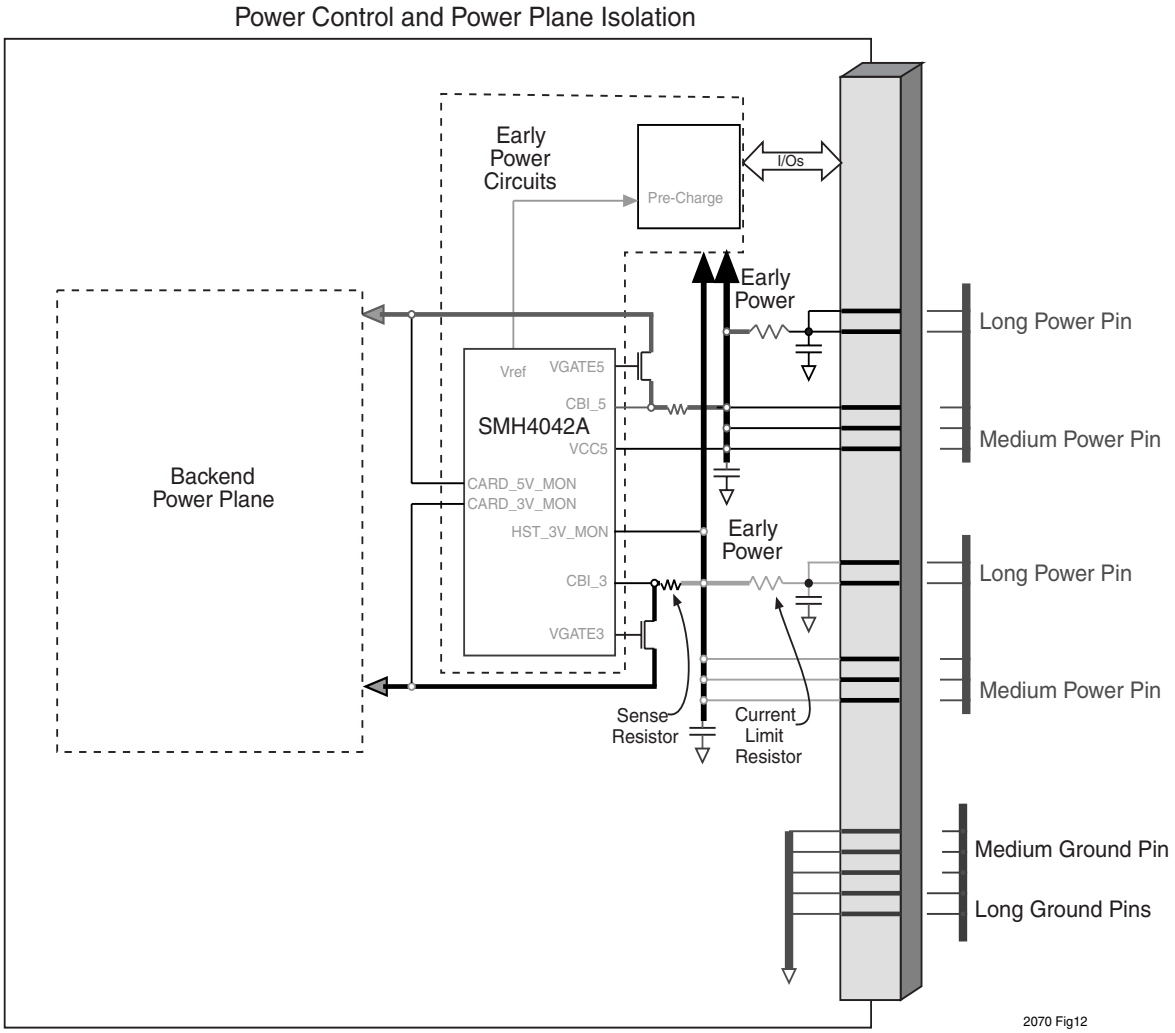


Figure 12. Power Control and Power Plane Isolation

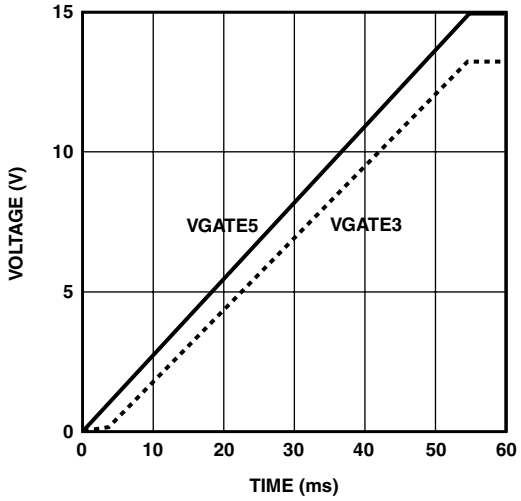
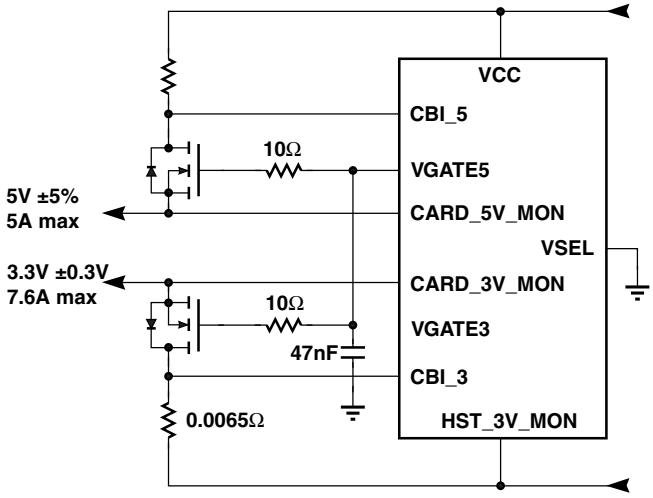


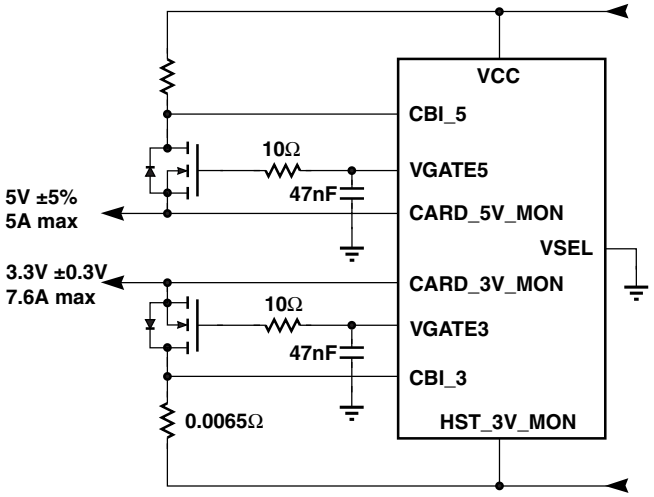
Figure 13. Typical Delay: VGATE5 to VGATE3

POWER SWITCHING OPTIONS

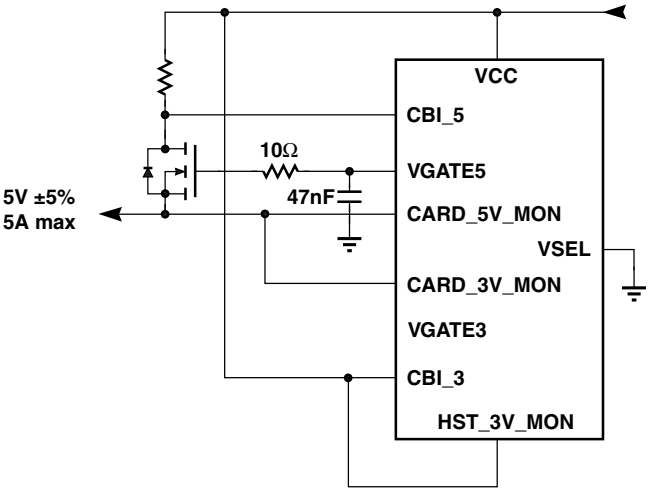
The figures below illustrate four possible methods for wiring the SMH4042A. In the upper left example both power FETs are connected to a single VGATE output. This should be used when the design requires the backend voltages to be powered-up simultaneously. In the upper right example both VGATE outputs are being used so that the 3.3V slew lags the 5V slew. The two bottom circuits illustrate the wiring for single power supply boards. Note how the VSEL pin is biased differently for the two applications.



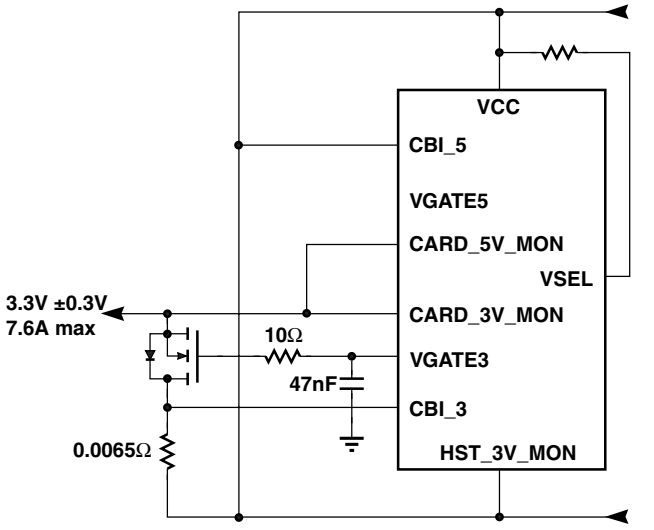
Dual Voltage, Single Slew Rate Implementation



Dual Voltage, Dual Slew Rate Implementation



Single 5V Implementation



Single 3.3V Implementation

Figure 14. Four Power Switching Implementations

I/O Buffers

Depending upon the application requirements there are a number of silicon solutions that employ low on-resistance CMOS switches. Figure 15 shows one implementation using a QuickSwitch® from Quality Semiconductor. This particular device exhibits very Flat R_{ON} characteristics from 0 to 5V. The only drawback is the extra space required for the external pull-up resistors.

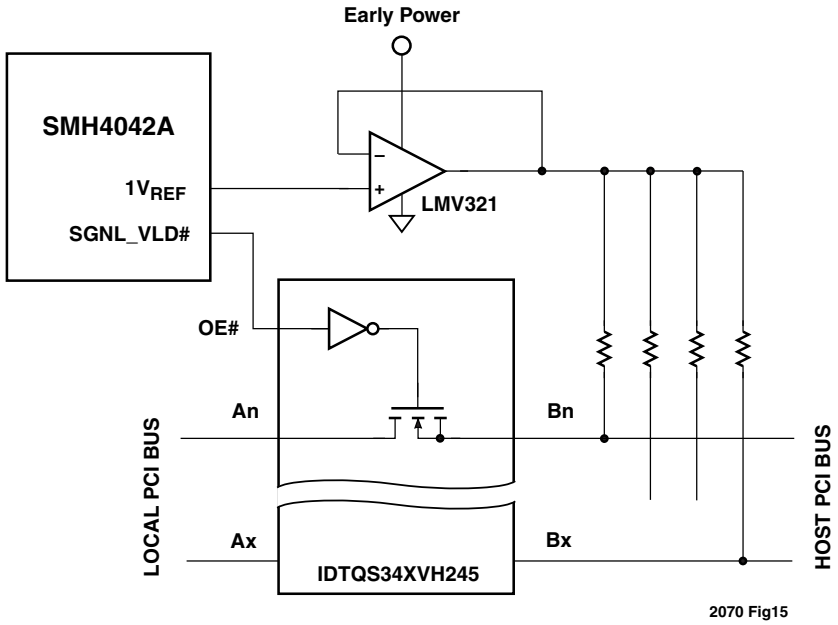


Figure 15. Bus Buffers with External Pull-ups

Figure 16 shows another implementation, but the pull-up resistor structure is incorporated in the switch. The circuit also automatically switches the bias voltage out of the circuit as the CMOS switches are enabled. A potential advantage is the ability to place the interface closer to the edge of the card. The board designer should evaluate requirements and design goals to determine the best solution. The bus switches are available from both Texas Instruments and Pericom Semiconductor.

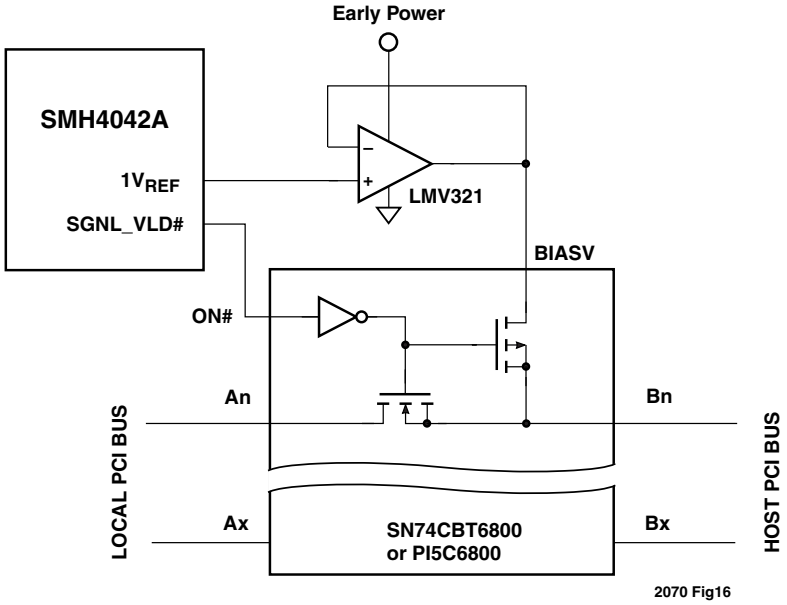


Figure 16. Bus Buffers with Integrated Pull-ups

I/O Pre-charge

The ***CompactPCI*** specs require the add-in board to pre-charge the board's I/Os before making contact with bus pins, and sets the pre-charge voltage at 1V ±0.1V. The SMH4042A provides an accurate 1V reference output that is accurate and stable prior to the medium length pins making contact. The 1VREF output should be the reference input to a unity gain op amp circuit. Figure 17 is a typical implementation utilizing a common op amp.

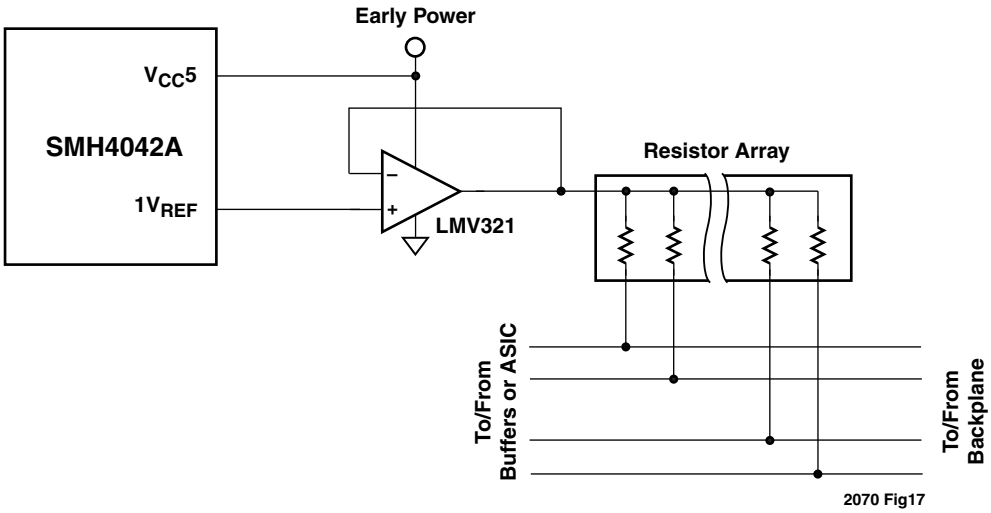


Figure 17. I/O Pre-charge Circuit

SPECIAL CONSIDERATIONS

The example application shown in Figure 11 shows both of the BD_SEL inputs being used independently. These two inputs are effectively ANDed internally and they must both be low before any sequencing will proceed. In most design cases the BD_SEL1# connection to an injector switch is redundant and realistically can be grounded.

The ***CompactPCI*** Hot Swap specification does provide a mechanism for implementing high availability systems using "Full Hot Swap" boards. This capability entails integrating the injector/ejector handle, the blue LED and a board status signal. Section 2.3.2 of the ***CompactPCI*** Hot Swap specification states the following.

- "A signal (ENUM#) is provided to notify the system host that either a board has been freshly inserted or is about to be extracted."
- "A switch, actuated with the lower ejector handle of the board, is used to signal the insertion or impending extraction of a board."
- "A blue LED, located on the board is illuminated when it is permissible to extract a board."

Figure 18 illustrates a possible implementation of the circuits needed. It should be noted this will require a status register that works in conjunction with the switch logic to generate the ENUM# signal. Notice the blue LED circuit and the active high reset output used to activate a current boost circuit for the LED. The sequence of operations is as follows:

- **The long pins engage.**
- Power is supplied to the SMH4042A, the LED and the BD_SEL pull-up resistor.
- V(I/O) is either the early 5V or the early 3V, dependent upon the interface operating levels.
- The LED is illuminated by LOCAL_PCI_RST# going low.

- **The medium length pins contact.**
- The ENUM# signal should not be active at this point.
- **The board is fully inserted and the injector switch is closed.**
- ENUM# is driven low.
- BD_SEL# makes contact (optional: the pull-up on the board indicates to the host the presence of a board.)
- The host responds to the ENUM# signal and drives BD_SEL# low.
- This provides the last gating item to the SMH4042A before it will begin the power-on sequence.

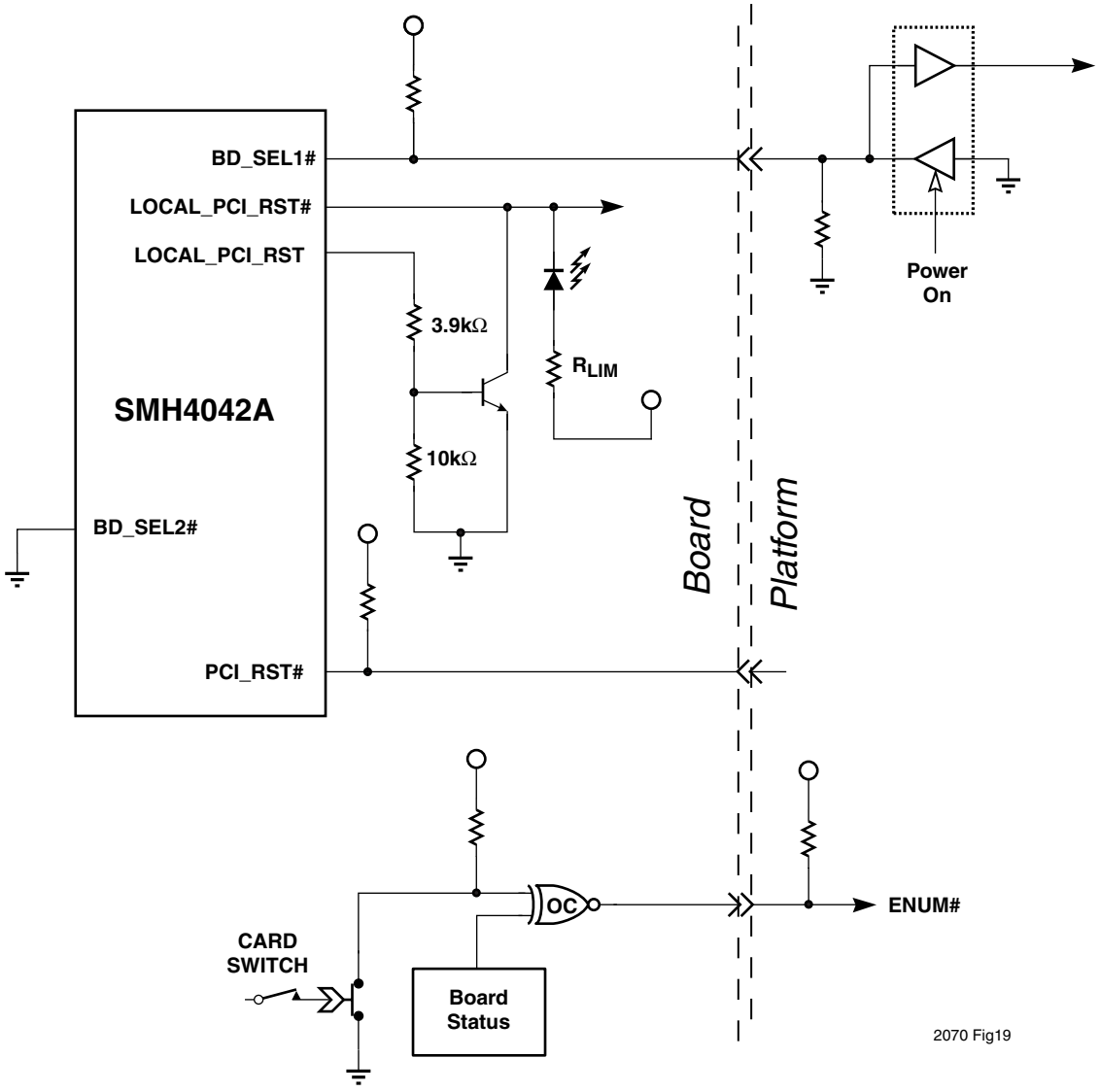


Figure 18. Full Hot Swap Board/Host Interface

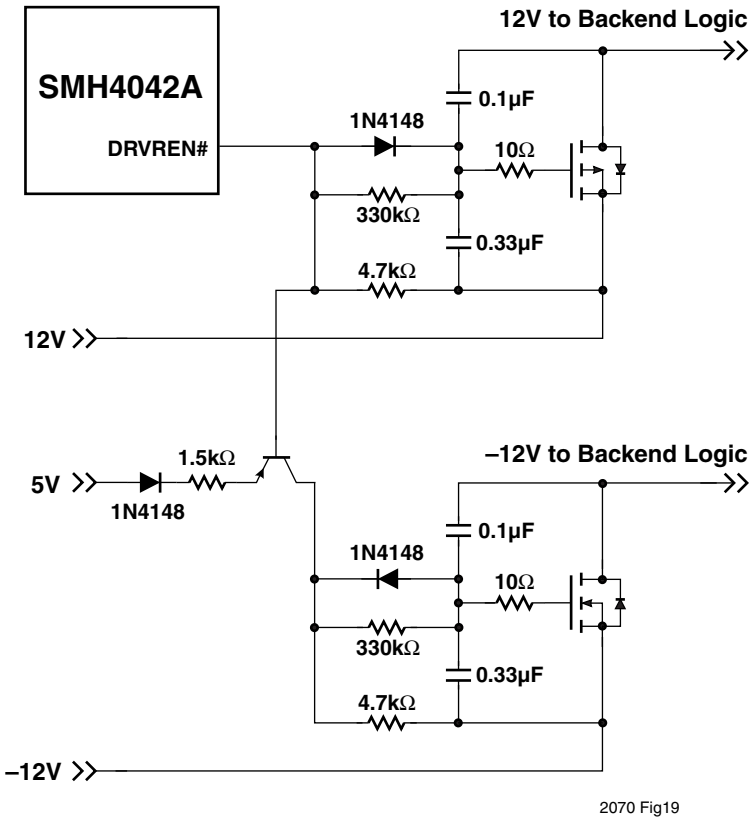


Figure 19. Using DRVREN# to switch 12V and –12V to the Backend Logic

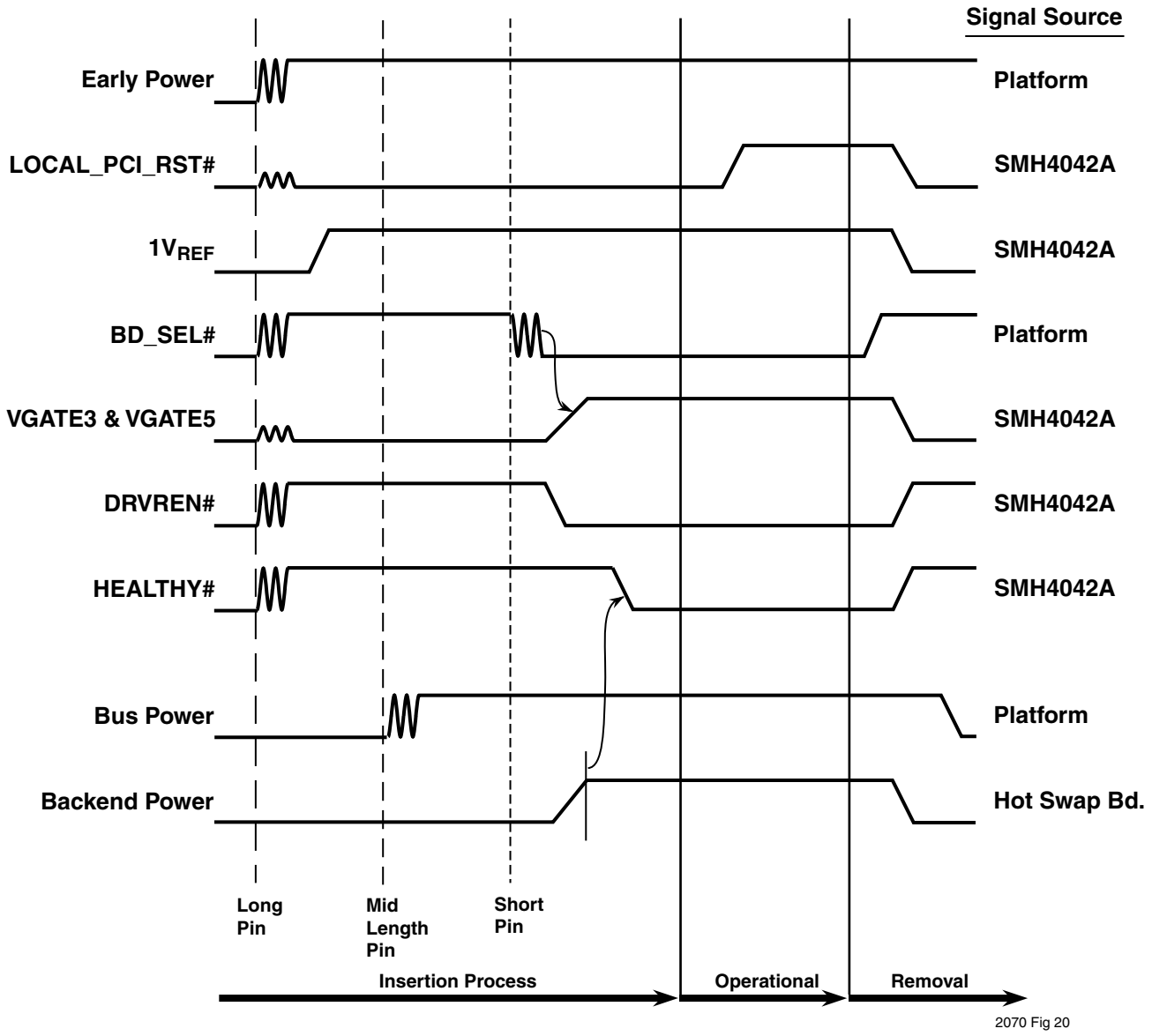


Figure 20. Typical *CompactPCI* Power On Sequence for a Non-High Availability System

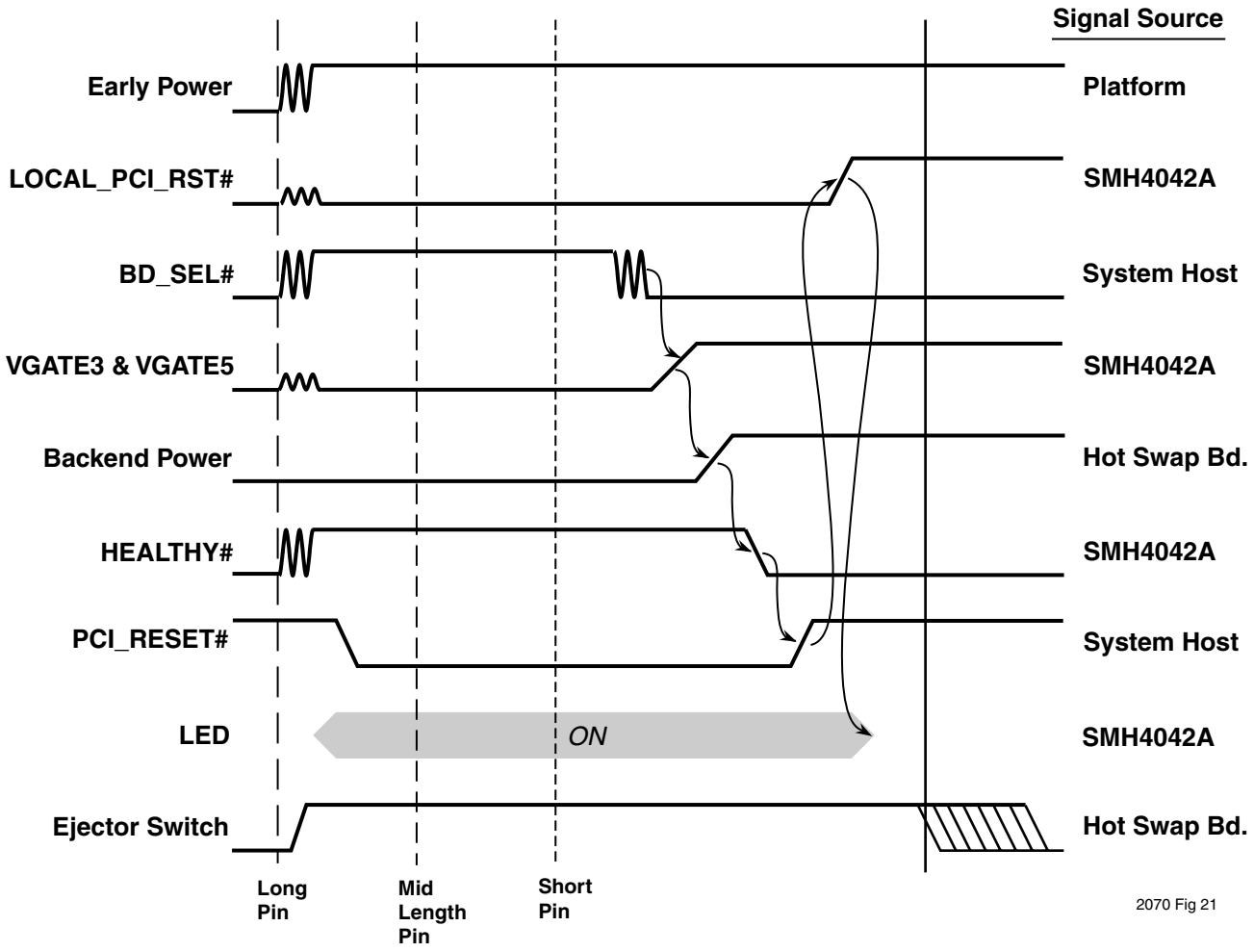


Figure 21. Typical *CompactPCI* Power On Sequence for a Full Hot Swap Board Using the S39421

Although the primary application for the SMH4042A is as a voltage controller for ***CompactPCI*** or VME boards, it is versatile enough to be used as a Hot Plug controller on a host PCI card. The functional blocks are similar to those of the ***CompactPCI*** implementation but they are now resident on the motherboard. The same circuits shown for switching the voltages on the card can also be used for controlling the slot voltages.

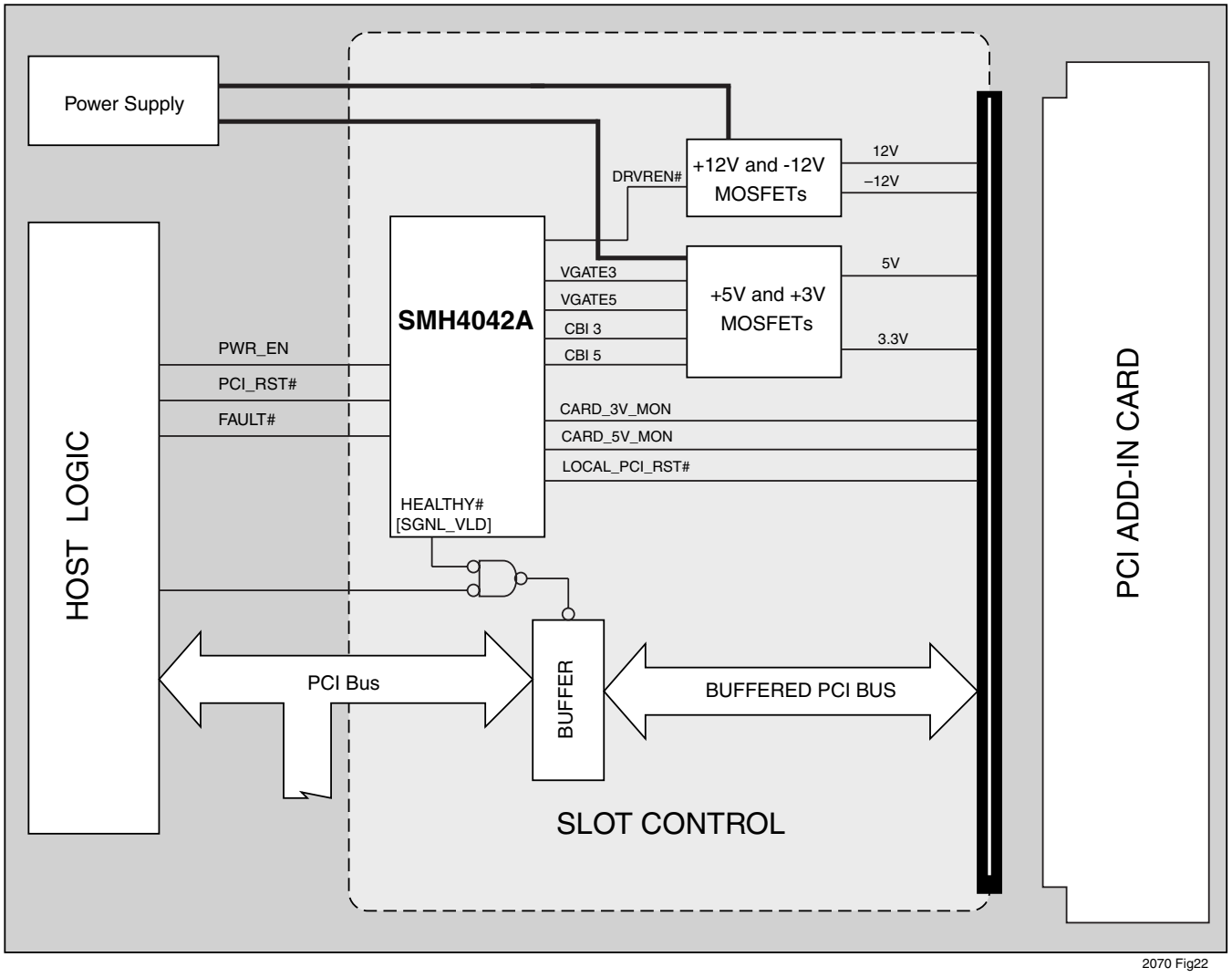


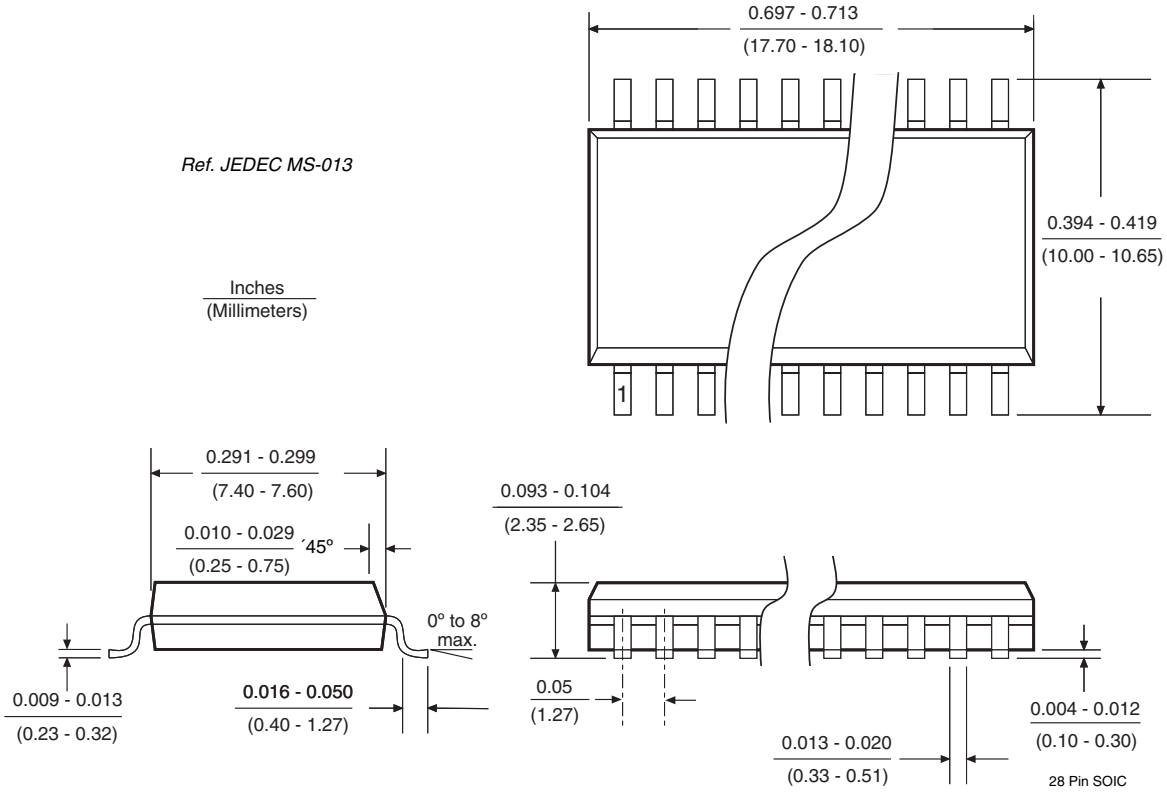
Figure 22. Diagram for a PCI Hot Plug Slot Implementation

PACKAGES

28 PIN SOIC PACKAGE

Ref. JEDEC MS-013

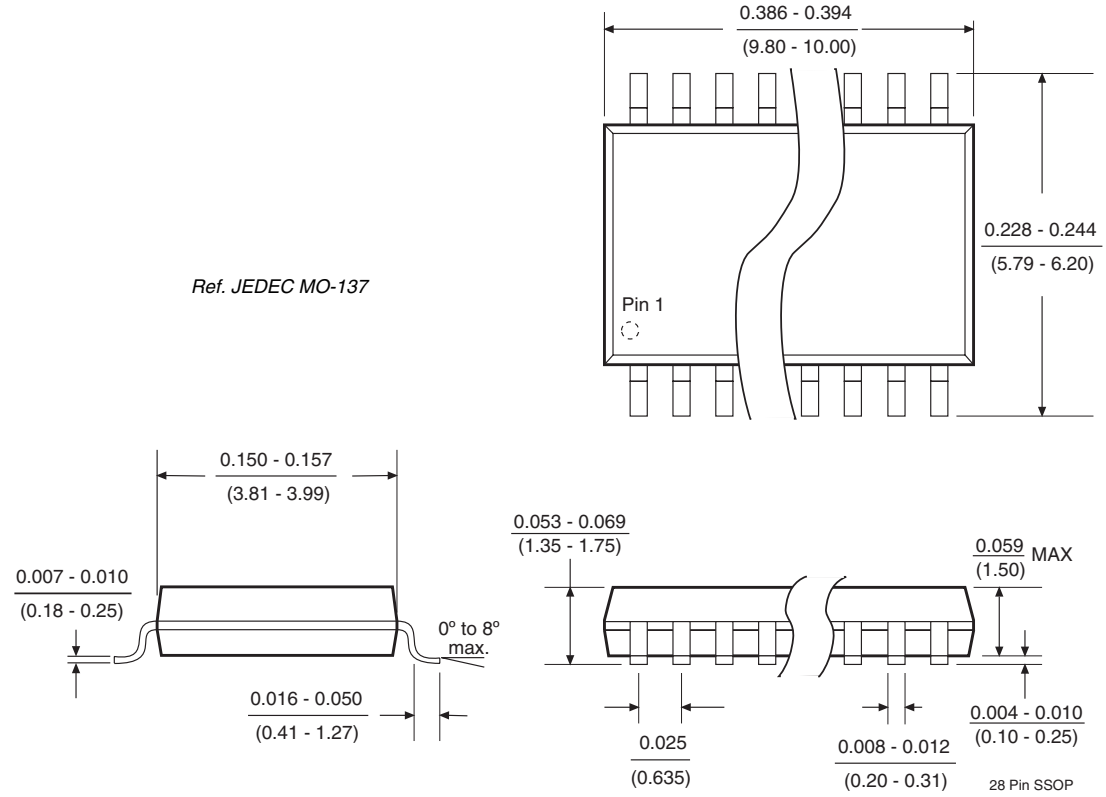
Inches
(Millimeters)



28 Pin SOIC

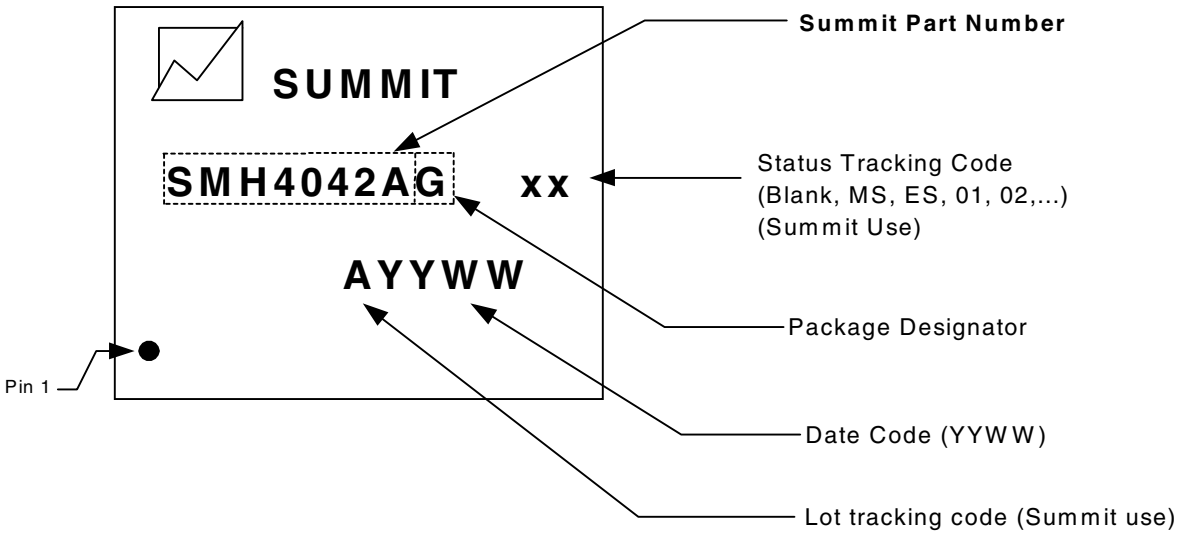
28 PIN SSOP PACKAGE

Ref. JEDEC MO-137



28 Pin SSOP

ORDERING INFORMATION



Drawing not to scale

ORDERING INFORMATION

SMH4042A G A G M

Summit Part Number

Package
G=28 Lead SSOP
S=28 Lead SOIC

$V_{TRIP}V_{CC}5$
A=4.375V
B=4.625V

V_{TRIP}HST_3V_MON
G=2.65V
H=2.80V
K=2.95V
L=3.10V

V_{TRIP}OFFSET
M=+50mV
N=-50mV

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