QL5130 QuickPCI Data Sheet

QUICKLOGIC

● ● ● ● ● ● **33 MHz/32-Bit PCI Target with Embedded Programmable Logic and Dual Port SRAM**

Device Highlights

High Performance PCI Controller

- 32-bit/33 MHz PCI Target

- Zero-wait-state PCI Target provides 132 MBps transfer rates

- Programmable backend interface to optional local processor

- Independent PCI bus (33 MHz) and local bus (up to 160 MHz) clocks

- Fully customizable PCI configuration space

- Configurable FIFOs with depths up to 128

- Reference design with driver code (Win 95/98/2000/NT4.0) available

- PCI v2.2 compliant

- Supports Type 0 configuration cycles

- 3.3 V, 5 V tolerant PCI signaling supports universal PCI adapter designs

- 3.3 V CMOS in 144-pin TQFP, 208-pin PQFP and 256-PBGA

- Supports endian conversions

- Unlimited continuous burst transfers supported

Extendable PCI Functionality

- Support for configuration space from 0x40 to 0x3FF

- Power management, compact PCI, hot-swap/hot-plug compatible

- PCI v2.2 Power Management Spec compatible

- PCI v2.2 Vital Product Data (VPD) configuration support

Programmable Logic

- 57 K system gates/619 logic cells

- 13,824 RAM bits, up to 157 I/O pins

- 250 MHz 16-bit counters, 275 MHz datapaths, 160 MHz FIFOs

- All backend interface and glue-logic can be implemented on chip

- Six 64-deep FIFOs (two RAMs each) or three 128-deep FIFOs (four RAMs each) or a combination that requires twelve or less QuickLogic RAM modules

- Two 32-bit busses interface between the PCI controller and the programmable logic

Figure 1: QL5130 Block Diagram
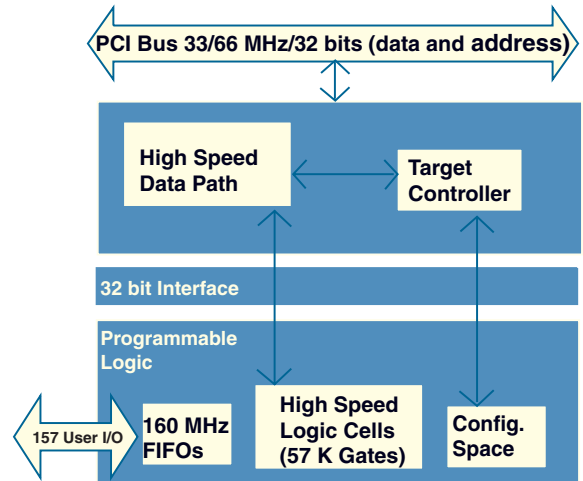
Architecture Overview

The QL5130 device in the QuickLogic QuickPCI Embedded Standard Product (ESP) family provides a complete and customizable PCI interface solution combined with 57,000 system gates of programmable logic. This device eliminates any need for the designer to worry about PCI bus compliance, yet allows for the maximum 32-bit PCI bus bandwidth (132 MBps).

The programmable logic portion of the device contains 619 QuickLogic logic cells and 12 QuickLogic dual-port RAM blocks. These configurable RAM blocks can be configured in many width/depth combinations. They can also be combined with logic cells to form FIFOs, or be initialized via Serial EEPROM on power-up and used as ROMs. See **RAM Module Features** on page 7 for more information.

The QL5130 device meets PCI v2.2 electrical and timing specifications and has been fully hardware-tested. The QL5130 device features 3.3 V operation with multi-volt compatible I/Os. Therefor, it can easily operate in 3.3 V systems and is fully compatible with 3.3 V, 5 V and Universal PCI card development.

PCI Interface

The PCI target is PCI v2.2 compliant and supports 32-bit/33 MHz operation. It is capable of zero wait-state infinite-length read and write transactions (132 MBps). Transaction control is available via the user interface as retries, wait-states, or premature transaction termination may be induced if necessary. The PCI configuration registers are implemented in the programmable region of the device, leaving the designer with ample flexibility to support optional features.

The QL5130 device supports maximum 32-bit PCI transfer rates, so many applications exist which are ideally suited to the device's high performance. High-speed data communications, telecommunications, and computing systems are just a few of the broad range of applications areas that can benefit from the high speed PCI interface and programmable logic.

PCI Configuration Space

The QL5130 supports customization of required Configuration Registers such as Vendor ID, Device ID, Subsystem Vendor ID, etc. QuickLogic provides a reference Configuration Space design block.

Since the PCI Configuration Registers are implemented in the programmable region of the QL5130, the designer can implement optional features such as multiple 32-bit Base Address Registers (BARs) and multiple functions, as well as support the following PCI commands: I/O Read, I/O Write, Memory Read, Memory Write, Config Read (required), Configuration Write (required), Memory Read Multiple, Memory Read Line, and Memory Write and Invalidate. Additionally, the device supports Extended Capabilities Registers, Expansion ROMs, power management, CompactPCI hot-plug/hot-swap, Vital Product Data, I_20, and mailbox registers.

Address and Command Decode

PCI address and command decoding is performed by logic in the programmable section of the device. This allows support for any size of memory or I/O space for backend logic. It also allows the designer to implement any subset of the PCI commands supported by the QL5130. QuickLogic provides a reference Address Register/Counter and Command Decode block.

Architecture Overview

The RAM modules in the programmable region can be used to create configurable 32-bit FIFOs. Each 32-bit FIFO can be independently assigned to Target address space for read pre-fetch or write posting. Using the 12 QuickLogic RAM modules, the combinations include:

- 6 independent 64-deep FIFO (2 RAMs each), or

- 3 independent 128-deep FIFOs (4 RAMs each), or

- a combination of the above that requires 12 or less QuickLogic RAM Modules

Asynchronous FIFOs (with independent read and write clocks) are also supported.

QuickWorks SpDE has a Creation Wizard that is used to create FIFOs.

Internal PCI Interface

The symbol used to connect to the PCI interface of the QL5130 is shown in **Figure 2**. This symbol is used in schematic or mixed schematic/HDL design flows in the QuickWorks software.

Figure 2: PCI Interface Symbol
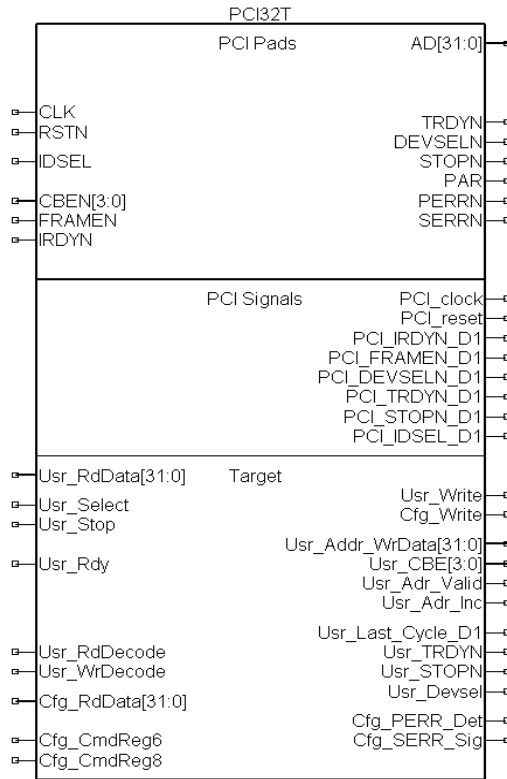
Internal Interface Signal Descriptions

Signals used to connect to the PCI interface in the QL5130 are described in **Table 1**. The direction of the signal indicates if it is an input provided by the local interface (I) or an output provided by the PCI interface (O).

Table 1: QL5130 PCI32T Target Interface Signals

Signal	Type	Description
Usr_Addr_WrData[31:0]	O	Target address and target write data. During all target accesses, the address is presented on Usr_Addr_WrData[31:0] at the same time Usr_Adr_Valid is active. During target write transactions, this port also presents valid write data to the PCI configuration space or user logic when Usr_Adr_Inc is active. During master read transactions, this port also presents valid data read from PCI to the backend. This is the registered version of the PCI AD[31:0] signal.
Usr_CBE[3:0]	O	PCI command and byte enables. During target accesses, the PCI command is presented on Usr_CBE[3:0] at the same time Usr_Adr_Valid is active. This port also presents active-low byte enables to the PCI configuration space or user logic. This is the registered version of the PCI CBEN[3:0] signal.
Usr_Adr_Valid	O	Indicates the beginning of a PCI transaction, and that a target address is valid on Usr_Addr_WrData[31:0] and the PCI command is valid on Usr_CBE[3:0]. When this signal is active, the target address must be latched and decoded to determine if this address belongs to the device memory or I/O space. Also, the PCI command must be decoded to determine the type of PCI transaction. On subsequent clocks of a target access, this signal is low, indicating that the address is no longer on Usr_Addr_WrData[31:0].
Usr_Adr_Inc	O	This signal, when asserted, indicates that the target address should be incremented, because the previous data transfer has completed. During burst target accesses, the target address is only presented to the backend at the beginning of the transaction when Usr_Adr_Valid is active, and must therefore be latched and incremented (by 4) for subsequent data transfers. For target write transactions, Usr_Adr_Inc indicates valid data on Usr_Addr_WrData[31:0] that must be accepted by the backend logic (regardless of the state of Usr_Rdy). For read transactions, Usr_Adr_Inc signals to the backend that the core has presented the read data on the PCI bus (has asserted TRDYN).
Usr_RdDecode	I	This signal must be asserted by the backend when a user read command (e.g., Memory Read, Memory Read Line, Memory Read Multiple, I/O Read, etc.) has been decoded from Usr_CBE[3:0]. It is acknowledged by the core only when Usr_Adr_Valid is active.
Usr_WrDecode	I	This signal must be asserted by the backend when a user write command (e.g., Memory Write, Memory Write and Invalidate, I/O Write, etc.) has been decoded from Usr_CBE[3:0]. It is acknowledged by the core only when Usr_Adr_Valid is active.
Usr_Select	I	This signal must be driven active when the address on Usr_Addr_WrData[31:0] has been decoded and determined to be within the address space of the device. Usr_Addr_WrData[31:0] must be compared to each of the valid Base Address Registers in the PCI configuration space. Also, this signal must be gated by the Memory Access Enable or I/O Access Enable registers in the PCI configuration space (Command Register bits 1 or 0 at offset 04h). This signal is acknowledged by the core only when Usr_Adr_Valid is active.
Usr_Write	O	This signal is active throughout a "user write" transaction, which has been decoded by Usr_WrDecode at the beginning of the transaction. The write strobe for individual DWORDs of data (on Usr_Addr_WrData[31:0]) during a user write transaction should be generated by logically ANDing this signal with Usr_Adr_Inc.
Cfg_Write	O	This signal is active throughout a "configuration write" transaction. The write strobe for individual DWORDs of data (on Usr_Addr_WrData[31:0]) during a configuration write transaction should be generated by logically ANDing this signal with Usr_Adr_Inc.
Cfg_RdData[31:0]	I	Data from the PCI configuration registers, required to be presented during PCI configuration reads.
Usr_RdData[31:0]	I	Data from the backend, required to be presented during user reads.
Cfg_CmdReg6	I	Bits 6 from the Command Register in the PCI configuration space (offset 04h). Parity Error Response. If high, the core uses PERRN to report data parity errors. Otherwise the core always tristates PERRN.

Table 1: QL5130 PCI32T Target Interface Signals (Continued)

Signal	Type	Description
Cfg_CmdReg8	I	Bits 8 from the Command Register in the PCI configuration space (offset 04h). SERRN Enable. If high, the core uses SERRN to report address parity errors if Cfg_CmdReg6 is high. Otherwise the core always tristates SERRN.
Cfg_PERR_Det	O	Parity error detected on the PCI bus. When this signal is active, bit 15 of the Status Register must be set in the PCI configuration space (offset 04h).
Cfg_SERR_Sig	O	System error asserted on the PCI bus. When this signal is active, the Signaled System Error bit, bit 14 of the Status Register, must be set in the PCI configuration space (offset 04h).
Usr_TRDYN	O	Copy of the TRDYN signal as driven by the PCI target interface. Valid only within target accesses to the core.
Usr_STOPN	O	Copy of the STOPN signal as driven by the PCI target interface. Valid only within target accesses to the core.
Usr_DEVSEL	O	Inverted copy of the DEVSELN signal as driven by the PCI target interface. Valid only within target accesses to the core.
Usr_Last_Cycle_D1	O	Active one clock cycle after the last data phase occurs on PCI. Active only for one clock cycle.
Usr_Rdy	I	Used to delay (add wait states to) a target PCI transaction when the backend needs additional time to provide data (read) or accept data (write). Subject to PCI latency restrictions if PCI compliance is needed.
Usr_Stop	I	Used to prematurely stop a PCI target access.

Array of Logic Cells

A wide range of additional features complements the QL5130 device. The FPGA portion of the device is 5 V and 3.3 V PCI-compliant and can perform high-speed logic functions such as 160 MHz FIFOs. I/O pins provide individually controlled output enables, dedicated input/feedback registers, and full JTAG capability for boundary scan and test. In addition, the QL5130 device provides the benefits of nonvolatility, high design security, immediate functionality on power-up, and a single chip solution.

The QL5130 programmable logic architecture consists of an array of user-configurable logic building blocks, called logic cells, set beneath a grid of metal wiring channels similar to those of a gate array (see **Figure 3**). Through ViaLink® elements located at the wire intersections, the output(s) of any cell may be programmed to connect to the input(s) of any other cell. Using the programmable logic in the QL5130, designers can quickly and easily customize their "backend" design for any number of applications.

Figure 3: Logic Cell

RAM Module Features

The QL5130 device has twelve 1,152-bit RAM modules, for a total of 13,824 RAM bits. Using two "mode" pins, designers can configure each module into 64 (deep) x18 (wide), 128x9, 256x4, or 512x2 blocks (see **Figure 4**). The blocks are also easily cascadable to increase their effective width or depth. See **Table 2** for RAM mode configurations.

Figure 4: RAM Module

RAM Module

MODE[1:0]	ASYNCRD
WA[a:0]	RA[a:0]
WD[w:0]	RD[w:0]
WE	RE
WCLK	RCLK

Table 2: RAM Configurations

Mode	Address Buses [a:0]	Data Buses [w:0]
64x18	[5:0]	[17:0]
128x9	[6:0]	[8:0]
256x4	[7:0]	[3:0]
512x2	[8:0]	[1:0]

The RAM modules are dual-ported, with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 9 address lines, allowing word lengths of up to 18 bits and address spaces of up to 512 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules. This approach allows up to 512-deep configurations as large as 28 bits wide in the QL5130 device.

A similar technique can be used to create depths greater than 512 words. In this case, address signals higher than the eighth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

JTAG Support

JTAG pins support IEEE standard 1149.1a to provide boundary scan capability for the QL5130 device. Six pins are dedicated to JTAG and programming functions on each QL5130 device, and are unavailable for general design input and output signals. TDI, TDO, TCK, TMS, and TRSTB are JTAG pins. A sixth pin, STM, is used only for programming.

Development Tools

Software support for the QL5130 device is available through the QuickWorks® development package. QuickWorks is fully integrated into the Windows 98, 2000, NT, ME and XP operating systems. It provides design, layout, pre- and post-layout simulation and external stimulus design tools as shown in **Figure 5**. The program that links all these applications together and acts as the design flow manager is called Seamless pASIC Design Environment (SpDE). The term "pASIC" is a registered trademark of QuickLogic Corporation and refers to a QuickLogic FPGA, or "programmable ASIC."

QuickWorks can be used to perform the following functions in the design process:

- Design
- Pre-layout Simulation
- Synthesis
- Placement and Optimization
- Post-layout Simulation

Figure 5: QuickWorks Design Flow
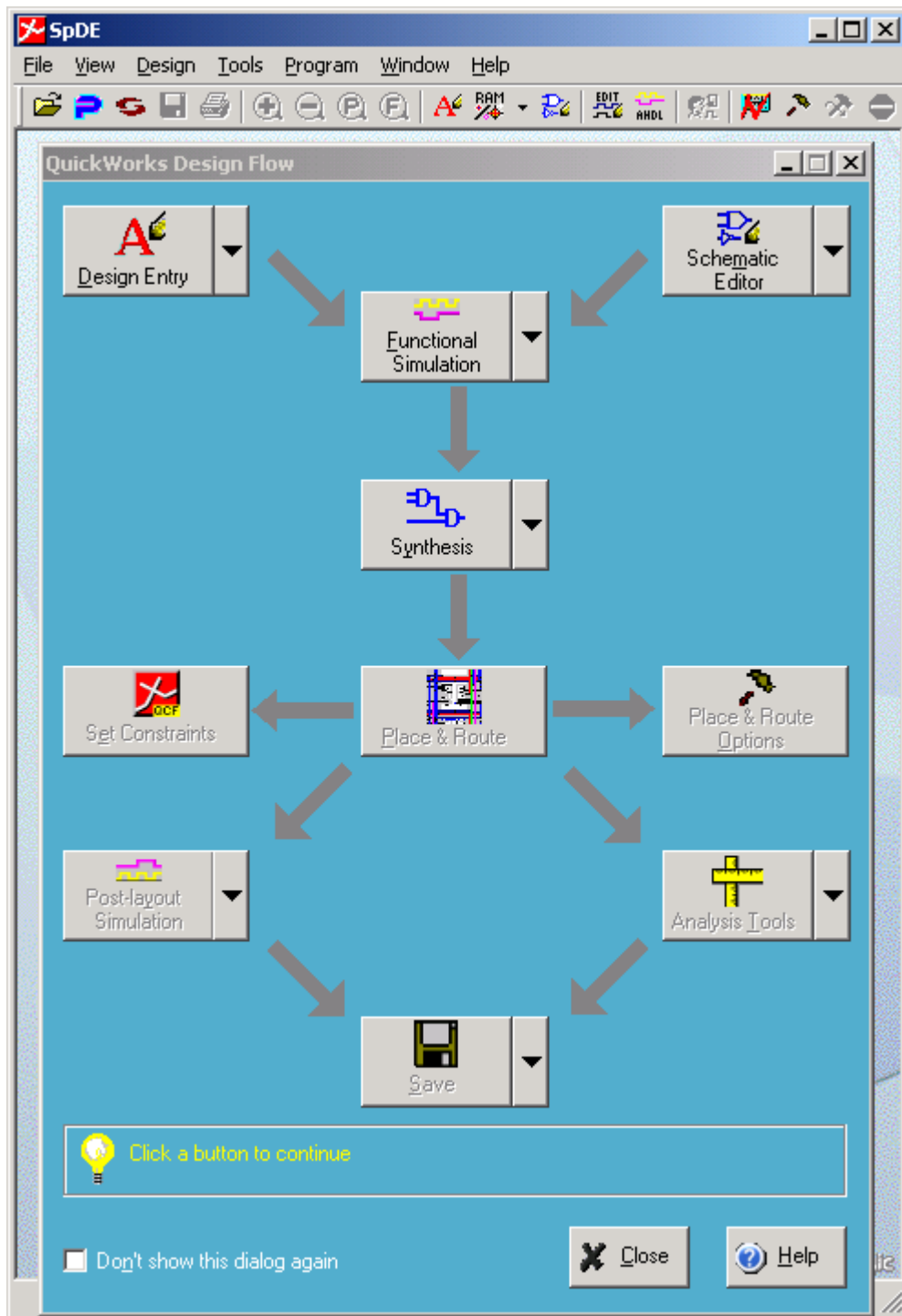
The UNIX-based QuickTools™ package is a subset of QuickWorks and provides a solution for designers who use schematic-only design flow third-party tools for design entry, synthesis, or simulation. QuickTools reads EDIF netlists and provides support for all QuickLogic devices. QuickTools also supports a wide range of third-party modeling and simulation tools.

QL5130 External Device Pins

Table 3 describes the different types of devices pins. **Table 4** describes the external pins on the QL5130 device, some of which connect to the PCI bus, and others that are programmable as user IO.

Table 3: Pin Types

Type	Description
IN	Input. A standard input-only signal
OUT	Totem pole output. A standard active output driver
T/S	Tri-state. A bi-directional, tri-state input/output pin
S/T/S	Sustained Tri-state. An active low tri-state signal driven by one PCI agent at a time. It must be driven high for at least one clock before being disabled (set to Hi-Z). A pull-up needs to be provided by the PCI system central resource to sustain the inactive state once the active driver has released the signal.
O/D	Open Drain. Allows multiple devices to share this pin as a wired-or.

Table 4: QL5130 External Device Pins

Pin/Bus Name	Type	Function
VCC	IN	Supply pin. Tie to 3.3V supply.
VCCIO	IN	Supply pin for I/O. Set to 3.3V for 3.3V I/O, 5V for 5.0V compliant I/O
GND	IN	Ground pin. Tie to GND on the PCB.
I/O	T/S	Programmable Input/Output/Tri-State/Bi-directional Pin.
GLCK/I	IN	Programmable Global Network or Input-only pin. Tie to VCC or GND if unused.
ACLK/I	IN	Programmable Array Network or Input-only pin. Tie to VCC or GND if unused.
TDI/RSI[a]	IN	JTAG Data In/Ram Init. Serial Data In. Tie to VCC if unused. Connect to Serial EPROM data for RAM init.
TDO/RCO[a]	OUT	JTAG Data Out/Ram Init Clock. Leave unconnected if unused. Connect to Serial EPROM clock for RAM init.
TCK	IN	JTAG Clock. Tie to GND if unused.
TMS	IN	JTAG Test Mode Select. Tie to VCC if unused.
TRSTB/RRO[a]	IN	JTAG Reset/RAM Init. Reset Out. Tie to GND if unused. Connect to Serial EPROM reset for RAM init.
STM	IN	QuickLogic Reserved pin. Tie to GND on the PCB.
AD[31:0]	T/S	PCI Address and Data: 32 bit multiplexed address/data bus.
CBEN[3:0]	T/S	PCI Bus Command and Byte Enables: Multiplexed bus which contains byte enables for AD[31:0] or the Bus Command during the address phase of a PCI transaction.
PAR	T/S	PCI Parity: Even Parity across AD[31:0] and C/BEN[3:0] busses. Driven one clock after address or data phases. Master drives PAR on address cycles and PCI writes. The Target drives PAR on PCI reads.
FRAMEN	S/T/S	PCI Cycle Frame: Driven active by current PCI Master during a PCI transaction. Driven low to indicate the address cycle, driven high at the end of the transaction.
DEVSELN	S/T/S	PCI Device Select. Driven by a Target that has decoded a valid base address.
CLK	IN	PCI System Clock Input.
RSTN	IN	PCI System Reset Input
PERRN	S/T/S	PCI Data Parity Error. Driven active by the initiator or target two clock cycles after a data parity error is detected on the AD and C/BEN busses.
SERRN	O/D	PCI System Error: Driven active when an address cycle parity error, data parity error during a special cycle, or other catastrophic error is detected.
IDSEL	IN	PCI Initialization Device Select. Use to select a specific PCI Agent during System Initialization.
IRDYN	S/T/S	PCI Initiator Ready. Indicates the Initiator's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
TRDYN	S/T/S	PCI Target Ready. Indicates the Target's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
STOPN	S/T/S	PCI Stop. Used by a PCI Target to end a burst transaction.

a. See Quick Note 65 at http://quicklogic.com/images/quicknote65.pdf for information on RAM initialization.

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 5** through **Table 7**.

Table 5: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
VCCIO Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to VCCIO + 0.5 V	Storage Temperature	-65°C to + 150°C
Latch-up Immunity	±200 mA	Lead Temperature	300° C

Table 6: Operating Range

Symbol	Parameter		Industrial		Commercial		Unit
			Min	Max	Min	Max	
VCC	Supply Voltage		3.0	3.6	3.0	3.6	V
VCCIO	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-40	85	0	70	°C
K	Delay Factor	-A Speed Grade	0.43	0.90	0.46	0.88	n/a

Table 7: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
VIH	Input HIGH Voltage		0.5 VCC	VCCIO+ 0.5	V
VIL	Input LOW Voltage		-0.5	0.3 VCC	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 µA	0.9 VCC		V
VOL	Output LOW Voltage	IOL = 16 mA		0.45	V
		IOL = 1.5 mA		0.1 VCC	V
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-10	10	µA
CI	I/O Input Capacitance[a]	-	-	10	pF
IOS	Output Short Circuit Current[b]	VO = GND VO = VCC	-15 40	-180 210	mA mA
ICC	D.C. Supply Current[c]	VI.VIO = VCCIO or GND	0.50 typ.	2	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	µA

a. Capacitance is sample tested only. Clock pins are 12 pF maximum.
b. Only one output at a time. Duration should not exceed 30 seconds.
c. For -A commercial grade device only. Maximum ICC is 3 mA for all industrial grade devices. For AC conditions, contact QuickLogic Customer Engineering.

AC Characteristics

The AC Specifications (at VCC = 3.3 V, TA = 25° C (K = 1.00)) are provided in **Table 8** through **Table 15**.

(To calculate delays, multiply the appropriate K factor in **Table 6** operating ranges by the following numbers.)

Table 8: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	**2**	**3**	**4**	**5**
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output[b]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge[b]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock-to-Q delay: the amount of time taken by the flip-flop to output after the active clock edge.	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time: required minimum time the clock stays high	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time: required minimum time that the clock stays low	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay: time between when the flip-flop is "set" (high) and when the output is consequently "set" (high)	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width: time that the SET signal must remain high/low	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width: time that the RESET signal must remain high/low	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at VCC=3.3 V and TA=25×C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.
b. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 9: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	5
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0.0	0.0	0.0	0.0	0.0
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0.0	0.0	0.0	0.0	0.0
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0.0	0.0	0.0	0.0	0.0
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	5.0	5.3	5.6	5.9	7.1

a. Stated timing for worst case Propagation Delay over process variation at VCC=3.3 V and TA=25×C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 10: RAM Cell Synchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0.0	0.0	0.0	0.0	0.0
t_{SRE}	RE setup time to RCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HRE}	RE hold time to RCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0.0	0.0	0.0	0.0	0.0
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD[a]	4.0	4.3	4.6	4.9	6.1

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 11: RAM Cell Synchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
r$_{PDRD}$	RA to RD: time between when the READ ADDRESS is input and when the DATA is output[a]	3.0	3.3	3.6	3.9	5.1

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 12: Input-Only Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	12	24
t$_{IN}$	High drive input delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t$_{INI}$	High drive input, inverting delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t$_{ISU}$	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t$_{IH}$	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t$_{ICLK}$	Input register clock-to-Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t$_{IRST}$	Input register reset delay: time between when the flip-flop is "reset"(low) and when the output is consequently "reset" (low)	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t$_{IESU}$	Input register clock enable setup time: time "enable" must be stable before the active clock edge	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t$_{IEH}$	Input register clock enable hold time: time "enable" must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 13: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	10	11
t_{ACK}	Array clock delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global clock pin delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global clock buffer delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.

Table 14: I/O Cell Input Delays

Symbol	Parameter	Propagation Delays (ns) Fanout[a]					
		1	2	3	4	8	10
$t_{I/O}$	Input delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input register clock-to-Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input register reset delay: time between when the flip-flop is "reset"(low) and when the output is consequently "reset" (low)	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input register clock enable setup time: time "enable" must be stable before the active clock edge	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input register clock enable hold time: time "enable" must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 15: I/O Cell Output Delays

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay low to high (90% of H)	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay high to low (10% of L)	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay tri-state to high (90% of H)	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay tri-state to low (10% of L)	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay high to tri-State[a]	2.0				
t_{PLZ}	Output Delay low to tri-State[a]	1.2				

a. The following loads are used for t_{PXZ}:
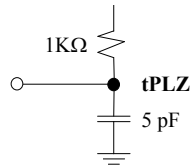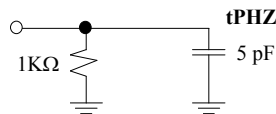
QL5130 - 144 TQFP Pinout Diagram

Figure 6: 144-pin TQFP

PIN #1

PIN #109

QuickPCI
QL5130-33APF144C

PIN #37

PIN #73
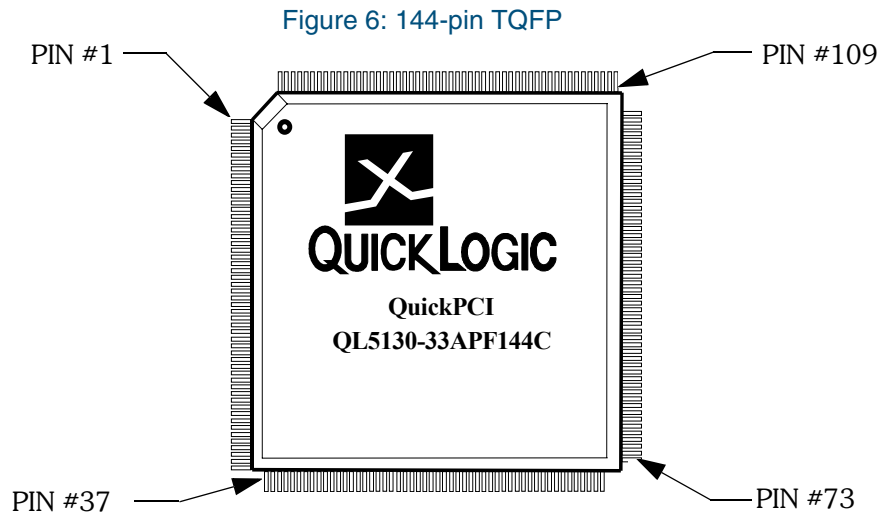
QL5130 - 144 TQFP Pinout Table

Table 16: QL5130 - 144 TQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	37	AD[21]	73	AD[4]	109	TCK
2	I/O	38	TDI/RSI	74	AD[3]	110	STM
3	I/O	39	AD[20]	75	AD[2]	111	I/O
4	I/O	40	AD[19]	76	AD[1]	112	I/O
5	I/O	41	AD[18]	77	AD[0]	113	I/O
6	I/O	42	VCC	78	I/O	114	VCC
7	VCC	43	AD[17]	79	VCC	115	I/O
8	I/O	44	AD[16]	80	I/O	116	I/O
9	I/O	45	CBEN[2]	81	I/O	117	I/O
10	I/O	46	FRAMEN	82	I/O	118	I/O
11	I/O	47	IRDYN	83	I/O	119	I/O
12	I/O	48	TRDYN	84	I/O	120	I/O
13	I/O	49	DEVSELN	85	I/O	121	I/O
14	I/O	50	GND	86	I/O	122	GND
15	GND	51	STOPN	87	GND	123	I/O
16	I/O	52	PERRN	88	I/O	124	I/O
17	GCLK/I	53	SERRN	89	GCLK/I	125	I/O
18	ACLK/I	54	GND	90	ACLK/I	126	GND
19	VCC	55	PAR	91	VCC	127	I/O
20	RSTN	56	CBEN[1]	92	GCLK/I	128	I/O
21	CLK	57	AD[15]	93	GCLK/I	129	I/O
22	VCC	58	VCCIO	94	VCC	130	VCCIO
23	I/O	59	AD[14]	95	I/O	131	I/O
24	AD[31]	60	AD[13]	96	I/O	132	I/O
25	AD[30]	61	AD[12]	97	I/O	133	I/O
26	AD[29]	62	AD[11]	98	I/O	134	I/O
27	AD[28]	63	AD[10]	99	I/O	135	I/O
28	AD[27]	64	AD[9]	100	I/O	136	I/O
29	AD[26]	65	AD[8]	101	I/O	137	I/O
30	GND	66	GND	102	GND	138	GND
31	AD[25]	67	CBEN[0]	103	I/O	139	I/O
32	AD[24]	68	AD[7]	104	I/O	140	I/O
33	CBEN[3]	69	AD[6]	105	I/O	141	I/O
34	IDSEL	70	AD[5]	106	I/O	142	I/O
35	AD[23]	71	TRSTB/RRO	107	I/O	143	TDO/RCO
36	AD[22]	72	TMS	108	I/O	144	I/O

Summary: 47 PCI pins, 71 user I/O, 4 GCLK, and 2 ACLK.

QL5130 - 208 PQFP Pinout Diagram

Figure 7: 208-pin PQFP
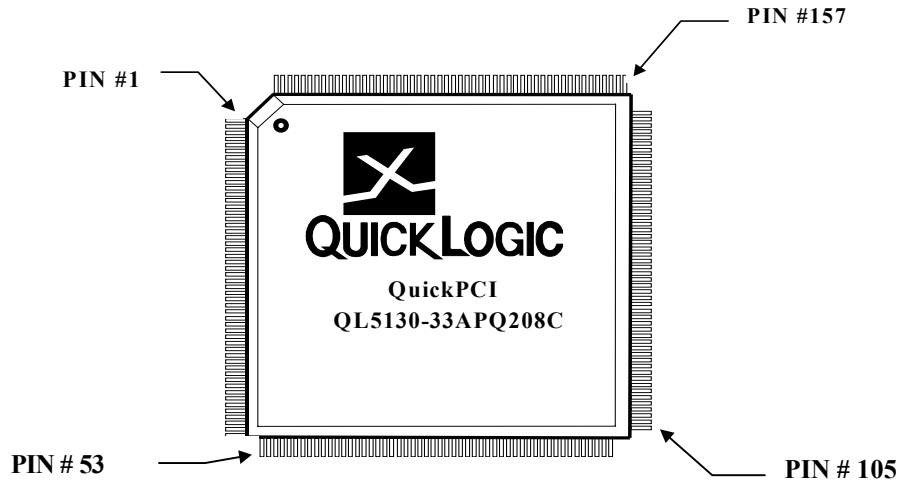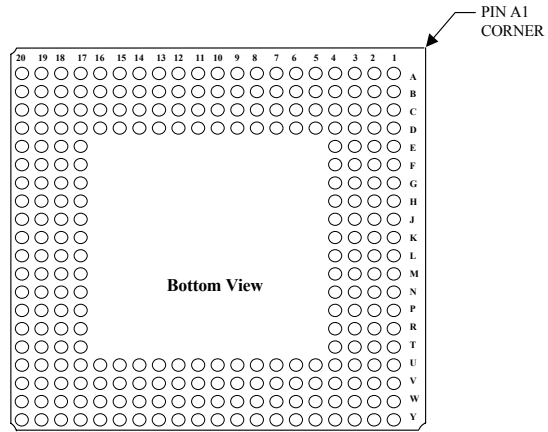
QL5130 - 208 PQFP Pinout Table

Table 17: QL5130 - 208 PQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	36	AD[28]	71	AD[13]	106	I/O	141	I/O	176	I/O
2	I/O	37	AD[27]	72	AD[12]	107	I/O	142	I/O	177	GND
3	I/O	38	AD[26]	73	GND	108	I/O	143	I/O	178	I/O
4	I/O	39	AD[25]	74	AD[11]	109	I/O	144	I/O	179	I/O
5	I/O	40	AD[24]	75	AD[10]	110	I/O	145	VCC	180	I/O
6	I/O	41	VCC	76	AD[9]	111	I/O	146	I/O	181	I/O
7	I/O	42	CBEN[3]	77	AD[8]	112	I/O	147	GND	182	GND
8	I/O	43	GND	78	GND	113	I/O	148	I/O	183	I/O
9	I/O	44	IDSEL	79	CBEN[0]	114	VCC	149	I/O	184	I/O
10	VCC	45	AD[23]	80	AD[7]	115	I/O	150	I/O	185	I/O
11	I/O	46	AD[22]	81	AD[6]	116	GND	151	I/O	186	I/O
12	GND	47	AD[2]1	82	AD[5]	117	I/O	152	I/O	187	VCCIO
13	I/O	48	AD[20]	83	VCCIO	118	I/O	153	I/O	188	I/O
14	I/O	49	AD[19]	84	AD[4]	119	I/O	154	I/O	189	I/O
15	I/O	50	AD[18]	85	AD[3]	120	I/O	155	I/O	190	I/O
16	I/O	51	AD[17]	86	AD[2]	121	I/O	156	I/O	191	I/O
17	I/O	52	AD[16]	87	AD[1]	122	I/O	157	TCK	192	I/O
18	I/O	53	CBEN[2]	88	AD[0]	123	I/O	158	STM	193	I/O
19	I/O	54	TDI	89	I/O	124	I/O	159	I/O	194	I/O
20	I/O	55	FRAMEN	90	I/O	125	I/O	160	I/O	195	I/O
21	I/O	56	IRDYN	91	I/O	126	I/O	161	I/O	196	I/O
22	I/O	57	TRDYN	92	I/O	127	GND	162	I/O	197	I/O
23	GND	58	DEVSELN	93	I/O	128	I/O	163	GND	198	I/O
24	I/O	59	GND	94	I/O	129	GCLK/I	164	I/O	199	GND
25	RSTN	60	STOPN	95	GND	130	ACLK/I	165	VCC	200	I/O
26	ACLK/I	61	VCC	96	I/O	131	VCC	166	I/O	201	VCC
27	CLK	62	I/O	97	VCC	132	GCLK/I	167	I/O	202	I/O
28	GCLK/I	63	I/O	98	I/O	133	GCLK/I	168	I/O	203	I/O
29	CLK	64	PERRN	99	I/O	134	VCC	169	I/O	204	I/O
30	VCC	65	I/O	100	I/O	135	I/O	170	I/O	205	I/O
31	I/O	66	SERRN	101	I/O	136	I/O	171	I/O	206	I/O
32	I/O	67	PAR	102	I/O	137	I/O	172	I/O	207	TDO
33	AD[31]	68	CBEN[1]	103	TRSTB	138	I/O	173	I/O	208	I/O
34	AD[30]	69	AD[15]	104	TMS	139	I/O	174	I/O		
35	AD[29]	70	AD[14]	105	I/O	140	I/O	175	I/O		

Summary: 47 PCI pins, 121 user I/O, 4 GCLK, and 2 ACLK.

QL5130 - 256 PBGA Pinout Diagram

Figure 8: 256-pin PBGA

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QL5130 - 256 PBGA Pinout Table

Table 18: QL5130 - 256 PBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GND	C4	I/O	E19	I/O	L2	ACLK/I	T17	I/O	V20	I/O
A2	I/O	C5	I/O	E20	I/O	L3	RSTN	T18	I/O	W1	I/O
A3	I/O	C6	I/O	F1	I/O	L4	GCLK/I	T19	NC	W2	I/O
A4	I/O	C7	I/O	F2	I/O	L17	VCC	T20	I/O	W3	TDI
A5	I/O	C8	I/O	F3	I/O	L18	I/O	U1	I/O	W4	I/O
A6	I/O	C9	VCCIO	F4	VCC	L19	I/O	U2	I/O	W5	AD[27]
A7	I/O	C10	I/O	F17	VCC	L20	I/O	U3	I/O	W6	CBEN[3]
A8	I/O	C11	I/O	F18	NC	M1	I/O	U4	GND	W7	AD[21]
A9	I/O	C12	I/O	F19	I/O	M2	I/O	U5	AD[26]	W8	AD[20]
A10	I/O	C13	I/O	F20	I/O	M3	I/O	U6	VCC	W9	CBEN[2]
A11	I/O	C14	I/O	G1	I/O	M4	NC	U7	AD[22]	W10	DEVSELN
A12	I/O	C15	I/O	G2	NC	M17	NC	U8	GND	W11	PERRN
A13	I/O	C16	I/O	G3	I/O	M18	I/O	U9	FRAMEN	W12	CBEN[1]
A14	I/O	C17	I/O	G4	I/O	M19	I/O	U10	VCC	W13	PAR
A15	I/O	C18	I/O	G17	I/O	M20	I/O	U11	I/O	W14	AD[10]
A16	I/O	C19	I/O	G18	I/O	N1	I/O	U12	I/O	W15	AD[9]
A17	I/O	C20	I/O	G19	NC	N2	I/O	U13	GND	W16	AD[5]
A18	I/O	D1	I/O	G20	I/O	N3	I/O	U14	AD[11]	W17	AD[1]
A19	TCK	D2	I/O	H1	I/O	N4	GND	U15	VCC	W18	AD[0]
A20	I/O	D3	I/O	H2	I/O	N17	GND	U16	AD[4]	W19	I/O
B1	TDO	D4	GND	H3	I/O	N18	I/O	U17	GND	W20	TRSTB
B2	I/O	D5	I/O	H4	GND	N19	I/O	U18	I/O	Y1	I/O
B3	I/O	D6	VCC	H17	GND	N20	I/O	U19	I/O	Y2	NC
B4	I/O	D7	I/O	H18	I/O	P1	I/O	U20	I/O	Y3	I/O
B5	I/O	D8	GND	H19	I/O	P2	I/O	V1	I/O	Y4	AD[31]
B6	I/O	D9	I/O	H20	I/O	P3	I/O	V2	NC	Y5	AD[29]
B7	I/O	D10	I/O	J1	I/O	P4	I/O	V3	I/O	Y6	AD[25]
B8	I/O	D11	VCC	J2	I/O	P17	I/O	V4	AD[30]	Y7	AD[23]
B9	I/O	D12	I/O	J3	NC	P18	I/O	V5	AD[28]	Y8	AD[19]
B10	I/O	D13	GND	J4	I/O	P19	NC	V6	AD[24]	Y9	AD[17]
B11	I/O	D14	I/O	J17	NC	P20	I/O	V7	IDSEL	Y10	IRDYN
B12	I/O	D15	VCC	J18	I/O	R1	NC	V8	AD[18]	Y11	I/O
B13	I/O	D16	I/O	J19	I/O	R2	I/O	V9	AD[16]	Y12	SERRN
B14	I/O	D17	GND	J20	GCLK/I	R3	I/O	V10	TRDYN	Y13	AD[14]
B15	I/O	D18	I/O	K1	I/O	R4	VCC	V11	STOPN	Y14	AD[12]
B16	I/O	D19	I/O	K2	I/O	R17	VCC	V12	VCCIO	Y15	AD[8]
B17	NC	D20	I/O	K3	I/O	R18	I/O	V13	AD[15]	Y16	AD[7]
B18	STM	E1	NC	K4	VCC	R19	I/O	V14	AD[13]	Y17	AD[3]
B19	NC	E2	I/O	K17	GCLK/I	R20	I/O	V15	CBEN[0]	Y18	I/O
B20	I/O	E3	I/O	K18	ACLK/I	T1	NC	V16	AD[6]	Y19	I/O
C1	I/O	E4	I/O	K19	GCLK/I	T2	I/O	V17	AD[2]	Y20	NC
C2	I/O	E17	I/O	K20	NC	T3	I/O	V18	I/O		
C3	I/O	E18	I/O	L1	CLK	T4	NC	V19	TMS		

Summary: 47 PCI pins, 151 user I/O, 4 GCLK, and 2 ACLK.

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Revision History

Revision	Date	Originator and Comments
Rev. A	September 1999	
Rev. B	December 1999	
Rev. C	July 2004	Bernhard Andretzky and Kathleen Murchek Converted to new format. Added Summary to pinout tables.

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