
PF0231A

MOS FET Power Amplifier Module for ADC Handy Phone

HITACHI

ADE-208-378A (Z)
2nd. Edition
July 1996

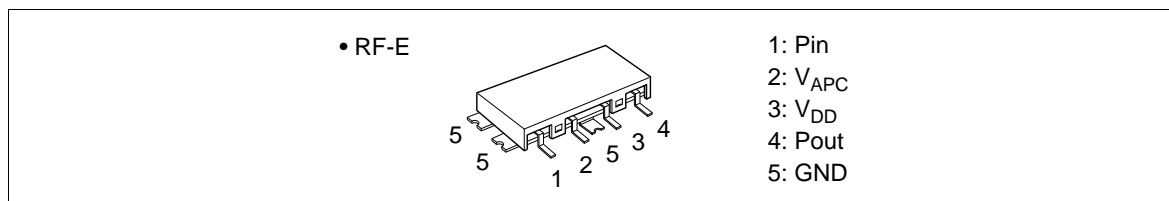
Application

For ADC class3 824 to 849 MHz

Features

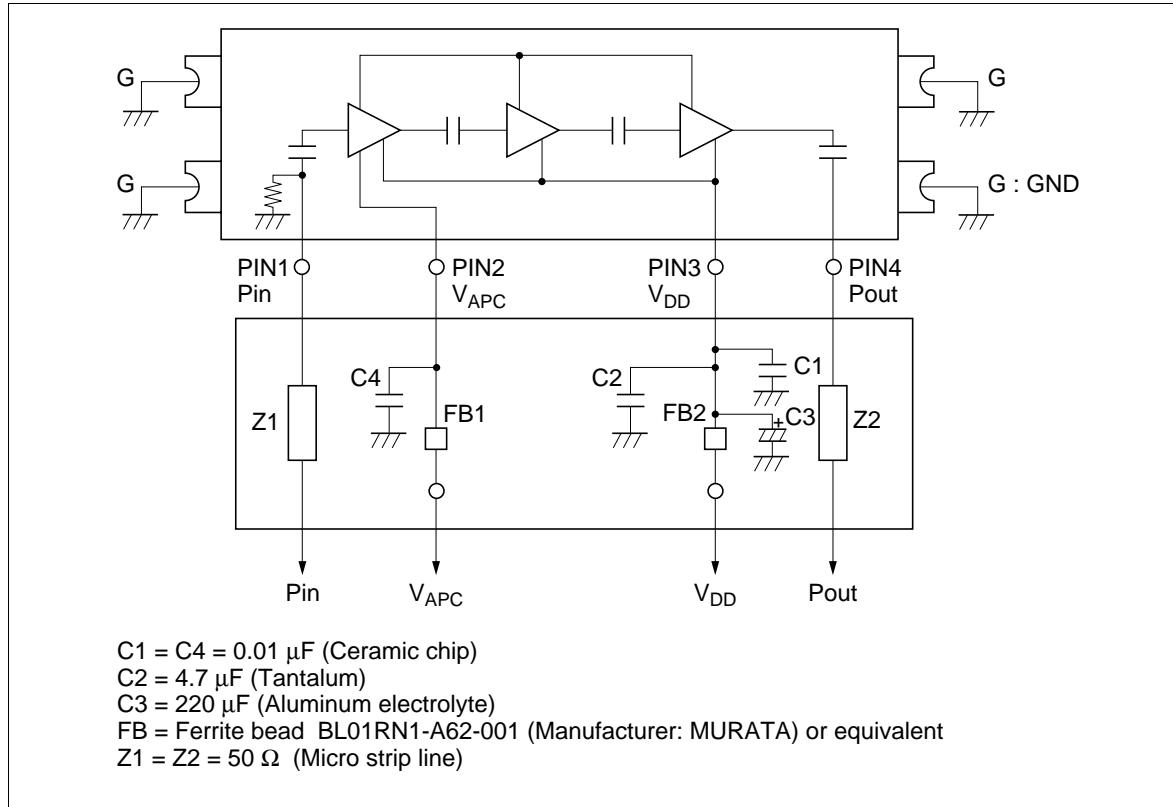
- Low voltage operation 4.8 V
- High efficiency: 42% Typ for CW
34% Typ for $\pi/4$ -DQPSK
- Simple Pout control: Controllable by VAPC
- Low power control current: 600 μ A Typ.

Pin Arrangement



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Internal Diagram and External Circuit



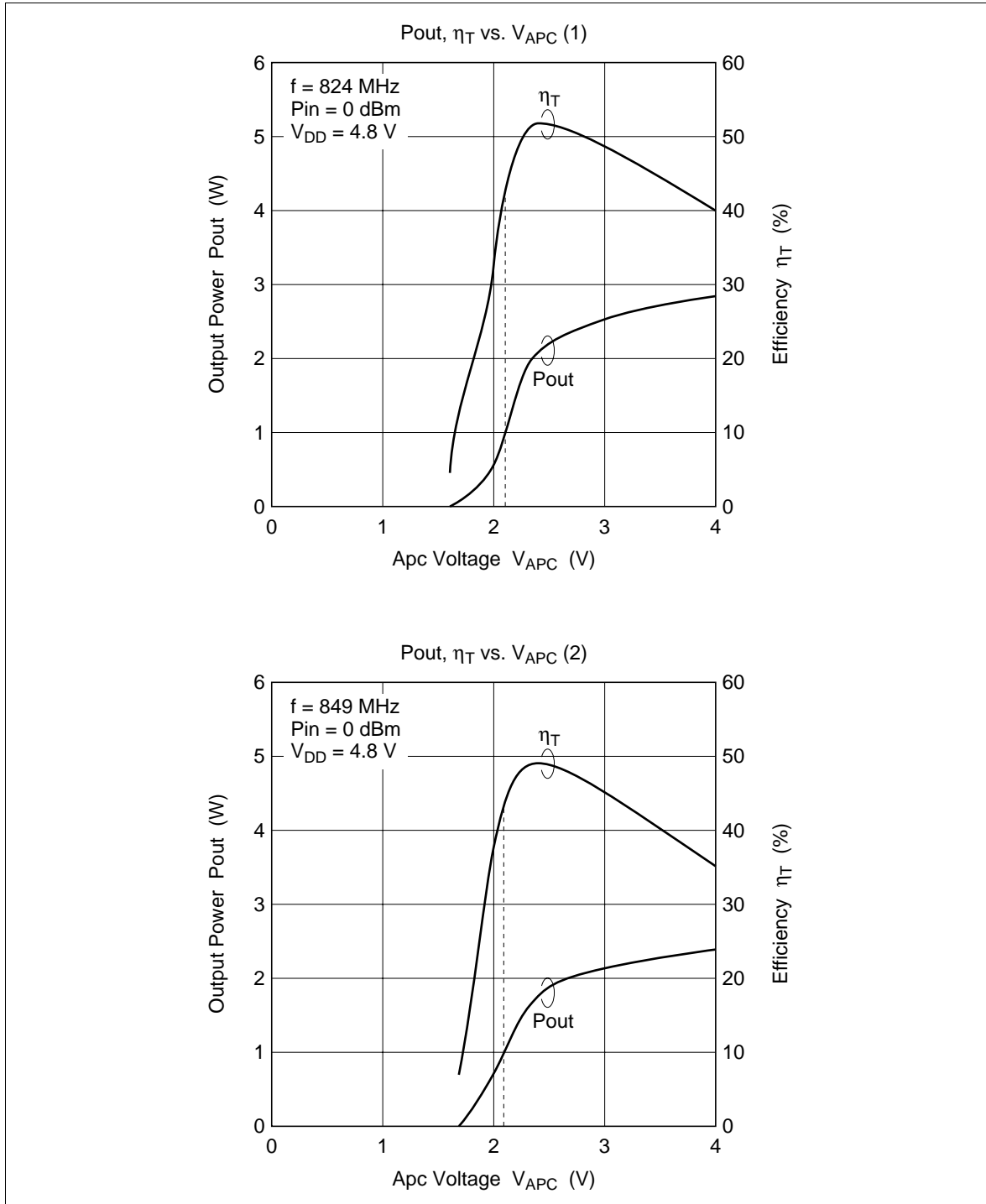
Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$)

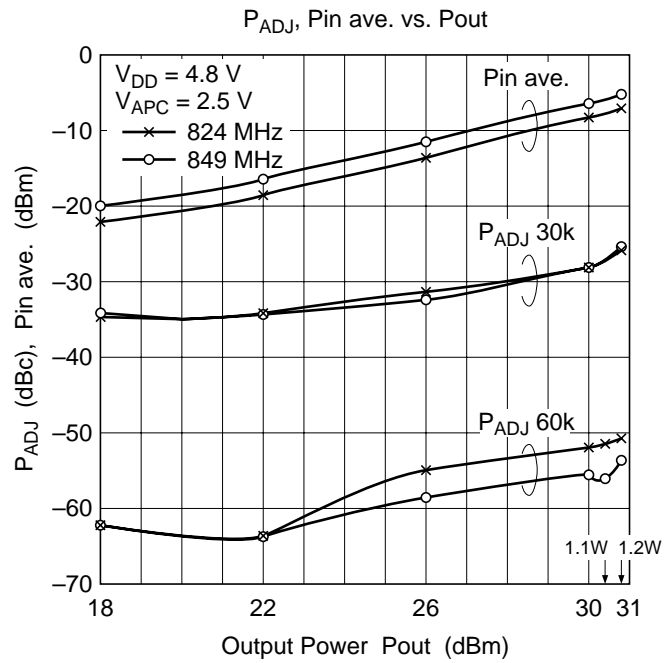
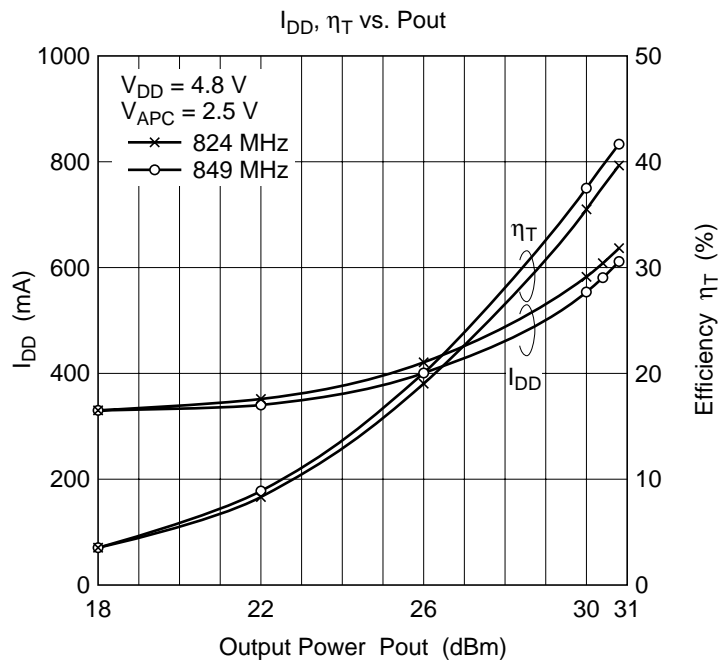
Item	Symbol	Rating	Unit
Supply voltage	VDD	10	V
Supply current	IDD	1.5	A
VAPC voltage	VAPC	4.5	V
Input power	Pin	20	mW
Operating case temperature	T_c (op)	-30 to +100	$^\circ\text{C}$
Storage temperature	T_{stg}	-30 to +100	$^\circ\text{C}$

Electrical Characteristics ($T_c = 25^\circ\text{C}$)

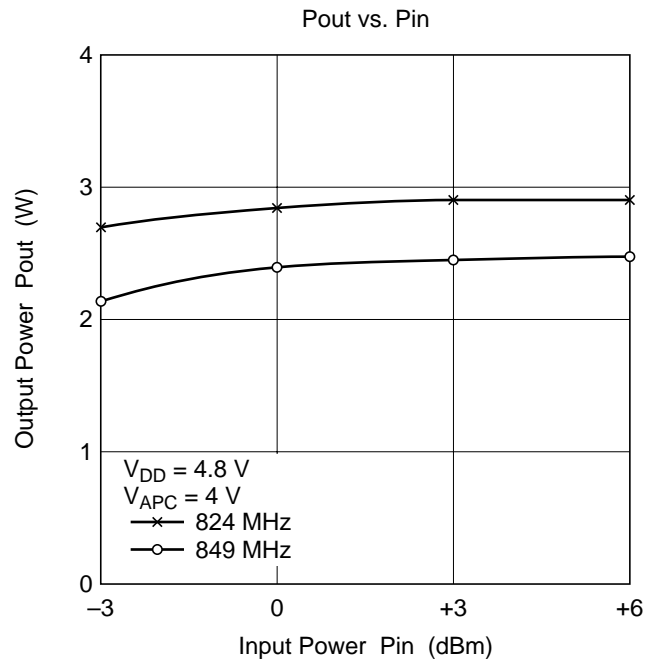
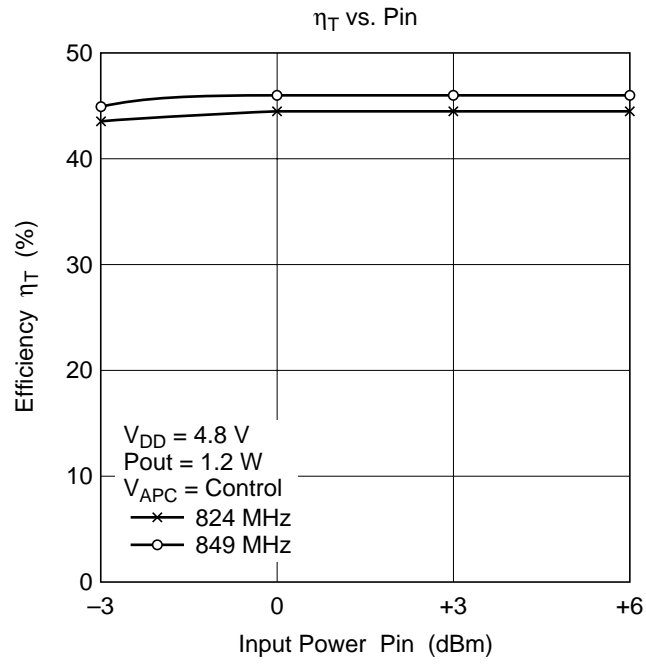
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Frequency range	f	824	—	849	MHz	—
Drain cutoff current	IDS	—	—	100	μA	VDD = 10 V, VAPC = 0 V
Total efficiency(1)	η_T (1)	37	42	—	%	Pin = 1 mW, VDD = 4.8 V,
2nd harmonic distortion	2nd H.D.	—	-35	-30	dBc	Pout = 1.2 W (at VAPC controlled),
3rd harmonic distortion	3rd H.D.	—	-40	-30	dBc	RL = Rg = 50 Ω
Input VSWR	VSWR (in)	—	1.5	3	—	
Output power	Pout	1.6	2.1	—	W	Pin = 1 mW, VDD = 4.8 V, VAPC = 4.0 V, RL = Rg = 50 Ω
Isolation	—	—	-40	-35	dBm	Pin = 1 mW, VDD = 4.8 V, VAPC = 0.5 V, RL = Rg = 50 Ω
Total efficiency(2)	η_T (2)	30	34	—	%	Pin = controlled (p/4-DQPSK, $\sqrt{\alpha} =$
Adjacent channel	PADJ (30k)	—	-30	-27	dBc	0.35, 48.6kbps), BW = 24.3 kHz with
leakage power	PADJ (60k)	—	-55	-47	dBc	R-NYQT, Pout = 1.0 W ave., VDD = 4.8 V, VAPC = 2.5 V
Load VSWR tolerance	—	No degradation			—	Pin = 1 mW, VDD = 6 V, Pout \leq 1.4 W, t = 10 sec., Output VSWR = 20:1 All phases
Stability	—	No parasitic oscillation			—	Pin = 1 mW, VDD = 4 to 6 V, Pout \leq 1.4 W, Output VSWR = 3:1 All phases, Rg = 50 Ω

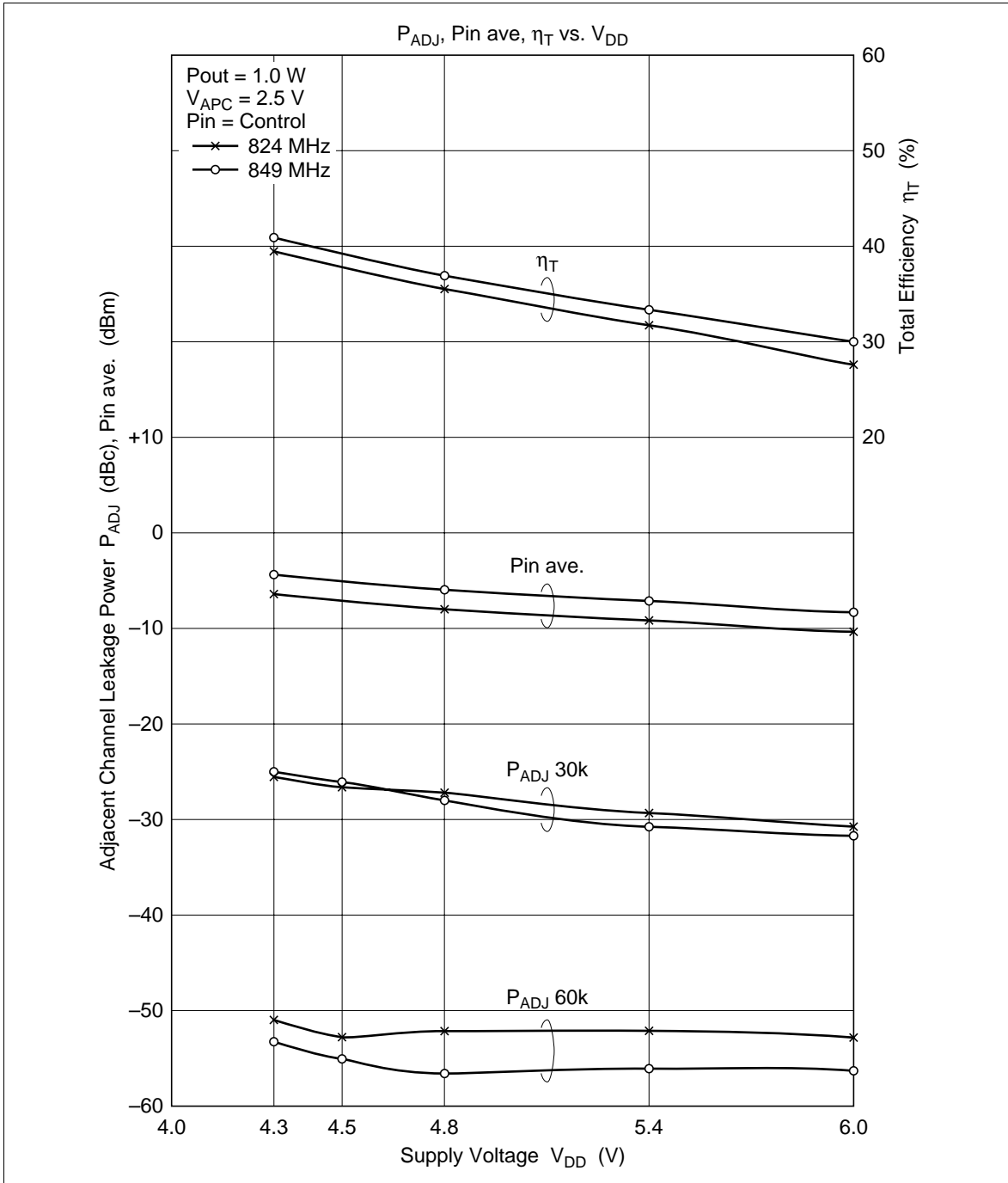
Characteristics Curve



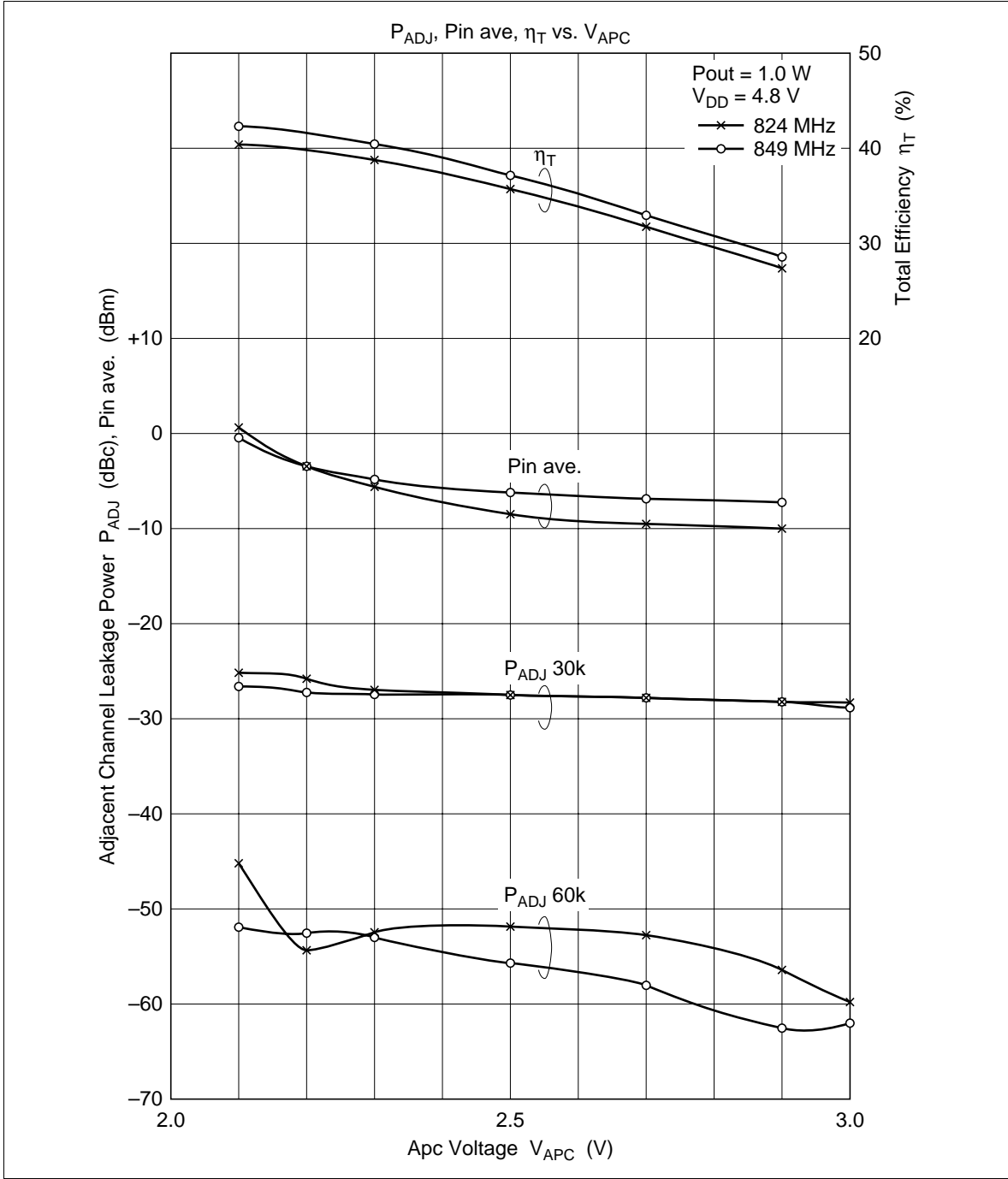


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Package Dimensions

Unit: mm

