NUD3105

Integrated Relay, Inductive Load Driver

This device is used to switch inductive loads such as relays, solenoids incandescent lamps , and small DC motors without the need of a free-wheeling diode. The device integrates all necessary items such as the MOSFET switch, ESD protection, and Zener clamps. It accepts logic level inputs thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

- Provides a Robust Driver Interface Between D.C. Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays from 3.0 V to 5.0 V Rail
- Capable of Driving Relay Coils Rated up to 2.5 W at 5.0 V
- Internal Zener Eliminates the Need of Free-Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter Systems Operation
- Low $V_{DS(ON)}$ Reduces System Current Drain

Typical Applications

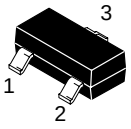
- Telecom: Line Cards, Modems, Answering Machines, FAX
- Computers and Office: Photocopiers, Printers, Desktop Computers
- Consumer: TVs and VCRs, Stereo Receivers, CD Players, Cassette Recorders
- Industrial:Small Appliances, Security Systems, Automated Test Equipment, Garage Door Openers
- Automotive: 5.0 V Driven Relays, Motor Controls, Power Latches, Lamp Drivers

ON Semiconductor®

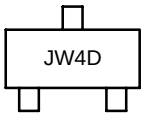
http://onsemi.com

Relay, Inductive Load Driver
Silicon SMALLBLOCK™
0.5 Ampere, 8.0 V Clamp

MARKING DIAGRAM

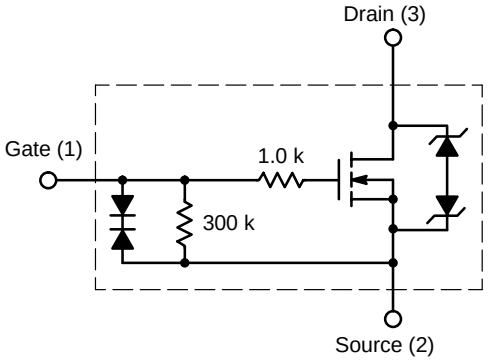


SOT-23
TO-236
CASE 318



JW4 = Specific Device Code
D = Date Code

INTERNAL CIRCUIT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping
NUD3105LT1	SOT-23	3000 Units/Reels

Maximum Ratings (T_J = 25°C unless otherwise specified)

Symbol	Rating	Value	Unit
V_{DSS}	Drain to Source Voltage - Continuous	6.0	V_{dc}
V_{GS}	Gate to Source Voltage – Continuous	6.0	V_{dc}
I_D	Drain Current – Continuous	500	mA
E_z	Single Pulse Drain-to-Source Avalanche Energy ($T_{Jinitial}$ = 25°C) (Note 2)	50	mJ
E_{zpk}	Repetitive Pulse Zener Energy Limit (DC ≤ 0.01%) (f = 100 Hz, DC = 0.5)	4.5	mJ
T_J	Junction Temperature	150	°C
T_A	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
P_D	Total Power Dissipation (Note 1) Derating Above 25°C	225 1.8	mW mW/°C
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient	556	°C/W

1. This device contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL_STD-883, Method 3015.
   Machine Model Method 200 V.
2. Refer to the section covering Avalanche and Energy and Figure 12.

Typical Electrical Characteristics (T_J = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
V_{BRDSS}	Drain to Source Sustaining Voltage (Internally Clamped) (I_D = 10 mA)	6.0	8.0	9.0	V
B_{VGSO}	I_g = 1.0 mA	-	-	8.0	V
I_{DSS}	Drain to Source Leakage Current (V_{DS} = 5.5 V , V_{GS} = 0 V, T_J = 25°C) (V_{DS} = 5.5 V, V_{GS} = 0 V, T_J = 85°C)	 - -	 - -	 15 15	μA
I_{GSS}	Gate Body Leakage Current (V_{GS} = 3.0 V, V_{DS} = 0 V) (V_{GS} = 5.0 V, V_{DS} = 0 V)	 5.0 -	 - -	 19 50	μA
ON CHARACTERISTICS					
$V_{GS(th)}$	Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1.0 mA) (V_{GS} = V_{DS}, I_D = 1.0 mA, T_J = 85°C)	 0.8 0.8	 1.2 -	 1.4 1.4	V
$R_{DS(on)}$	Drain to Source On-Resistance (I_D = 250 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 3.0 V) (I_D = 500 mA, V_{GS} = 5.0 V) (I_D = 500 mA, V_{GS} = 3.0 V, T_J=85°C) (I_D = 500 mA, V_{GS} = 5.0 V, T_J=85°C)	 - - - - -	 - - - - -	 1.2 1.3 0.9 1.3 0.9	Ω
$I_{DS(on)}$	Output Continuous Current (V_{DS} = 0.25 V, V_{GS} = 3.0 V) (V_{DS} = 0.25 V, V_{GS} = 3.0 V, T_J = 85°C)	 300 200	 400 -	 - -	mA
g_{FS}	Forward Transconductance (V_{OUT} = 5.0 V, I_{OUT} = 0.25 A)	350	570	-	mmhos
DYNAMIC CHARACTERISTICS					
C_{iss}	Input Capacitance (V_{DS} = 5.0 V,V_{GS} = 0 V, f = 1.0 MHz)	-	25	-	pF
C_{oss}	Output Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 1.0 MHz)	-	37	-	pF

Typical Electrical Characteristics (T_J = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
C_{rss}	Transfer Capacitance (V_{DS} = 5.0 V, V_{GS} = 0 V, f = 1.0 MHz)	-	8.0	-	pF
SWITCHING CHARACTERISTICS					
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Units**
	Propagation Delay Times:				nS
t_{PHL}	High to Low Propagation Delay; Figure 1 (5.0 V)	-	25	-	
t_{PLH}	Low to High Propagation Delay; Figure 1 (5.0 V)	-	80	-	
t_{PHL}	High to Low Propagation Delay; Figure 1 (3.0 V)	-	44	-	
t_{PLH}	Low to High Propagation Delay; Figure 1 (3.0 V)	-	44	-	
	Transition Times:				nS
t_f	Fall Time; Figure 1 (5.0 V)	-	23	-	
t_r	Rise Time; Figure 1 (5.0 V)	-	32	-	
t_f	Fall Time; Figure 1 (3.0 V)	-	53	-	
t_r	Rise Time; Figure 1 (3.0 V)	-	30	-	-

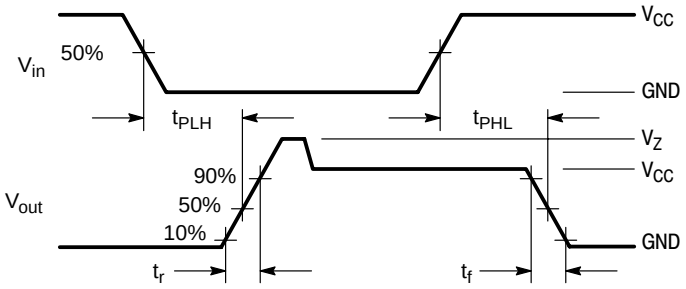


Figure 1. Switching Waveforms

TYPICAL CHARACTERISTICS

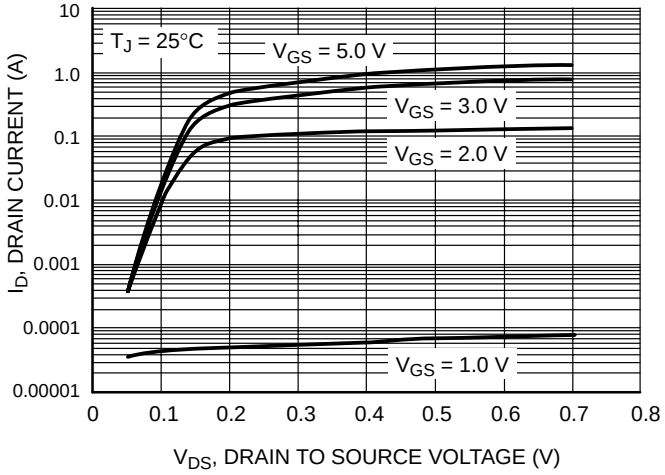


Figure 2. Output Characteristics

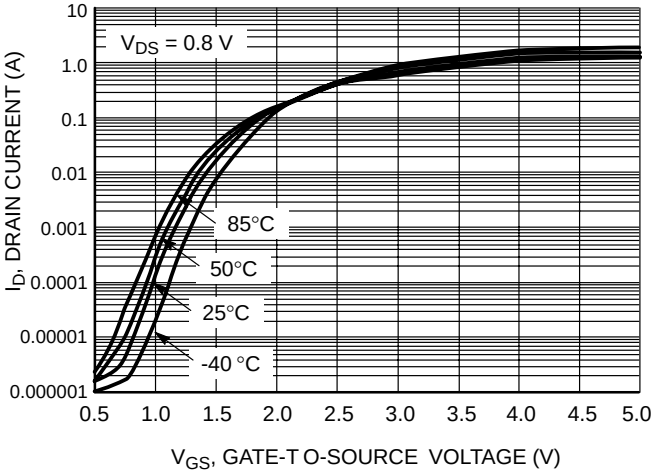


Figure 3. Transfer Function

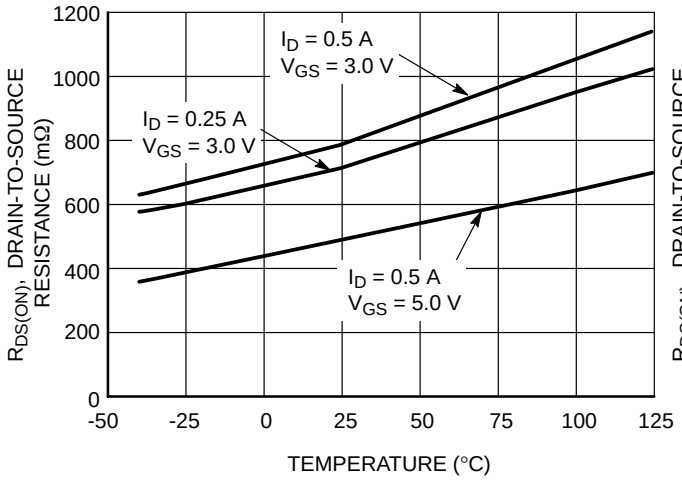


Figure 4. On Resistance Variation vs. Temperature

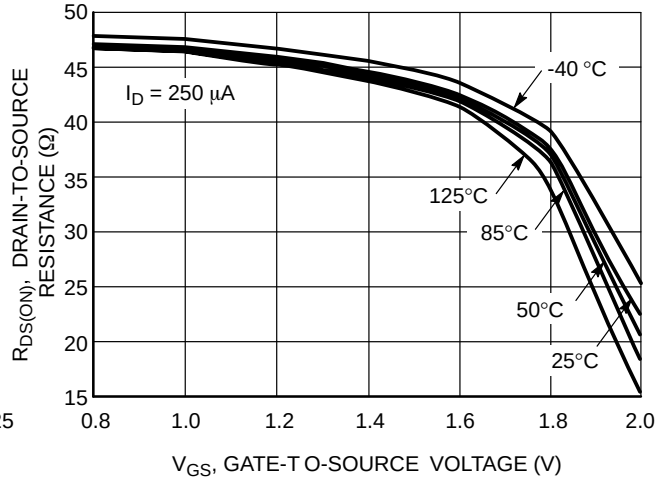


Figure 5. $R_{DS(ON)}$ Variation with Gate-T o-Source Voltage

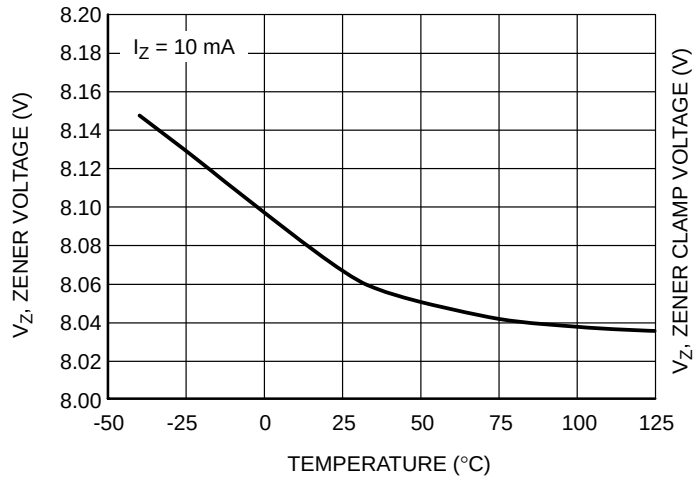


Figure 6. Zener Voltage vs. Temperature

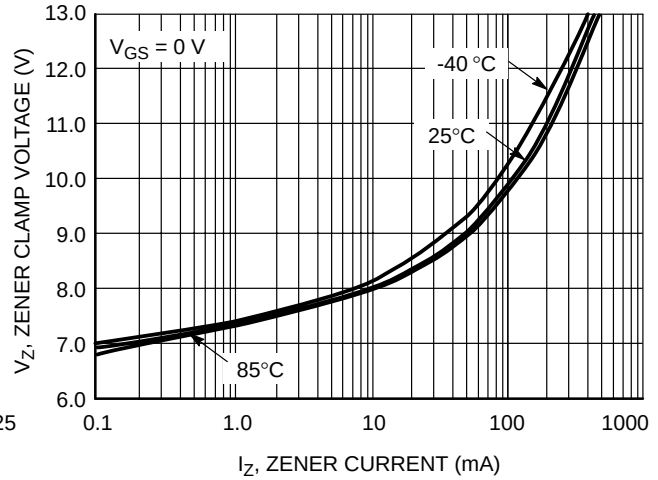


Figure 7. Zener Clamp Voltage vs. Zener Current

TYPICAL CHARACTERISTICS

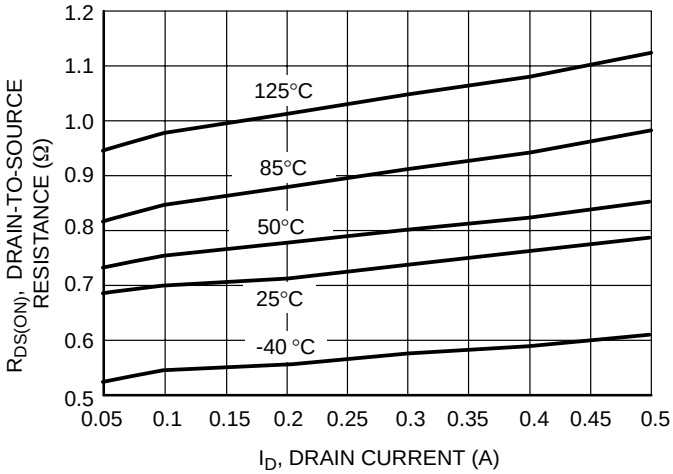


Figure 8. On-Resistance vs. Drain Current and Temperature

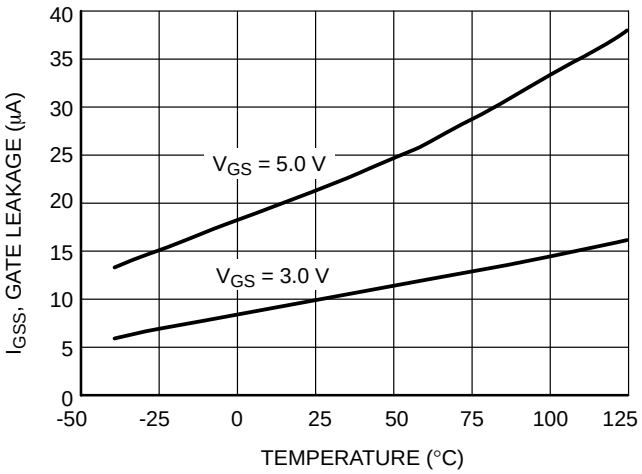


Figure 9. Gate Leakage vs. Temperature

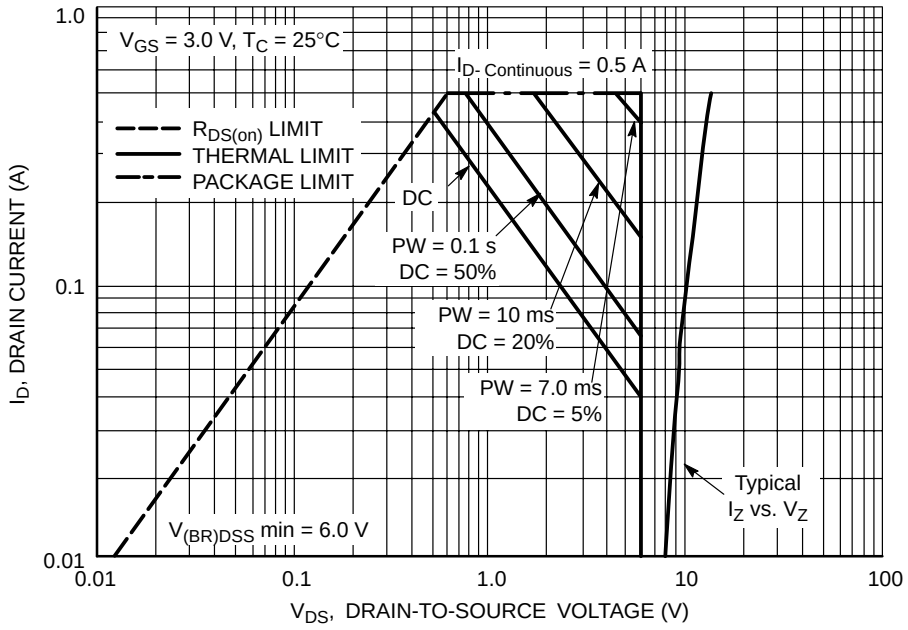


Figure 10. Safe Operating Area

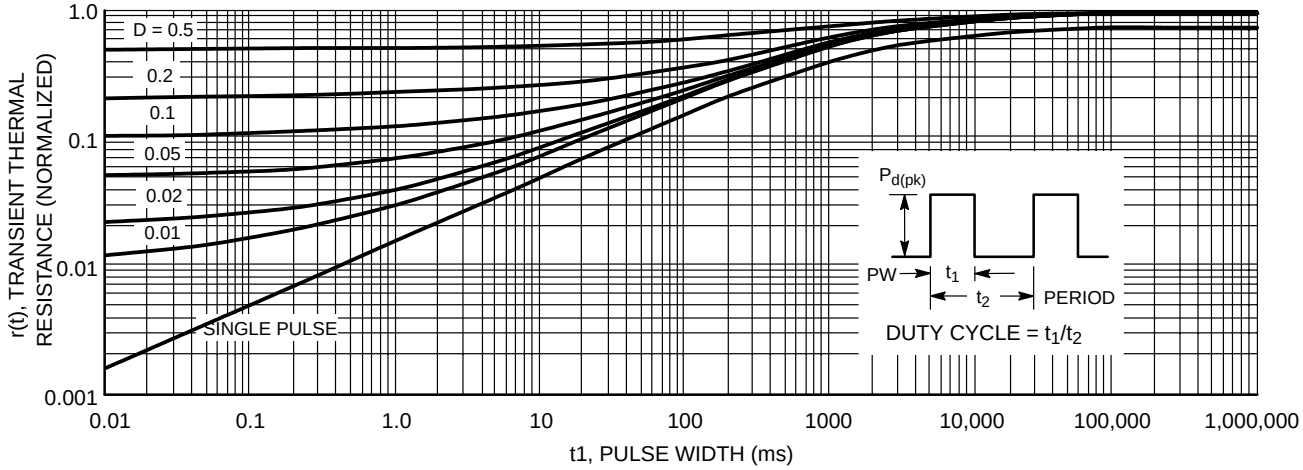


Figure 11. Transient Thermal Response

Avalanche Energy

The drain-to-source clamp, internal to the NUD3105, is designed to protect the device during avalanche energy produced by a load such as an inductor or relay. In many cases, the upper limit of this clamp will be a function of the current through it and the drain-to-source breakdown voltage. The maximum material voltage of the NUD3105 is between 12 and 13 volts. Thus, as the breakdown exceeds 13 V, the device will fail due to the material voltage. This 12 V and 13 V on the clamp corresponds to a current through the clamp of 320 to 440 mA, respectively. The avalanche energy graph, given in Figure 12, is actually limited by the material voltage and the clamp current.

Repetitive Avalanche Energy is based upon $T_J$max, T_A, $R_{\theta JA}$, Transient Thermal Response, Frequency and duty cycle.

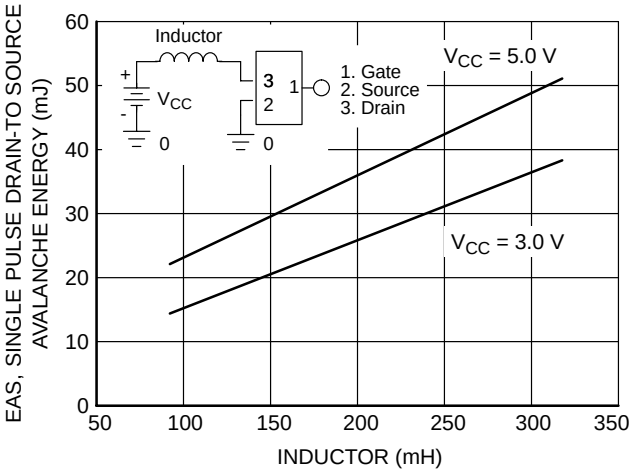


Figure 12. Avalanche Energy

Using TTR Designing for Pulsed Operation

For a repetitive pulse operating condition, time averaging allows one to increase a device's peak power dissipation rating above the average rating by dividing by the duty cycle of the repetitive pulse train. Thus, a continuous rating of 200 mW of dissipation is increased to 1.0 W peak for a 20% duty cycle pulse train. However, this only holds true for pulse widths which are short compared to the thermal time constant of the semiconductor device to which they are applied.

For pulse widths which are significant compared to the thermal time constant of the device, the peak operating condition begins to look more like a continuous duty operating condition over the time duration of the pulse. In these cases, the peak power dissipation rating cannot be merely time averaged by dividing the continuous power rating by the duty cycle of the pulse train. Instead, the average power rating can only be scaled up a reduced amount in accordance with the device's transient thermal response, so that the device's max junction temperature is not exceeded.

Figure 11 of the NUD3105LT1 data sheet plots its transient thermal resistance, r(t) as a function of pulse width in ms for various pulse train duty cycles as well as for a single pulse and illustrates this effect. For short pulse widths near the left side of the chart, r(t), the factor, by which the continuous duty thermal resistance is multiplied to determine how much the peak power rating can be increased above the average power rating, approaches the duty cycle of the pulse train, which is the expected value. However, as the pulse width is increased, that factor eventually approaches 1.0 for all duty cycles indicating that the pulse width is sufficiently long to appear as a continuous duty condition to this device. For the NUD3105LT1, this pulse width is about 100 seconds. At this and larger pulse widths, the peak power dissipation capability is the same as the continuous duty power capability.

To use Figure 11 to determine the peak power rating for a specific application, enter the chart with the worst case pulse condition, that is the max pulse width and max duty cycle and determine the worst case r(t) for your application. Then calculate the peak power dissipation allowed by using the equation,

$$Pd(pk) = (T_{Jmax} - T_{Amax}) \div (R_{\theta JA} * r(t))$$

$$Pd(pk) = (150°C - T_{Amax}) \div (556°C/W * r(t))$$

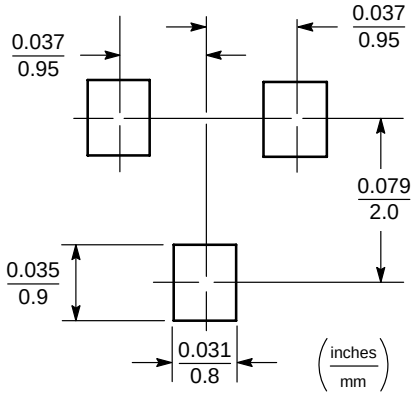
Thus for a 20% duty cycle and a PW = 40 ms, Figure 10 yields r(t) = 0.3 and when entered in the above equation, the max allowable Pd(pk) = 390 mW for a max T_A = 85°C.

Also note that these calculations assume a rectangular pulse shape for which the rise and fall times are insignificant compared to the pulse width. If this is not the case in a specific application, then the V_O and I_O waveforms should be multiplied together and the resulting power waveform integrated to find the total dissipation across the device. This then would be the number that has to be less than or equal to the Pd(pk) calculated above. A circuit simulator having a waveform calculator may prove very useful for this purpose.

INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23

SOT-23 POWER DISSIPATION

The power dissipation of the SOT-23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT-23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT-23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

Designing with this Data Sheet

1. Determine the maximum inductive load current (at max V_{CC}, min coil resistance & usually minimum temperature) that the NUD3105 will have to drive and make sure it is less than the max rated current.
2. For pulsed operation, use the Transient Thermal Response of Figure 11 and the instructions with it to determine the maximum limit on transistor power dissipation for the desired duty cycle and temperature range.
3. Use Figures 10, 11 and 12 with the SOA notes to insure that instantaneous operation does not push the device beyond the limits of the SOA plot.
4. Verify that the circuit driving the gate will meet the $V_{GS(th)}$ from the Electrical Characteristics table.
5. Using the max output current calculated in step 1, check Figure 7 to insure that the range of Zener clamp voltage over temperature will satisfy all system & EMI requirements.
6. Use I_{GSS} and I_{DSS} from the Electrical Characteristics table to insure that "OFF" state leakage over temperature and voltage extremes does not violate any system requirements.
7. Review circuit operation and insure none of the device max ratings are being exceeded.

APPLICATIONS DIAGRAMS

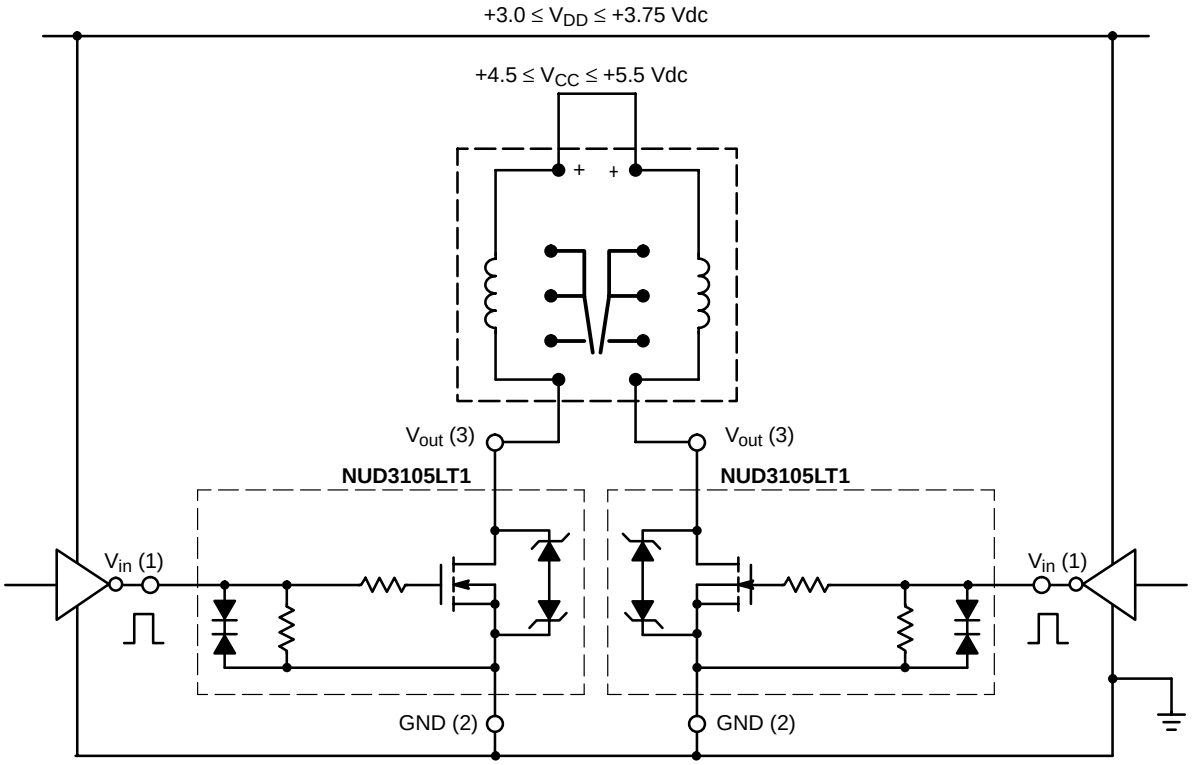


Figure 13. A 200 mW, 5.0 V Dual Coil Latching Relay Application with 3.0 V Level Translating Interface

Max Continuous Current Calculation

for TX2-5V Relay, R1 = 178 Ω Nominal @ R_A = 25°C

Assuming ±10% Make Tolerance,
R1 = 178 Ω * 0.9 = 160 Ω Min @ T_A = 25°C

T_C for Annealed Copper Wire is 0.4%/°C

R1 = 160 Ω * [1+(0.004) * (-40°-25 °)] = 118 Ω Min @ -40°C

I_O Max = (5.5 V Max - 0.25V) /118 Ω = 45 mA

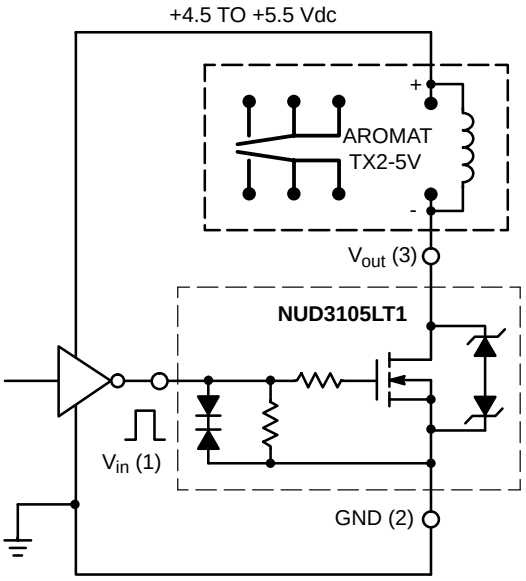


Figure 14. A 140 mW, 5.0 V Relay with TTL Interface

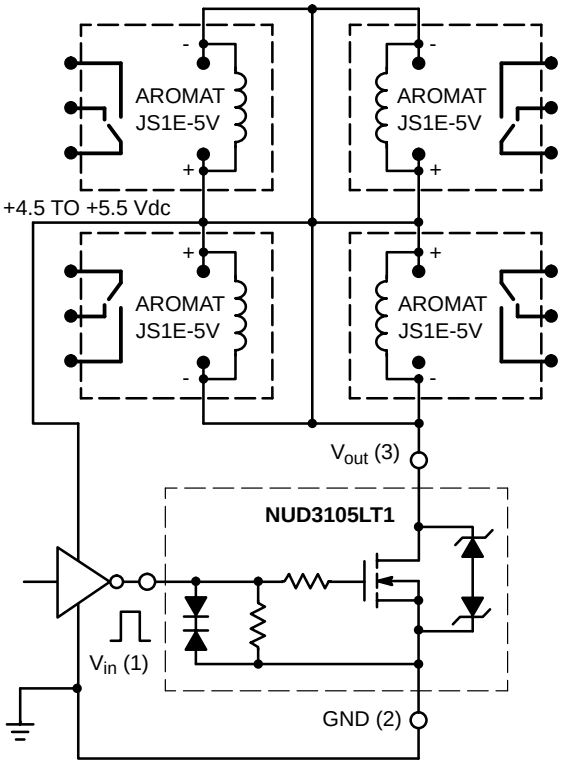
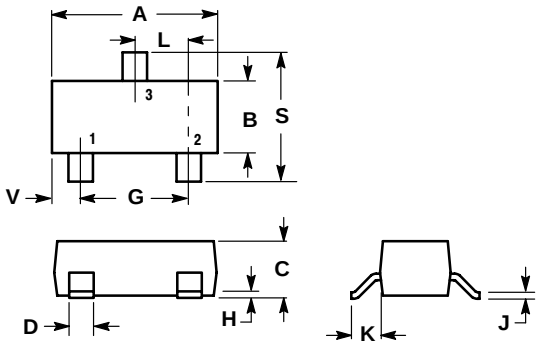


Figure 15. A Quad 5.0 V, 360 mW Coil Relay Bank

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−03 AND −07 OBSOLETE, NEW STANDARD 318−08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

Notes

SMALLBLOCK is a trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.