FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13702-1E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90520 Series

MB90522/523/F523/V520

■ DESCRIPTION

The MB90520 series is a general-purpose 16-bit microcontroller developed and designed by Fujitsu for process control applications in consumer products that require high-speed real-time processing.

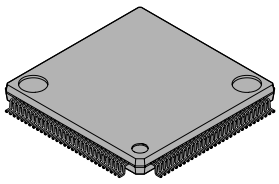
The instruction set of F²MC-16LX CPU core inherits AT architecture of F²MC*1 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90520 series has peripheral resources of 8/10-bit A/D converter, a 8-bit D/A converter, UART (SCI), extended I/O serial interfaces 0 and 1, 8/16-bit up/down counter/timers 0 and 1, 8/16-bit PPG timers 0 and 1, I/O timer (16-bit free-run timers 1 and 2, input captures 0 and 1 (ICU), output compares 0 and 1 (OCU)), LCD controller/driver.

*1: F²MC stands for FUJITSU Flexible Microcontroller.

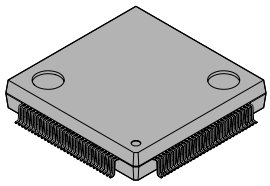
■ PACKAGE

120-pin Plastic LQFP



(FPT-120P-M05)

120-pin Plastic QFP



(FPT-120P-M13)

MB90520 Series

■ FEATURES

- Clock
  Embedded PLL clock multiplication circuit
  Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 3 MHz to 16 MHz).
  The system can be operated by an oscillation sub-clock (rated at 32.768 kHz).
  Minimum instruction execution time: 62.5 ns (at oscillation of 4 MHz, four times the PLL clock, operation at V_{CC} of 5.0 V)
- Maximum memory space
  16 Mbytes
- Instruction set optimized for controller applications
  Ri65data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed
  4-byte instruction queue
- Enhanced interrupt function
  8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI^2OS): Up to 16 channels
- Embedded ROM size and types
  Mask ROM: 64 kbytes/128 kbytes
  Flash ROM: 256 kbytes
  Embedded RAM size: 4 kbytes/10 kbytes (mass-produced products)
  4 kbytes (flash memory)
  6 kbytes (evaluation chip)
- Low-power consumption (stand-by) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Hardware stand-by mode
  Clock mode (mode in which other than sub-oscillation and timebase timer are stopped)
- Process
  CMOS technology
- I/O port
  General-purpose I/O ports (CMOS): 53 ports
  General-purpose I/O ports (via pull-up resistors): 24 ports
  General-purpose I/O ports (open-drain): 8 ports
  Total: 85 ports

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- Timer
  Timebase timer/watchdog timer: 1 channel
  8/16-bit PPG timers 0, 1: 8-bit × 2 channels or 16-bit × 1 channel
  16-bit re-load timers 0, 1: 2 channels
- 16-bit I/O timer
  16-bit free-run timers 1, 2: 2 channels
  Input captures 0, 1 (ICU): Generates an interrupt request by latching a 16-bit free-run timer counter value upon detection of an edge input to the pin.
  Output compares 0, 1 (OCU): Generates an interrupt request and reverse the output level upon detection of a match between the 16-bit free-run timer counter value and the compare setting value.
  8/16-bit up/down counter/timers 0, 1: 1 channel (8-bit × 2 channels)
- Extended I/O serial interfaces 0, 1: 1 channel
- UART (SCI)
  With full-duplex double buffer
  Clock asynchronized or clock synchronized transmission can be selectively used.
- DTP/external interrupt circuit (8 channels)
  A module for starting extended intelligent I/O service (EI^{2}OS) and generating an external interrupt triggered by an external input.
- Wake-up interrupt
  Receives external interrupt requests and generates an interrupt request upon an “L” level input.
- Delayed interrupt generation module
  Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  8/10-bit resolution can be selectively used.
  Starting by an external trigger input.
  Conversion time: 16.0 µs or slower
- 8-bit D/A converter (based on the R-2R system)
  8-bit resolution: 2 channels (independent)
  Setup time: 12.5 µs
- Clock timer: 1 channel
- LCD controller/driver
  A common driver and a segment driver that can directly drive the LCD (liquid crystal display) panel
- Clock output function

Note: Do not set external bus mode for the MB90520 series because it cannot be operated in this mode.

MB90520 Series

■ PRODUCT LINEUP

Item \ Part number		MB90522	MB90523	MB90F523	MB90V520
Classification		Mass-produced products (mask ROM products)		Mass-produced product (flash ROM product)	Evaluation product
ROM size		64 kbytes	128 kbytes		None
RAM size		6 kbytes			
CPU functions		The number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits			
		Minimum execution time: 62.5 ns (at machine clock of 16 MHz)		Minimum execution time: 100 ns (at machine clock of 10 MHz)	Minimum execution time: 62.5 ns (at machine clock of 16 MHz)
		Interrupt processing time: 1.5 µs (at machine clock of 16 MHz, minimum value)			
Ports		General-purpose I/O ports (CMOS output): 53 General-purpose I/O ports (via pull-up resistor): 24 General-purpose I/O ports (N-ch open-drain output): 8 Total: 85			
UART (SCI)		Clock synchronized transmission (62.5 kbps to 1 Mbps) Clock asynchronized transmission (1202 bps to 9615 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.			
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Scan conversion mode (converts two or more successive channels and can program up to 8 channels.) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)			
8/16-bit PPG timers 0, 1		Number of channels: 1 (8-bit × 2 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: 62.5 ns to 1 µs (at oscillation of 4 MHz, machine clock of 16 MHz)			
8/16-bit up/down counter/ timers 0, 1		Number of channels: 1 (8-bit × 2 channels) Event input: 6 channels 8-bit up/down counter/timer used: 2 channels 8-bit re-load/compare function supported: 1 channel			
16-bit I/O timer	16-bit free-run timers 1, 2	Number of channels: 2 Overflow interrupts			

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Item \ Part number		MB90522	MB90523	MB90F523	MB90V520
16-bit I/O timer	Output compares 0, 1 (OCU)	Number of channels: 8 Pin input factor: A match signal of compare register			
	Input captures 0, 1 (ICU)	Number of channels: 2 Rewriting a register value upon a pin input (rising, falling, or both edges)			
DTP/external interrupt circuit		Number of inputs: 8 Started by a rising edge, a falling edge, an “H” level input, or an “L” level input. External interrupt circuit or extended intelligent I/O service (EI^{2}OS) can be used.			
Wake-up intrrupt		Number of inputs: 8 Started by an “L” level input.			
Delayed interrupt generation module		An interrupt generation module for switching tasks Used in real-time operating systems.			
Extended I/O serial interfaces 0, 1		Clock synchronized transmission (3125 bps to 1 Mbps) LSB first/MSB first			
Timebase timer		18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)			
8-bit D/A converter		8-bit resolution Number of channels: 2 channels Based on the R-2R system			
LCD controller/driver		Number of common output pins: 4 Number of segment output pins: 32 Number of power supply pins for LCD drive: 4 RAM for LCD indication: 16 bytes Booster for LCD drive: Internal Split resistor for LCD drive: Internal			
Watchdog timer		Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)			
Low-power consumption (stand-by) mode		Sleep/stop/CPU intermittent operation/clock timer/hardware stand-by			
Process		CMOS			
Power supply voltage for operation*		3.0 V to 5.5 V		4.0 V to 5.5 V	3.0 V to 5.5 V

* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)
Assurance for the MB90V520 is given only for operation with a tool at a power voltage of 3.0 V to 5.5 V, an operating temperature of 0 to 55 degrees centigrade, and an operating frequency of 1 MHz to 16 MHz.

MB90520 Series

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90522	MB90523	MB90F523
FPT-120P-M05	○	○	○
FPT-120P-M13	○	○	○

○ : Available ×: Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

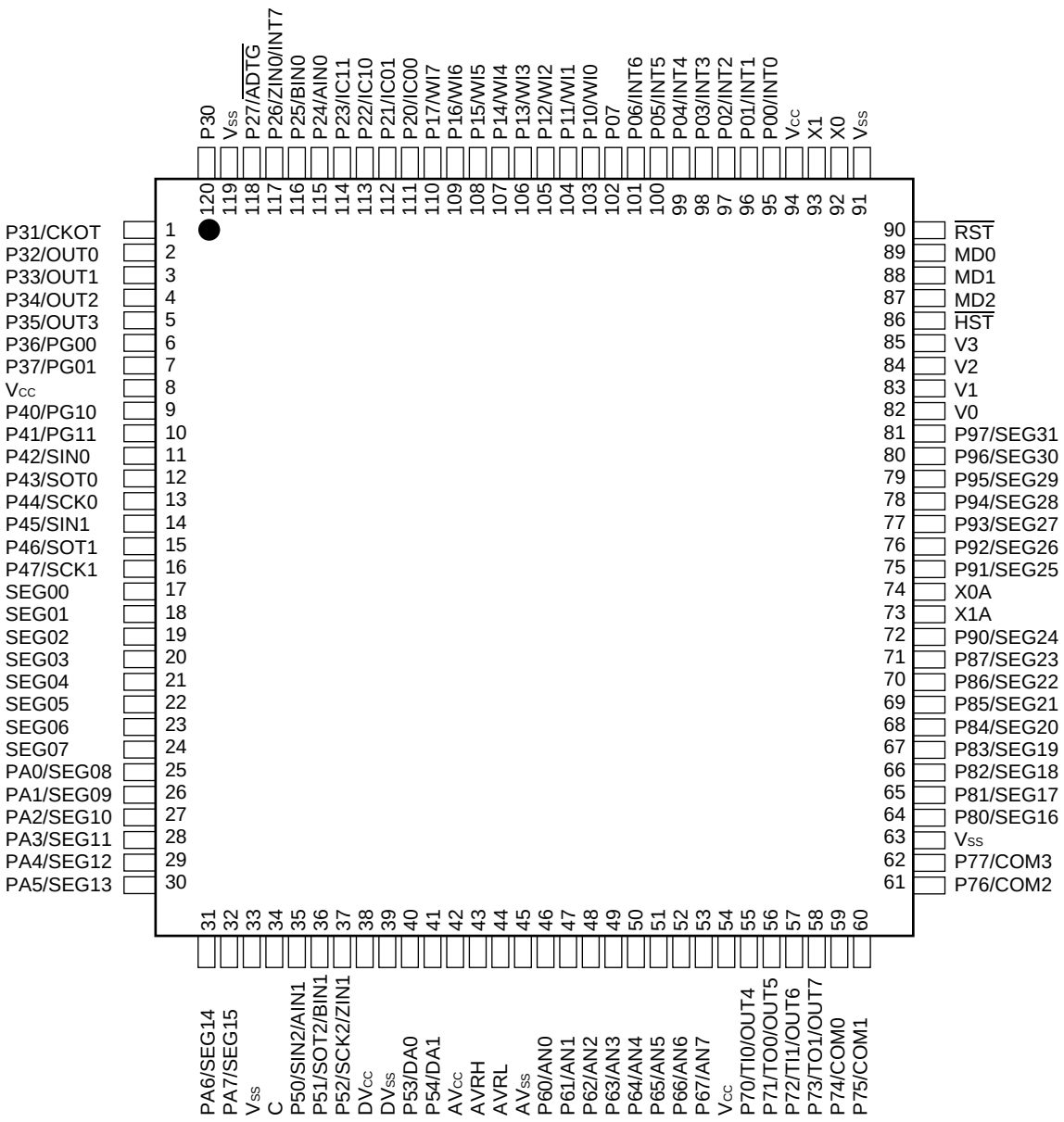
Memory Size

In evaluation with an evaluation chips, note the difference between the evaluation chip and the chip actually used. The following items must be taken into consideration.

- The MB90V520 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V520, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF3FFF_H$ to mapped to bank FE and FF only. (This setting can be changed by configuring the deveolpment tool.)
- In the MB90522, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FF0000_H$ to $FF3FFF_H$ to bank FF only.
- In the MB90523/F523, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF3FFF_H$ to bank FE and bank FF.

■ PIN ASSIGNMENT

(Top view)



(FPT-120P-M05)
(FPT-120P-M13)

■ PIN DESCRIPTION

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
92, 93	X0, X1	A	This is a high-speed crystal oscillator pin.
74, 73	X0A, X1A	B	This is a low-speed crystal oscillator pin.
89 to 87	MD0 to MD2	C	This is an input pin for selecting operation modes. Connect directly to V_{CC} or V_{SS}.
90	$\overline{RST}$	C	This is external reset request signal.
86	$\overline{HST}$	C	This is a hardware stand-by input pin.
95 to 101	P00 to P06	D	This is a general-purpose I/O port. This function can be set by the port 0 input pull-up resistor setup register (RDR0) for input. For output, however, this function is invalid.
	INT0 to INT6		This is a request input pin of the DTP/external interrupt circuit ch.0 to ch.6.
102	P07	D	This is a general-purpose I/O port. This function can be set by the port 0 input pull-up resistor setup register (RDR0) for input. For output, however, this function is invalid.
103 to 110	P10 to 17	D	This is a general-purpose I/O port. This function can be set by the port 1 input pull-up resistor setup register (RDR1) for input. For output, however, this function is invalid.
	WI0 to WI7		This is an I/O pin for wake-up interrupts.
111, 112, 113, 114	P20, P21, P22, P23	E	This is a general-purpose I/O port.
	IC00, IC01, IC10, IC11		This is a trigger input pin for input capture (ICU) 0 and 1. Since this input is used as required for input capture 0 and 1 (ICU) ch.0, ch.01, ch.10 and ch.11 input operation, output by other functions must be suspended except for intentional operation.
115	P24	E	This is a general-purpose I/O port.
	AIN0		This port can be used as count clock A input for 8/16-bit up/down counter/timer 0.
116	P25	E	This is a general-purpose I/O port.
	BIN0		This port can be used as count clock B input for 8/16-bit up/down counter/timer 0.

*1: FPT-120P-M05
*2: FPT-120P-M13

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Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
117	P26	F	This is a general-purpose I/O port.
	ZIN0		This port can be used as count clock Z input for 8/16-bit up/down counter/timer 0.
	INT7		This is a request input pin of the DTP/external interrupt circuit ch.7.
118	P27	F	This is a general-purpose I/O port.
	$\overline{\text{ADTG}}$		This is external trigger input pin of the 8/10-bit A/D converter. Since this input is used as required for 8/10-bit A/D converter input operation, output by other functions must be suspended except for intentional operation.
120	P30	E	This is a general-purpose I/O port.
1	P31	E	This is a general-purpose I/O port.
	CKOT		This is a clock monitor function output pin. This function is vaild when clock monitor output is enabled.
2	P32	E	This is a general-purpose I/O port. This function becomes vaild when waveform output from the OUT0 is disabled.
	OUT0		This is an event output pins for output compare 0 (OCU) ch.0. This function is valid when output for each channel is enabled.
3	P33	E	This is a general-purpose I/O port. This function becomes vaild when waveform output from the OUT1 is disabled.
	OUT1		This is an event output pins for output compare 0 (OCU) ch.1. This function is valid when output for each channel is enabled.
4	P34	E	This is a general-purpose I/O port. This function becomes vaild when waveform output from the OUT2 is disabled.
	OUT2		This is an event output pins for output compare 0 (OCU) ch.2. This function is valid when output for each channel is enabled.
5	P35	E	This is a general-purpose I/O port. This function becomes vaild when waveform output from the OUT3 is disabled.
	OUT3		This is an event output pins for output compare 0 (OCU) ch.3. This function is valid when output for each channel is enabled.
6	P36	E	This is a general-purpose I/O port. This function becomes vaild when waveform output from the PG00 is disabled.
	PG00		This is an output pin of 8/16-bit PPG timer 0. This function becomes valid when waveform output from PG00 is enabled.

*1: FPT-120P-M05
*2: FPT-120P-M13

(Continued)

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
7	P37	E	This is a general-purpose I/O port. This function becomes vaild when waveform output from the PG01 is disabled.
	PG01		This is an output pin of 8/16-bit PPG timer 0. This function becomes valid when waveform output from PG01 is enabled.
9, 10	P40, P41	D	This is a general-purpose I/O port. This function becomes vaild when waveform output from the PG10 and PG11 are disabled. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	PG10, PG11		This is an output pin of 8/16-bit PPG timer 1. This function becomes valid when waveform outputs from PG10 and PG11 are enabled.
11	P42	D	This is a general-purpose I/O port. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SIN0		This is a serial data input pin of UART (SCI). Because this input is used as required when UART (SCI) is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally. When using other output functions as well, disable output during SIN operation.
12	P43	D	This is a general-purpose I/O port. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SOT2		This is a serial data output pin of UART (SCI). This function becomes valid when serial data output from UART (SCI) is enabled.
13	P44	D	This is a general-purpose I/O port. This function can be set by the pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SCK0		This is a serial clock I/O pin of UART (SCI). This function becomes valid when serial clock output from UART (SCI) is enabled.
14	P45	D	This is a general-purpose I/O port. This function can be set by the port 4 input pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SIN1		This is a data input pin for extended I/O serial interface 0. Since this input is used as required for serial data input operation, output by other functions must be suspended except for intentional operation. When using other output functions as well, disable output during SIN operation.

*1: FPT-120P-M05
*2: FPT-120P-M13

(Continued)

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
15	P46	E	This is a general-purpose I/O port. This function can be set by the port 4 input pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SOT1		This is a data output pin for extended I/O serial interface 0. This function becomes valid when serial data output from SOT1 is enabled.
16	P47	D	This is a general-purpose I/O port. This function can be set by the port 4 input pull-up resistor setup register (RDR4) for input. For output, however, this function is invalid.
	SCK1		This is a serial clock I/O pin for extended I/O serial interface 0. This function becomes valid when serial clock output from SCK1 is enabled.
35	P50	D	This is a general-purpose I/O port.
	SIN2		This is a data input pin for extended I/O serial interface 1. Since this input is used as required for serial data input operation, output by other functions must be suspended except for intentional operation.
	AIN1		This port can be used as count A input for 8/16-bit up/down counter/timer 1.
36	P51	D	This is a general-purpose I/O port.
	SOT2		This function becomes valid when serial data output from SOT2 is enabled.
	BIN1		This port can be used as count B input for 8/16-bit up/down counter/timer 1.
37	P52	D	This is a general-purpose I/O port.
	SCK2		This is a serial clock I/O pin for extended I/O serial interface 1. This function becomes valid when serial clock output from serial SCK2 is enabled.
	ZIN1		This port can be used as control clock Z input for 8/16-bit up/down counter/timer 1.
40, 41	P53, P54	I	This is a general-purpose I/O port.
	DA0, DA1		These are analog signal output pins for 8-bit D/A converter ch.0 and ch.1.
46 to 53	P60 to P67	K	This is a general-purpose I/O port. The input function become valid when the analog input enable register (ADER) is set to select a port.
	AN0 to AN7		These are analog input pins of the 8/10-bit A/D converter. This function is valid when the analog input enable register (ADER) is enabled.

*1: FPT-120P-M05
*2: FPT-120P-M13

(Continued)

Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
55, 57	P70, P72	E	This is a general-purpose I/O port.
	TI0, TI1		These are event input pins for 16-bit re-load timers 0 and 1. Since this input is used as required for 16-bit re-load timers 0 and 1 operation, output by other functions must be suspended except for intentional operation.
	OUT4, OUT6		These are event output pins for output compare 1 (OCU) ch.4 and ch.6. This function is valid when output for each channel is enabled.
56, 58	P71, P73	E	This is a general-purpose I/O port. This function is valid with TO0 and TO1 output disabled.
	TO0, TO1		These are output pins for 16-bit re-load timers 0 and 1. This function is valid with TO0 and TO1 output is enabled.
	OUT5, OUT7		These are event output pins for output compare 1 (OCU) ch.5 and ch.7. This function is valid when output for each channel is enabled.
59 to 62	P74 to P77	L	This is a general-purpose I/O port. This function is valid with port output specified for the LCD controller/driver control register.
	COM to COM3		These are common pins for the LCD controller/driver. This function is valid with common output specified for the LCD controller/driver control register.
64 to 71	P80 to P87	L	This is a general-purpose I/O port. This function is valid with port output specified for the LCD controller/driver control register.
	SEG16 to SEG23		These are segment outputs for the LCD controller/driver. This function is valid with common output specified for the LCD controller/driver control register.
72, 75 to 81	P90, P91 to P97	M	This is a general-purpose I/O port. The maximum I_{OL} can be 10mA. This function is valid with port output specified for the LCD controller/driver control register.
	SEG24, SEG25 to SEG31		These are ports for the LCD controller/driver. This function is valid with common output specified for the LCD controller/driver control register.
17 to 24	SEG00 to SEG07	F	These are pins dedicated to LCD segments 00 to 07 for the LCD controller/driver.
25 to 32	PA0 to PA7	L	This is a general-purpose I/O port. This function is valid with port output specified for the LCD controller/driver control register.
	SEG08 to SEG15		These are pins for LCD segments 08 to 15 for the LCD controller/driver. Units of four ports or segments can be selected by the internal register in the LCD controller.

*1: FPT-120P-M05
*2: FPT-120P-M13

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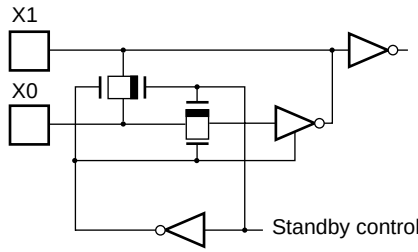
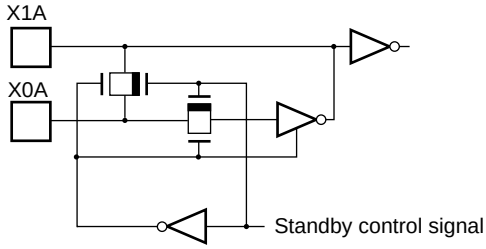
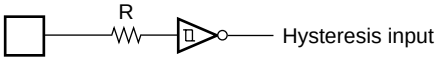
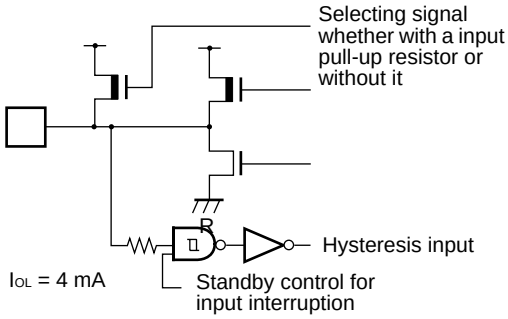
Pin no. LQFP-120*1 QFP-120*2	Pin name	Circuit type	Function
34	C	G	This is a capacitance pin for power supply stabilization. Connect an external ceramic capacitor rated at about 0.1 µF. This capacitor is not, however, required for the M90F523 (flash product).
82 to 85	V0 to V3	N	This is a pin for the reference power supply for the LCD controller/ driver.
8, 54, 94	V_{CC}	Power supply	This is power supply (5.0 V) input pin to the digital circuit.
33, 63, 91 119	V_{SS}	Power supply	This provides the GND level (0.0 V) input pin for the digital circuit.
42	AV_{CC}	H	This is power supply to the analog circuit. Make sure to turn on/turn off this power supply with a voltage exceeding AV_{CC} applied to V_{CC}.
43	AVRH	J	This is a reference voltage input to the analog circuit. Make sure to turn on/turn off this power supply with a voltage exceeding AVRH applied to AV_{CC}.
44	AVRL	H	This is a reference voltage input to the analog circuit.
45	AV_{SS}	H	This is a GND level of the analog circuit.
38	DV_{CC}	H	This is the Vref input pin for the D/A converter. The voltage to be applied must not exceed V_{CC}.
39	DV_{SS}	H	This is the GND level pin for the D/A converter. The potential must be the same as V_{SS}.

*1: FPT-120P-M05
*2: FPT-120P-M13

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-speed oscillation feedback resistor approx. 1MΩ
B		• Low-speed oscillation feedback resistor approx. 1MΩ
C		• Hysteresis input rated at about 50 kΩ
D		• Hysteresis input can be set the input pull-up resistor CMOS level output • Rated at about 50 kΩ • Provided with a standby control function for input interruption

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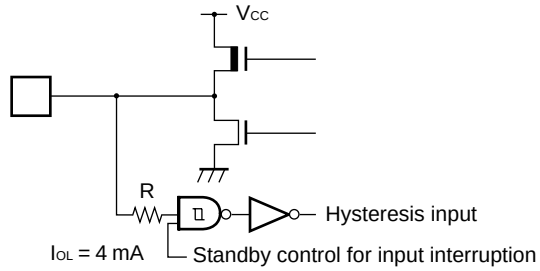
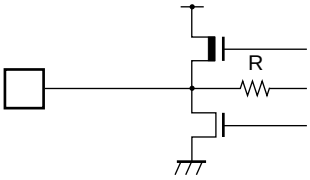
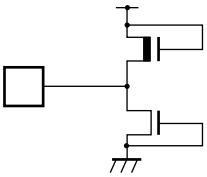
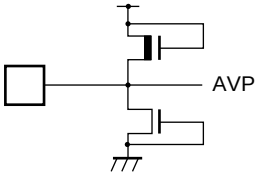
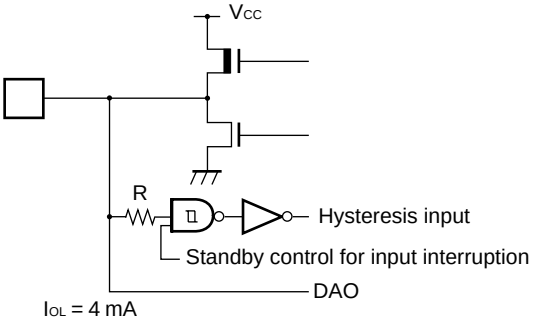
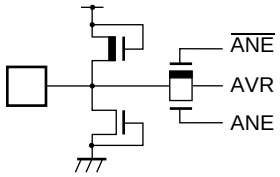
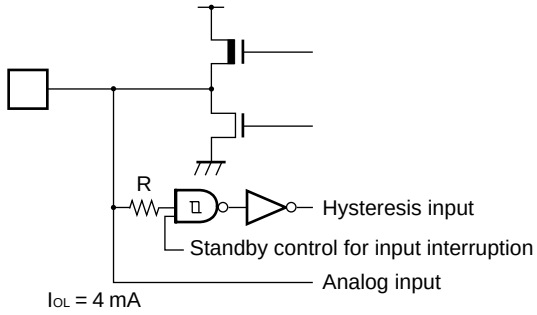
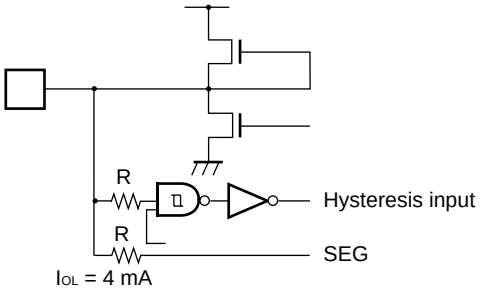
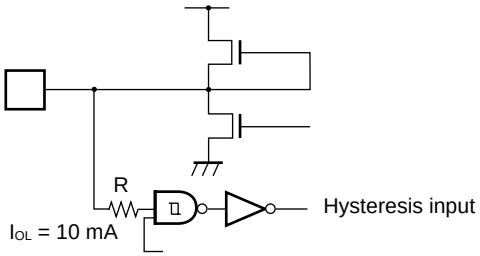
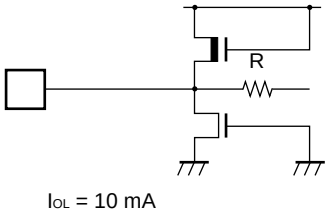
Type	Circuit	Remarks
E		• CMOS hysteresis input/output • CMOS level output • Provided with a standby control function for input interruption
F		• Pins dedicated to segment output
G		• C pin output (Pin for capacitor connection) N.C. pin for the MB90F523
H		• Analog power input protector
I		• CMOS hysteresis input/output • Pin for analog output/CMOS output (During analog output, CMOS output is not produced.) (Analog output has priority over CMOS output: DAE = 1) • Provided with a standby control function for input interruption

(Continued)

Type	Circuit	Remarks
J		• Input pin for ref+ power for the A/D converter Provided with a power protection
K		• Hysteresis input/analog input • CMOS output • Provided with a standby control for input interruption
L		• Hysteresis input/output • Segment input • Standby control to cut off the input is available in segment input operation
M		• Hysteresis input • N-ch open-drain output (High current for LCD drive) • Standby control to cut off the input is available in segment input operation
N		• Reference power supply pin for the LCD controller

■ HANDLING DEVICES

1. Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS}.

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC}, AVRH, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

And also make sure the voltage applied to the LCD power supply pin (V3 to V0) doesn't exceed the power supply voltage (V_{CC}).

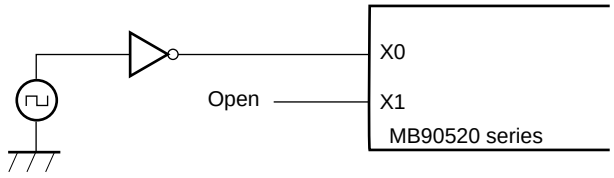
2. Connection of Unused Pins

Leaving unused pins open may result in abnormal operations. Clamp the pin level by connecting it to a pull-up or a pull-down resistor.

3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

- **Using external clock**



4. Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level and abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 µF between V_{CC} and V_{SS} pin near the device.

5. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an grand area for stabilizing the operation.

6. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply, D/A converter power supply (AV_{CC}, AVRH, AVRL, DV_{CC}, DV_{SS}) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that AVRH and DV_{CC} not exceed AV_{CC} (turning on/off the analog and digital supplies simultaneously is acceptable).

7. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter and those of D/A converter to $AV_{CC} = DV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

8. N.C. Pin

The N.C. (internally connected) pin must be opened for use.

9. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more μs (0.2 V to 2.7 V).

10. Use of SEG/COM Pins for the LCD Controller/Driver as Ports

In MB90520 series, pins SEG08 to SEG31, and COM0 to COM3 can also be used general-purpose ports. The electrical standard is such that pins SEG08 to SEG23, and COM0 to COM3 have the same ratings as the CMOS output port, while pins SEG24 to SEG31 have the same ratings as the open-drain type.

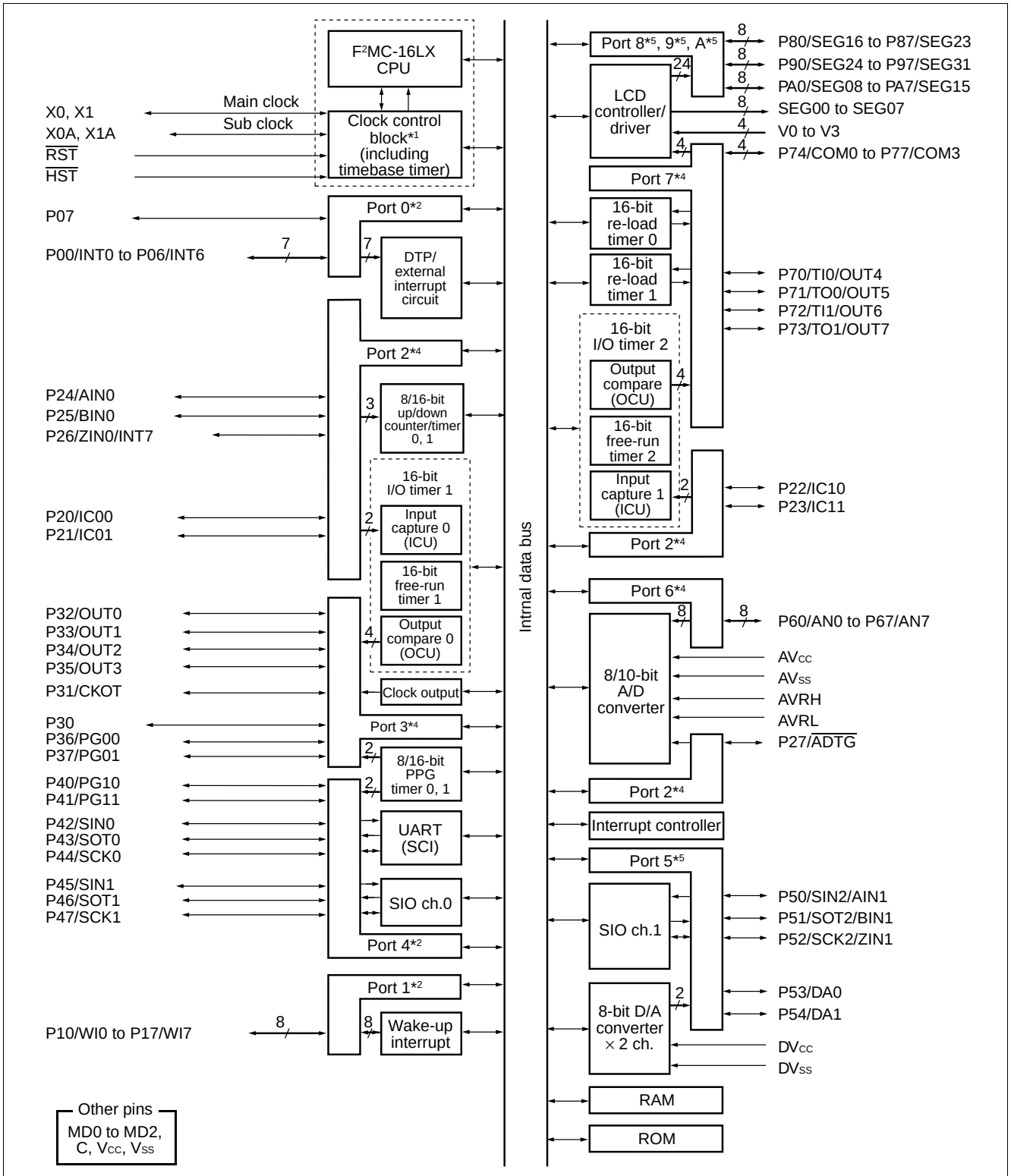
11. Initialization

In the device, there are internal registers which is initialized only by a power-on reset. To initialize these registers turning on the power again.

12. Interrupt Recovery from the Standby State

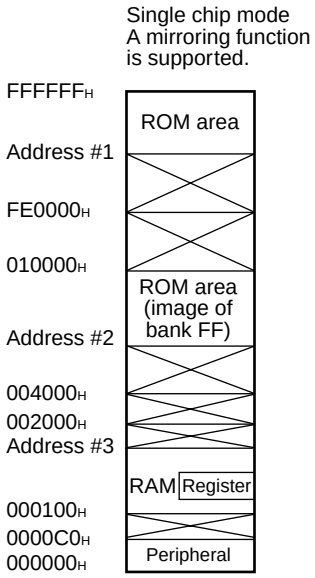
“H” level request must be an input request when using an external interrupt to recover from the standby state. In this case “L” level request may occur malfunction.

■ BLOCK DIAGRAM



Notes: One 16-bit free-run timer 1 is supported although two free-run timers are seemingly supported.
*1: The clock control circuit comprises a watchdog timer, a timebase timer, and a power consumption controller.
*2: A register for setting a pull-up resistor is supported.
*3: This is a high-current port for LCD drive.
*4: A register for setting a pull-up resistor is supported. A signal in the CMOS level is input and output.
*5: Also used for LCD output. With this port used as is, N-ch open-drain output develops. A register for setting a pull-up resistor.

■ MEMORY MAP



Part number	Address #1*	Address #2*	Address #3*
MB90522	FF0000H	004000H	001100H
MB90523	FE0000H	004000H	001100H
MB90F523	FE0000H	004000H	001100H

: Internal access memory

: Access prohibited

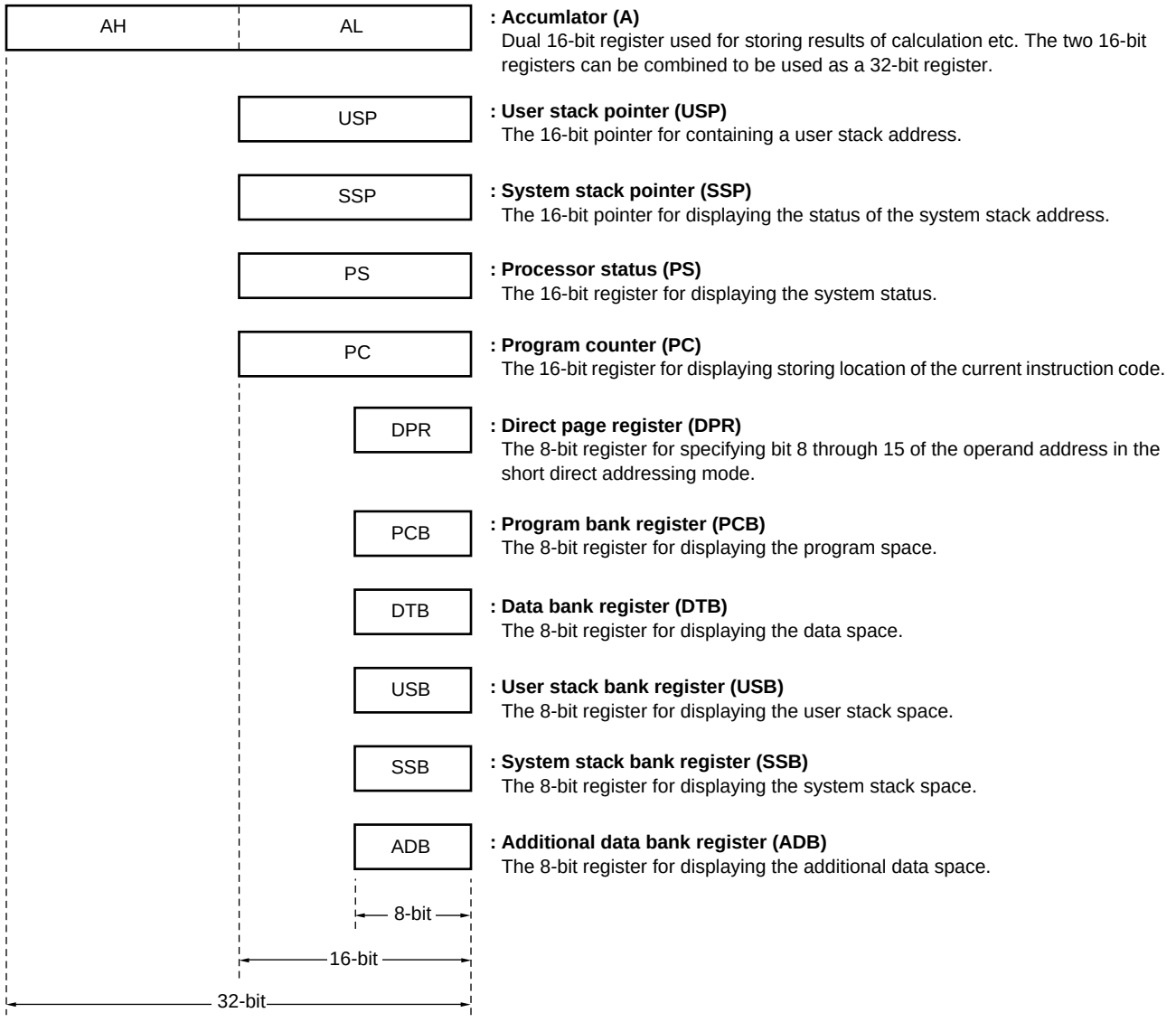
*: Addresses #1, #2 and #3 are unique to the product type.

Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 is assigned to the same address, enabling reference of the table on the ROM without stating “far”.

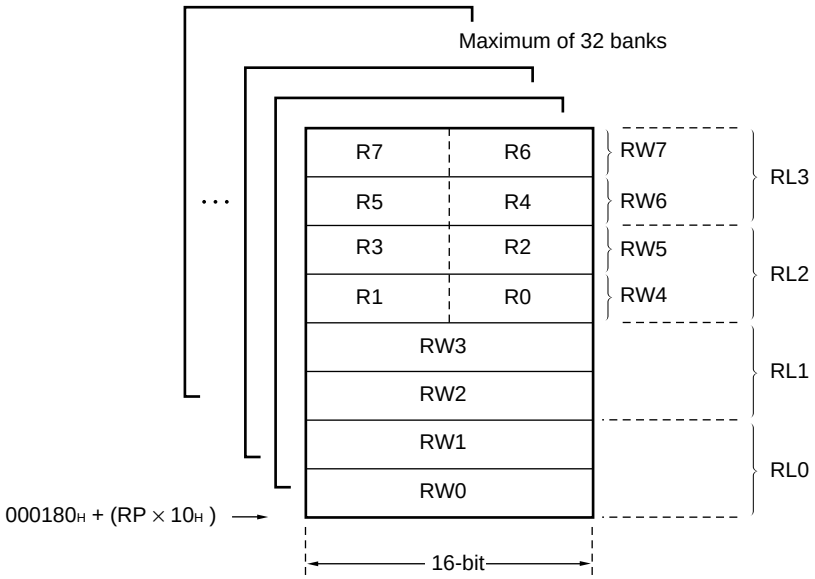
For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 48k bytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 00400H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH

■ F²MC-16LX CPU PROGRAMMING MODEL

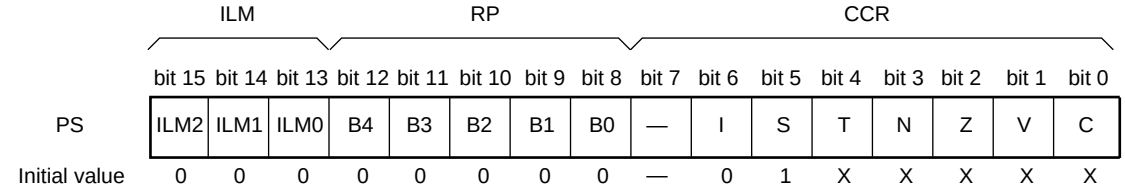
- **Dedicated registers**



- **General-purpose registers**



- **Processor status (PS)**



— : Unused
X : Indeterminate

■ I/O MAP

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
000000H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	---XXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	Port 7	XXXXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	XXXXXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	XXXXXXXXB
00000AH	PDRA	Port A data register	R/W	Port A	XXXXXXXXB
00000BH	LCDCMR	Port 7/COM pin selection register	R/W	Port 7, LCD controller/driver	----0000B
00000CH	PDRC	Port C data register	R/W	Port C	XXXXXXXXB
00000CH	OCP4	OCU compare register ch.4	R/W	16-bit I/O timer (output compare 1 (OCU) section)	XXXXXXXXB
00000DH					XXXXXXXXB
00000EH	(Disabled)				
00000FH	EIFR	Wake-up interrupt flag register	R/W	Wake-up interrupt	-------0B
000010H	DDR0	Port 0 direction register	R/W	Port 0	00000000B
000011H	DDR1	Port 1 direction register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction register	R/W	Port 3	00000000B
000014H	DDR4	Port 4 direction register	R/W	Port 4	00000000B
000015H	DDR5	Port 5 direction register	R/W	Port 5	---00000B
000016H	DDR6	Port 6 direction register	R/W	Port 6	00000000B
000017H	DDR7	Port 7 direction register	R/W	Port 7	00000000B
000018H	DDR8	Port 8 direction register	R/W	Port 8	00000000B
000019H	DDR9	Port 9 direction register	R/W	Port 9	00000000B
00001AH	DDRA	Port A direction register	R/W	Port A	00000000B
00001BH	ADER	Analog input enable register	R/W	Port 6, A/Dconverter	11111111B
00001CH	OCP5	OCU compare register ch.5	R/W	16-bit I/O timer (output compare 1 (OCU) section)	XXXXXXXXB
00001DH					XXXXXXXXB
00001EH	(Disabled)				
00001FH	EICR	Wake-up interrupt enable register	W	Wake-up interrupt	00000000B

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
000020H	SMR	Serial mode register	R/W	UART (SCI)	0 0 0 0 0 0 0 0B
000021H	SCR	Serial control register	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR/ SODR	Serial input data register/ serial output data register	R/W		XXXXXXXXB
000023H	SSR	Serial status register	R/W		0 0 0 0 1 – 0 0B
000024H	SMCSL0	Serial mode control lower status register 0	R/W	Extended I/O serial interface 0	– – – – 0 0 0 0B
000025H	SMCSH0	Serial mode control upper status register 0	R/W		0 0 0 0 0 0 1 0B
000026H	SDR0	Serial data register 0	R/W		XXXXXXXXB
000027H	CDCR	Communications prescaler control register	R/W	Communications prescaler control register	0 – – – 1 1 1 1B
000028H	SMCSL1	Serial mode control lower status register 1	R/W	Extended I/O serial interface 1	– – – – 0 0 0 0B
000029H	SMCSH1	Serial mode control upper status register 1	R/W		0 0 0 0 0 0 1 0B
00002AH	SDR1	Serial data register 1	R/W		XXXXXXXXB
00002BH	(Disabled)				
00002CH	OCS45	OCU control status register ch.45	R/W	16-bit I/O timer (output compare 1 (OCU) section)	0 0 0 0 – – 0 0B
00002DH					– – – – 0 0 0 0B
00002EH	OCS67	OCU control status register ch.67	R/W		0 0 0 0 – – 0 0B
00002FH					– – – – 0 0 0 0B
000030H	ENIR	DTP/interrupt enable register	R/W	DTP/external interrupt circuit	0 0 0 0 0 0 0 0B
000031H	EIRR	DTP/interrupt factor register	R/W		XXXXXXXXB
000032H	ELVR	Request level setting register	R/W		0 0 0 0 0 0 0 0B
000033H					0 0 0 0 0 0 0 0B
000034H	OCP6	OCU compare register ch.6	R/W	16-bit I/O timer (output compare 1 (OCU) section)	XXXXXXXXB
000035H					XXXXXXXXB
000036H	ADCS1	A/D control status register lower digits	R/W	8/10-bit A/D converter	0 0 0 0 0 0 0 0B
000037H	ADCS2	A/D control status register upper digits	R/W		0 0 0 0 0 0 0 0B
000038H	ADCR1	A/D data register lower digits	R		XXXXXXXXB
000039H	ADCR2	A/D data register upper digits	R/W		0 0 0 0 1 – XXB
00003AH	DADR0	D/A converter data register ch.0	R/W	8/10-bit D/A converter	XXXXXXXXB
00003BH	DADR1	D/A converter data register ch.1	R/W		XXXXXXXXB
00003CH	DACR0	D/A control register 0	R/W		– – – – – – – 0B
00003DH	DACR1	D/A control register 1	R/W		– – – – – – – 0B

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
00003E$_H$	CLKR	Clock output enable register	R/W	Clock monitor function	– – – – 0 0 0 0 $_B$
00003F$_H$	(Disabled)				
000040$_H$	PRLL0	PPG0 re-load register L	R/W	8/16-bit PPG timer 0, 1	X X X X X X X X $_B$
000041$_H$	PRLH0	PPG0 re-load register H	R/W		X X X X X X X X $_B$
000042$_H$	PRLL1	PPG1 re-load register L	R/W		X X X X X X X X $_B$
000043$_H$	PRLH1	PPG1 re-load register H	R/W		X X X X X X X X $_B$
000044$_H$	PPGC0	PPG0 operating mode control register	R/W		0 – 0 0 0 – – 1 $_B$
000045$_H$	PPGC1	PPG1 operating mode control register	R/W		0 X 0 0 0 0 0 1 $_B$
000046$_H$	PPGOE0/ PPGOE1	PPG0 and 1 output control registers	R/W		0 0 0 0 0 0 0 0 $_B$
000047$_H$	(Disabled)				
000048$_H$	TMCSR0	Timer control status register ch.0	R/W	16-bit re-load timer 0	0 0 0 0 0 0 0 0 $_B$
000049$_H$					– – – – 0 0 0 0 $_B$
00004A$_H$	TMR0/ TMRLR0	16-bit timer register ch.0/ 16-bit re-load register ch.0	R/W		X X X X X X X X $_B$
00004B$_H$					X X X X X X X X $_B$
00004C$_H$	TMCSR1	Timer control status register ch.1	R/W	16-bit re-load timer 1	0 0 0 0 0 0 0 0 $_B$
00004D$_H$					– – – – 0 0 0 0 $_B$
00004E$_H$	TMR1/ TMRLR1	16-bit timer register ch.1/ 16-bit re-load register ch.1	R/W		X X X X X X X X $_B$
00004F$_H$					X X X X X X X X $_B$
000050$_H$	IPCP0	ICU data register ch.0	R	16-bit I/O timer (input compare 0, 1 (ICU) section)	X X X X X X X X $_B$
000051$_H$					X X X X X X X X $_B$
000052$_H$	IPCP1	ICU data register ch.1	R		X X X X X X X X $_B$
000053$_H$					X X X X X X X X $_B$
000054$_H$	ICS01	ICU control status register	R/W		0 0 0 0 0 0 0 0 $_B$
000055$_H$	(Disabled)				
000056$_H$	TCDT1	Free-run timer data register 1	R/W	16-bit I/O timer (16-bit free-run timer 1 section)	0 0 0 0 0 0 0 0 $_B$
000057$_H$					0 0 0 0 0 0 0 0 $_B$
000058$_H$	TCCS1	Free-run timer control status register 1	R/W		0 0 0 0 0 0 0 0 $_B$
000059$_H$	(Disabled)				

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
00005A$_H$	OCP0	OCU compare register ch.0	R/W	16-bit I/O timer (output compare 0 (OCU) section)	XXXXXXXX$_B$
00005B$_H$					XXXXXXXX$_B$
00005C$_H$	OCP1	OCU compare register ch.1	R/W		XXXXXXXX$_B$
00005D$_H$					XXXXXXXX$_B$
00005E$_H$	OCP2	OCU compare register ch.2	R/W		XXXXXXXX$_B$
00005F$_H$					XXXXXXXX$_B$
000060$_H$	OCP3	OCU compare register ch.3	R/W		XXXXXXXX$_B$
000061$_H$					XXXXXXXX$_B$
000062$_H$	OCS01	OCU control status register ch.01	R/W		0000––00$_B$
000063$_H$					–––00000$_B$
000064$_H$	OCS23	OCU control status register ch.23	R/W		0000––00$_B$
000065$_H$					–––00000$_B$
000066$_H$	TCDT2	Free-run timer data register 2	R/W	16-bit I/O timer (16-bit free-run timer 2 section)	00000000$_B$
000067$_H$					00000000$_B$
000068$_H$	TCCS2	Free-run timer control status register 2	R/W		00000000$_B$
000069$_H$	(Disabled)				
00006A$_H$	LCR0	LCDC control registers 0 and 1	R/W	LCD controller/ driver	00010000$_B$
00006B$_H$	LCR1		R/W		00000000$_B$
00006C$_H$	OCP7	OCU compare register ch.7	R/W	16-bit I/O timer (output compare 1 (OCU) section)	XXXXXXXX$_B$
00006D$_H$					XXXXXXXX$_B$
00006E$_H$	(Disabled)				
00006F$_H$	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	–––––––1$_B$
000070$_H$ to 00007F$_H$	VRAM	RAM for LCD indication	R/W	LCD controller/ driver	XXXXXXXX$_B$
000080$_H$	UDCR0	Up/down count register 0	R	8/16-bit up/down counter/timer 0, 1	00000000$_B$
000081$_H$	UDCR1	Up/down count register 1	R		00000000$_B$
000082$_H$	RCR0	Re-load compare register 0	W		00000000$_B$
000083$_H$	RCR1	Re-load compare register 1	W		00000000$_B$
000084$_H$	CSR0	Counter status register 0	R/W		00000000$_B$
000085$_H$	(Reserved area)*3				
000086$_H$	CCRL0	Counter control register 0	R/W	8/16-bit up/down counter/timer 0, 1	–0000000$_B$
000087$_H$	CCRH0				00000000$_B$
000088$_H$	CSR1	Counter status register 1	R/W		00000000$_B$

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
000089H	(Reserved area)*3				
00008AH	CCRL1	Counter control register 1	R/W	8/16-bit up/down counter/timer 0, 1	– 0 0 0 0 0 0 0 B
00008BH	CCRH1				– 0 0 0 0 0 0 0 B
00008CH	RDR0	Port 0 input pull-up resistor setup register	R/W	Port 0	0 0 0 0 0 0 0 0 B
00008DH	RDR1	Port 1 input pull-up resistor setup register	R/W	Port 1	0 0 0 0 0 0 0 0 B
00008EH	RDR4	Port 4 input pull-up resistor setup register	R/W	Port 4	0 0 0 0 0 0 0 0 B
00008FH to 00009DH	(Area used by the system)*3				
00009EH	PACSR	Program address detection control status register	R/W	Address match detection function	0 0 0 0 0 0 0 0 B
00009FH	DIRR	Delayed interrupt factor generation/ cancellation register	R/W	Delayed interrupt generation module	– – – – – – – 0 B
0000A0H	LPMCR	Low-power consumption mode control register	R/W!	Low-power consumption (stand-by) mode	0 0 0 1 1 0 0 0 B
0000A1H	CKSCR	Clock select register	R/W		1 1 1 1 1 1 0 0 B
0000A2H to 0000A7H	(Disabled)				
0000A8H	WDTC	Watchdog timer control register	R/W	Watchdog timer	X X X X X X X X B
0000A9H	TBTC	Timebase timer control register	R/W	Timebase timer	1 – – 0 0 1 0 0 B
0000AAH	WTC	Clock timer control register	R/W	Clock timer	1 X 0 0 0 0 0 0 B
0000ABH to 0000ADH	(Disabled)				
0000AEH	FMCS	Flash control register	R/W	Flash interface	1 – – 0 0 1 0 0 B
0000AFH	(Disabled)				

(Continued)

(Continued)

Address	Abbreviated register name	Register name	Read/ write	Resource name	Initial value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01	R/W		00000111B
0000B2H	ICR02	Interrupt control register 02	R/W		00000111B
0000B3H	ICR03	Interrupt control register 03	R/W		00000111B
0000B4H	ICR04	Interrupt control register 04	R/W		00000111B
0000B5H	ICR05	Interrupt control register 05	R/W		00000111B
0000B6H	ICR06	Interrupt control register 06	R/W		00000111B
0000B7H	ICR07	Interrupt control register 07	R/W		00000111B
0000B8H	ICR08	Interrupt control register 08	R/W		00000111B
0000B9H	ICR09	Interrupt control register 09	R/W		00000111B
0000BAH	ICR10	Interrupt control register 10	R/W		00000111B
0000BBH	ICR11	Interrupt control register 11	R/W		00000111B
0000BCH	ICR12	Interrupt control register 12	R/W		00000111B
0000BDH	ICR13	Interrupt control register 13	R/W		00000111B
0000BEH	ICR14	Interrupt control register 14	R/W		00000111B
0000BFH	ICR15	Interrupt control register 15	R/W		00000111B
0000C0H to 0000FFH	(External area)*1				
000100H to 00####H	(RAM area)*2				
00####H to 001FEFH	(Reserved area)*3				
001FF0H	PADR0	Program address detection register 0	R/W	Program patch processing	XXXXXXXXB
001FF1H		Program address detection register 1	R/W		XXXXXXXXB
001FF2H		Program address detection register 2	R/W		XXXXXXXXB
001FF3H	PADR1	Program address detection register 3	R/W		XXXXXXXXB
001FF4H		Program address detection register 4	R/W		XXXXXXXXB
001FF5H		Program address detection register 5	R/W		XXXXXXXXB
001FF6H to 001FFFH	(Reserved area)*3				

Descriptions for read/write

R/W: Readable and writable

R: Read only

W: Write only

Descriptions for initial value

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is indeterminate.

– : This bit is not used. The initial value is indeterminate.

*1: This area is the only external access area having an address of 0000FF$_H$ or lower. An access operation to this area is handled as that to external I/O area.

*2: For details of the RAM area, see the memory map.

*3: The reserved area is basically disabled because it is used in the system.

*4: Area used by the system is the area set by the resistor for evaluating tool.

Notes:
- For bits that is initialized by an reset operation, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.
  For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.
- The addresses following 0000FF$_H$ are reserved. No external bus access signal is generated.
- Boundary ####$_H$ between the RAM area and the reserved area varies with the product model.
- Channels 0 to 3 of the OCU compare register use 16-bit free-run timer 2, while channels 4 to 7 of the OCU compare register use 16-bit free-run timer 1. 16-bit free-run timer 1 is also used by input captures (ICU) 0 and 1.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt source	EI²OS support	Interrupt vector		Interrupt control register		Priority
		Number	Address	ICR	Address	
Reset	×	# 08	FFFFDC$_H$	—	—	High
INT9 instruction	×	# 09	FFFFD8$_H$	—	—	
Exception	×	# 10	FFFFD4$_H$	—	—	
8/10-bit A/D converter	○	# 11	FFFFD0$_H$	ICR00	0000B0$_H$	
Timebase timer	×	# 12	FFFFCC$_H$			
DTP0/DTP1 (external interrupt 0/ external interrupt 1)	○	# 13	FFFFC8$_H$	ICR01	0000B1$_H$	
16-bit free-run timer 1 overflow	×	# 14	FFFFC4$_H$			
Extended I/O serial interface 0	○	# 15	FFFFC0$_H$	ICR02	0000B2$_H$	
Wake-up interrupt	×	# 16	FFFFBC$_H$			
Extended I/O serial interface 1	○	# 17	FFFFB8$_H$	ICR03	0000B3$_H$	
DTP2/DTP3 (external interrupt 2/ external interrupt 3)	○	# 18	FFFFB4$_H$			
8/16-bit PPG timer 0 counter borrow	×	# 19	FFFFB0$_H$	ICR04	0000B4$_H$	
DTP4/DTP5 (external interrupt 4/ external interrupt 5)	○	# 20	FFFFAC$_H$			
8/16-bit up/down counter/timer 0 compare match	○	# 21	FFFFA0$_H$	ICR05	0000B5$_H$	
8/16-bit up/down counter/timer 0 overflow/inversion	○	# 22	FFFFA4$_H$			
8/16-bit PPG timer 1 counter borrow	×	# 23	FFFFA0$_H$	ICR06	0000B6$_H$	
DTP6/DTP7 (external interrupt 6/ external interrupt 7)	○	# 24	FFFF9C$_H$			
Output compare 1 (OCU) ch.4/ch.5 match	○	# 25	FFFF98$_H$	ICR07	0000B7$_H$	
Clock prescaler	×	# 26	FFFF94$_H$			
Output compare 1 (OCU) ch.6/ch.7 match	○	# 27	FFFF90$_H$	ICR08	0000B8$_H$	
16-bit free-run timer 2 overflow	×	# 28	FFFF8C$_H$			
8/16-bit up/down counter/timer 1 compare match	○	# 29	FFFF88$_H$	ICR09	0000B9$_H$	
8/16-bit up/down counter/timer 1 overflow/inversion	○	# 30	FFFF84$_H$			
Input capture 0 (ICU) include	○	# 31	FFFF80$_H$	ICR10	0000BA$_H$	
Input capture 1 (ICU) include	○	# 32	FFFF7C$_H$	ICR10	0000BA$_H$	Low

(Continued)

(Continued)

Interrupt source	EI²OS support	Interrupt vector		Interrupt control register		Priority
		Number	Address	ICR	Address	
Output compare 0 (OCU) ch.0 match	○	# 33	FFFF78H	ICR11	0000BBH	High
Output compare 0 (OCU) ch.1 match	○	# 34	FFFF74H			
Output compare 0 (OCU) ch.2 match	○	# 35	FFFF70H	ICR12	0000BCH	
Output compare 0 (OCU) ch.3 match	×	# 36	FFFF6CH			
UART (SCI) reception complete	◎	# 37	FFFF68H	ICR13	0000BDH	
16-bit re-load timer 0	○	# 38	FFFF64H			
UART (SCI) transmission complete	◎	# 39	FFFF60H	ICR14	0000BEH	
16-bit re-load timer 1	○	# 40	FFFF5CH			
Reserved	×	# 41	FFFF58H	ICR15	0000BFH	
Delayed interrupt generation module	×	# 42	FFFF54H			Low

○ : Can be used

× : Can not be used

◎ : Can be used. With EI²OS stop function.

■ PERIPHERALS

1. I/O Port

(1) Input/Output Port

Port 0 through 8, A are general-purpose I/O ports having a combined function as a resource input. The input output ports function as general-purpose I/O port only in the single-chip mode.

- Operation as output port
  The pin is configured as an output port by setting the corresponding bit of the DDR register to “1”.
  Writing data to PDR register when the port is configured as output, the data is retained in the output latch in the PDR and directly output to the pin.

  The value of the pin (the same value retained in the output latch of PDR) can be read out by reading the PDR register.

Note: When a read-modify-write type instruction (e.g. bit set instruction) is performed to the port data register, the destination bit of the operation is set to the specified value, not affecting the bits configured by the DDR register for output, however, values of bits configured by the DDR register as inputs are changed because input values to the pins are written into the output latch. To avoid this situation, configure the pins by the DDR register as output after writing output data to the PDR register when configuring the bit used as input as outputs.

- Operation as input port
  The pin is configured as an input by setting the corresponding bit of the DDR register to “0”.

  When the pin is configured as an input, the output buffer is turned-off and the pin is put into a high-impedance status.

  When a data is written into the PDR register, the data is retained in the output latch of the PDR, but pin outputs are unaffected.

  Reading the PDR register reads out the pin level (“0” or “1”).

(2) Register Configuration

- Port 0 data register (PDR0)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000000H	(PDR1)	P07	P06	P05	P04	P03	P02	P01	P00	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 data register (PDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000001H	P17	P16	P15	P14	P13	P12	P11	P10	(PDR0)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 2 data register (PDR2)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000002H	(PDR3)	P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 3 data register (PDR3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000003H	P37	P36	P35	P34	P33	P32	P31	P30	(PDR2)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 4 data register (PDR4)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000004H	(PDR5)	P47	P46	P45	P44	P43	P42	P41	P40	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 5 data register (PDR5)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000005H	—	—	—	P54	P53	P52	P51	P50	(PDR4)	- - -XXXXXB
	—	—	—	R/W	R/W	R/W	R/W	R/W		

- Port 6 data register (PDR6)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000006H	(PDR7)	P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7 data register (PDR7)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000007H	P77	P76	P75	P74	P73	P72	P71	P70	(PDR6)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 8 data register (PDR8)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000008H	(PDR9)	P87	P86	P85	P84	P83	P82	P81	P80	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 9 data register (PDR9)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000009H	P97	P96	P95	P94	P93	P92	P91	P90	(PDR8)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

(Continued)

- Port A data register (PDRA)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00000A$_H$	(LCDCMR)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	XXXXXXXX$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 0 direction register (DDR0)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000010$_H$	(DDR1)	D07	D06	D05	D04	D03	D02	D01	D00	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 direction register (DDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000011$_H$	D17	D16	D15	D14	D13	D12	D11	D10	(DDR0)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 2 direction register (DDR2)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000012$_H$	(DDR3)	D27	D26	D25	D24	D23	D22	D21	D20	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 3 direction register (DDR3)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000013$_H$	D37	D36	D35	D34	D33	D32	D31	D30	(DDR2)	00000000$_B$
				R/W	R/W	R/W	R/W	R/W		

- Port 4 direction register (DDR4)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000014$_H$	(DDR5)	D47	D46	D45	D44	D43	D42	D41	D40	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 5 direction register (DDR5)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000015$_H$	—	—	—	D54	D53	D52	D51	D50	(DDR4)	- - - 00000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 6 direction register (DDR6)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000016$_H$	(DDR7)	D67	D66	D65	D64	D63	D62	D61	D60	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 7 direction register (DDR7)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000017$_H$	D77	D76	D75	D74	D73	D72	D71	D70	(DDR6)	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 8 direction register (DDR8)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000018$_H$	(DDR9)	D87	D86	D85	D84	D83	D82	D81	D80	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

(Continued)

(Continued)

- Port 9 direction register (DDR9)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000019H	D97	D96	D95	D94	D93	D92	D91	D90	(DDR8)	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port A direction register (DDRA)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00001AH	(ADER)	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 0 input pull-up resistor setup register (RDR0)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00008CH	(RDR1)	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Port 1 input pull-up resistor setup register (RDR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00008DH	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	(RDR0)	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- Port 4 input pull-up resistor setup register (RDR4)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00008EH	(Disabled)	RD47	RD46	RD45	RD44	RD43	RD42	RD41	RD40	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Analog input enable register (ADER)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00001BH	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	(DDRA)	11111111B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

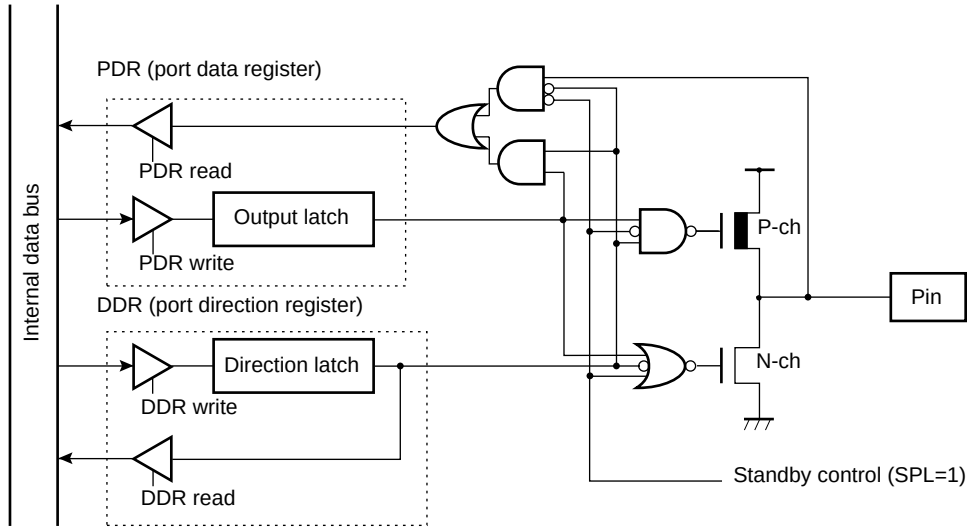
- Port 7/COM pin selection register (LCDCMR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00000BH	—	—	—	—	COM3	COM2	COM1	COM0	(PDRA)	----0000B
	—	—	—	—	R/W	R/W	R/W	R/W		

R/W : Readable and writable
— : Unused
X : Indeterminate

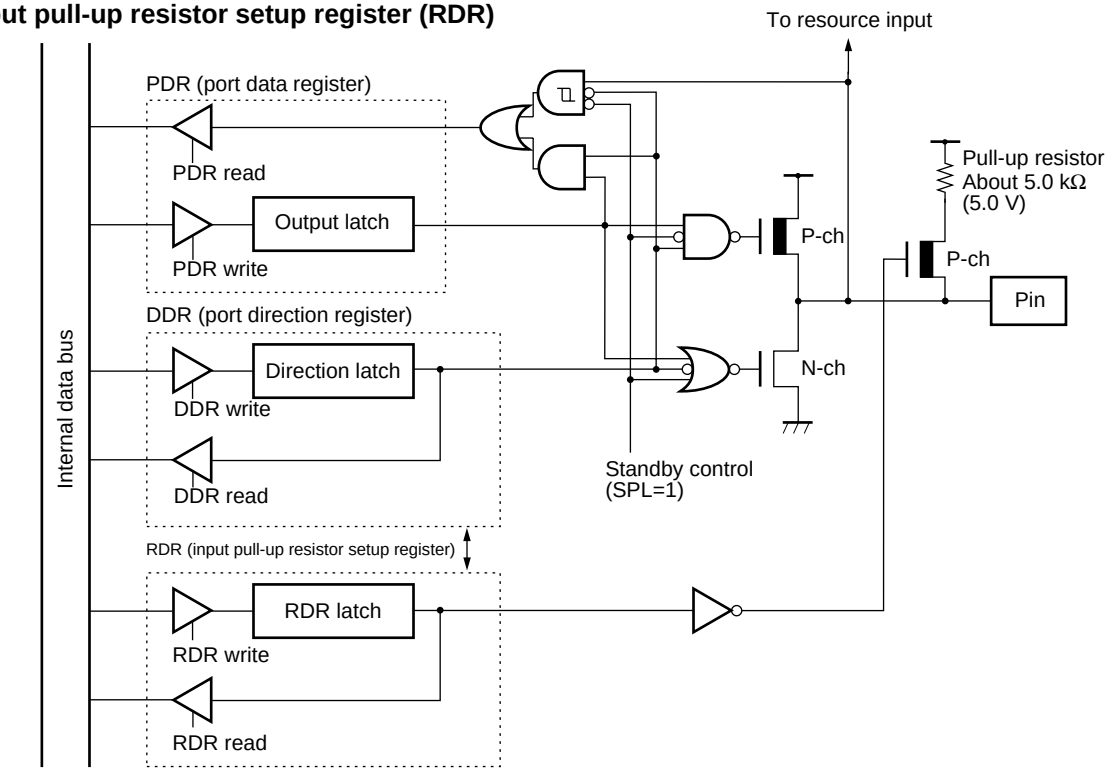
(3) Block Diagram

- **Input/output port**



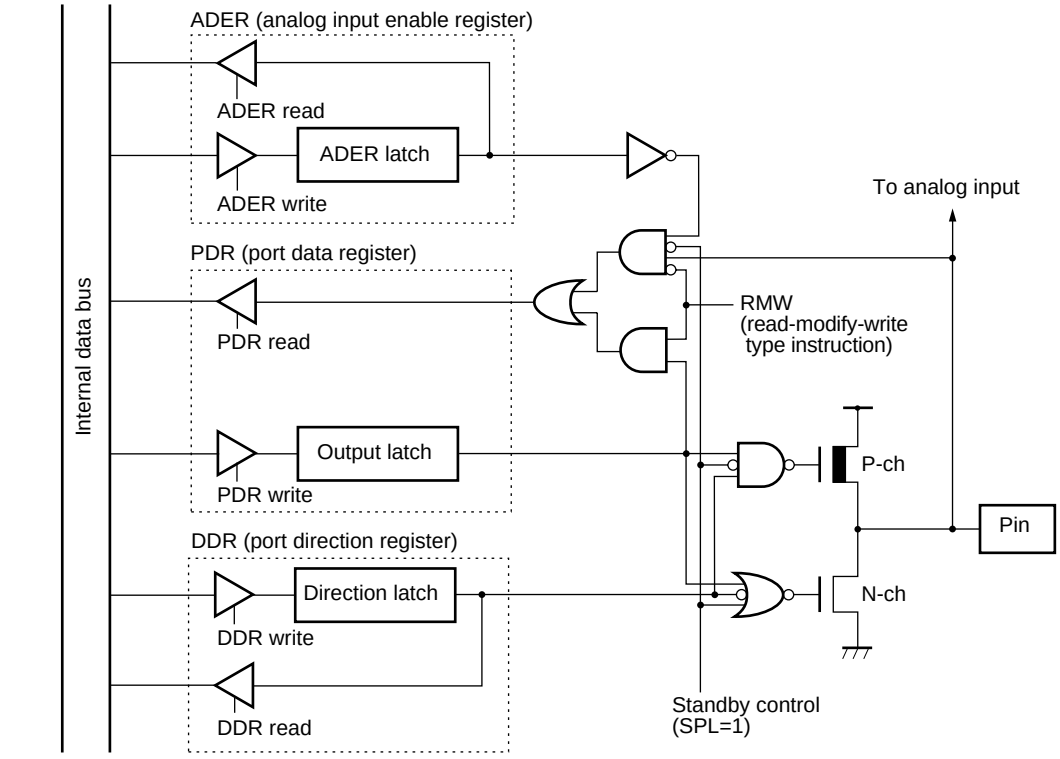
Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

- **Input pull-up resistor setup register (RDR)**



Standby control: Stop, timebase timer mode and SPL=1

- **Analog input enable register (ADER)**



Standby control: Stop, timebase timer mode and SPL=1

2. Timebase Timer

The timebase timer is a 18-bit free-run counter (timebase counter) for counting up in synchronization to the internal count clock (divided-by-2 of oscillation) with an interval timer function for selecting an interval time from four types of 2^{12}/HCLK, 2^{14}/HCLK, 2^{16}/HCLK, and 2^{19}/HCLK.

The timebase timer also has a function for supplying operating clocks for the timer output for the oscillation stabilization time or the watchdog timer etc.

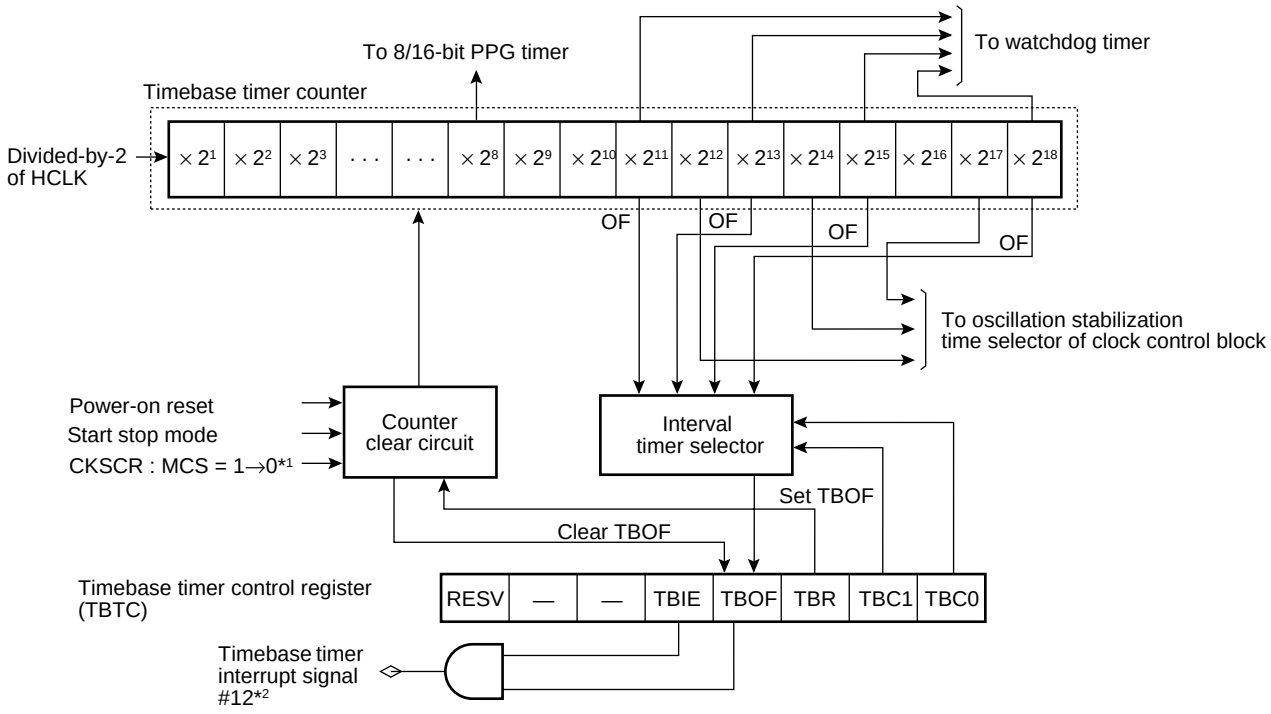
(1) Register Configuration

- Timebase timer control register (TBTC)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
0000A9H	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0	(WDTC)	1--00000B
	—	—	—	R/W	R/W	R/W	R/W	R/W		

R/W: Readable and writable
— : Unused
RESV: Reserved bit

(2) Block Diagram



OF: Overflow
HCLK: Oscillation clock
*1: Switch machine clock from oscillation clock to PLL clock
*2: Interrupt number

3. Watchdog Timer

The watchdog timer is a 2-bit counter operating with an output of the timebase timer and resets the CPU when the counter is not cleared for a preset period of time.

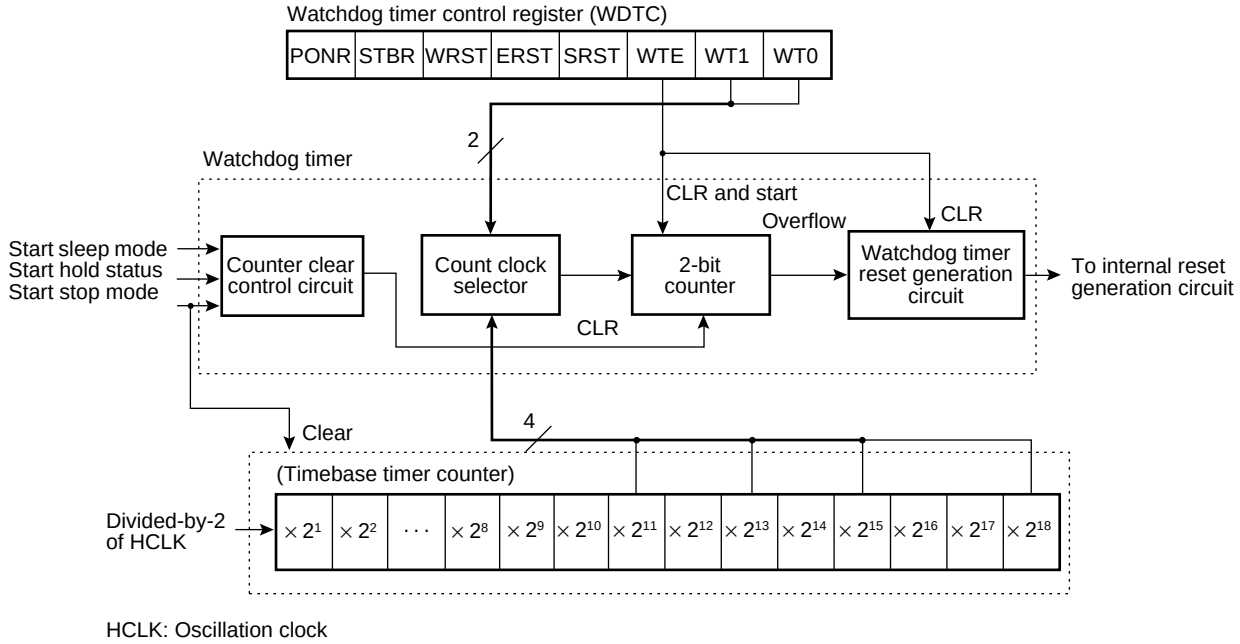
(1) Register Configuration

- Watchdog timer control register (WDTC)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A8H	(TBTC)	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	XXXXXXXXB
		R	R	R	R	R	W	W	W	

R : Read only
W: Write only
X : Indeterminate

(2) Block Diagram



HCLK: Oscillation clock

4. 8/16-bit PPG Timer 0, 1

The 8/16-bit PPG timer is a 2-CH re-load timer module for outputting pulse having given frequencies/duty ratios.

The two modules performs the following operation by combining functions.

- 8-bit PPG output 2-CH independent operation mode
  This is a mode for operating independent 2-CH 8-bit PPG timer, in which PPG0 and PPG1 pins correspond to outputs from PPG0 and PPG1 respectively.
- 16-bit PPG timer output operation mode
  In this mode, PPG0 and PPG1 are combined to be operated as a 1-CH 8/16-bit PPG timer 0 and 1 operating as a 16-bit timer. Because PPG0 and PPG1 outputs are reversed by an underflow from PPG1 outputting the same output pulses from PPG0 and PPG1 pins.
- 8 + 8-bit PPG timer output operation mode
  In this mode, PPG0 is operated as an 8-bit communications pre-scaler, in which an underflow output of PPG0 is used as a clock source for PPG1. A toggle output of PPG0 and PPG output of PPG1 are output from PPG0 and PPG1 respectively.
- PPG output operation
  A pulse wave with any period/duty ratio is output. The module can also be used as a D/A converter with an external add-on circuit.

(1) Register Configuration

- PPG0 operating mode control register (PPGC0)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000044H	(PPGC1)	PEN0	—	PE00	PIE0	PUF0	—	—	RESV	0-000--1B
		R/W	—	R/W	R/W	R/W	—	—	—	

- PPG1 operating mode control register (PPGC1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000045H	PEN1	—	PE10	PIE1	PUF1	MD1	MD0	RESV	(PPGC0)	0X000001B
	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W		

- PPG0 output control register (PPGOE0)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000046H	(Disabled)	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	PE11	PE01	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG1 output control register (PPGOE1)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000046H	(Disabled)	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	PE11	PE01	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- PPG0 re-load register H (PRLH0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000041H									(PRLL0)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- PPG1 re-load register H (PRLH1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
000043H									(PRLL1)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- PPG0 re-load register L (PRLL0)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000040H	(PRLH0)									XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

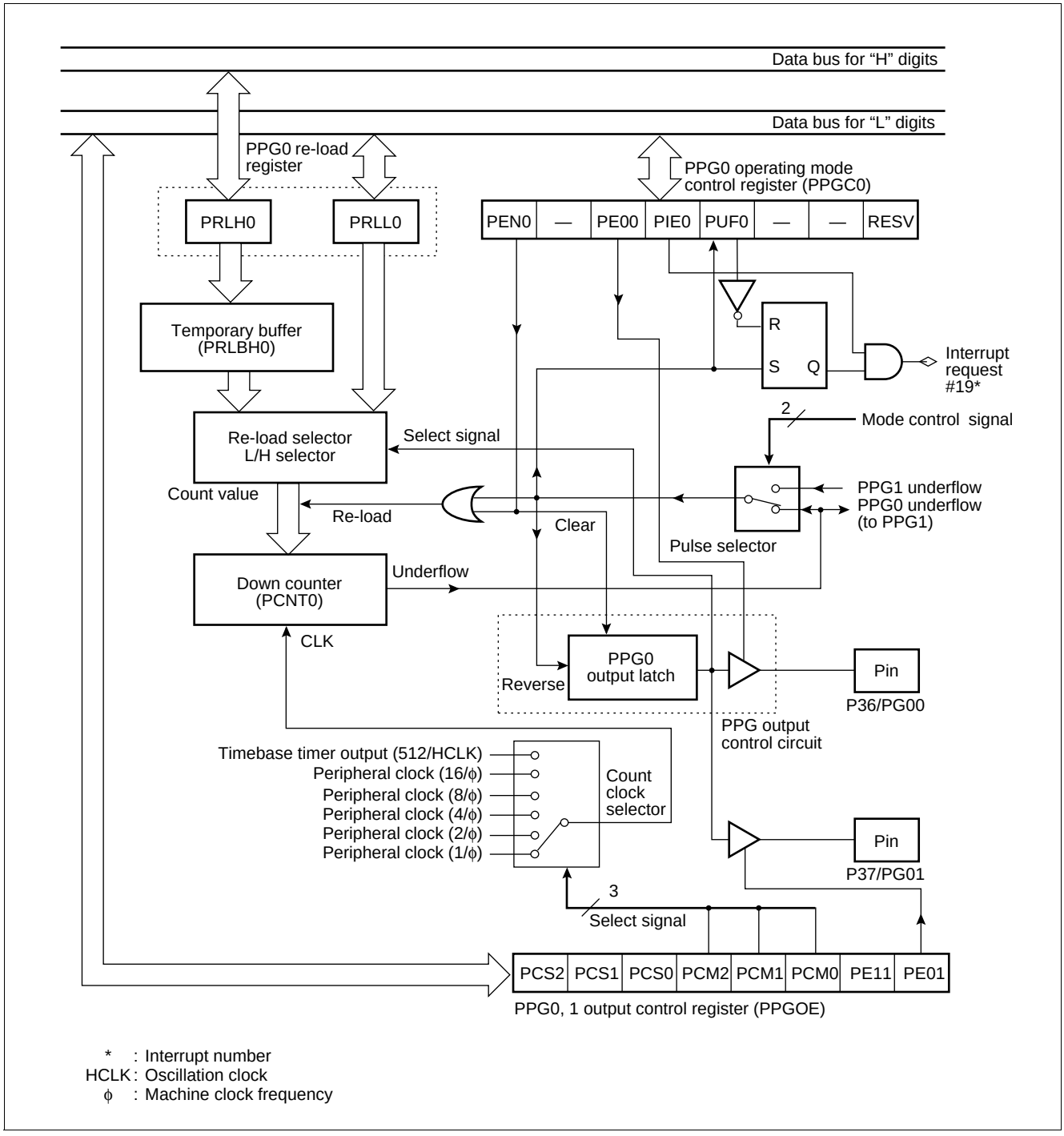
- PPG1 re-load register L (PRLL1)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000042H	(PRLH1)									XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
— : Unused
X : Indeterminate
RESV: Reserved bit

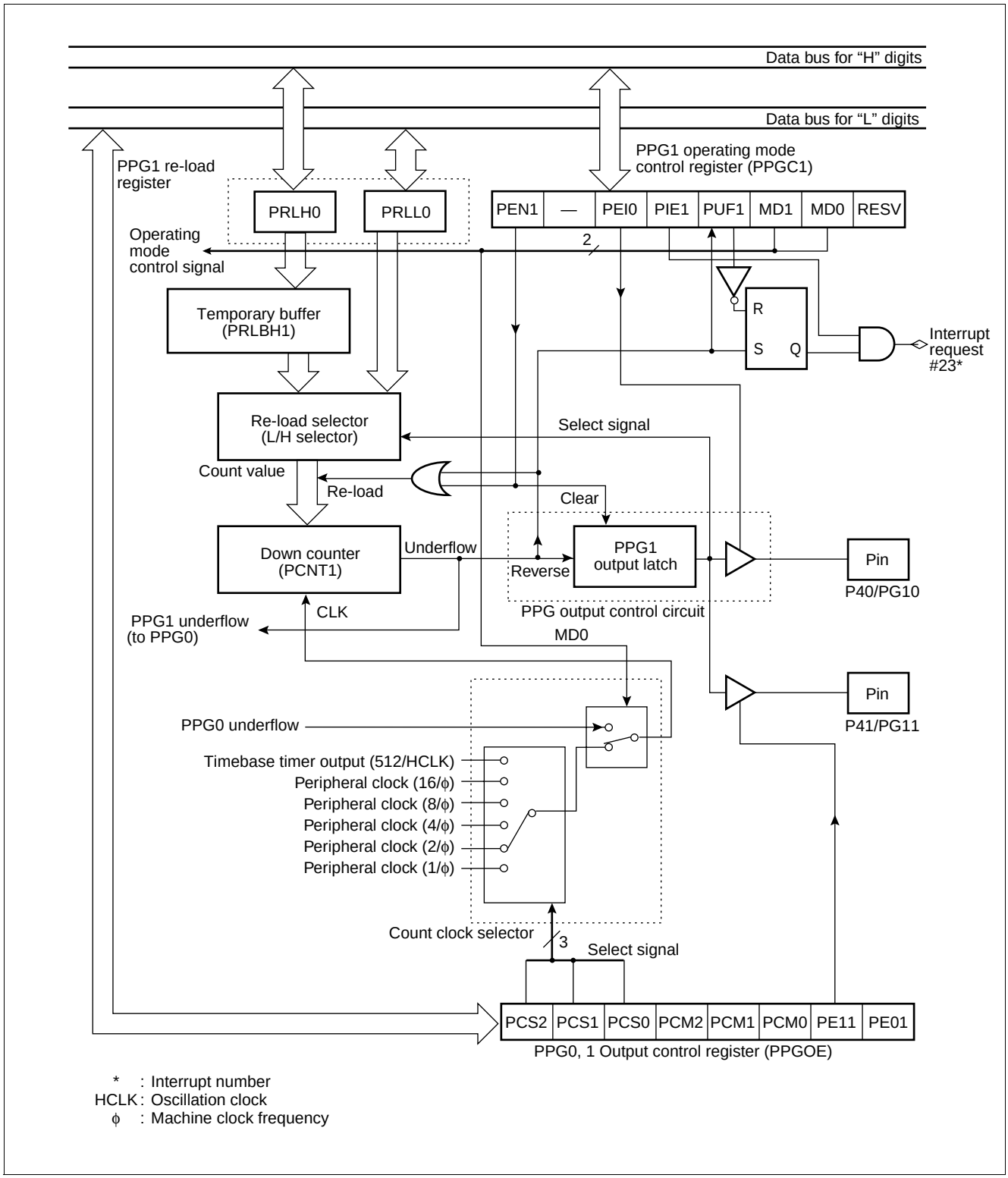
(2) Block Diagram

- **Block diagram of 8/16-bit PPG timer 0**



* : Interrupt number
HCLK : Oscillation clock
ϕ : Machine clock frequency

- **Block diagram of 8/16-bit PPG timer 1**



* : Interrupt number
HCLK : Oscillation clock
ϕ : Machine clock frequency

5. 16-bit Re-load Timer 0, 1 (With an Event Count Function)

The 16-bit re-load timer has an internal clock mode for counting down in synchronization to three types of internal clocks and an event count mode for counting down detecting a given edge of the pulse input to the external bus pin, and either of the two functions can be selectively used.

For this timer, an “underflow” is defined as the timing of transition from the counter value of “0000_H” to “$FFFF_H$”. According to this definition, an underflow occurs after [re-load register setting value + 1] counts.

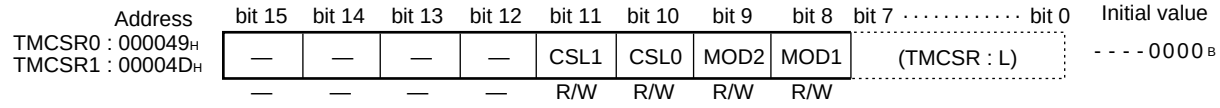
In operaring the counter, the re-load mode for repeating counting operation after re-loading a counter value after an underflow or the one-shot mode for stopping the counting operation after an underflow can be selectively used.

Because the timer can generate an interrupt upon an underflow, the timer conforms to the extended intelligent I/O service (EI^2OS).

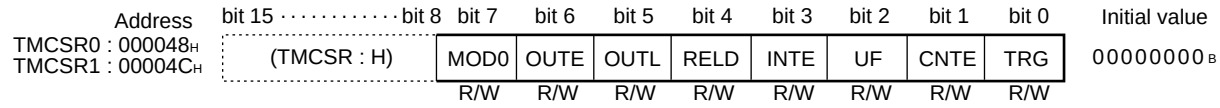
The MB90520 series has 2 channels of 16-bit re-load timers.

(1) Register Configuration

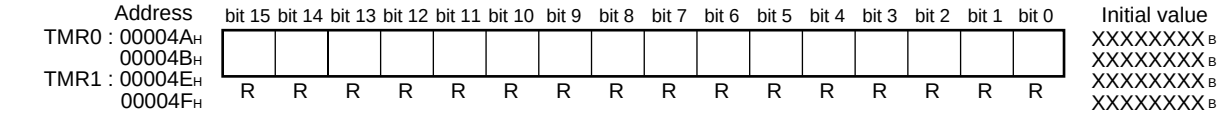
- Timer control status register upper digits ch.0, ch.1 (TMCSR0, TMCSR1 : H)



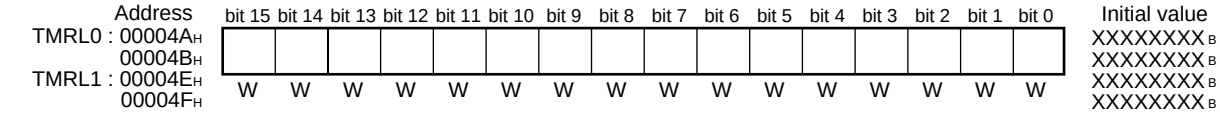
- Timer control status register lower digits ch.0, ch.1 (TMCSR0, TMCSR1 : L)



- 16-bit timer register upper and lower digits ch.0, ch.1 (TMR0, TMR1)

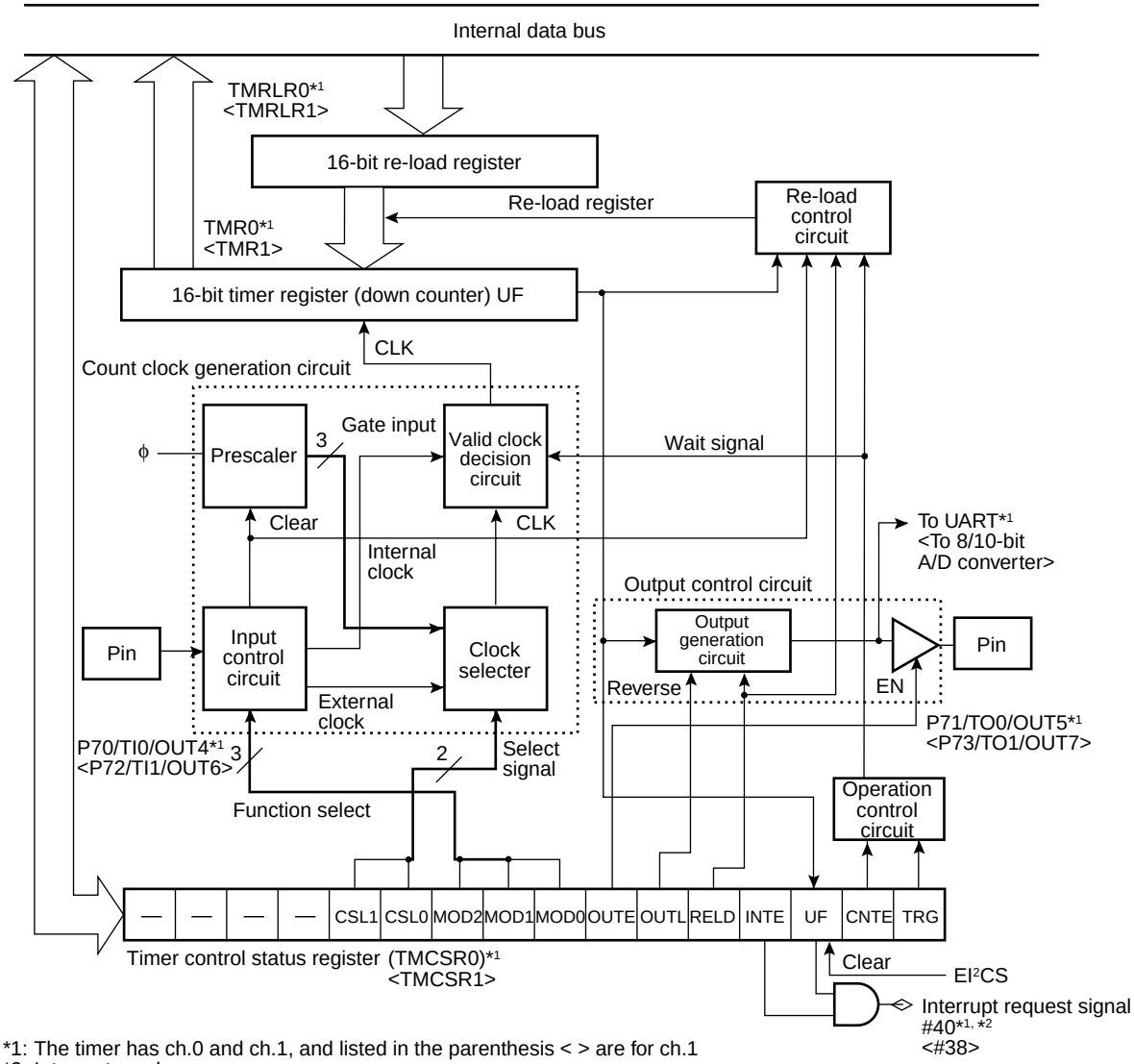


- 16-bit re-load register upper and lower digits ch.0, ch.1 (TMRL0, TMRL1)



R/W : Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate

(2) Block Diagram

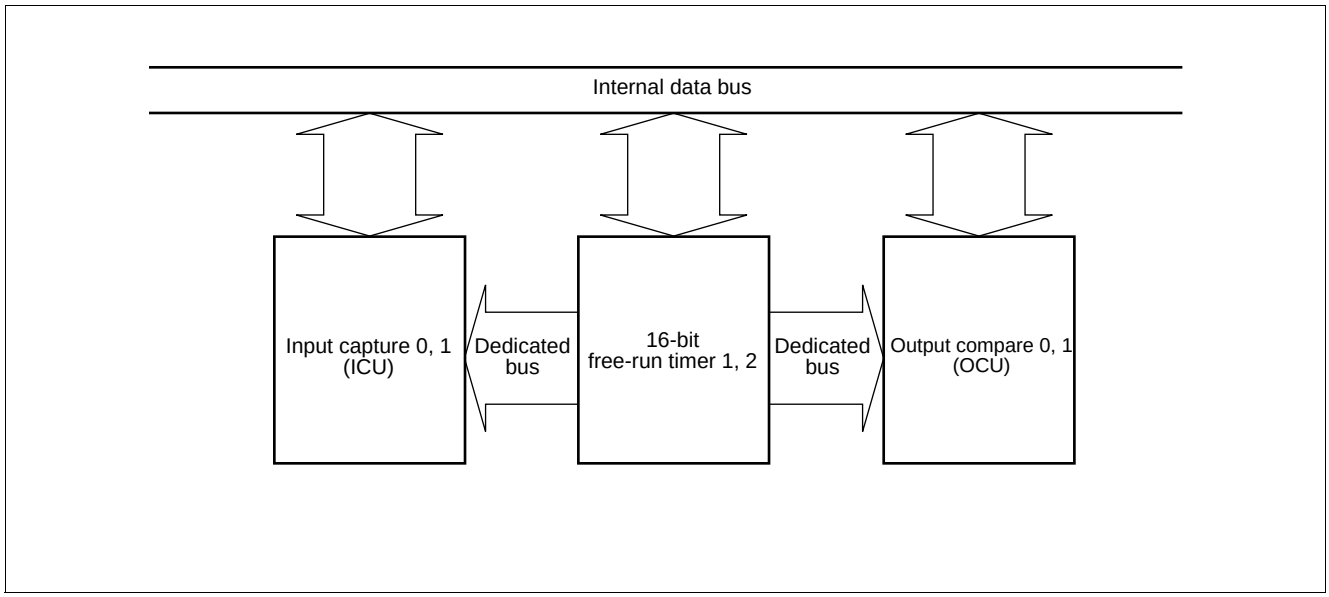


*1: The timer has ch.0 and ch.1, and listed in the parenthesis < > are for ch.1
*2: Interrupt number
ϕ: Machine clock frequency

6. 16-bit I/O Timer

The 16-bit I/O timer module consists of two 16-bit free-run timer, two input capture circuits (ICU), and eight output comparators (OCU). This module allows two independent waveforms to be output on the basis of the 16-bit free-run timer. Input pulse width and external clock periods can, therefore, be measured.

- **Block diagram**



(1) 16-bit Free-run Timer 1, 2

The 16-bit free-run timer consists of a 16-bit up counter, a control register, and a communications prescaler register. The value output from the timer counter is used as basic timer (base timer) for input capture (ICU) and output compare (OCU).

- A counter operation clock can be selected from four internal clocks (ϕ/4, ϕ/16, ϕ/32 and ϕ/64).
- An interrupt can be generated by overflow of counter value or compare match with OCU compare register 0 and 4. (Compare match requires mode setup.)
- The counter value can be initialized to "0000H" by a reset, software clear or compare match with OCU compare register 0 and 4.

- **Register configuration**

- Free-run timer data register 1, 2 (TCDT1, TCDT2)

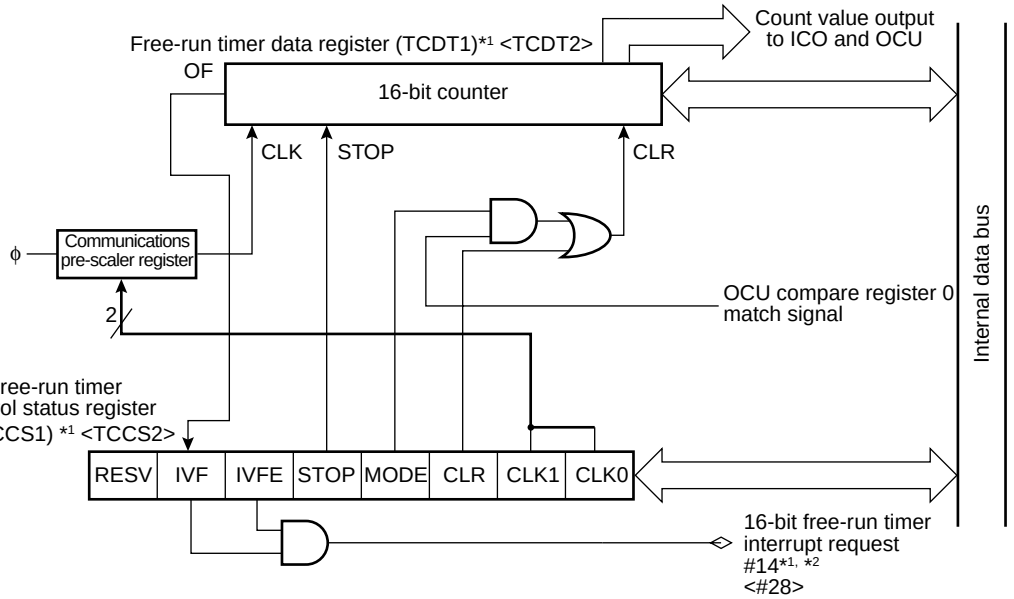
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TCDT1 : 000056H	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	00000000B
000057H																	00000000B
TCDT2 : 000066H																	00000000B
000067H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	00000000B

- Free-run timer control status register 1, 2 (TCCS1, TCCS2)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TCCS1 : 000058H	(Disabled)	RESV	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0	00000000B
TCCS2 : 000068H		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	00000000B

R/W: Readable and writable
RESV: Reserved bit

- **Block diagram**



*1: The timer has ch.1 and ch.2, and listed in the parenthesis < > are for ch.2.
*2: Interrupt number
ϕ : Machine clock frequency
OF : Overflow

(2) Input Capture 0, 1 (ICU)

The input capture (ICU) generates an interrupt request to the CPU simultaneously with a storing operation of current counter value of the 16-bit free-run timer to the ICU data register (IPCP) upon an input of a trigger edge to the external pin.

There are two sets (two channels) of the input capture external pins and ICU data registers, enabling measurements of maximum of four events.

- The input capture has two sets of external input pins (IN0, IN1) and ICU registers (IPCP), enabling measurements of maximum of four events.
- A trigger edge direction can be selected from rising/falling/both edges.
- The input capture can be set to generate an interrupt request at the storage timing of the counter value of the 16-bit free-run timer to the ICU data register (IPCP).
- The input compare conforms to the extended intelligent I/O service (EI^{2}OS).
- The input capture (ICU) function is suited for measurements of intervals (frequencies) and pulse-widths.

- **Register configuration**

- ICU data register ch.0 ch.1 (IPCP0, IPCP1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
IPCP0 : 000051H IPCP1 : 000053H	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	(IPCP0, IPCP1)	XXXXXXXXB
	R	R	R	R	R	R	R	R		

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
IPCP0 : 000050H IPCP1 : 000052H	(IPCP0, IPCP1)	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXXB
		R	R	R	R	R	R	R	R	

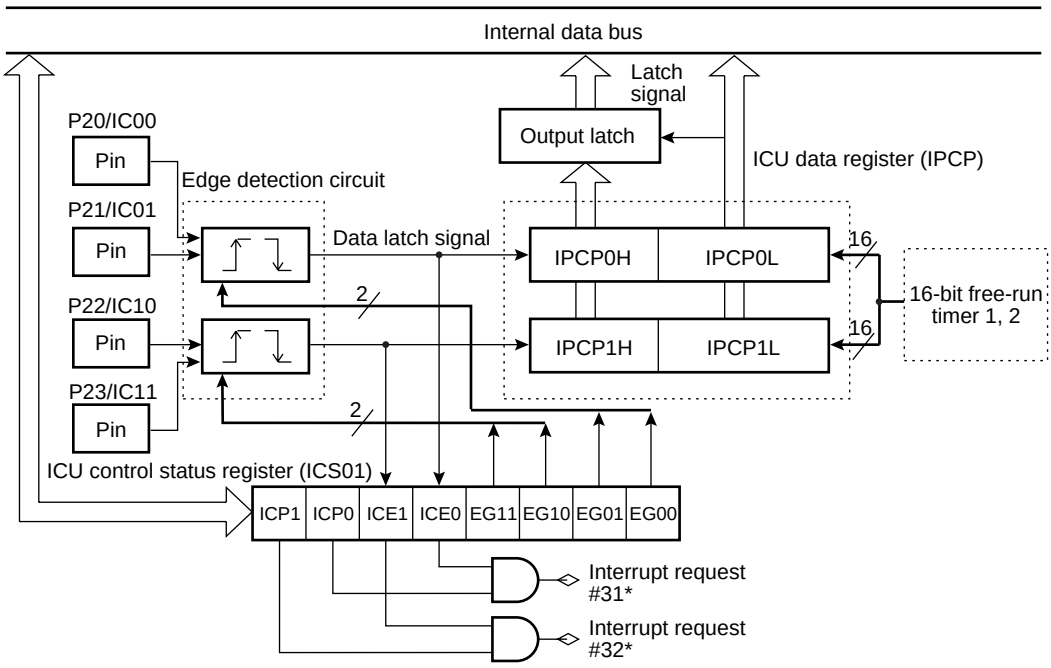
Note: This register holds a 16-bit free-run timer value when the valid edge of the corresponding external pin input waveform is detected. (You can word-access this register, but you cannot program it.)

- ICU cnotrol status register (ICS01)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000054H	(Disabled)	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
R : Read only
X : Unused

- **Block diagram**



* : Interrupt number

(3) Output Compare 0, 1 (OCU)

The output compare (OCU) is two sets of compare units consisting of a eight-channel OCU compare registers, a comparator and a control register.

An interrupt request can be generated for each channel upon a match detection by performing time-division comparison between the OCU compare data register setting value and the counter value of the 16-bit free-run timer.

The OUT pin can be used as a waveform output pin for reversing output upon a match detection or a general-purpose output port for directly outputting the setting value of the CMOD bit.

- **Register Configuration**

- OCU control status register ch.1, ch.23, ch.45, ch.67 (OCS01, OCS23, OCS45, OCS67)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
ch.01 : OCS01 : 0000063H ch.23 : OCS23 : 0000065H ch.45 : OCS45 : 000002DH ch.67 : OCS67 : 000002FH	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	(OCS)	- - - 00000B
	—	—	—	R/W	R/W	R/W	R/W	R/W		

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ch.01 : OCS01 : 000062H ch.23 : OCS23 : 000064H ch.45 : OCS45 : 00002CH ch.67 : OCS67 : 00002EH	(OCS)	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000 - - 00B
		R/W	R/W	R/W	R/W	—	—	R/W	R/W	

- OCU control status register ch.0 to ch.7 (OCS0 to OCS7)

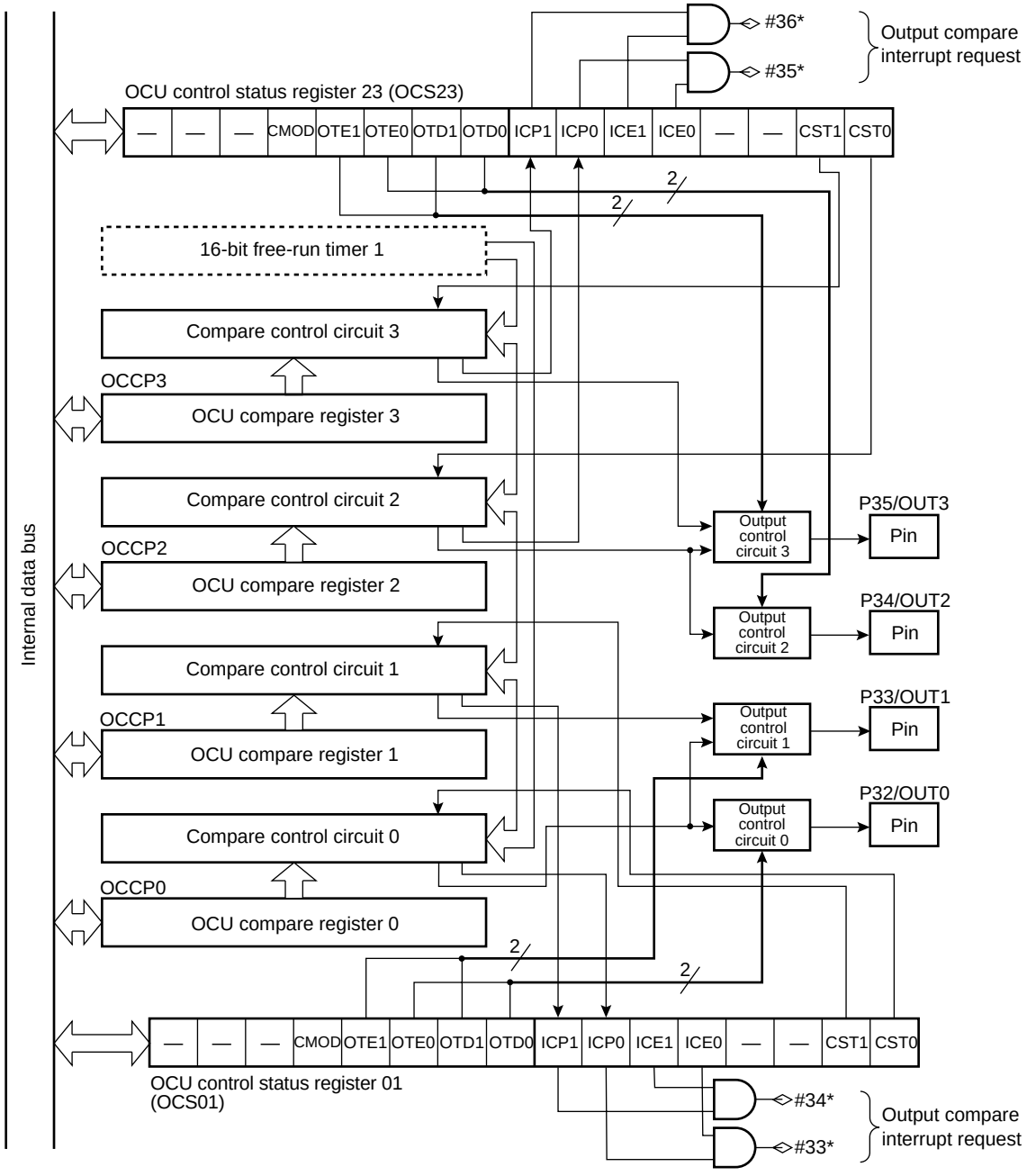
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8		Initial value
ch.0 : OCP0 : 00005BH ch.1 : OCP1 : 00005DH ch.2 : OCP2 : 00005FH ch.3 : OCP3 : 000061H ch.4 : OCP0 : 00000DH ch.5 : OCP1 : 00001DH ch.6 : OCP2 : 000035H ch.7 : OCP3 : 00006DH	C15	C14	C13	C12	C11	C10	C09	C08	(OCP)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ch.0 : OCP0 : 00005AH ch.1 : OCP1 : 00005CH ch.2 : OCP2 : 00005EH ch.3 : OCP3 : 000060H ch.4 : OCP0 : 00000CH ch.5 : OCP1 : 00001CH ch.6 : OCP2 : 000034H ch.7 : OCP3 : 00006CH	(OCP)	C07	C06	C05	C04	C03	C02	C01	C00	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
— : Unused
X : Indeterminate

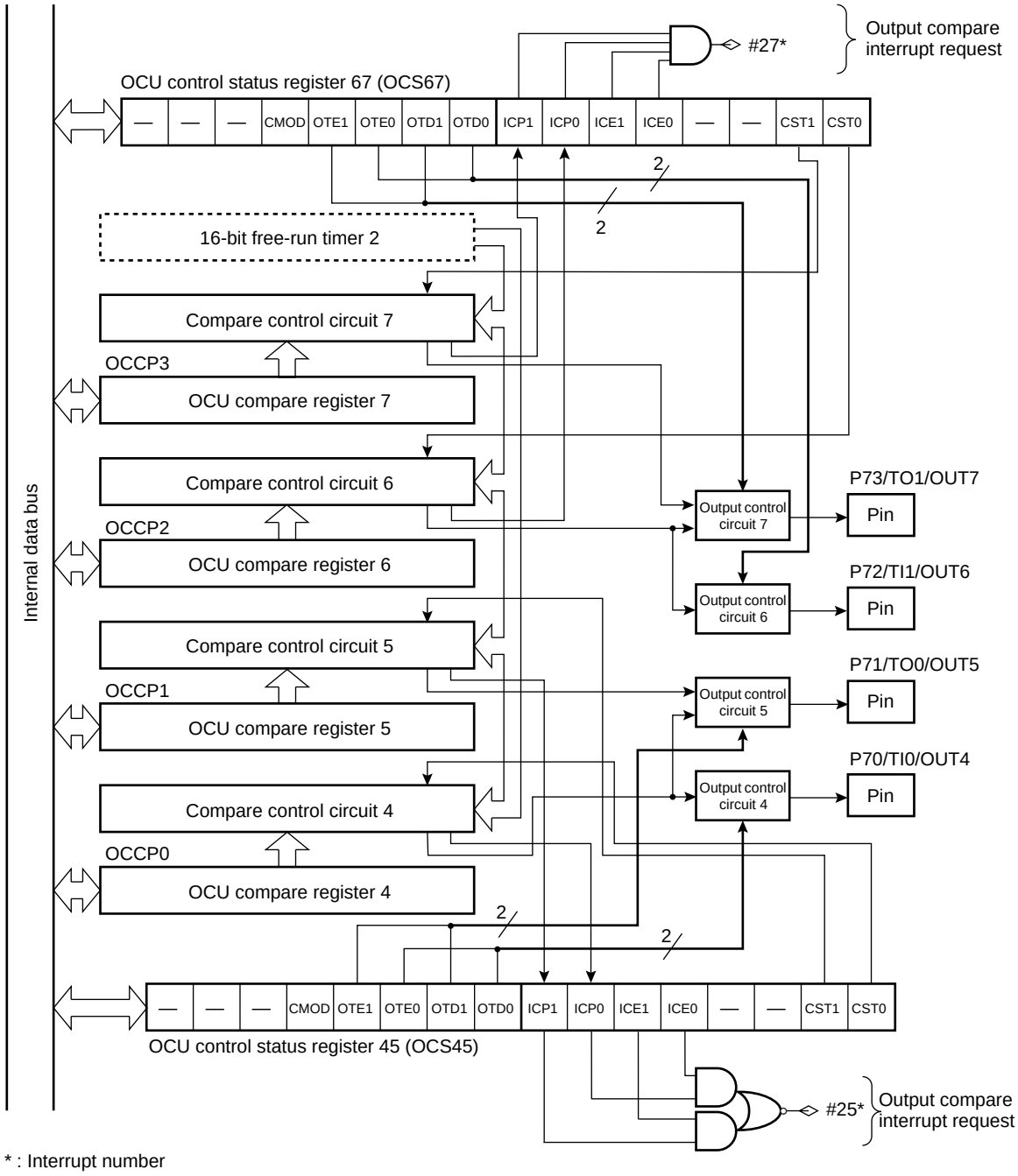
- **Block diagram**

- **Output compare 0 (OCU)**



* : Interrupt number

- **Output compare 1**



* : Interrupt number

7. 8/16-bit Up/Down Counter/Timer 0, 1

The 8/16-bit up/down counter/timer consists of six event input pins, two 8-bit up/down counters, two 8-bit re-load compare registers, and their controllers.

(1) Register Configuration

- Up/down count register 0 (UDCR0)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000080H	(UDCR1)	D07	D06	D05	D04	D03	D02	D01	D00	00000000B
		R	R	R	R	R	R	R	R	

- Up/down count register 1 (UDCR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000081H	D17	D16	D15	D14	D13	D12	D11	D10	(UDCR0)	00000000B
	R	R	R	R	R	R	R	R		

- Re-load compare register 0 (RCR0)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000082H	(RCR1)	D07	D06	D05	D04	D03	D02	D01	D00	00000000B
		W	W	W	W	W	W	W	W	

- Re-load compare register 1 (RCR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000083H	D17	D16	D15	D14	D13	D12	D11	D10	(RCR0)	00000000B
	W	W	W	W	W	W	W	W		

- Counter status register 0, 1 (CSR0, CSR1)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
CSR0 : 000084H CSR1 : 000088H	(Reserved area)	CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R	R	

- Counter control register 0, 1 (CCRL0, CCRL1)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
CSRL0 : 000086H CSRL1 : 00008AH	(CCRH0, CCRH1)	—	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0	-0000000B
		—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Counter control register 0 (CCRH0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000087H	M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0	(CCRL0)	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

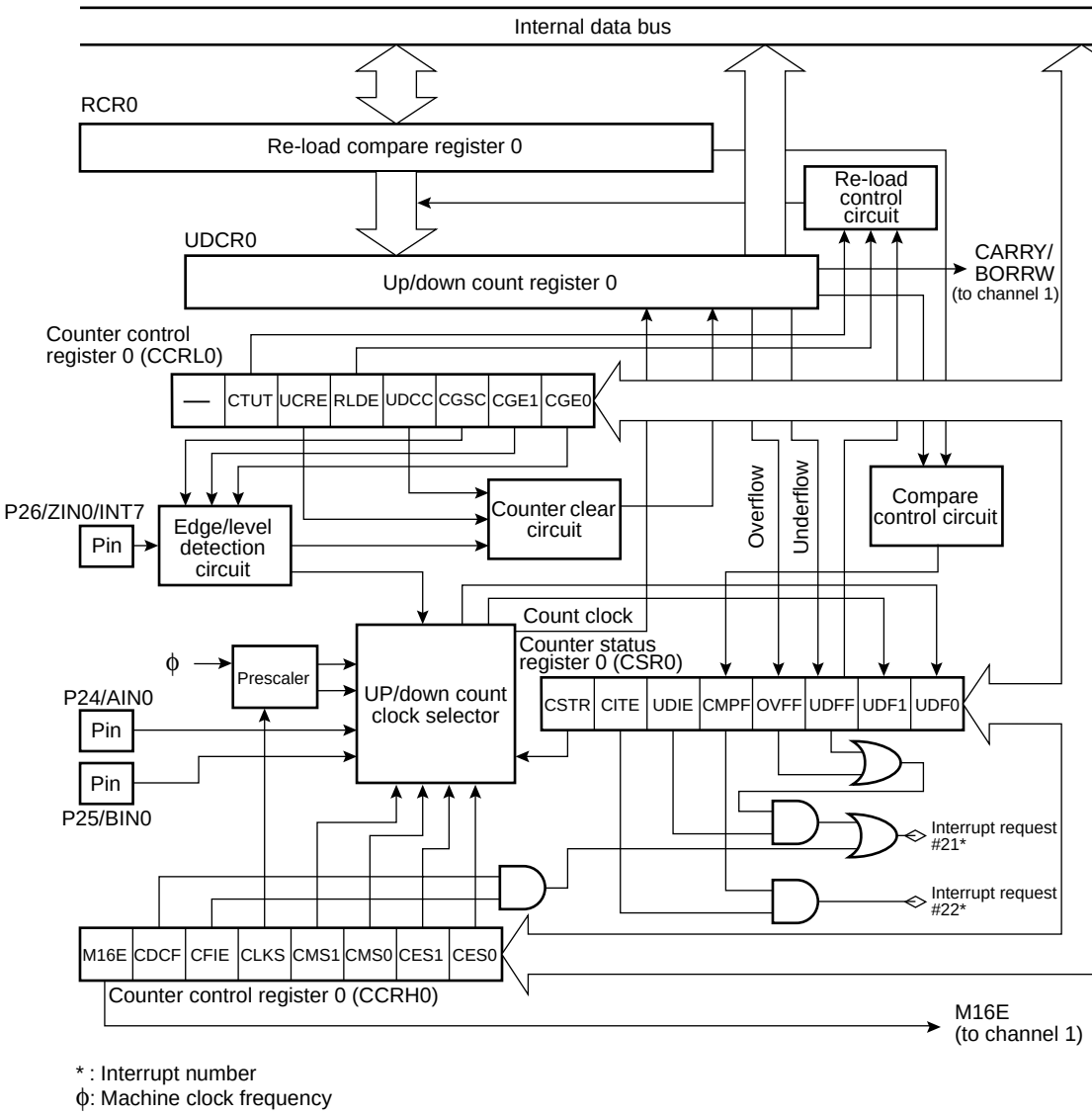
- Counter control register 1 (CCRH1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00008BH	—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0	(CCRL1)	-0000000B
	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

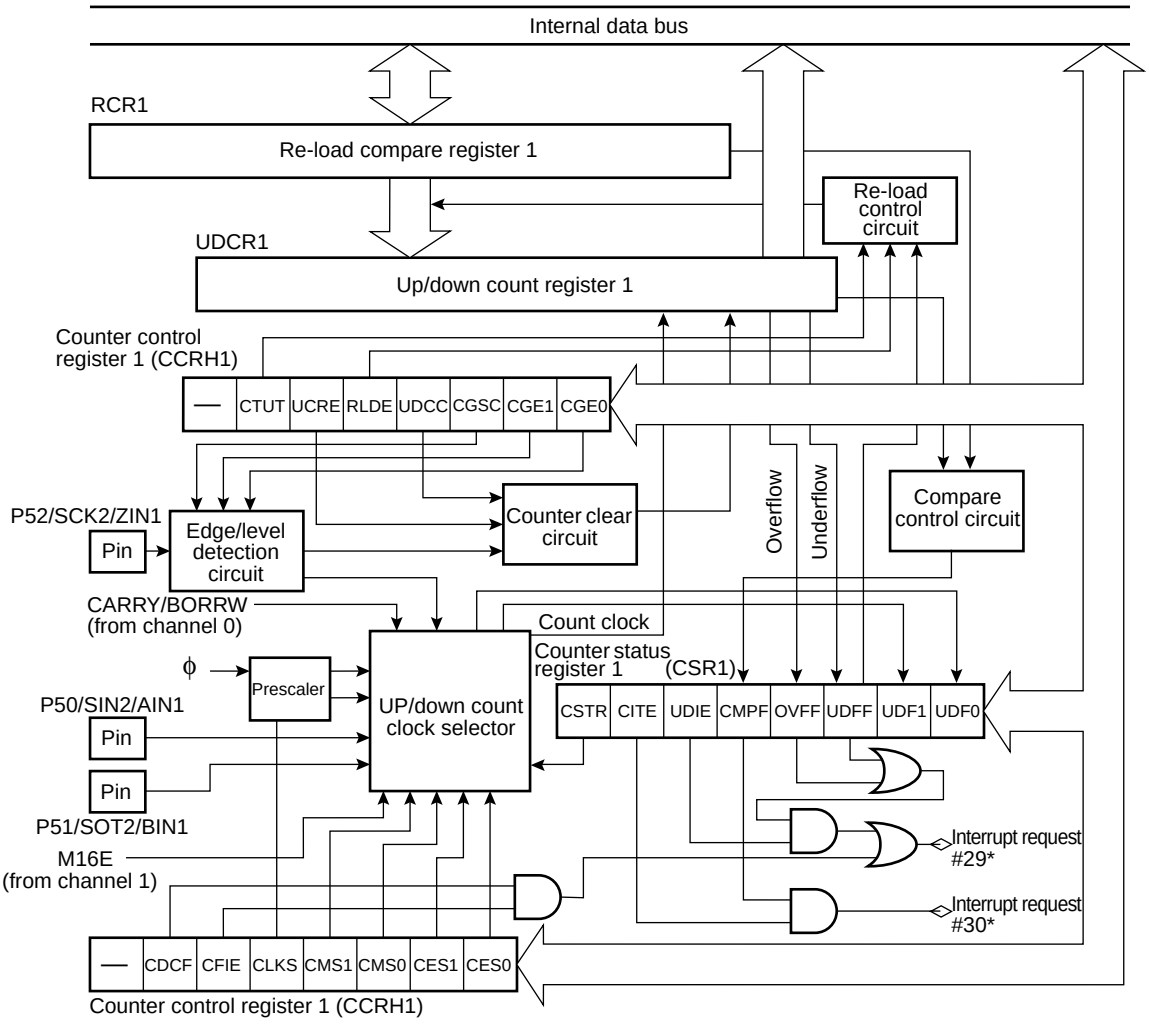
R/W : Readable and writable
R : Read only
W : Write only
— : Unused

(2) Block Diagram

- **Block diagram of 8/16-bit up/down counter/timer 0**



- **Block diagram of 8/16-bit up/down counter/timer 1**



* : Interrupt number
ϕ: Machine clock frequency

8. Extended I/O Serial Interface 0, 1

The extended I/O serial interface transfers data using a clock synchronization system having an 8-bit x 1 channel configuration.

For data transfer, you can select LSB first/MSB first.

(1) Register Configuration

- Serial mode control upper status register 0, 1 (SMCSH0, SMCSH1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
SMCSH0 : 000025H SMCSH1 : 000029H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	(SMCSL)	00000010B
	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W		

- Serial mode control lower status register 0, 1 (SMCSL0, SMCSL1)

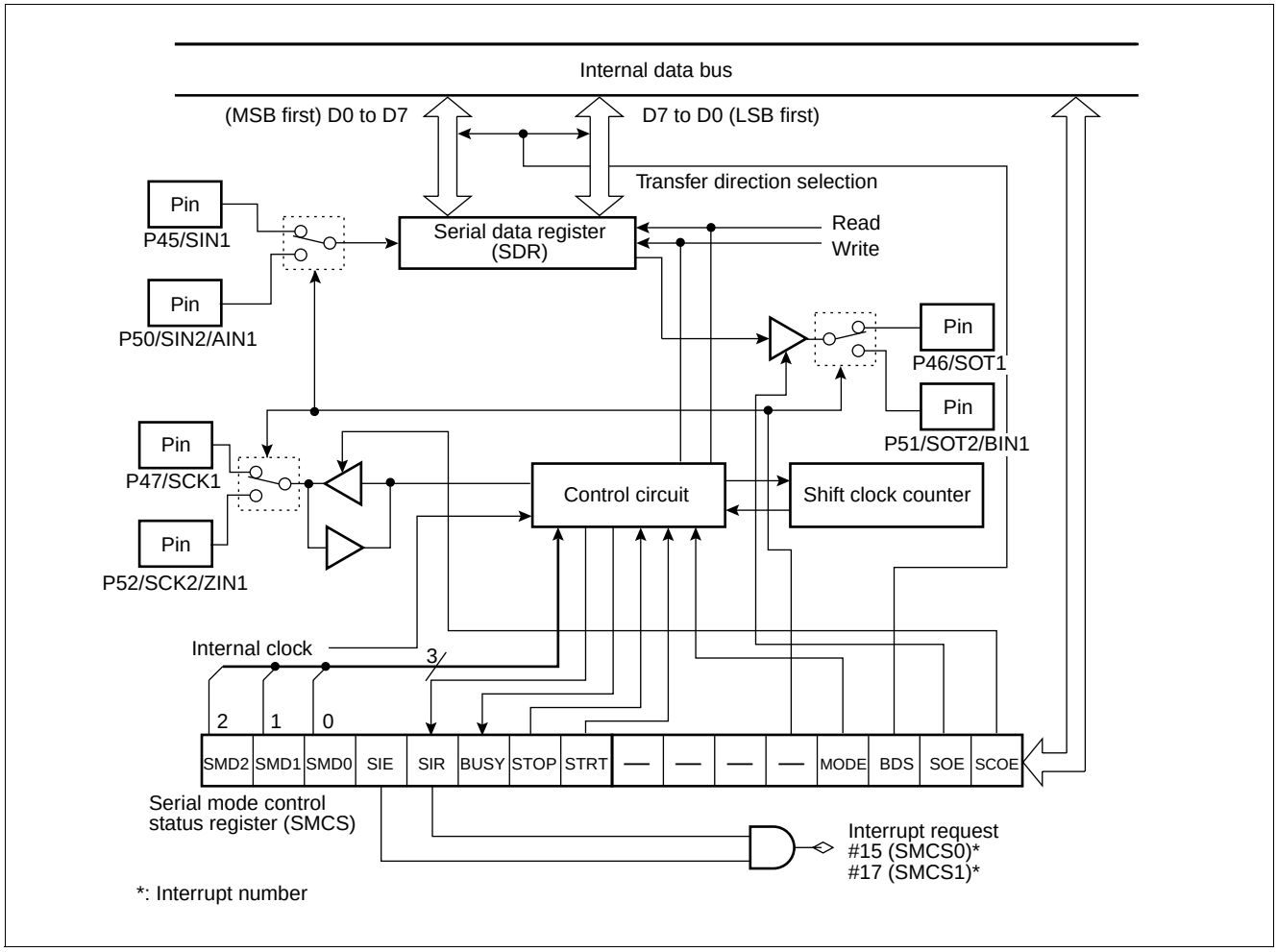
Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
SMCSL0 : 000024H SMCSL1 : 000028H	(SMCSH)	—	—	—	—	MODE	BDS	SOE	SCOE	----0000B
		—	—	—	—	R/W	R/W	R/W	R/W	

- Serial data register 0, 1 (SDR0, SDR1)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
SDR0 : 000026H SDR1 : 00002AH	(CDCR, disabled)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
R : Read only
— : Unused
X : Indeterminate

(2) Block Diagram



9. UART (SCI)

UART (SCI) is general-purpose serial data communication interface for performing synchronous or asynchronous communication (start-stop synchronization system).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (with start and stop bit)
  Clock asynchronized (start-stop synchronization system)
- Baud rate: Embedded dedicated baud rate generator
  External clock input possible
  Internal clock (a clock supplied from 16-bit re-load timer can be used.)
  Asynchronization 9615 bps/31250 bps/4808 bps/2404 bps/1202 bps
  CLK synchronization 1 Mbps/500 kbps/250 kbps/125 kbps/62.5 kbps
  } Internal machine clock For 6 MHz, 8 MHz, 10 MHz, 12 MHz and 16 MHz
- Data length: 7 bit to 9 bit selective (without a parity bit)
  6 bit to 8 bit selective (with a parity bit)
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
  Overrun error
  Parity error (multi-processor mode is supported, enabling setup of any baud rate by an external clock.)
- Interrupt request: Receive interrupt (receive complete, receive error detection)
  Receive interrupt (transmit complete)
  Transmit/receive conforms to extended intelligent I/O service (EI^2OS)

(1) Register Configuration

- Serial control register (SCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000021H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	(SMR)	00000100B
	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W		

- Serial mode register (SMR)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000020H	(SCR)	MD1	MD0	CS2	CS1	CS0	RESV	SCKE	SOE	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Serial status register (SSR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000023H	PE	ORE	FRE	RDRF	TRDE	—	RIE	TIE	(SIDR/SODR)	00001-00B
	R	R	R	R	R	—	R/W	R/W		

- Serial input data register (SIDR)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022H	(SSR)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		R	R	R	R	R	R	R	R	

- Serial output data register (SODR)

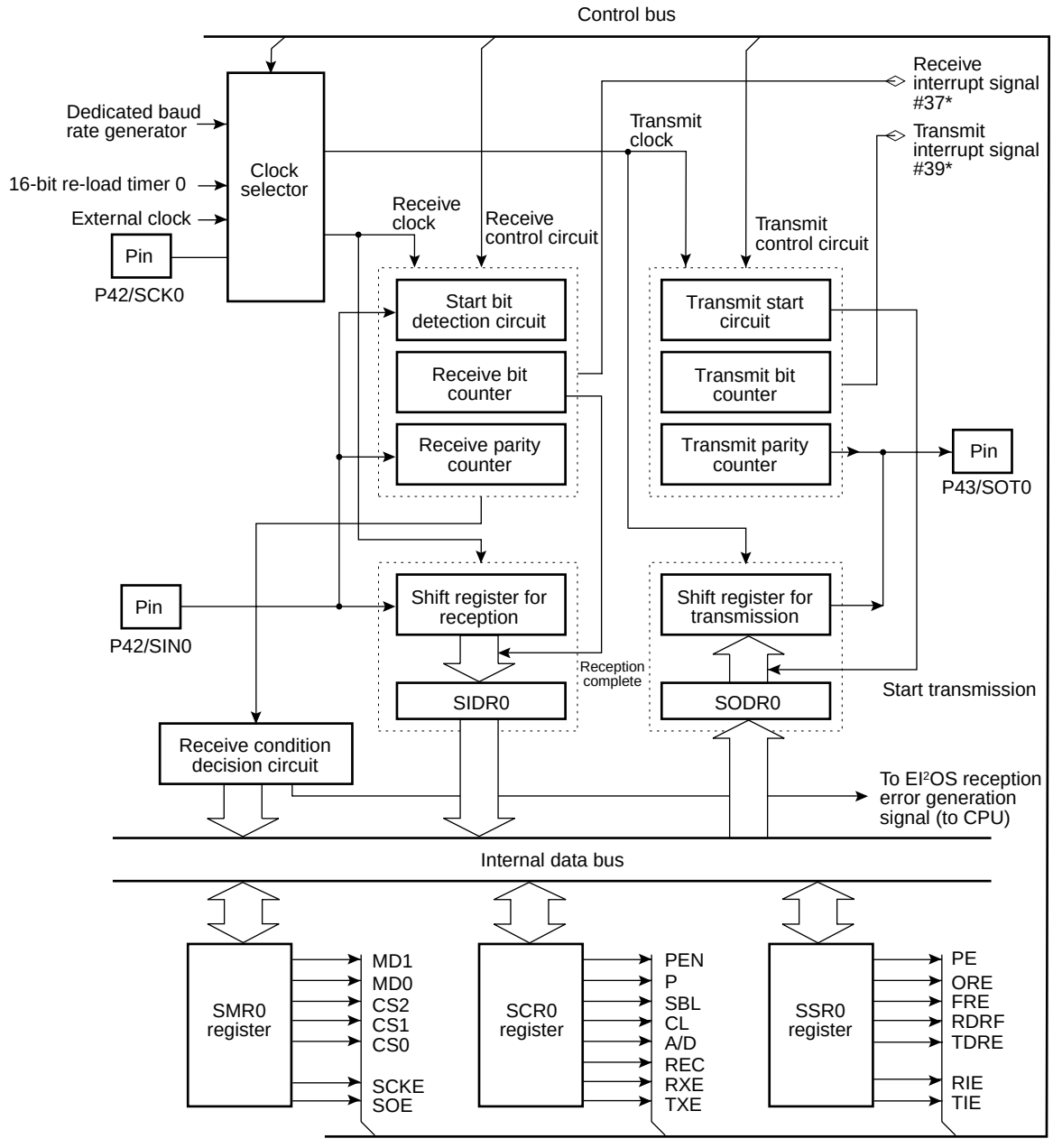
Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022H	(SSR)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		W	W	W	W	W	W	W	W	

- Communications prescaler control register (CDCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000027H	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	(SDR0)	0---1111B
	R/W	—	—	—	R/W	R/W	R/W	R/W		

R/W: Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate
RESV : Reserved bit

(2) Block Diagram



* : Interrupt number

10. DTP/External Interrupt Circuit

DTP (Data Transfer Peripheral), which is located between the peripheral circuit outside the device and the F²MC-16LX CPU, receives an interrupt request or DMA request generated by the external peripheral circuit* for transmission to the F²MC-16LX CPU. DTP is used to activate the intelligent I/O service or interrupt processing. As request levels, two types of “H” and “L” can be selected for the intelligent I/O service. Rising and falling edges as well as “H” and “L” can be selected for an external interrupt request.

* : The external peripheral circuit is connected outside the MB90520 series device.

(1) Register Configuration

- DTP/interrupt factor register (EIRR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000031H	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	(ENIR)	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- DTP/interrupt enable register (ENIR)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000030H	(EIRR)	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

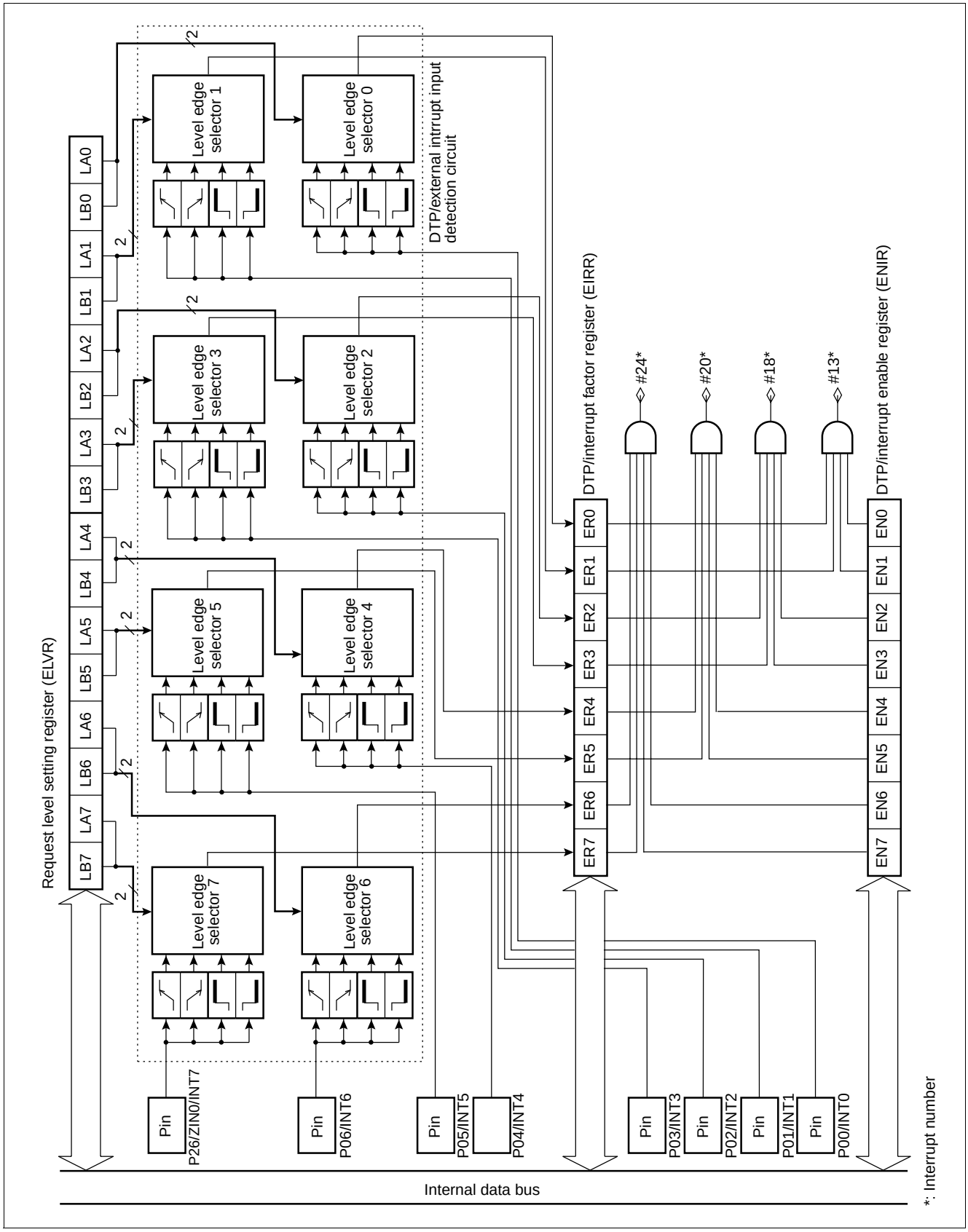
- Request level setting register (ELVR)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
Low order address 000032H	(ELVR upper)	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
High order address 000033H	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	(ELVR lower)	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

R/W: Readable and writable
X : Indeterminate

(2) Block Diagram



11. Wake-up Interrupt

Wake-up intrrupts transmits interrupt request (“L” level) generated by peripheral equipment located between external periphera devices and the F²MC-16LX CPU to the CPU and invokes interrupt processing.

The interrupt does not conform to the exterded intelligent I/O service (EI²OS).

(1) Register Configuration

- Wake-up interrupt flag register (EIFR)

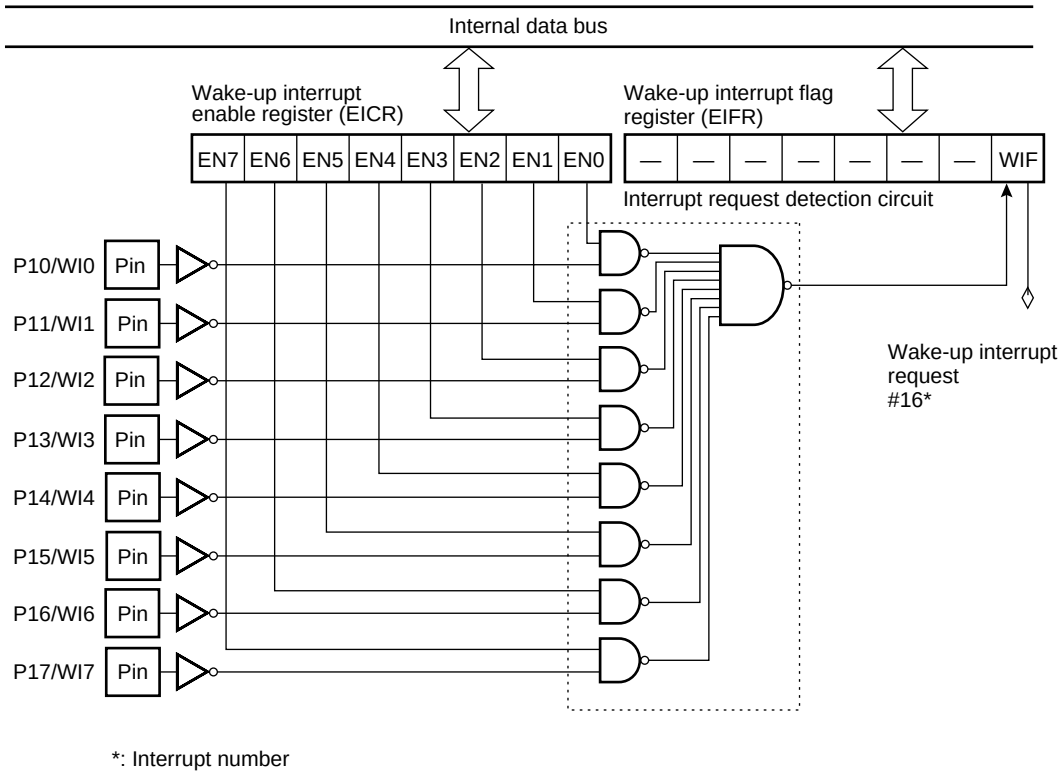
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00000F$_H$	—	—	—	—	—	—	—	WIF	(Disabled)	- - - - - - - 0$_B$
	—	—	—	—	—	—	—	R/W		

- Wake-up interrupt enable register (EICR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00001F$_H$	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	(Disabled)	00000000$_B$
	W	W	W	W	W	W	W	W		

R/W: Readable and writable
W : Write only
— : Unused

(2) Block Diagram



*: Interrupt number

12. Delayed Interrupt Generation Module

The delayed interrupt generation module generates interrupts for switching tasks for development on a real-time operating system (REALOS series). The module can be used to generate softwarewise generates hardware interrupt requests to the CPU and cancel the interrupts.

This module does not conform to the extended intelligent I/O service (EI^{2}OS).

(1) Register Configuration

- Delayed interrupt factor generation/cancellation register (DIRR)

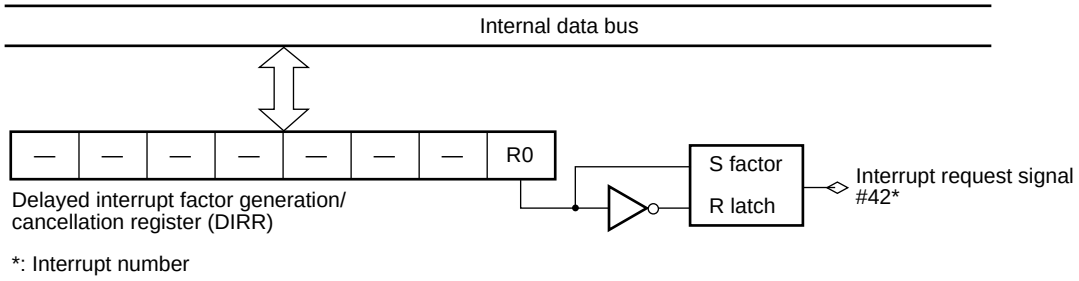
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00009F$_H$	—	—	—	—	—	—	—	R0	(PACSR)	- - - - - - - 0$_B$
	—	—	—	—	—	—	—	R/W		

Note: Upon a reset, an interrupt is canceled.

R/W: Readable and writable
— : Unused

The DIRR is the register used to control delay interrupt request generation/cancellation. Programming this register with “1” generates a delay interrupt request. Programming this register with “0” cancels a delay interrupt request. Upon a reset, an interrupt is canceled. The reserved bit area can be programmed with either “0” or “1”. For future extension, however, it is recommended that bit set and clear instructions be used to access this register.

(2) Block Diagram



13. 8/10-bit A/D Converter

The 8/10-bit A/D converter has a function of converting analog voltage input to the analog input pins (input voltage) to digital values (A/D conversion) and has the following features.

- Minimum conversion time: 16.3 µs (at machine clock of 16 MHz, including sampling time)
- Minimum sampling period: 4 µs/8 µs/16 µs/256 µs (at machine clock of 16 MHz)
- Compare time: 99/176 machine cycles per channel.
  (99 machine cycles are used for a machine clock below 10 MHz.)
- Conversion method: RC successive approximation method with a sample and hold circuit.
- 8/10-bit resolution
- Analog input pins: Selectable from eight channels by software
  Single conversion mode: Selects and converts one channel.
  Scan conversion mode: Converts two or more successive channels. Up to eight channels can be programmed.
  Continuous conversion mode: Repeatedly converts specified channels.
  Stop conversion mode: Stops conversion after completing a conversion for one channel and wait for the next activation (conversion can be started synchronously.)
- Interrupt requests can be generated and the extended intelligent I/O service (EI^{2}OS) can be started after the end of A/D conversion. Furthermore, A/D conversion result data can be transferred to the memory, enabling efficient continuous processing.
- When interrupts are enabled, there is no loss of data even in continuous operations because the conversion data protection function is in effect.
- Starting factors for conversion: Selected from software activation, and external trigger (falling edge).

(1) Register Configuration

- A/D control status register upper digits (ADCS2)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000037H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	RESV	(ADCS1)	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	W	R/W		

- A/D control status register lower digits (ADCS1)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000036H	(ADCS2)	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- A/D data register upper digits (ADCR2)

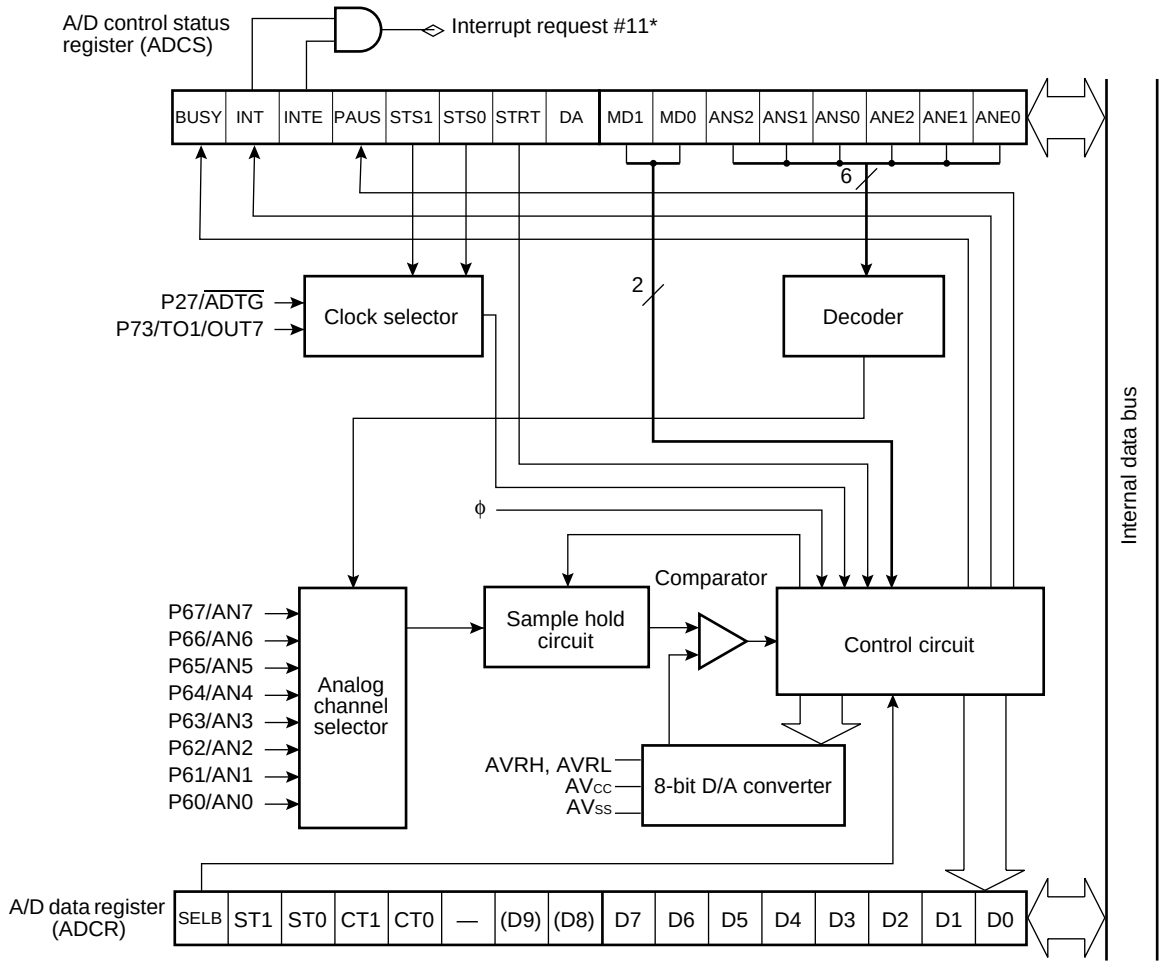
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000039H	RESV	ST1	ST0	CT1	XCT0	—	(D9)	(D8)	(ADCR1)	00001-XXB
	W	W	W	W	W	—	R	R		

- A/D data register lower digits (ADCR1)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000038H	(ADCR2)	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
		R	R	R	R	R	R	R	R	

R/W: Readable and writable
R : Read only
W : Write only
— : Unused
X : Indeterminate
RESV : Reserved bit

(2) Block Diagram



ϕ : Machine clock frequency
TO : 16-bit PPG timer channel 1 output
* : Interrupt number

14. 8-bit D/A Converter

The 8-bit D/A converter, which is based on the R-2R system, supports 8-bit resolution mode. It contains two channels each of which can be controlled in terms of output by the D/A control register.

(1) Register Configuration

- D/A converter data register ch.0 (DADR0)

Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003A$_H$	(DADR1)	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	XXXXXXXX$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- D/A converter data register ch.1 (DADR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
00003B$_H$	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	(DADR0)	XXXXXXXX$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- D/A control register 0 (DACR0)

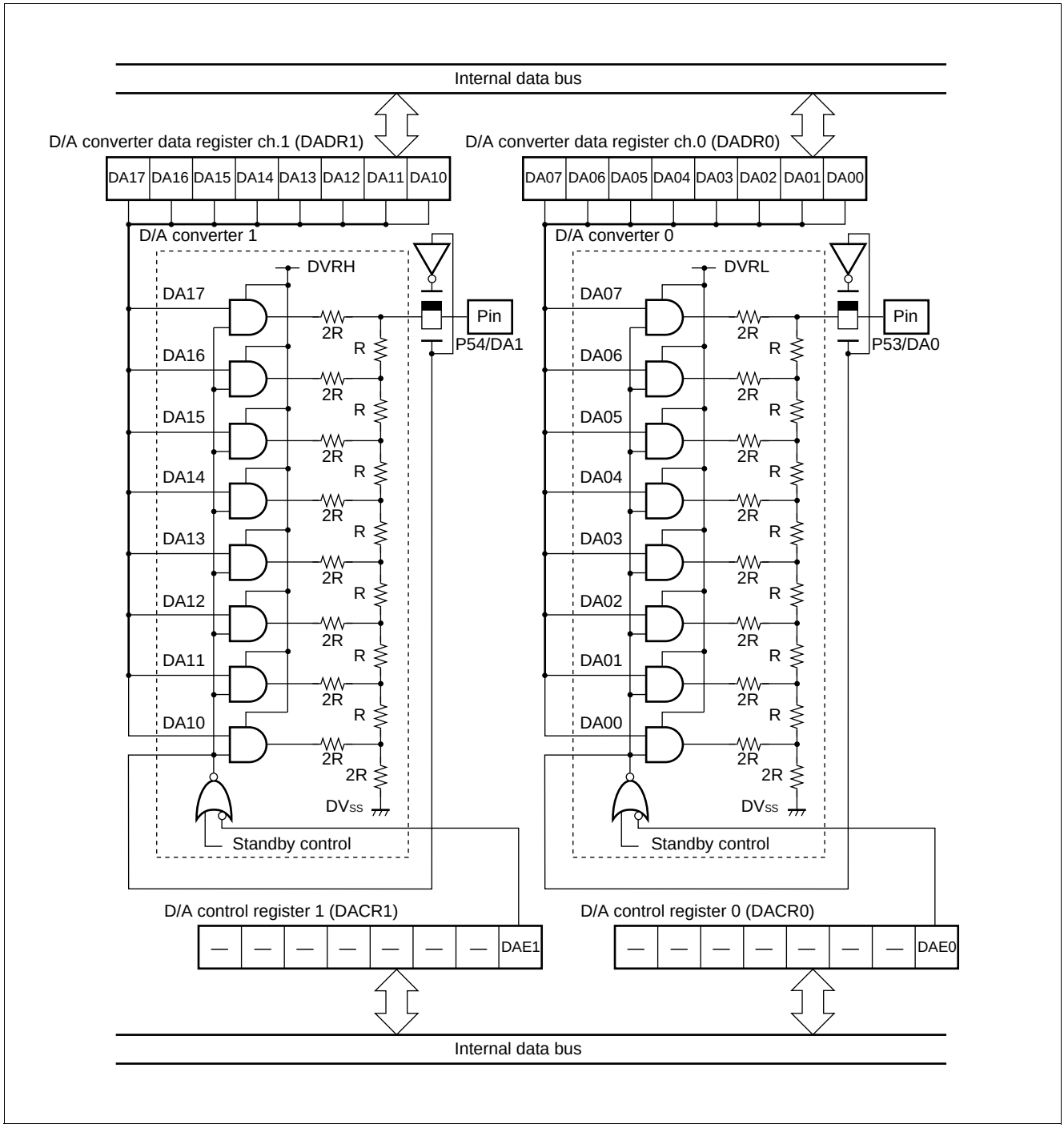
Address	bit 15 ··· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003C$_H$	(DACR1)	—	—	—	—	—	—	—	DAE0	- - - - - - - 0$_B$
		—	—	—	—	—	—	—	R/W	

- D/A control register 1 (DACR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ··· bit 0	Initial value
00003D$_H$	—	—	—	—	—	—	—	DAE1	(DACR0)	- - - - - - - 0$_B$
	—	—	—	—	—	—	—	R/W		

R/W: Readable and writable
— : Unused
X : Indeterminate

- **Block Diagram**



15. Clock Timer

The clock timer control register (WTC) controls operation of the clock timer, and time for an interval interrupt.

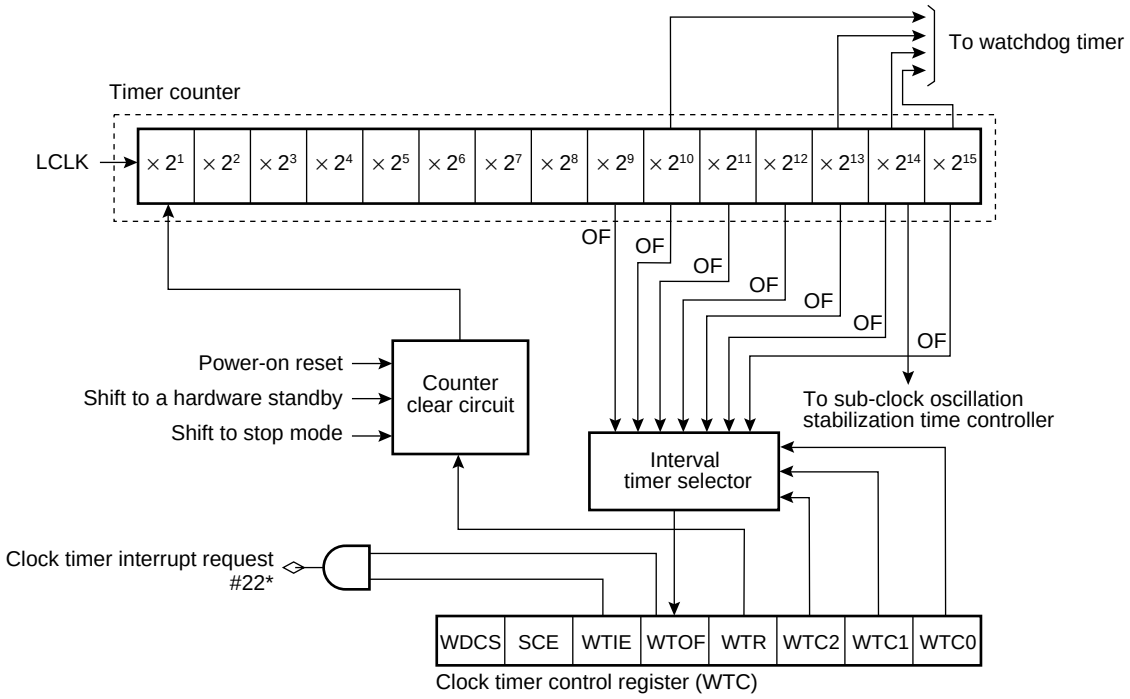
(1) Register Configuration

- Clock timer control register (WTC)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000AA$_H$	(Disabled)	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	1X000000$_B$
		R/W	R	R/W	R/W	R	R/W	R/W	R/W	

R/W: Readable and writable
R : Read only
X : Indeterminate

(2) Block Diagram



* : Interrupt number
OF : Overflow
LCLK : Oscillation sub-clock frequency

16.LCD Controller/Driver

The LCD controller/driver, which contains a 16-byte display data memory, controls LCD indication using four common output pins and 32 segment output pins. It can select three types of duty output, and directly drive the LCD (liquid crystal display) panel.

(1) Register Configuration

- LCDC control register 0 (LCR0)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00006AH	(LCR1)	CSS	LCEN	VSEL	BK	MS1	MS0	FP1	FP0	00010000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- LCDC control register 1 (LCR1)

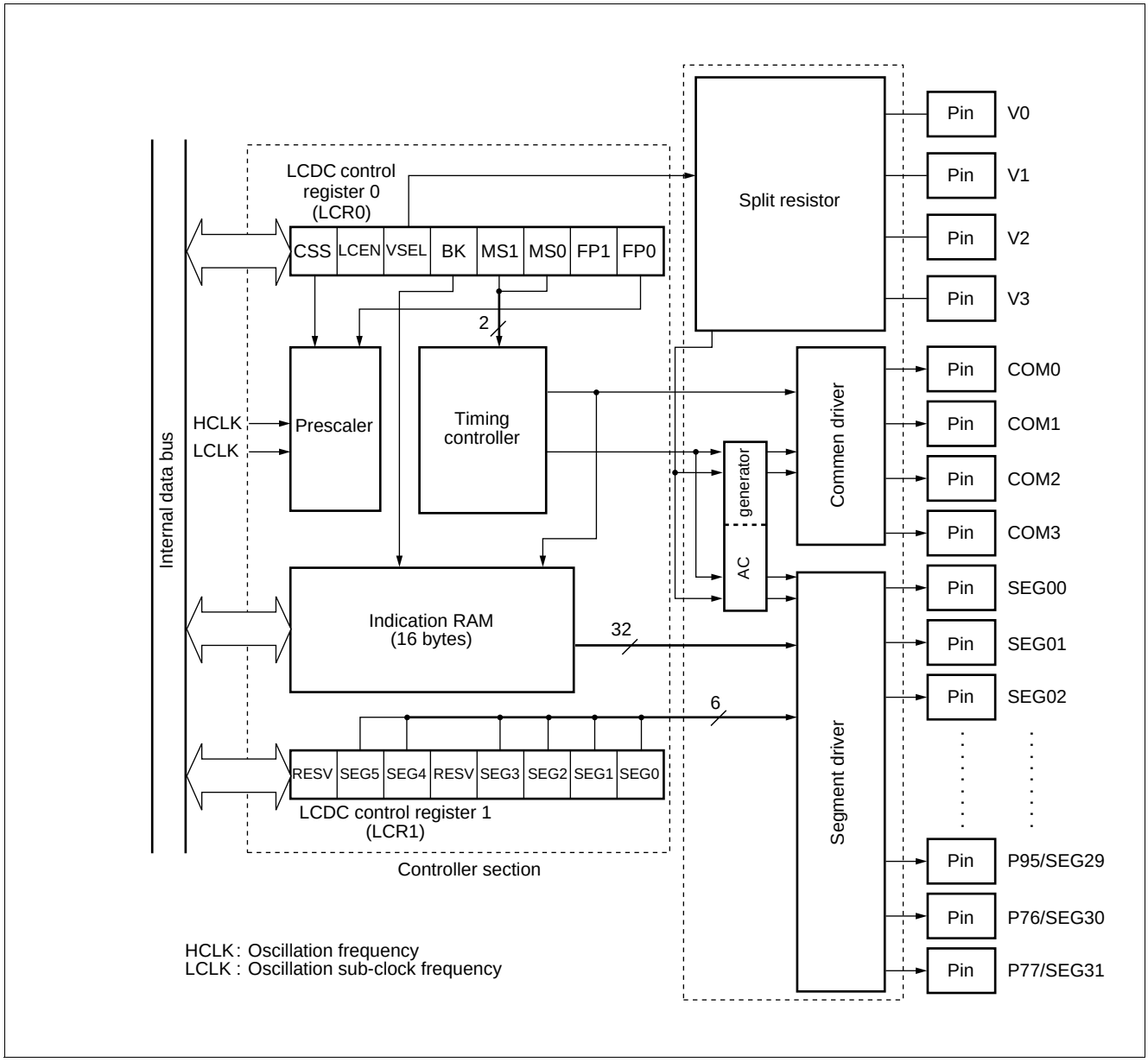
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00006BH	RESV	SEG5	SEG4	RESV	SEG3	SEG2	SEG1	SEG0	(LCR10)	00000000B
					R/W	R/W	R/W	R/W		

- Port 7/COM pin selection register (LCDCMR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00000BH	—	—	—	—	COM3	COM2	COM1	COM0	(PDRA)	----0000B
	—	—	—	—	R/W	R/W	W	R/W		

R/W: Readable and writable
— : Unused
X : Indeterminate
RESV : Reserved bit

(2) Block Diagram



17. Communications Prescaler Register

This register controls machine clock division.

Output from the communications prescaler register is used for UART0 (SCI), UART1 (SCI), and extended I/O serial interface.

The communications prescaler register is so designed that a constant baud rate may be acquired for various machine clocks.

(1) Register Configuration

- Communications prescaler control register (CDCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
000027H	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	(SDR0)	0---1111B
	R/W	—	—	—	R/W	R/W	R/W	R/W		

R/W: Readable and writable
— : Unused

18. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit and flag are prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at “1”, the interrupt flag is set at “1” and the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code. The interrupt flag is cleared to “0” by writing 0 by an instruction.

(1) Register Configuration

- Program address detection register 0 to 2 (PADR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Low order address) : 001FF0H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Middle order address) : 001FF1H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (High order address) : 001FF2H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection register 3 to 5 (PADR1)

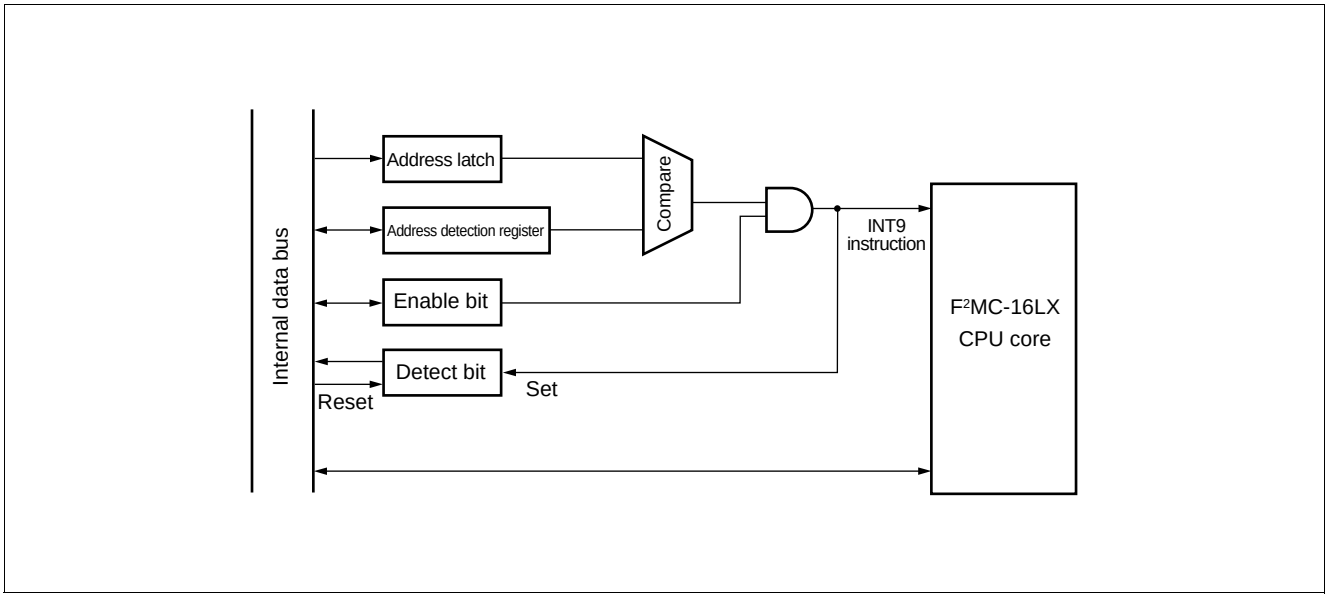
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Low order address) : 001FF3H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Middle order address) : 001FF4H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (High order address) : 001FF5H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection control status register (PACSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00009EH	RESV	RESV	RESV	RESV	AD1E	AD1D	AD0E	AD0D	00000000B
	—	—	—	—	R/W	R/W	R/W	R/W	

R/W: Readable and writable
— : Unused
X : Indeterminate
RESV : Reserved bit

(2) Block Diagram



19. ROM Mirroring Function Selection Module

The ROM mirroring function selection module can select what the FF bank allocated the ROM sees through the 00 bank according to register settings.

(1) Register Configuration

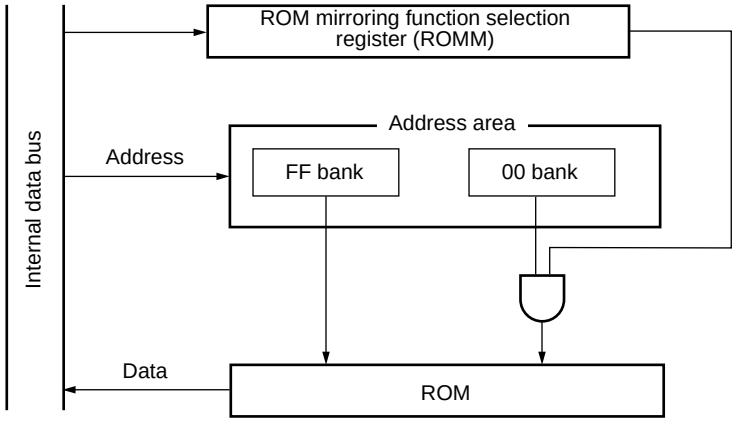
- ROM mirroring function selection register (ROMM)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
00006F$_H$	—	—	—	—	—	—	—	MI	(Disabled)	- - - - - - - 1$_B$
	—	—	—	—	—	—	—	W		

W : Write only
— : Unused

Note: Do not access this register during operation at addresses 004000$_H$ to 00FFFF$_H$.

(2) Block Diagram



20. Low-power Consumption (Stand-by) Mode

The F²MC-16LX has the following CPU operating mode configured by selection of an operating clock and clock operation control.

- **Clock mode**
  PLL clock mode : A mode in which the CPU and peripheral equipment are driven by PLL-multiplied oscillation clock (HCLK).
  Main clock mode: A mode in which the CPU and peripheral equipment are driven by divided-by-2 of the oscillation clock (HCLK).
  The PLL multiplication circuits stops in the mainclock mode.
- **CPU intermittent operation mode**
  The CPU intermittent operation mode is a mode for reducing power consumption by operating the CPU intermittently while external bus and peripheral functions are operated at a high-speed.
- **Hardware stand-by mode**
  The hardware standby mode is a mode for reducing power consumption by stopping clock supply to the CPU by the low-power consumption control circuit, stopping clock supplies to the CPU and peripheral functions (timebase timer mode), and stopping oscillation clock (stop mode, hardware standby mode). Of these modes, modes other than the PLL clock mode are power consumption modes.

(1) Register Configuration

- Clock select register (CKSCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7 ····· bit 0	Initial value
0000A1H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	(LPMCR)	11111100B
	R	R	R/W	R/W	R/W	R/W	R/W	R/W		

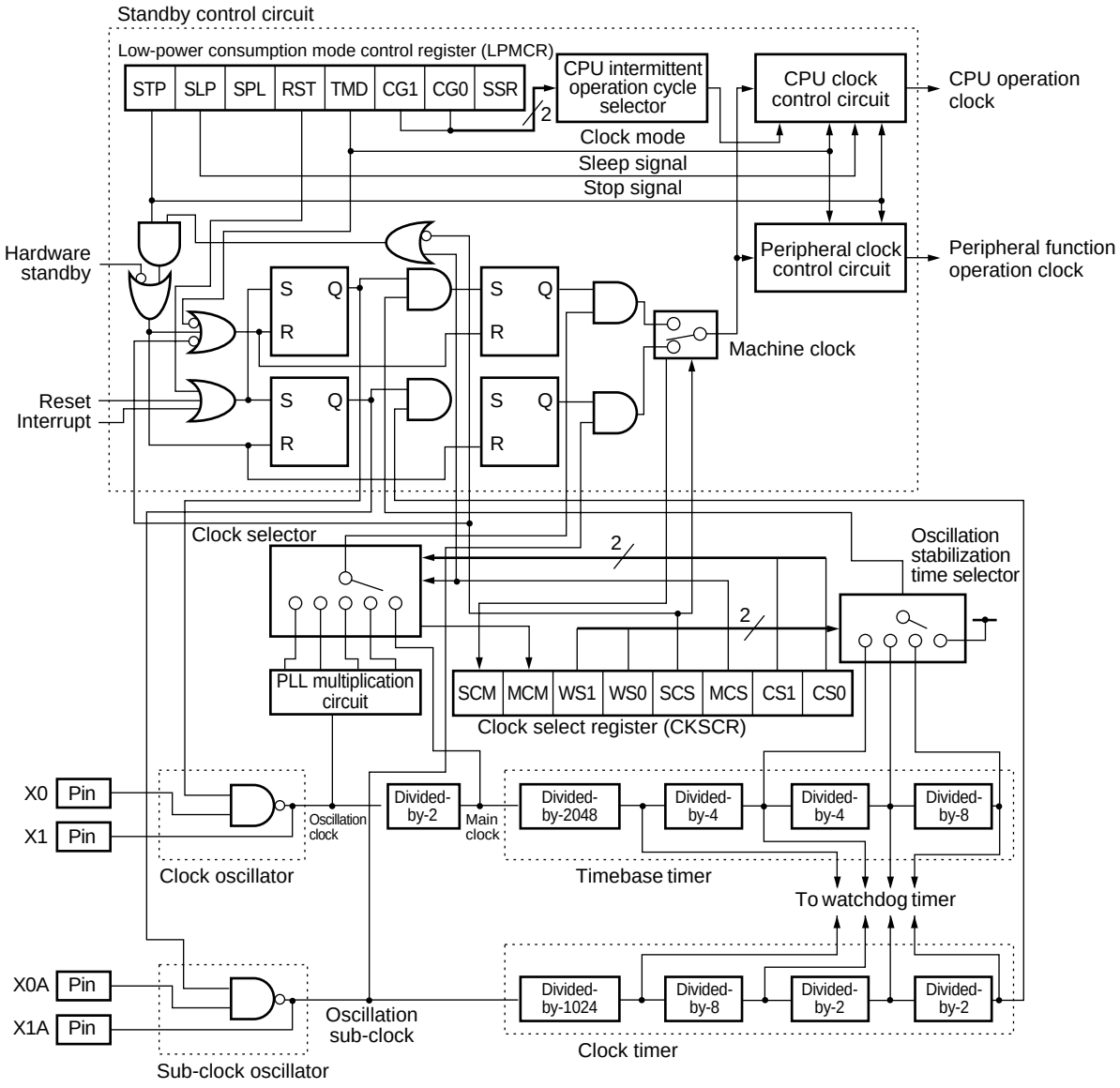
- Low-power consumption mode control register (LPMCR)

Address	bit 15 ····· bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A0H	(CKSCR)	STP	SLP	SPL	RST	TMD	CG1	CG0	SSR	00011000B
		W	W	R/W	W	W	R/W	R/W	R/W	

R/W: Readable and writable
R : Read only
W : Write only

MB90520 Series

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	*1
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	*1
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	*1
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 6.0	V	*2
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	*5
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: AV_{CC}, AVRH, AVRL, and DV_{CC} shall never exceed V_{CC}. AVRL shall never exceed AVRH.
*2: V_I and V_O shall never exceed V_{CC} + 0.3 V.
*3: The maximum output current is a peak value for a corresponding pin.
*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.
*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating currnet × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90523)
	V_{CC}	4.5	5.5	V	Normal operation (MB90F523) Guaranteed frequency = 10 MHz at 4.0 V to 4.5V
	V_{CC}	3.0	5.5	V	Retains status at the time of operation stop
Smoothing capacitor	C_S	0.1	1.0	µF	*
Operating temperature	T_A	–40	+85	°C	

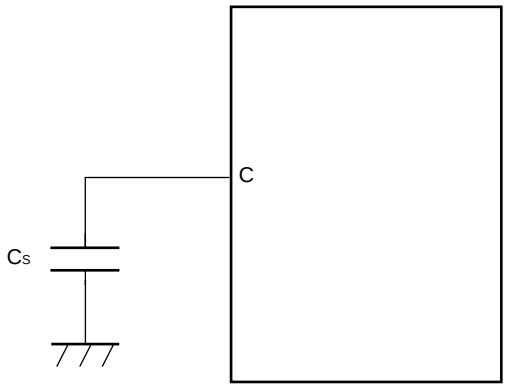
* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

- **C pin diagram**



3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	CMOS input pin	V_{CC} = 3.0 V to 5.5 V (MB90523) V_{CC} = 4.0 V to 5.5 V (MB90F523)	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	CMOS hysteresis input pin		0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHM}	MD pin input		V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	CMOS input pin		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	CMOS hysteresis input pin		V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD pin input		V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH}	Other than P90 and P97	V_{CC} = 4.5 V I_{OH} = –2.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 4.5 V I_{OL} = 2.0 mA	—	—	0.4	V	
Open-drain output leakage current	I_{leak}	Output pin P90 to P97	—	—	0.1	5	µA	
Input leakage current	I_{IL}	Other than P90 and P97	V_{CC} = 5.5 V $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P40 to P47, $\overline{RST}$, MD0, MD1	—	15	30	100	kΩ	
Pull-down resistance	R_{DOWN}	MD0 to MD2	—	15	30	100	kΩ	

(Continued)

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V Normal operation	—	30	40	mA	MB90523
	I_{CC}	V_{CC}		—	85	130	mA	MB90F523
	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V A/D converter operation	—	35	45	mA	MB90523
	I_{CC}	V_{CC}		—	90	140	mA	MB90F523
	I_{CC}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V D/A converter operation	—	40	50	mA	MB90523
	I_{CC}	V_{CC}		—	95	145	mA	MB90F523
	I_{CC}	V_{CC}	When data written in flash mode is erased	—	95	140	mA	MB90F523
	I_{CCS}	V_{CC}	Internal operation at 16 MHz V_{CC} at 5.0 V In sleep mode	—	7	12	mA	MB90523
	I_{CCS}	V_{CC}		—	5	30	mA	MB90F523
	I_{CCL}	V_{CC}	Internal operation at 8 kHz V_{CC} at 5.0 V T_A = +25°C Subsystem operatin	—	0.1	1.0	mA	MB90523
	I_{CCL}	V_{CC}		—	4	7	mA	MB90F523
	I_{CCLS}	V_{CC}	Internal operation at 8 kHz V_{CC} at 5.0 V T_A = +25°C In subsleep mode	—	30	50	mA	MB90523
	I_{CCLS}	V_{CC}		—	0.1	1	mA	MB90F523
	I_{CCT}	V_{CC}	Internal operation at 8 kHz V_{CC} at 5.0 V T_A = +25°C In clock mode	—	15	30	µA	MB90523
	I_{CCT}	V_{CC}		—	30	50	µA	MB90F523
	I_{CCH}	V_{CC}	T_A = +25°C In stop mode	—	5	20	µA	MB90523
	I_{CCH}	V_{CC}		—	0.1	10	µA	MB90F523
	I_{CCH}	V_{CC}	T_A = +25°C (max.) In stop mode	—	—	200	µA	MB90F523
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	—	—	10	80	pF	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
LCD split resistor	R_{LCD}	V0 to V1, V1 to V2, V2 to V3	—	50	100	200	kΩ	
Output impedance for COM0 to COM3	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
Output impedance for SEG00 to SEG31	R_{VSEG}	SEG00 to SEG31		—	—	15	kΩ	
LCDC leak current	I_{LCKC}	V0 to V3, COM1 to COM3, SEG00 to SEG31	—	—	—	±5	µA	

* : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice.The power supply current is measured with an external clock.

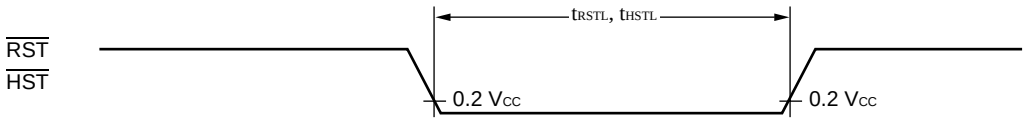
4. AC Characteristics

(1) Reset, Hardware Standby Input Timing

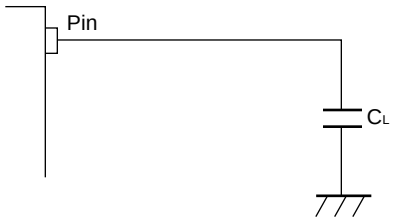
(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	4 t_{CP}*	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$		4 t_{CP}*	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



- **Measurement conditions for AC ratings**



C_L is a load capacitance connected to a pin under test.

Capacitors of C_L = 30 pF must be connected to CLK and ALE pins, while C_L of 80 pF must be connected to address data bus (AD15 to AD00), $\overline{RD}$, and $\overline{WR}$ pins.

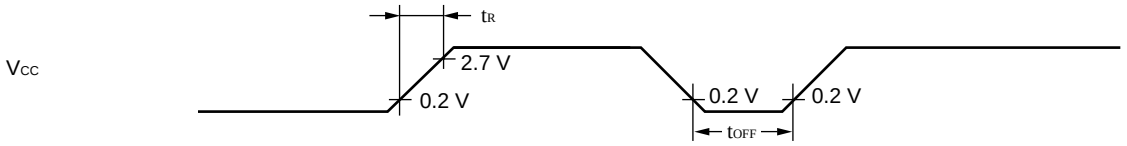
(2) Specification for Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

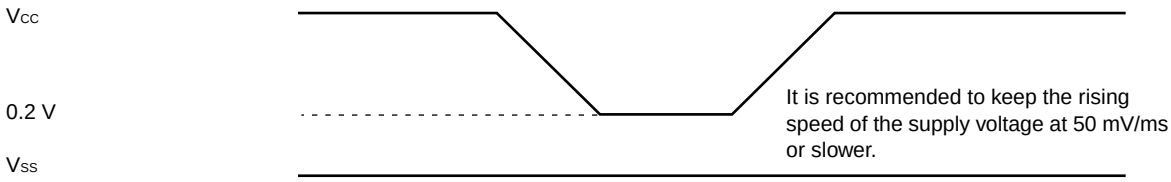
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}		4	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes: • The above ratings are values for causing a power-on reset.
• When $\overline{HST}$ is set to “L”, apply power according to this table to cause a power-on reset irrespective of whether or not a power-on reset is required.
• There are internal registers which can be initialized only by a power-on reset. Apply power according to this rating to ensure initialization of the registers.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 mV or fewer per second, however, you can use the PLL clock.



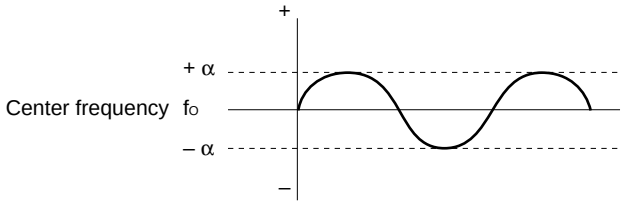
(3) Clock Timings

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	
	F_C	X0, X1	4.0 V to 4.5 V	3	—	10	MHz	MB90F523
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		62.5	—	333	ns	
	t_{HCYL}	X0, X1	4.0 V to 4.5 V	100	—	333	ns	MB90F523
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		10	—	—	ns	Recommened duty ratio of 30% to 70%
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rising/falling time	t_{CR}, t_{CF}	X0, X0A		—	—	5	ns	External clock operation
Internal operating clock frequency	f_{CP}	—		1.5	—	16	MHz	When the main clock is used
	f_{CP}	—	4.0 V to 4.5 V	1.5	—	10	MHz	When the main clock is used
	f_{LCP}	—		—	8.192	—	kHz	Subclock operation
Internal operating clock cycle time	t_{CP}	—		62.5	—	333	ns	When the main clock is used
	t_{CP}	—	4.0 V to 4.5 V	100	—	333	ns	When the main clock is used
	t_{LCP}	—		—	122.1	—	µs	Subclock operation
Frequency fluctuation rate locked	Δf	—		—	—	5	%	*

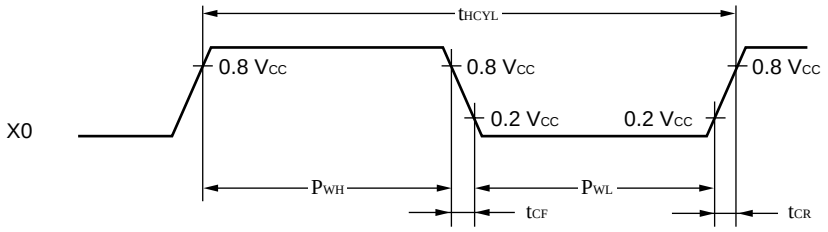
* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{f_O} \times 100\ (\%)$$

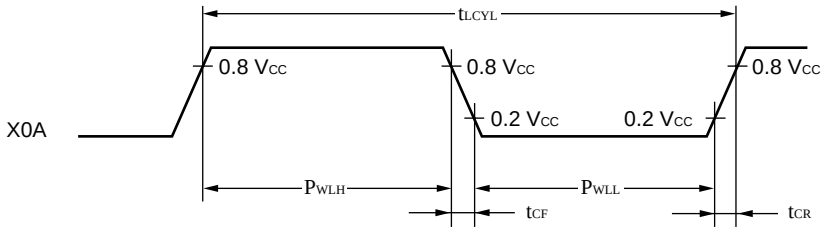


The PLL frequency deviation changes periodically from the preset frequency “(about CLK × (1CYC to 50 CYC)”, thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

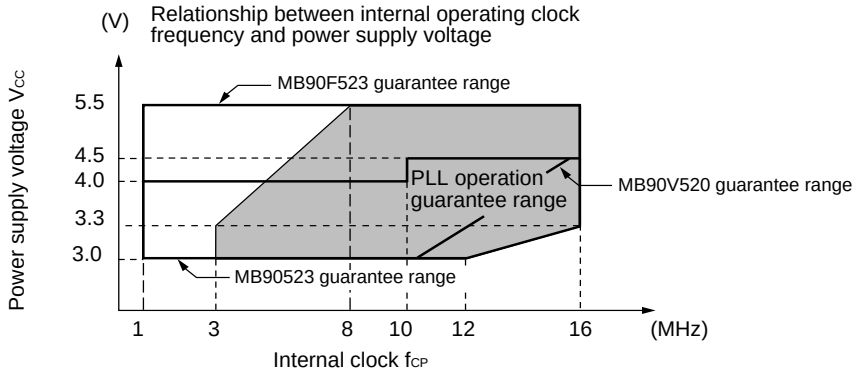
- **X0, X1 clock timing**

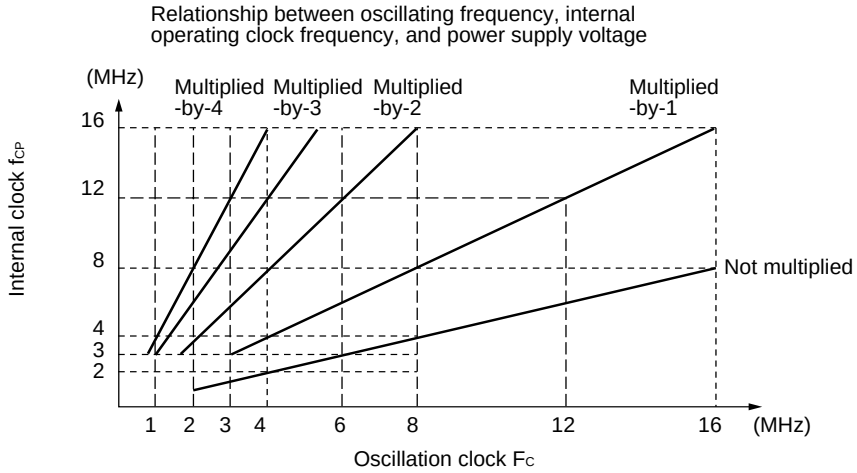


- **X0A, X1A clock timing**



- **PLL operation guarantee range**

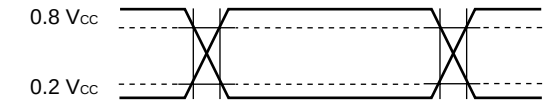




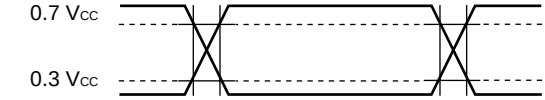
The AC ratings are measured for the following measurement reference voltages.

- **Input signal waveform**

Hystheresis input pin

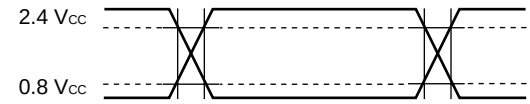


Pins other than hystheresis input/MD input



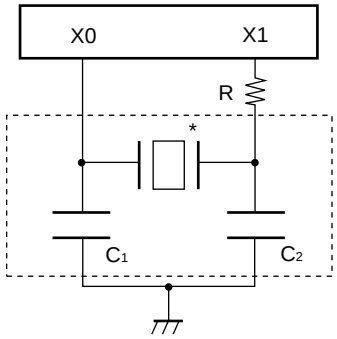
- **Output signal waveform**

Hystheresis input pin



(4) Recommended Resonator Manufactures

- **Sample application of ceramic resonator**



- **Mask ROM product (MB90522, MB90523)**

Resonator manufacturer*	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CSA32.00MXZ040	32.00	5	5	Not required
TDK Corporation	CCR3.52MC3 to CCR6.96MC3	3.52 to 6.96	Built-in	Built-in	Not required
	CCR7.0MC5 to CCR12.0MC5	7.00 to 12.00	Built-in	Built-in	Not required
	CCR20.0MSC6 to CCR32.0MSC6	20.00 to 32.00	Built-in	Built-in	Not required

(Continued)

(Continued)

- **Flash ROM product (MB90F523)**

Resonator manufacturer*	Resonator	Frequency (MHz)	C_1 (pF)	C_2 (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CST32.00MXZ040	32.00	5	5	Not required
TDK Corporation	CCR3.52MC3 to CCR6.96MC3	3.52 to 6.96	Built-in	Built-in	Not required
	CCR7.0MC5 to CCR12.0MC5	7.0 to 12.0	Built-in	Built-in	Not required
	CCR20.0MSC6 to CCR32.0MSC6	20.0 to 32.0	Built-in	Built-in	Not required

Inquiry:Murata Mfg. Co., Ltd..

- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.): TEL 65-758-4233

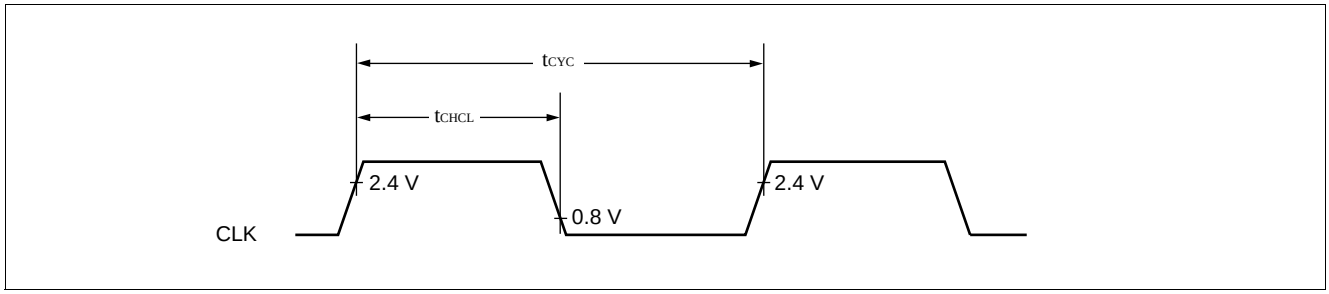
TDK Corporation

- TDK Corporation of America
  Chicago Regional Office: TEL 1-708-803-6100
- TDK Electronics Europe GmbH
  Components Division: TEL 49-2102-9450
- TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- TDK Hongkong Co., Ltd.: TEL 852-736-2238
- Korea Branch, TDK Corporation: TEL 82-2-554-6636

(5) Clock Output Timing

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	V_{CC} = 5.0 V ±10%	62.5	—	ns	
	t_{CYC}	CLK	V_{CC} = 5.0 V ±10% 4.0 V to 4.5 V	100	—	ns	MB90F523
CLK ↑ → CLK ↓	t_{CHCL}	CLK	V_{CC} = 5.0 V ±10%	20	—	ns	
	t_{CHCL}	CLK	V_{CC} = 5.0 V ±10% 4.0 V to 4.5 V	32	—	ns	MB90F523

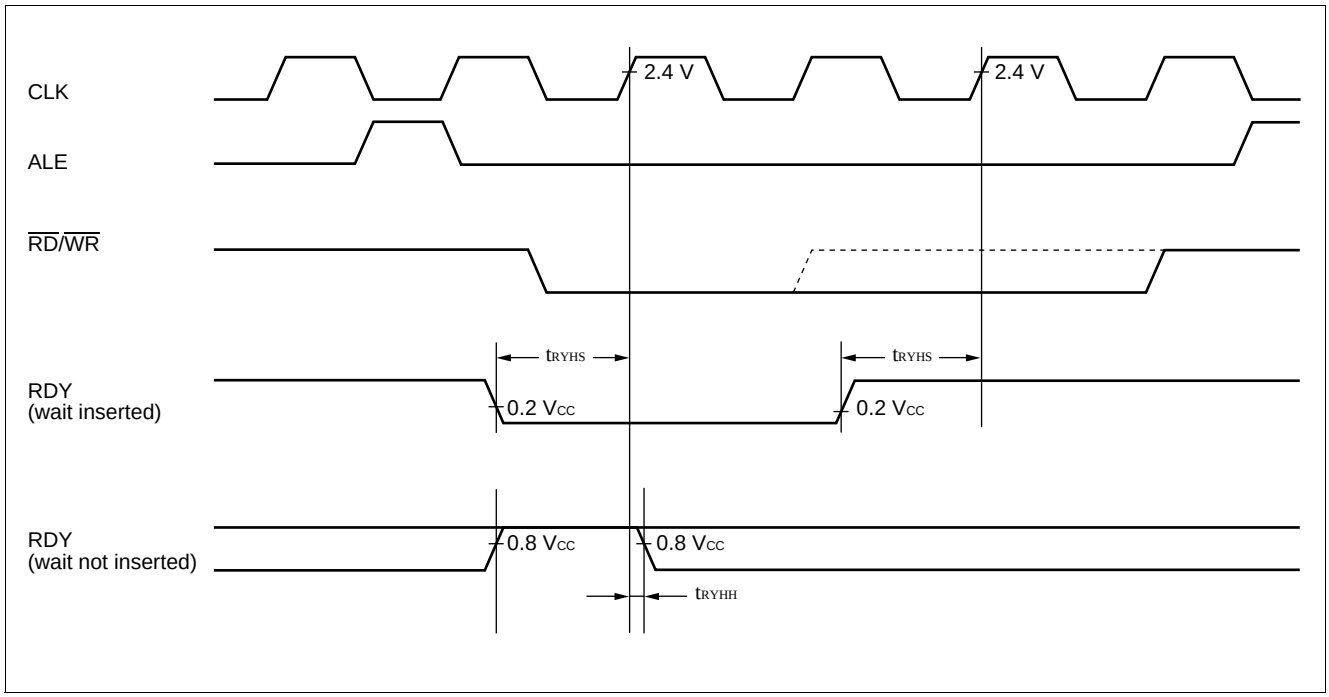


(6) Ready Input Timing

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: Use the automatic ready function when the setup time for the rising edge of the RDY signal is not sufficient.



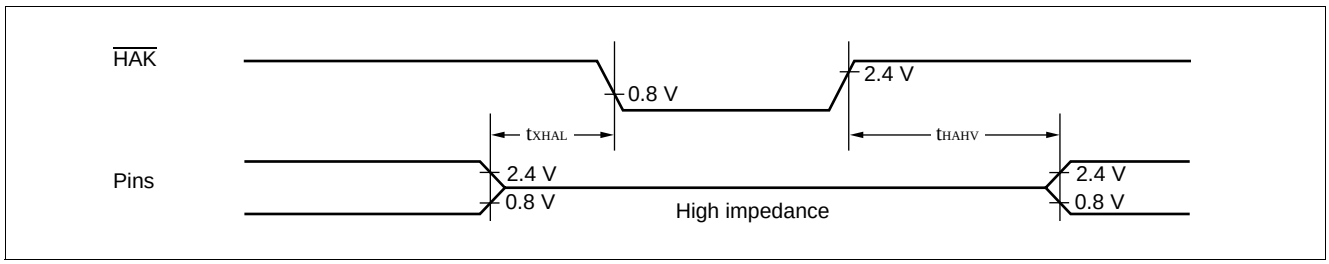
(7) Hold Timing

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pins in floating status → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	1 t_{CP}*	ns	
$\overline{HAK}$ ↑ → pin valid time	t_{HAHV}	$\overline{HAK}$		1 t_{CP}*	2 t_{CP}*	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

Note: More than 1 machine cycle is needed before $\overline{HAK}$ changes after HRQ pin is fetched.



(8) UART (SCI) Timing

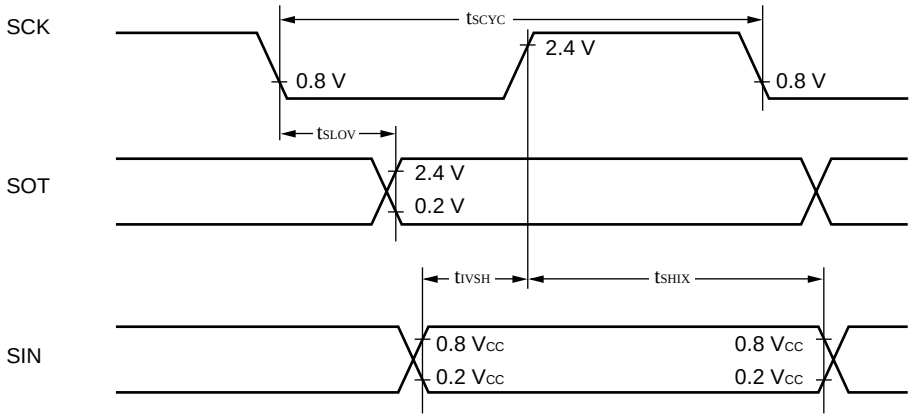
($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal shift clock mode C_L = 80 pF + 1 TTL for an output pin	8 t_{CP}*	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		– 80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK4	External shift clock mode C_L = 80 pF + 1 TTL for an output pin	4 t_{CP}*	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK4		4 t_{CP}*	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	

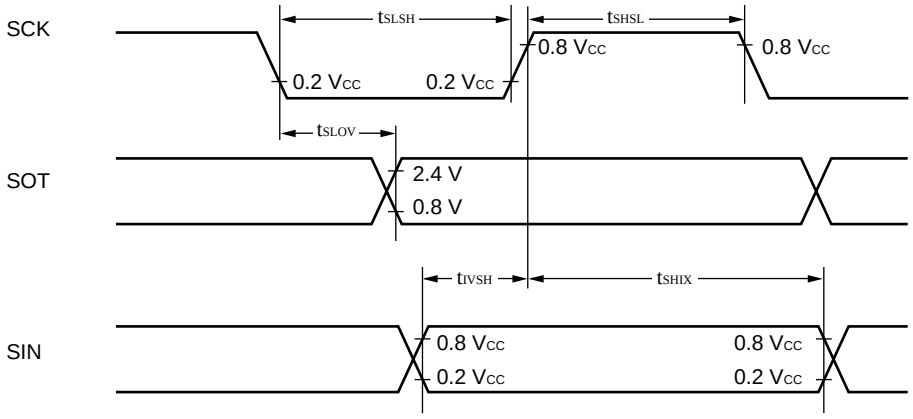
* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

Notes: • These are AC ratings in the CLK synchronous mode.
• C_L is the load capacitor value connected to pins while testing.

- **Internal shift clock mode**



- **External shift clock mode**

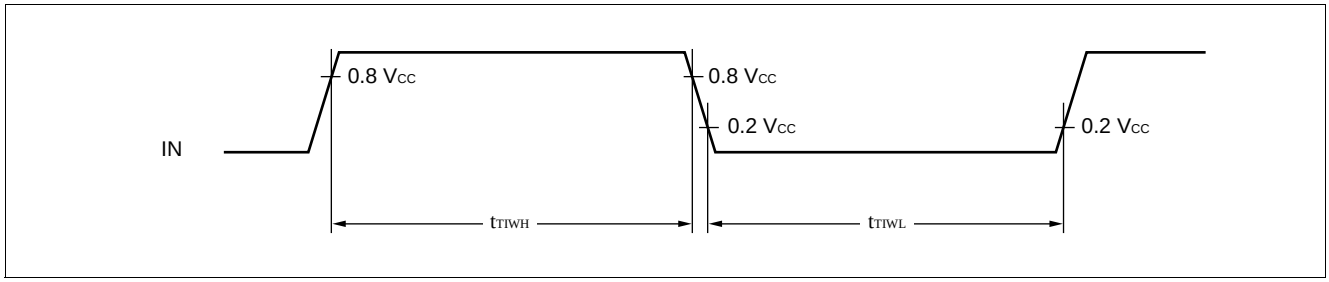


(9) Timer Input Timing

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}, t_{TIWL}	IN0, IN1	—	4 t_{CP}*	—	ns	

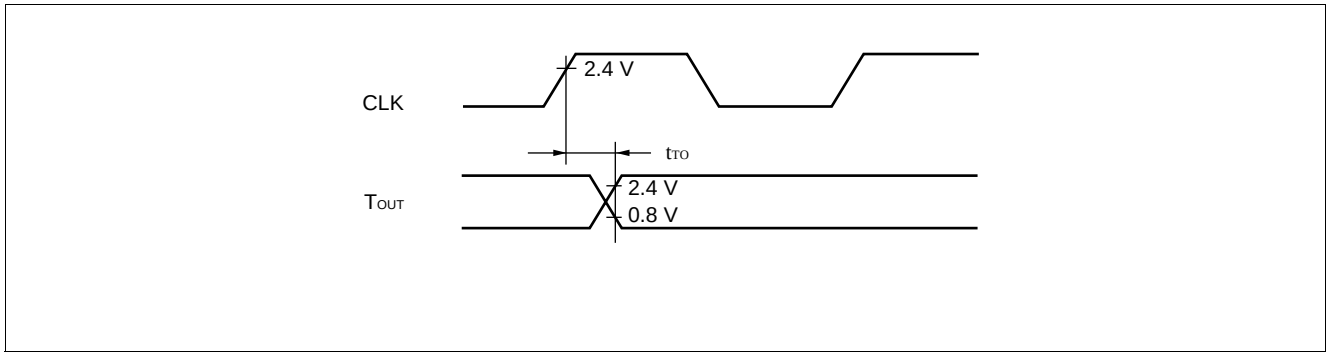
* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



(10) Timer Output Timing

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} transition time	t_{TO}	OUT0 to OUT3, PPG0, PPG1	—	30	—	ns	



5. A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, 3.0 V ≦ AVRH – AVRL, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution	—	—	—	—	8/10	—	bit
Total error	—	—		—	—	±5.0	LSB
Non-linear error	—	—		—	—	±2.5	LSB
Differential linearity error	—	—		—	—	±1.9	LSB
Zero transition voltage	V_{OT}	AN0 to AN7		AV_{SS} –3.5 LSB	+0.5 LSB	AV_{SS} +4.5 LSB	mV
Full-scale transition voltage	V_{FST}	AN0 to AN7		AVRH –6.5LSB	AVRH –1.5 LSB	AVRH +1.5 LSB	mV
Conversion time	—	—	V_{CC} = 5.0 V ±10% at machine clock of 16 MHz	176 t_{CP}*	—	—	ns
Sampling period	—	—	V_{CC} = 5.0 V ±10% at machine clock of 16 MHz	—	64 t_{CP}*	—	ns
Analog port input current	I_{AIN}	AN0 to AN7	—	—	—	10	µA
Analog input voltage	V_{AIN}	AN0 to AN7		AVRL	—	AVRH	V
Reference voltage	—	AVRH		AVRL + 2.7	—	AV_{CC}	V
	—	AVRL		0	—	AVRH –2.7	V
Power supply current	I_A	AV_{CC}		—	5	—	mA
	I_{AH}	AV_{CC}	Supply current when CPU stopped and 8/10-bit A/D converter not in operation (V_{CC} = AV_{CC} = AVRH = 5.0 V)	—	—	5	µA
Reference voltage supply current	I_R	AVRH	—	—	400	—	µA
	I_{RH}	AVRH	Supply current when CPU stopped and 8/10-bit A/D converter not in operation (V_{CC} = AV_{CC} = AVRH = 5.0 V)	—	—	5	µA
Offset between channels	—	AN0 to AN7	—	—	—	4	LSB

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”

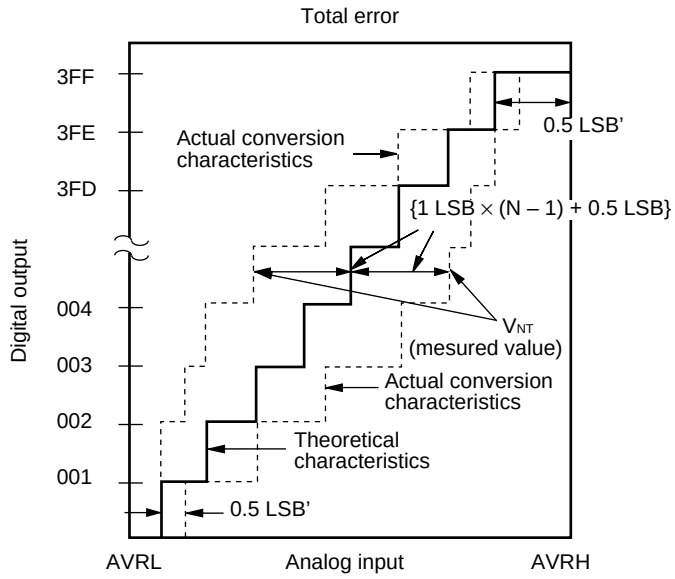
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB’ = (Theoretical value) $\frac{\text{AVRH} - \text{AVRL}}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB'}}$ [LSB]

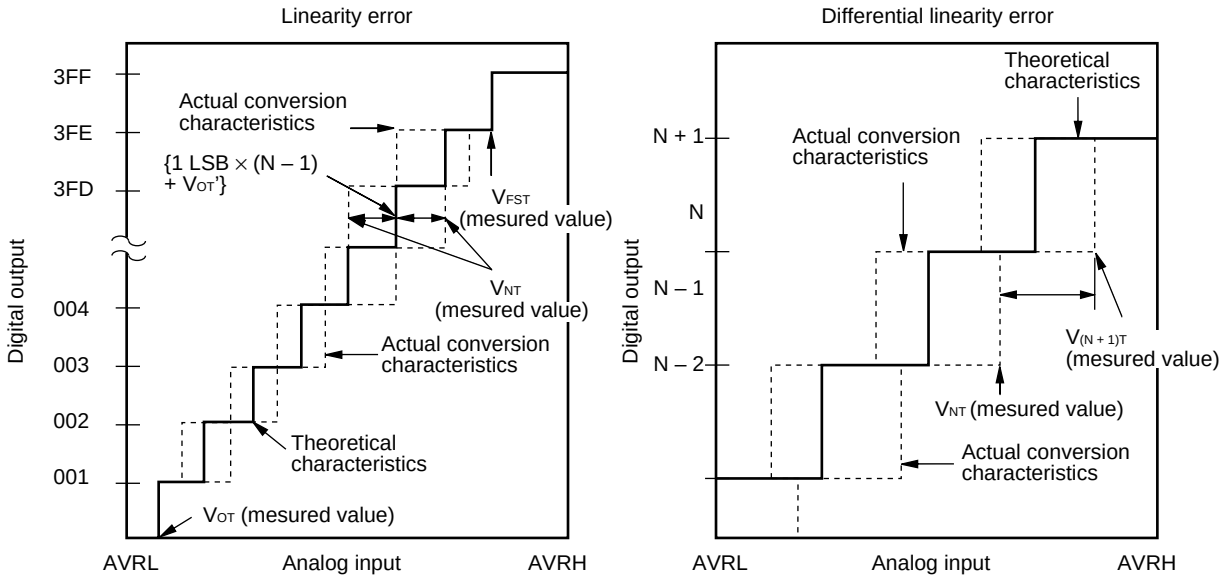
V_{OT}’ (Theoretical value) = AVRL + 0.5 LSB’ [V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST}’ (Theoretical value) = AVRH – 1.5 LSB’ [V]

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB'}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

7. Notes on Using A/D Converter

The impedance value of about 5 kΩ or lower for the external circuit of analog input are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @machine clock of 16 MHz).

- **Block diagram of analog input circuit model**

MB90523
R_{ON}: Approx. 1.5 kΩ
C: Approx. 3.0 pF
MB90F523
R_{ON}: Approx. 3.0 kΩ
C: Approx. 65 pF

Note: Listed values must be considered as standards.

- **Error**

The smaller the | AVRH – AVRL |, the greater the error would become relatively.

8. D/A Converter Electrical Characteristics

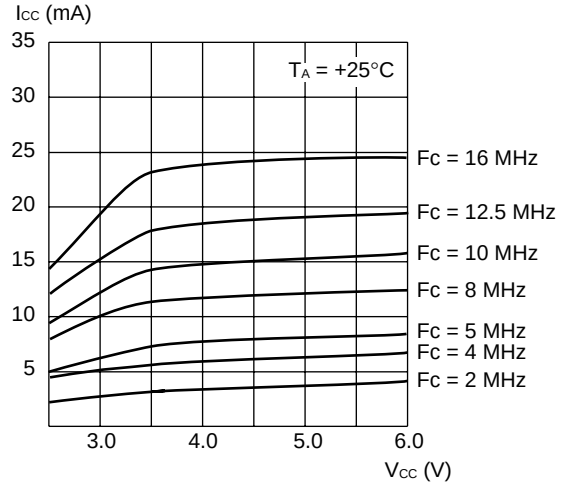
(AV_{CC} = V_{CC} = DV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = DV_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	8	—	bit	
Differential linearity error	—	—	—	—	±0.9	LSB	
Absolute accuracy	—	—	—	—	±1.2	%	
Linearity error	—	—	—	—	±1.5	LSB	
Conversion time	—	—	—	10	20	µs	Load capacitance: 20 pF
Analog reference voltage	—	DV_{CC}	V_{SS} + 3.0	—	AV_{CC}	V	
Reference voltage supply current	I_{DVR}	DV_{CC}	—	—	300	µA	
	I_{DVRS}	DV_{CC}	—	—	10	µA	In sleep mode
Analog output impedance	—	—	—	20	—	kΩ	

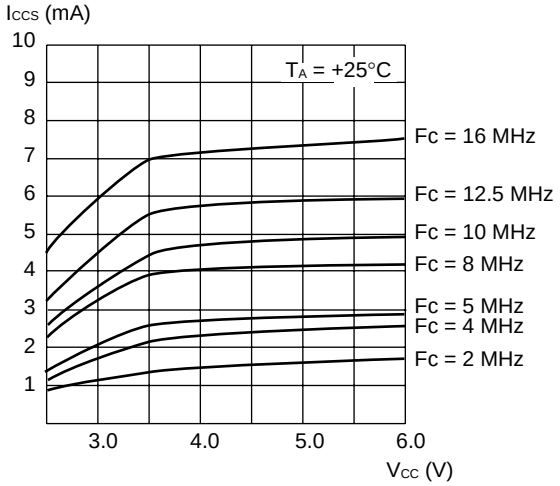
■ EXAMPLE CHARACTERISTICS

(1) Power Supply Current (MB90523)

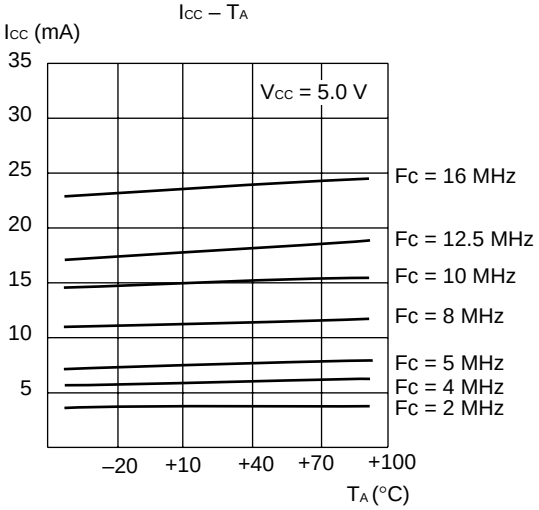
I_{CC} – V_{CC}



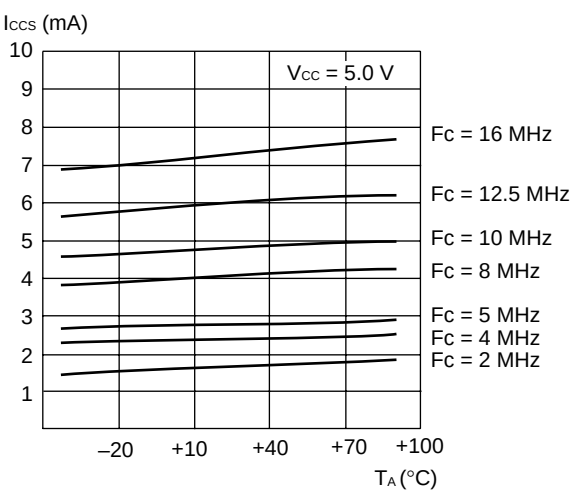
I_{CCS} – V_{CC}



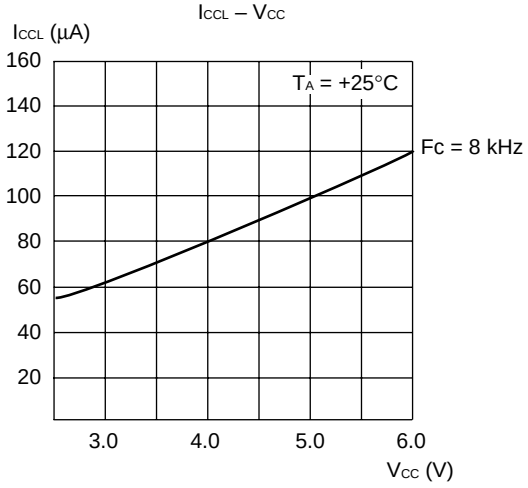
I_{CC} – T_A



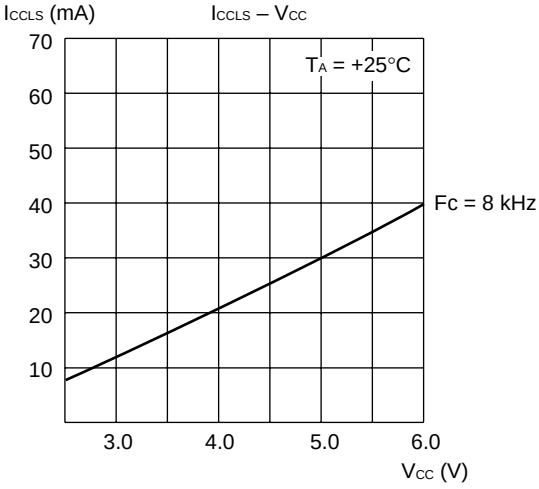
I_{CCS} – T_A



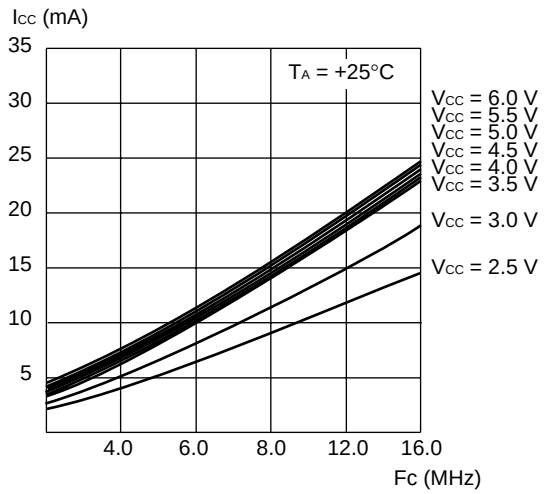
I_{CCL} – V_{CC}



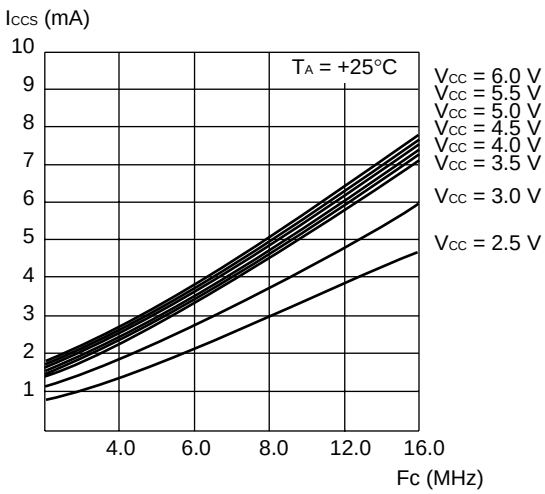
I_{CCLS} – V_{CC}



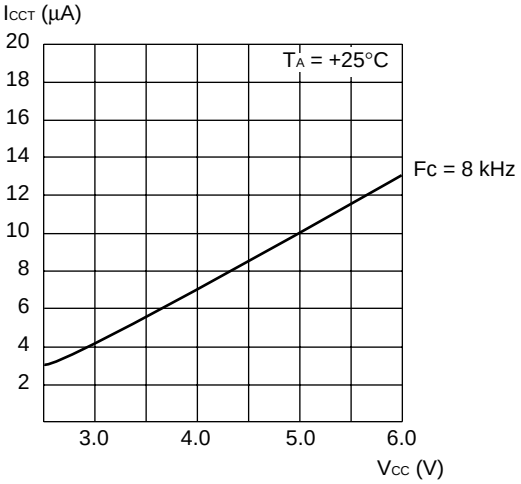
I_{CC} – Fc



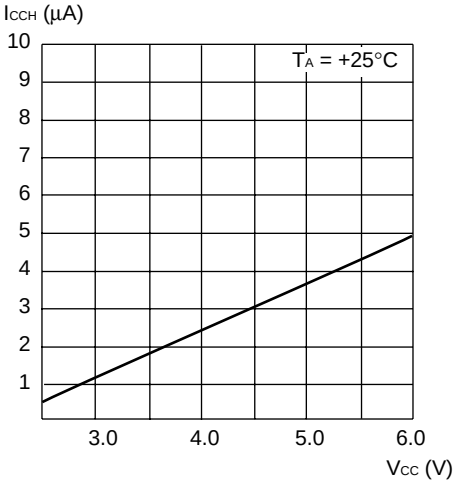
I_{CCS} – Fc



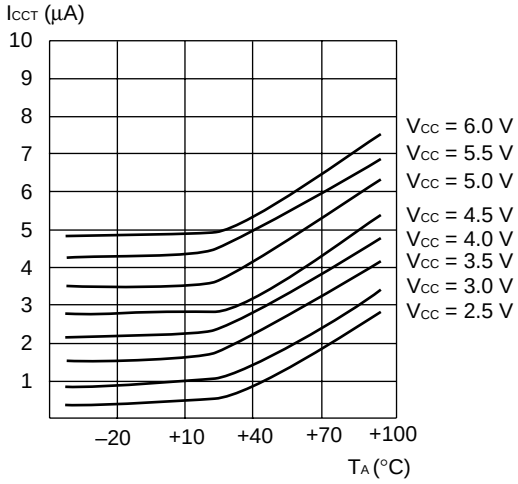
I_{CCT} – V_{CC}



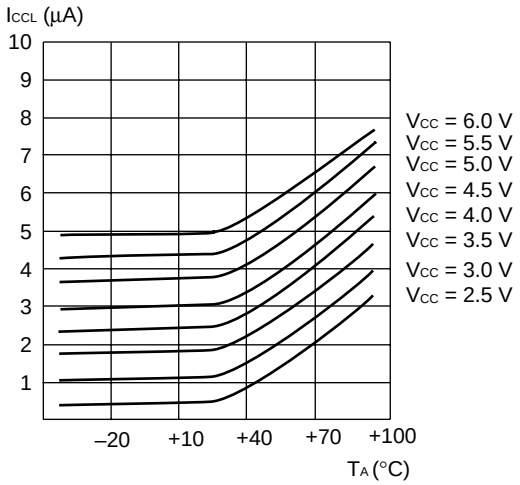
I_{CCH} – V_{CC}

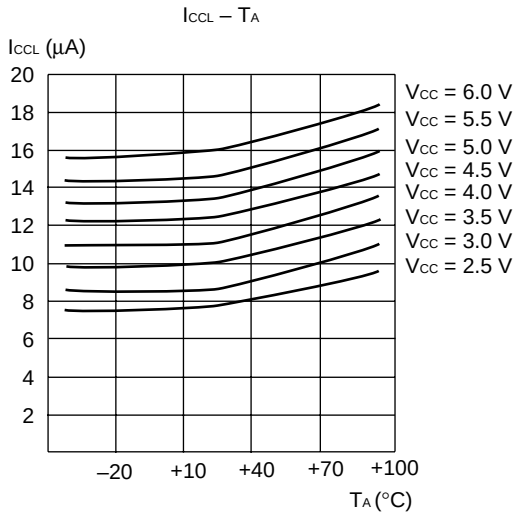


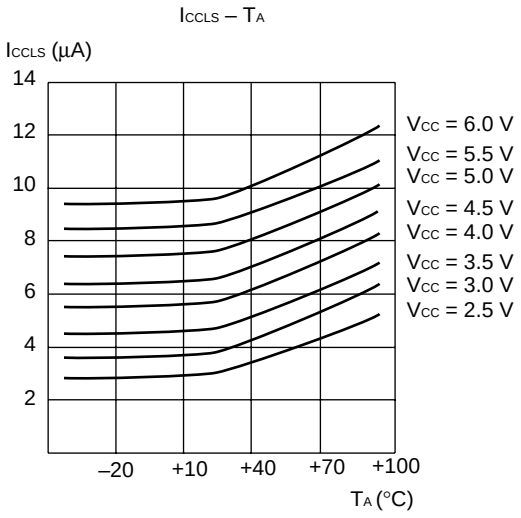
I_{CCT} – T_A



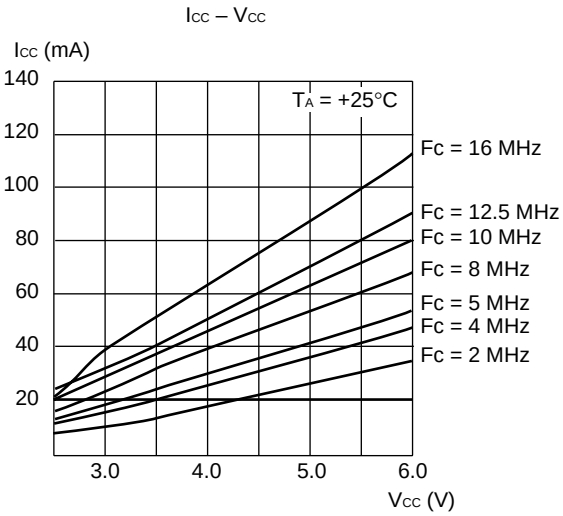
I_{CCH} – T_A

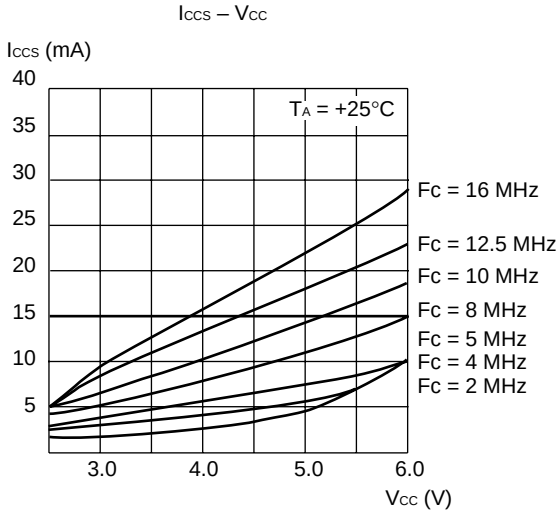


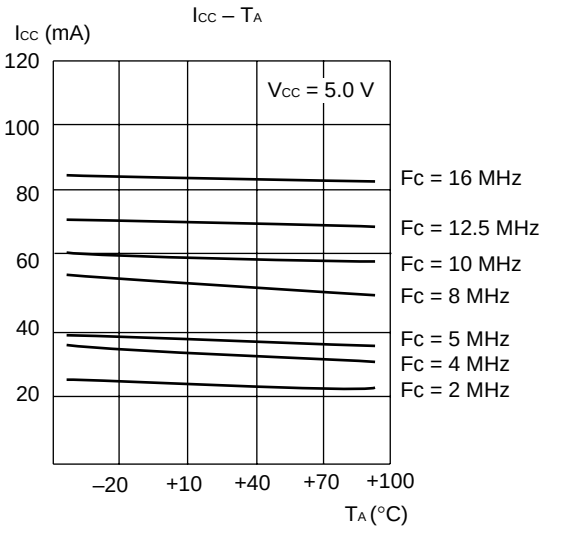


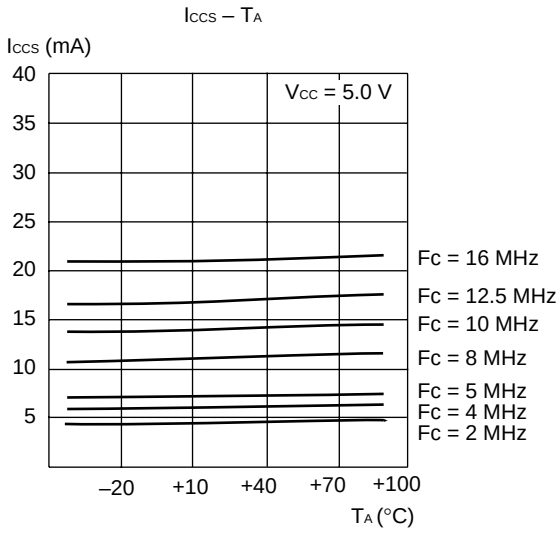


(2) Power Supply Current (MB90F523)

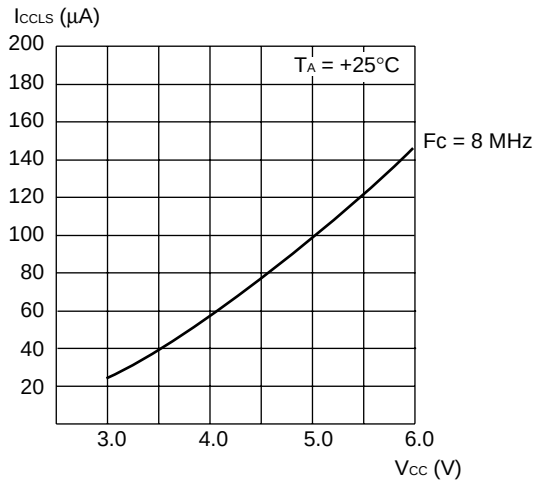




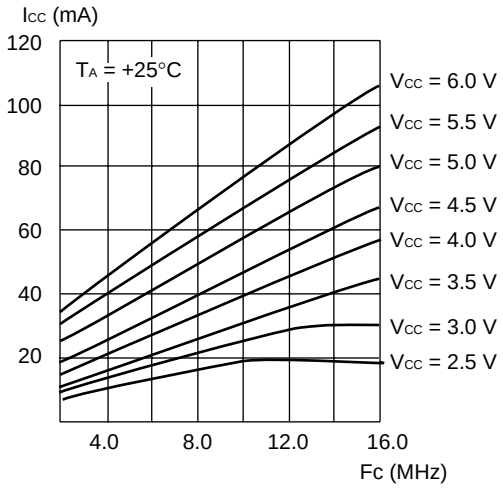




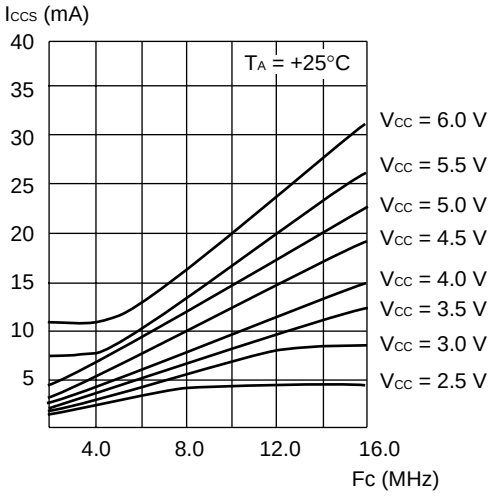
I_{CCS} – V_{CC}



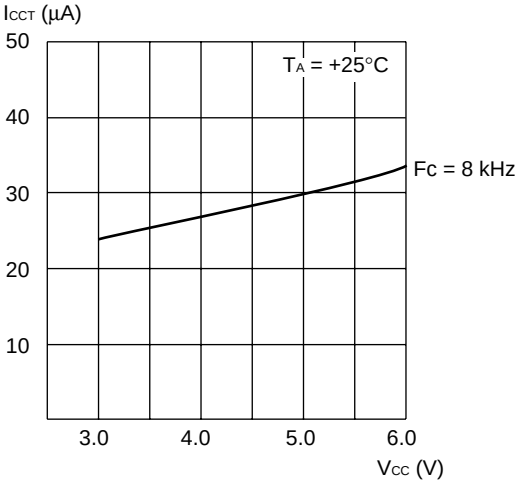
I_{CC} – Fc



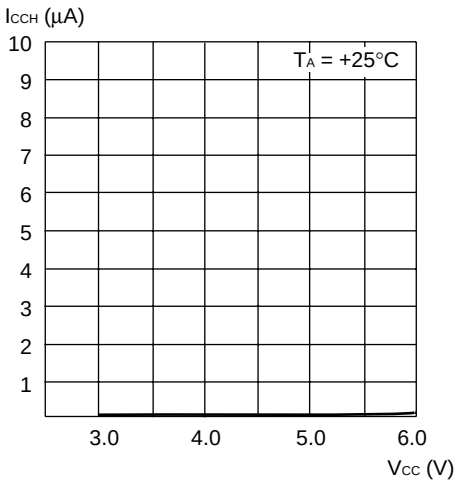
I_{CCS} – Fc

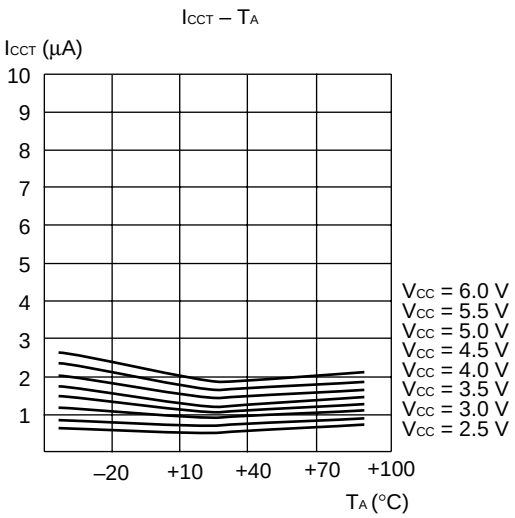


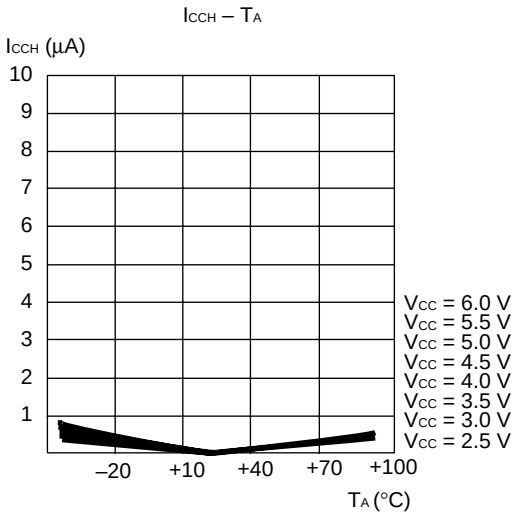
I_{CCT} – V_{CC}

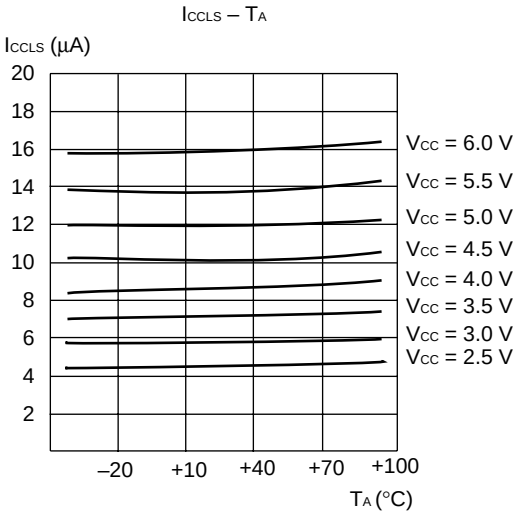


I_{CCH} – V_{CC}




ICCT – TA
ICCT (µA)
10
9
8
7
6
5
4
3
2
1
–20
+10
+40
+70
+100
TA (°C)
VCC = 6.0 V
VCC = 5.5 V
VCC = 5.0 V
VCC = 4.5 V
VCC = 4.0 V
VCC = 3.5 V
VCC = 3.0 V
VCC = 2.5 V


ICCH – TA
ICCH (µA)
10
9
8
7
6
5
4
3
2
1
–20
+10
+40
+70
+100
TA (°C)
VCC = 6.0 V
VCC = 5.5 V
VCC = 5.0 V
VCC = 4.5 V
VCC = 4.0 V
VCC = 3.5 V
VCC = 3.0 V
VCC = 2.5 V


ICCLS – TA
ICCLS (µA)
20
18
16
14
12
10
8
6
4
2
–20
+10
+40
+70
+100
TA (°C)
VCC = 6.0 V
VCC = 5.5 V
VCC = 5.0 V
VCC = 4.5 V
VCC = 4.0 V
VCC = 3.5 V
VCC = 3.0 V
VCC = 2.5 V

■ INSTRUCTIONS (340 INSTRUCTIONS)

Table 1 Description of items in instruction list

Item	Description
Mnemonic	English upper case and symbol: Described directly in assembler code. English lower case: Converted in assembler code. Number of letters after English lower case: Describes bit width in code.
#	Describes number of bytes.
~	Describes number of cycles. m : For branch operation n : For non-branch operation For other letters in other items, refer to table 4.
RG	Describes the number of times the register is accessed during instruction execution. Used to calculate a corrective value for CPU intermittent operation.
B	Describes correction value for calculating number of actual cycles (refer to table 5). Number of actual cycles is calculated by adding values in the ~section and section B.
Operation	Describes operation of instructions.
LH	Describes a special operation to the upper 8-bit of the lower 16-bit of the accumulator. Z : Transfer 0. X : Sign-extend and transfer. – : No transmission
AH	Describes a special operation to the upper 16-bit of the accumulator. * : Transmit from AL to AH. – : No transfer. Z : Transfer 00_H to AH. X : Sign-extend AL and transfer 00_H or FF_H to AH.
I	Describe status of I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry) flags. * : Changes after execution of instruction. – : No changes. S : Set after execution of instruction. R : Reset after execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Describes whether or not the instruction is a read-modify-write type (a data is read out from memory etc. in single cycle, and the result is written into memory etc.). * : Read-modify-write instruction – : Not read-modify-write instruction Note: Not used to addresses having different functions for reading and writing operations.

- **Number of execution cycles**

  The number of cycles required for instruction execution is acquired by adding the number of cycles for each instruction, a corrective value depending on the condition, and the number of cycles required for program fetch. Whenever the instruction being executed exceeds the two-byte (word) boundary, a program on an internal ROM connected to a 16-bit bus is fetched. If data access is interfered with, therefore, the number of execution cycles is increased.

  For each byte of the instruction being executed, a program on a memory connected to an 8-bit external data bus is fetched. If data access in interfered with, therefore, the number of execution cycles is increased.

  When a general-purpose register, an internal ROM, an internal RAM, an internal I/O device, or an external bus is accessed during intermittent CPU operation, the CPU clock is suspended by the number of cycles specified by the CG1/0 bit of the low-power consumption mode control register. When determining the number

of cycles required for instruction execution during intermittent CPU operation, therefore, add the value of the number of times access is done × the number of cycles suspended as the corrective value to the number of ordinary execution cycles.

Table 2 Description of Symbols in Instruction Table

Item	Description
A	32-bit accumlator The bit length is dependent on the instructions to be used. Byte : Lower 8-bit of AL Word :16-bit of AL Long : AL: 32-bit of AH
AH AL	Upper 16-bit of A Lower 16-bit of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Specify shortened direct address.
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Specify direct address. Specify physical direct address. bit0 to bit15 of addr24 bit16 to bit 23 of addr24
io	I/O area (000000_H to $0000FF_H$)
#imm4 #imm8 #imm16 #imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data calculated by sign-extending an 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset value

(Continued)

(Continued)

Item	Description
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address
rel	Specify PC relative branch.
ear eam	Specify effective address (code 00 to 07). Specify effective address (code 08 to 1F).
rlst	Register allocation

Table 3 Effective Address Field

Code	Symbol			Address type	Number of bytes in address extension block
00 01 02 03 04 05 06 07	R0 R1 R2 R3 R4 R5 R6 R7	RW0 RW1 RW2 RW3 RW4 RW5 RW6 RW7	RL0 (RL0) RL1 (RL1) RL2 (RL2) RL3 (RL3)	Register direct ea corresponds to byte, word, and long word from left respectively.	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3			Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +			Register indirect with post increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8			Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16			Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16			Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note: Number of bytes for address extension corresponds to “+” in the # (number of bytes) the number of bytes in detailed instruction rules part in the instruction table.

Table 4 Number of Execution Cycles for Effective Address in Addressing Modes

Code	Operand	(a) Number of execution cycles for addressing modes	Number of register accesses for addressing modes
00 to 07	Ri RWi RLi	Listed in instruction table	Listed in instruction table
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	4 4 2 1	2 2 0 0

Note: (a) is used for ~ (number of cycles) and B (correction value) detailed instruction rules in instruction table.

Table 5 Correction Value for Number of Cycles for Calculating Actual Number of Cycles

Operand	(b) byte		(c) word		(d) long	
	Number of cycles	Number of access	Number of cycles	Number of access	Number of cycles	Number of access
Internal register	+0	1	+0	1	+0	2
Internal memory even address Internal memory odd address	+0 +0	1 1	+0 +2	1 2	+0 +4	2 4
External data bus 16-bit even address External data bus 16-bit odd address	+1 +1	1 1	+1 +4	1 2	+2 +8	2 4
External data bus 8-bit	+1	1	+4	2	+8	4

Notes: • (b), (c), (d) is used for ~ (number of cycles) and B (correction value) in instruction table.
• When the external bus is used, cycles for wait insertion for the ready input and automatic ready operation must be added.

Table 6 Correction Value for Number of Cycles for Calculating Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus 16-bit	—	+3
External data bus 8-bit	+3	—

Notes: • When the external bus is used, cycles for wait insertion for the ready input and automatic ready operation must be added.
• Because execution of instruction is not delayed for all program fetch operations, use this value to calculate the worst case.

Table 7 Transmission Instruction (Byte) [41 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	–	–	–	*	*	–	–	–
MOV A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	–	–	–	*	*	–	–	–
MOV A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	–	–	–	*	*	–	–	–
MOV A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	–	–	–	*	*	–	–	–
MOV A, eam	2 +	3 + (a)	0	(b)	byte (A) ← (eam)	Z	*	–	–	–	*	*	–	–	–
MOV A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	–	–	–	*	*	–	–	–
MOV A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	–	–	–	*	*	–	–	–
MOV A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOV A, @RLi + disp8	3	10	2	(b)	byte (A) ← ((RLi) + disp8)	Z	*	–	–	–	*	*	–	–	–
MOVN A, #imm4	1	1	0	0	byte (A) ← imm4	Z	*	–	–	–	R	*	–	–	–
MOVX A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	–	–	–	*	*	–	–	–
MOVX A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	–	–	–	*	*	–	–	–
MOVX A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	–	–	–	*	*	–	–	–
MOVX A, ear	2	2	1	0	byte (A) ← (ear)	X	*	–	–	–	*	*	–	–	–
MOVX A, eam	2 +	3 + (a)	0	(b)	byte (A) ← (eam)	X	*	–	–	–	*	*	–	–	–
MOVX A, io	2	3	0	(b)	byte (A) ← (io)	X	*	–	–	–	*	*	–	–	–
MOVX A, #imm8	2	2	0	0	byte (A) ← imm8	X	*	–	–	–	*	*	–	–	–
MOVX A, @A	2	3	0	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOVX A, @RWi + disp8	2	5	1	(b)	byte (A) ← ((RWi) + disp8)	X	*	–	–	–	*	*	–	–	–
MOVX A, @RLi + disp8	3	10	2	(b)	byte (A) ← ((RLi) + disp8)	X	*	–	–	–	*	*	–	–	–
MOV dir, A	2	3	0	(b)	byte (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV addr16, A	3	4	0	(b)	byte (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV Ri, A	1	2	1	0	byte (Ri) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV ear, A	2	2	1	0	byte (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV eam, A	2 +	3 + (a)	0	(b)	byte (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV io, A	2	3	0	(b)	byte (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV @RLi + disp8, A	3	10	2	(b)	byte ((RLi) + disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV Ri, ear	2	3	2	0	byte (Ri) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOV Ri, eam	2 +	4 + (a)	1	(b)	byte (Ri) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOV ear, Ri	2	4	2	0	byte (ear) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV eam, Ri	2 +	5 + (a)	1	(b)	byte (eam) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV Ri, #imm8	2	2	1	0	byte (Ri) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV io, #imm8	3	5	0	(b)	byte (io) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV dir, #imm8	3	5	0	(b)	byte (dir) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV ear, #imm8	3	2	1	0	byte (ear) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV eam, #imm8	3 +	4 + (a)	0	(b)	byte (eam) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV @AL, AH /MOV @A, T	2	3	0	(b)	byte ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCH A, ear	2	4	2	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH A, eam	2 +	5 + (a)	0	2 × (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH Ri, ear	2	7	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH Ri, eam	2 +	9 + (a)	2	2 × (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 8 Transmission Instruction (Word, Long) [38 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	1	0	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2 +	3 + (a)	0	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	3	0	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi + disp8	2	5	1	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi + disp8	3	10	2	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW dir, A	2	3	0	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	4	0	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	1	0	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	2	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	1	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2 +	3 + (a)	0	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	3	0	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi + disp8, A	2	5	1	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi + disp8, A	3	10	2	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	3	2	0	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2 +	4 + (a)	1	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	4	2	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2 +	5 + (a)	1	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	5	0	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	1	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4 +	4 + (a)	0	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW @AL, AH /MOVW @A, T	2	3	0	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	4	2	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2 +	5 + (a)	0	2×(c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	7	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2 +	9 + (a)	2	2×(c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
MOVL A, ear	2	4	2	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2 +	5 + (a)	0	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	4	2	0	long (ear1) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2 +	5 + (a)	0	(d)	long (eam1) ← (A)	–	–	–	–	–	*	*	–	–	–

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 9 Add/Subtract (Byte, Word, Long) [42 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD	A,#imm8	2	2	0	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD	A, dir	2	5	0	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD	A, ear	2	3	1	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD	ear, A	2	3	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADD	eam, A	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC	A	1	2	0	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC	A, ear	2	3	1	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC	A	1	3	0	0	byte (A) ← (AH) + (AL) + (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
SUB	A, #imm8	2	2	0	0	byte (A) ← (A) – imm8	Z	–	–	–	–	*	*	*	*	–
SUB	A, dir	2	5	0	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB	A, ear	2	3	1	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB	ear, A	2	3	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUB	eam, A	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC	A	1	2	0	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC	A, ear	2	3	1	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC	A	1	3	0	0	byte (A) ← (AH) – (AL) – (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW	A	1	2	0	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW	A, ear	2	3	1	0	word (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDW	A, #imm16	3	2	0	0	word (A) ← (A) + imm16	–	–	–	–	–	*	*	*	*	–
ADDW	ear, A	2	3	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADDW	eam, A	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW	A, ear	2	3	1	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW	A	1	2	0	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW	A, ear	2	3	1	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW	A, #imm16	3	2	0	0	word (A) ← (A) – imm16	–	–	–	–	–	*	*	*	*	–
SUBW	ear, A	2	3	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUBW	eam, A	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW	A, ear	2	3	1	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL	A, ear	2	6	2	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL	A, eam	2 +	7 + (a)	0	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL	A, #imm32	5	4	0	0	long (A) ← (A) + imm32	–	–	–	–	–	*	*	*	*	–
SUBL	A, ear	2	6	2	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL	A, eam	2 +	7 + (a)	0	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL	A, #imm32	5	4	0	0	long (A) ← (A) – imm32	–	–	–	–	–	*	*	*	*	–

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 10 Increment/Decrement (Byte, Word, Long) [12 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC	ear	2	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INC	eam	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC	ear	2	3	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DEC	eam	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW	ear	2	3	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCW	eam	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW	ear	2	3	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECW	eam	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL	ear	2	7	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCL	eam	2 +	9 + (a)	0	2 × (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL	ear	2	7	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECL	eam	2 +	9 + (a)	0	2 × (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 11 Compare (Byte, Word, Long) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP	A	1	1	0	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP	A, ear	2	2	1	0	byte (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMP	A, eam	2 +	3 + (a)	0	(b)	byte (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMP	A, #imm8	2	2	0	0	byte (A) – imm8	–	–	–	–	–	*	*	*	*	–
CMPW	A	1	1	0	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW	A, ear	2	2	1	0	word (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPW	A, eam	2 +	3 + (a)	0	(c)	word (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPW	A, #imm16	3	2	0	0	word (A) – imm16	–	–	–	–	–	*	*	*	*	–
CMPL	A, ear	2	6	2	0	word (A) – (ear)	–	–	–	–	–	*	*	*	*	–
CMPL	A, eam	2 +	7 + (a)	0	(d)	word (A) – (eam)	–	–	–	–	–	*	*	*	*	–
CMPL	A, #imm32	5	3	0	0	word (A) – imm32	–	–	–	–	–	*	*	*	*	–

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 12 Unsigned Multiply/Division (Word, Long) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU	A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	–	–	–	–	–	–	–	*	*	–
DIVU	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	–	–	–	–	–	–	–	*	*	–
DIVU	A, eam	2 +	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	1	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2 +	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	1	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2 +	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: Set to 3 when the division-by-0, 7 for an overflow, and 15 for normal operation.
*2: Set to 4 when the division-by-0, 8 for an overflow, and 16 for normal operation.
*3: Set to 6 + (a) when the division-by-0, 9 + (a) for an overflow, and 19 + (a) for normal operation.
*4: Set to 4 when the division-by-0, 7 for an overflow, and 22 for normal operation.
*5: Set to 6 + (a) when the division-by-0, 8 + (a) for an overflow, and 26 + (a) for normal operation.
*6: When the division-by-0, (b) for an overflow, and 2 × (b) for normal operation.
*7: When the division-by-0, (c) for an overflow, and 2 × (c) for normal operation.
*8: Set to 3 when byte (AH) is zero, 7 when byte (AH) is not zero.
*9: Set to 4 when byte (ear) is zero, 8 when byte (ear) is not zero.
*10: Set to 5 + (a) when byte (eam) is zero, 9 + (a) when byte (eam) is not zero.
*11: Set to 3 when word (AH) is zero, 11 when word (AH) is not zero.
*12: Set to 4 when word (ear) is zero, 12 when word (ear) is not zero.
*13: Set to 5 + (a) when word (eam) is zero, 13 + (a) when word (eam) is not zero.

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 13 Signed Multiplication/Division (Word, Long) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIV	A	2	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	Z	–	–	–	–	–	–	*	*	–
DIV	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	Z	–	–	–	–	–	–	*	*	–
DIV	A, eam	2 +	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	Z	–	–	–	–	–	–	*	*	–
DIVW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	2	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2 +	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	2	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2 +	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: Set to 3 when the division-by-0, 8 or 18 for an overflow, and 18 for normal operation.
*2: Set to 3 when the division-by-0, 10 or 21 for an overflow, and 22 for normal operation.
*3: Set to 4 + (a) when the division-by-0, 11 + (a) or 22 + (a) for an overflow, and 23 + (a) for normal operation.
*4: Positive dividend: Set to 4 when the division-by-0, 10 or 29 for an overflow, and 30 for normal operation.
Negative dividend: Set to 4 when the division-by-0, 11 or 30 for an overflow and 31 for normal operation.
*5: Positive dividend: Set to 4 + (a) when the division-by-0, 11 + (a) or 30 + (a) for an overflow, and 31 + (a) for normal operation.
Negative dividend: Set to 4 + (a) when the division-by-0, 12 + (a) or 31 + (a) for an overflow, and 32 + (a) for normal operation.
*6: When the division-by-0, (b) for an overflow, and 2 × (b) for normal operation.
*7: When the division-by-0, (c) for an overflow, and 2 × (c) for normal operation.
*8: Set to 3 when byte (AH) is zero, 12 when the result is positive, and 13 when the result is negative.
*9: Set to 3 when byte (ear) is zero, 12 when the result is positive, and 13 when the result is negative.
*10: Set to 4 + (a) when byte (eam) is zero, 13 + (a) when the result is positive, and 14 + (a) when the result is negative.
*11: Set to 3 when word (AH) is zero, 12 when the result is positive, and 13 when the result is negative.
*12: Set to 3 when word (ear) is zero, 16 when the result is positive, and 19 when the result is negative.
*13: Set to 4 + (a) when word (eam) is zero, 17 + (a) when the result is positive, and 20 + (a) when the result is negative.

Notes:
- When overflow occurs during DIV or DIVW instruction execution, the number of execution cycles takes two values because of detection before and after an operation.
- When overflow occurs during DIV or DIVW instruction execution, the contents of AL are destroyed.
- For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 14 Logic 1 (Byte, Word) [39 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND	A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	–	–	–	–	–	*	*	R	–	–
AND	A, ear	2	3	1	0	byte (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
AND	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
AND	ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
AND	eam, A	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
OR	A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	–	–	–	–	–	*	*	R	–	–
OR	A, ear	2	3	1	0	byte (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
OR	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
OR	ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
OR	eam, A	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XOR	A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	–	–	–	–	–	*	*	R	–	–
XOR	A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XOR	A, eam	2 +	4 + (a)	0	(b)	byte (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XOR	ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XOR	eam, A	2 +	5 + (a)	0	2 × (b)	byte (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOT	A	1	2	0	0	byte (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOT	ear	2	3	2	0	byte (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOT	eam	2 +	5 + (a)	0	2 × (b)	byte (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*
ANDW	A	1	2	0	0	word (A) ← (AH) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	A, #imm16	3	2	0	0	word (A) ← (A) and imm16	–	–	–	–	–	*	*	R	–	–
ANDW	A, ear	2	3	1	0	word (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ANDW	ear, A	2	3	2	0	word (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	eam, A	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
ORW	A	1	2	0	0	word (A) ← (AH) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	A, #imm16	3	2	0	0	word (A) ← (A) or imm16	–	–	–	–	–	*	*	R	–	–
ORW	A, ear	2	3	1	0	word (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
ORW	ear, A	2	3	2	0	word (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	eam, A	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XORW	A	1	2	0	0	word (A) ← (AH) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	–	–	–	–	–	*	*	R	–	–
XORW	A, ear	2	3	1	0	word (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORW	A, eam	2 +	4 + (a)	0	(c)	word (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XORW	ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	eam, A	2 +	5 + (a)	0	2 × (c)	word (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOTW	A	1	2	0	0	word (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOTW	ear	2	3	2	0	word (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOTW	eam	2 +	5 + (a)	0	2 × (c)	word (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 15 Logic 2 (Long) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	6	2	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2 +	7 + (a)	0	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	6	2	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2 +	7 + (a)	0	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ear	2	6	2	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2 +	7 + (a)	0	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

Table 16 Sign Reverse (Byte, Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	3	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEG eam	2 +	5 + (a)	0	2×(b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	3	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEGW eam	2 +	5 + (a)	0	2×(c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

Table 17 Normalize Instruction (Long) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*1	1	0	long (A) ← Shift to where “1” is originally located byte (R0) ← Number of shifts in the operation	–	–	–	–	–	–	*	–	–	–

*1: Set to 4 when the accumulator is all “0”, otherwise set to 6 + (R0).

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 18 Shift Type Instruction (Byte, Word, Long) [18 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	0	byte (A) ← With right-rotate carry	–	–	–	–	–	*	*	–	*	–
ROLC A	2	2	0	0	byte (A) ← With left-rotate carry	–	–	–	–	–	*	*	–	*	–
RORC ear	2	3	2	0	byte (ear) ← With right-rotate carry	–	–	–	–	–	*	*	–	*	–
RORC eam	2 +	5 + (a)	0	2 × (b)	byte (eam) ← With right-rotate carry	–	–	–	–	–	*	*	–	*	*
ROLC ear	2	3	2	0	byte (ear) ← With left-rotate carry	–	–	–	–	–	*	*	–	*	–
ROLC eam	2 +	5 + (a)	0	2 × (b)	byte (eam) ← With left-rotate carry	–	–	–	–	–	*	*	–	*	*
ASR A, R0	2	*1	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSR A, R0	2	*1	1	0	byte (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRW A	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	–	–	–	–	*	*	*	–	*	–
LSRW A/SHRW A	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	–	–	–	–	*	R	*	–	*	–
LSLW A/SHLW A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	–	–	–	–	–	*	*	–	*	–
ASRW A, R0	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRW A, R0	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLW A, R0	2	*1	1	0	word (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–

*1: Set to 6 when R0 is 0, otherwise 5 + (R0).
*2: Set to 6 when R0 is 0, otherwise 6 + (R0).

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 19 Branch 1 [31 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	0	Branch if (Z) = 1	–	–	–	–	–	–	–	–	–	–
BNZ/BNE rel	2	*1	0	0	Branch if (Z) = 0	–	–	–	–	–	–	–	–	–	–
BC/BLO rel	2	*1	0	0	Branch if (C) = 1	–	–	–	–	–	–	–	–	–	–
BNC/BHS rel	2	*1	0	0	Branch if (C) = 0	–	–	–	–	–	–	–	–	–	–
BN rel	2	*1	0	0	Branch if (N) = 1	–	–	–	–	–	–	–	–	–	–
BP rel	2	*1	0	0	Branch if (N) = 0	–	–	–	–	–	–	–	–	–	–
BV rel	2	*1	0	0	Branch if (V) = 1	–	–	–	–	–	–	–	–	–	–
BNV rel	2	*1	0	0	Branch if (V) = 0	–	–	–	–	–	–	–	–	–	–
BT rel	2	*1	0	0	Branch if (T) = 1	–	–	–	–	–	–	–	–	–	–
BNT rel	2	*1	0	0	Branch if (T) = 0	–	–	–	–	–	–	–	–	–	–
BLT rel	2	*1	0	0	Branch if (V) xor (N) = 1	–	–	–	–	–	–	–	–	–	–
BGE rel	2	*1	0	0	Branch if (V) xor (N) = 0	–	–	–	–	–	–	–	–	–	–
BLE rel	2	*1	0	0	Branch if ((V) xor (N)) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BGT rel	2	*1	0	0	Branch if ((V) xor (N)) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BLS rel	2	*1	0	0	Branch if (C) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BHI rel	2	*1	0	0	Branch if (C) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BRA rel	2	*1	0	0	Branch unconditionally	–	–	–	–	–	–	–	–	–	–
JMP @A	1	2	0	0	word (PC) ← (A)	–	–	–	–	–	–	–	–	–	–
JMP addr16	3	3	0	0	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
JMP @ear	2	3	1	0	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
JMP @eam	2 +	4 + (a)	0	(c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
JMPP @ear *3	2	5	2	0	word (PC) ← (ear), (PCB) ← (ear + 2)	–	–	–	–	–	–	–	–	–	–
JMPP @eam *3	2 +	6 + (a)	0	(d)	word (PC) ← (eam), (PCB) ← (eam + 2)	–	–	–	–	–	–	–	–	–	–
JMPP addr24	4	4	0	0	word (PC) ← ad24 0 – 15, (PCB) ← ad24 16 – 23	–	–	–	–	–	–	–	–	–	–
CALL @ear *4	2	6	1	(c)	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
CALL @eam *4	2 +	7 + (a)	0	2 × (c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
CALL addr16 *5	3	6	0	(c)	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
CALLV #vct4 *5	1	7	0	2 × (c)	Vector call instruction	–	–	–	–	–	–	–	–	–	–
CALLP @ear *6	2	10	2	2 × (c)	word (PC) ← (ear) 0 – 15 (PCB) ← (ear) 16 – 23	–	–	–	–	–	–	–	–	–	–
CALLP @eam *6	2 +	11 + (a)	0	*2	word (PC) ← (eam) 0 – 15 (PCB) ← (eam) 16 – 23	–	–	–	–	–	–	–	–	–	–
CALLP addr24 *7	4	10	0	2 × (c)	word (PC) ← ad24 0 – 15, (PCB) ← ad24 16 – 23	–	–	–	–	–	–	–	–	–	–

*1: Set to 4 when branch is executed, and 3 when branch is not executed.
*2: (b) + 3 × (c)
*3: Reads (word) of the branch destination address.
*4: W pushes to stack (word), and R reads (word) of the branch destination address.
*5: Pushes to stack (word).
*6: W pushes to stack (long), and R reads (long) of the branch destination address.
*7: Pushes to stack (long).

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 20 Branch 2 (Byte) [19 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE	A, #imm8, rel	3	*1	0	0	Branch if byte (A) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE	A, #imm16, rel	4	*1	0	0	Branch if word (A) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CBNE	ear, #imm8, rel	4	*2	1	0	Branch if byte (ear) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CBNE	eam, #imm8, rel*10	4 +	*3	0	(b)	Branch if byte (eam) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE	ear, #imm16, rel	5	*4	1	0	Branch if word (ear) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CWBNE	eam, #imm16, rel*10	5 +	*3	0	(c)	Branch if word (eam) ≠ imm16	–	–	–	–	–	*	*	*	*	–
DBNZ	ear, rel	3	*5	2	0	byte (ear) = (ear) – 1, Branch if (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DBNZ	eam, rel	3 +	*6	2	2 × (b)	byte (eam) = (eam) – 1, Branch if (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
DWBNZ	ear, rel	3	*5	2	0	word (ear) = (ear) – 1, Branch if (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DWBNZ	eam, rel	3 +	*6	2	2 × (c)	word (eam) = (eam) – 1, Branch if (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
INT	#vct8	2	20	0	8 × (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT	addr16	3	16	0	6 × (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INTP	addr24	4	17	0	6 × (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT9		1	20	0	8 × (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
RETI		1	17	0	*7	Return from interrupt	–	–	*	*	*	*	*	*	*	–
LINK	#imm8	2	6	0	(c)	Stores old frame pointer in the beginning of the function, set new frame pointer, and reserves local pointer area	–	–	–	–	–	–	–	–	–	–
UNLINK		1	5	0	(c)	Restore old frame pointer from stack in the end of the function	–	–	–	–	–	–	–	–	–	–
RET *8		1	4	0	(c)	Return from subroutine	–	–	–	–	–	–	–	–	–	–
RETP *9		1	6	0	(d)	Return from subroutine	–	–	–	–	–	–	–	–	–	–

*1: Set to 5 when branch is executed, and 4 when branch is not executed.
*2: Set to 13 when branch is executed, and 12 when branch is not executed.
*3: Set to 7 + (a) when branch is executed, and 6 + (a) when branch is not executed.
*4: Set to 8 when branch is executed, and 7 when branch is not executed.
*5: Set to 7 when branch is executed, and 6 when branch is not executed.
*6: Set to 8 + (a) when branch is executed, and 7 + (a) when branch is not executed.
*7: Set to 3 × (b) + 2 × (c) when an interrupt request occurs, and 6 × (c) for return.
*8: Return from stack (word).
*9: Return from stack (long).
*10: Do not use the addressing mode of RWj + in CBNE/CWBNE instruction.

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 21 Miscellaneous Control Types (Byte, Word, Long) [28 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW	A	1	4	0	(c)	word (SP) ← (SP) – 2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW	AH	1	4	0	(c)	word (SP) ← (SP) – 2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW	PS	1	4	0	(c)	word (SP) ← (SP) – 2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW	rlst	2	*3	+&	*4	(PS) ← (PS) – 2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW	A	1	3	0	(c)	word (A) ← ((SP)), (SP) ← (SP) + 2	–	*	–	–	–	–	–	–	–	–
POPW	AH	1	3	0	(c)	word (AH) ← ((SP)), (SP) ← (SP) + 2	–	–	–	–	–	–	–	–	–	–
POPW	PS	1	4	0	(c)	word (PS) ← ((SP)), (SP) ← (SP) + 2	–	–	*	*	*	*	*	*	*	–
POPW	rlst	2	*2	+&	*4	(rlst) ← ((SP)), (SP) ← (SP) + 2n	–	–	–	–	–	–	–	–	–	–
JCTX	@A	1	14	0	6 × (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND	CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR	CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV	RP, #imm8	2	2	0	0	byte (RP) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	ILM, #imm8	2	2	0	0	byte (ILM) ← imm8	–	–	–	–	–	–	–	–	–	–
MOVEA	RWi, ear	2	3	1	0	word (RWi) ← ear	–	–	–	–	–	–	–	–	–	–
MOVEA	RWi, eam	2 +	2 + (a)	1	0	word (RWi) ← eam	–	–	–	–	–	–	–	–	–	–
MOVEA	A, ear	2	1	0	0	word(A) ← ear	–	*	–	–	–	–	–	–	–	–
MOVEA	A, eam	2 +	1 + (a)	0	0	word (A) ← eam	–	*	–	–	–	–	–	–	–	–
ADDSP	#imm8	2	3	0	0	word (SP) ← (SP) + ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP	#imm16	3	3	0	0	word (SP) ← (SP) + imm16	–	–	–	–	–	–	–	–	–	–
MOV	A, brgl	2	*1	0	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV	brg2, A	2	1	0	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
NOP		1	1	0	0	No operation	–	–	–	–	–	–	–	–	–	–
ADB		1	1	0	0	Prefix code for accessing AD space	–	–	–	–	–	–	–	–	–	–
DTB		1	1	0	0	Prefix code for accessing DT space	–	–	–	–	–	–	–	–	–	–
PCB		1	1	0	0	Prefix code for accessing PC space	–	–	–	–	–	–	–	–	–	–
SPB		1	1	0	0	Prefix code for accessing SP space	–	–	–	–	–	–	–	–	–	–
NCC		1	1	0	0	Prefix code for no change in flag	–	–	–	–	–	–	–	–	–	–
CMR		1	1	0	0	Prefix for common register bank	–	–	–	–	–	–	–	–	–	–

*1: PCB, ADB, SSB, USB, and SPB : 1 state
DTB, DPR : 2 states

*2: 7 + 3 × (number of POPs) + 2 × (the number of the last register to be POPed), 7 if rlst = 0(no transfer registers)

*3: 29 + 3 × (number of PUSHes) – 3 × (the number of the last register to be PUSHed), 8 if rlst = 0(no transfer registers)

*4: (Number of POPs) × (c), or (number of PUSHes) × (c)

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 22 Bit Manipulation Instruction [21 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB A, dir:bp	3	5	0	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB A, addr16:bp	4	5	0	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB A, io:bp	3	4	0	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB dir:bp, A	3	7	0	2 × (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB addr16:bp, A	4	7	0	2 × (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB io:bp, A	3	6	0	2 × (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
SETB dir:bp	3	7	0	2 × (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB addr16:bp	4	7	0	2 × (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB io:bp	3	7	0	2 × (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB dir:bp	3	7	0	2 × (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB addr16:bp	4	7	0	2 × (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB io:bp	3	7	0	2 × (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
BBC dir:bp, rel	4	*1	0	(b)	Branch if (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC addr16:bp, rel	5	*1	0	(b)	Branch if (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC io:bp, rel	4	*2	0	(b)	Branch if (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBS dir:bp, rel	4	*1	0	(b)	Branch if (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS addr16:bp, rel	5	*1	0	(b)	Branch if (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS io:bpvrel	4	*2	0	(b)	Branch if (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
SBBS addr16:bp, rel	5	*3	0	2 × (b)	Branch if (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
WBTS io:bp	3	*4	0	*5	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
WBTC io:bp	3	*4	0	*5	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–

*1: Set to 8 when branch is executed, and 7 when branch is not executed.
*2: Set to 7 when branch is executed, and 6 when branch is not executed.
*3: 10 if conditions are met, 9 when conditions are not met.
*4: Indeterminate times
*5: Until conditions are met

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 23 Accumulator Manipulation Instruction (Byte, Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	0	byte (A) 0 – 7 ↔ (A) 8 – 15	–	–	–	–	–	–	–	–	–	–
SWAPW/XCHW AL, AH	1	2	0	0	word (AH) ↔ (AL)	–	*	–	–	–	–	–	–	–	–
EXT	1	1	0	0	byte sign-extension	X	–	–	–	–	*	*	–	–	–
EXTW	1	2	0	0	word sign-extension	–	X	–	–	–	*	*	–	–	–
ZEXT	1	1	0	0	byte zero-extension	Z	–	–	–	–	R	*	–	–	–
ZEXTW	1	1	0	0	word zero-extension	–	Z	–	–	–	R	*	–	–	–

Table 24 String Instruction [10 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVSI	2	*2	*5	*3	byte transfer @AH + ← @AL +, Counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSD	2	*2	*5	*3	byte transfer @AH – ← @AL –, Counter = RW0	–	–	–	–	–	–	–	–	–	–
SCEQ/SCEQI	2	*1	*5	*4	byte search (@AH +) – AL, Counter = RW0	–	–	–	–	–	*	*	*	*	–
SCEQD	2	*1	*5	*4	byte search (@AH –) – AL, Counter = RW0	–	–	–	–	–	*	*	*	*	–
FISL/FILSI	2	6m + 6	*5	*3	byte fill @AH + ← AL, Counter = RW0	–	–	–	–	–	*	*	–	–	–
MOVSW/MOVSWI	2	*2	*8	*6	word transfer @AH + ← @AL +, Counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSWD	2	*2	*8	*6	word transfer @AH – ← @AL –, Counter = RW0	–	–	–	–	–	–	–	–	–	–
SCWEQ/SCWEQI	2	*1	*8	*7	word search (@AH +) – AL, Counter = RW0	–	–	–	–	–	*	*	*	*	–
SCWEQD	2	*1	*8	*7	word search (@AH –) – AL, Counter = RW0	–	–	–	–	–	*	*	*	*	–
FILSW/FILSWI	2	6m + 6	*8	*6	word fill @AH + ← AL, Counter = RW0	–	–	–	–	–	*	*	–	–	–

m: RW0 value (counter value)
n: Number of loops

*1: 5 when RW0 is 0, 4 + 7 × (RW0) when count out, and 7 × n + 5 when matched
*2: 5 when RW0 is 0, otherwise 4 + 8 × (RW0)
*3: To access different areas for source (b) × (RW0) + (b) × (RW0) and source destination, calculate item (b) independently.
*4: (b) × n
*5: 2 × (RW0)
*6: To access different areas for source (c) × (RW0) + (c) × (RW0) and source destination, calculate item (b) independently.
*7: (c) × n
*8: 2 × (RW0)

Note: For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 25 2-byte Instruction Map [Byte 1 = 6 FH]

	00	10	20	30	40	50	60	70	80	90	A0	B0	C0	D0	E0	F0
+0	MOV A, DTB	MOV DTB, A	MOVX A, @RL0 + d8	MOV @RL0 + d8, A	MOV A, @RL0 + d8											
+1	MOV A, ADB	MOV ADB, A														
+2	MOV A, SSB	MOV SSB, A	MOVX A, @RL1 + d8	MOV @RL1 + d8, A	MOV A, @RL1 + d8											
+3	MOV A, USB	MOV USB, A														
+4	MOV A, DPR	MOV DPR, A	MOVX A, @RL2 + d8	MOV @RL2 + d8, A	MOV A, @RL2 + d8											
+5	MOV A, @A	MOV @AL, AH														
+6	MOV A, PCB	MOVX A, @A	MOVX A, @RL3 + d8	MOV @RL3 + d8, A	MOV A, @RL3 + d8											
+7	ROLC A	RORC A														
+8				MOVW @RL0 + d8, A	MOVW A, @RL0 + d8			MUL A								
+9								MULW A								
+A				MOVW @RL1 + d8, A	MOVW A, @RL1 + d8			DIVU A								
+B																
+C	LSLW A, R0	LSLL A, R0	LSL A, R0	MOVW @RL2 + d8, A	MOVW A, @RL2 + d8											
+D	MOVW A, @A	MOVW @AL, AH	NRML A, R0													
+E	ASRW A, R0	ASRL A, R0	ASR A, R0	MOVW @RL3 + d8, A	MOVW A, @RL3 + d8											
+F	LSRW A, R0	LSRL A, R0	LSR A, R0													

Table 26 ea Instruction (9) [Byte 1 = 78 H]

	00	10	20	30	40	50	60	70	80	90	A0	B0	C0	D0	E0	F0
+0	MULU A, R0	MULU A, @RW0 + d8	MULUW A, RW0	MULUW A, @RW0 + d8	MUL A, R0	MUL A, @RW0 + d8	MULW A, RW0	MULW A, @RW0 + d8	DIVU A, R0	DIVU A, @RW0 + d8	DIVUW A, RW0	DIVUW A, @RW0 + d8	DIV A, R0	DIV A, @RW0 + d8	DIVW A, RW0	DIVW A, @RW0 + d8
+1	MULU A, R1	MULU A, @RW1 + d8	MULUW A, RW1	MULUW A, @RW1 + d8	MUL A, R1	MUL A, @RW1 + d8	MULW A, RW1	MULW A, @RW1 + d8	DIVU A, R1	DIVU A, @RW1 + d8	DIVUW A, RW1	DIVUW A, @RW1 + d8	DIV A, R1	DIV A, @RW1 + d8	DIVW A, RW1	DIVW A, @RW1 + d8
+2	MULU A, R2	MULU A, @RW2 + d8	MULUW A, RW2	MULUW A, @RW2 + d8	MUL A, R2	MUL A, @RW2 + d8	MULW A, RW2	MULW A, @RW2 + d8	DIVU A, R2	DIVU A, @RW2 + d8	DIVUW A, RW2	DIVUW A, @RW2 + d8	DIV A, R2	DIV A, @RW2 + d8	DIVW A, RW2	DIVW A, @RW2 + d8
+3	MULU A, R3	MULU A, @RW3 + d8	MULUW A, RW3	MULUW A, @RW3 + d8	MUL A, R3	MUL A, @RW3 + d8	MULW A, RW3	MULW A, @RW3 + d8	DIVU A, R3	DIVU A, @RW3 + d8	DIVUW A, RW3	DIVUW A, @RW3 + d8	DIV A, R3	DIV A, @RW3 + d8	DIVW A, RW3	DIVW A, @RW3 + d8
+4	MULU A, R4	MULU A, @RW4 + d8	MULUW A, RW4	MULUW A, @RW4 + d8	MUL A, R4	MUL A, @RW4 + d8	MULW A, RW4	MULW A, @RW4 + d8	DIVU A, R4	DIVU A, @RW4 + d8	DIVUW A, RW4	DIVUW A, @RW4 + d8	DIV A, R4	DIV A, @RW4 + d8	DIVW A, RW4	DIVW A, @RW4 + d8
+5	MULU A, R5	MULU A, @RW5 + d8	MULUW A, RW5	MULUW A, @RW5 + d8	MUL A, R5	MUL A, @RW5 + d8	MULW A, RW5	MULW A, @RW5 + d8	DIVU A, R5	DIVU A, @RW5 + d8	DIVUW A, RW5	DIVUW A, @RW5 + d8	DIV A, R5	DIV A, @RW5 + d8	DIVW A, RW5	DIVW A, @RW5 + d8
+6	MULU A, R6	MULU A, @RW6 + d8	MULUW A, RW6	MULUW A, @RW6 + d8	MUL A, R6	MUL A, @RW6 + d8	MULW A, RW6	MULW A, @RW6 + d8	DIVU A, R6	DIVU A, @RW6 + d8	DIVUW A, RW6	DIVUW A, @RW6 + d8	DIV A, R6	DIV A, @RW6 + d8	DIVW A, RW6	DIVW A, @RW6 + d8
+7	MULU A, R7	MULU A, @RW7 + d8	MULUW A, RW7	MULUW A, @RW7 + d8	MUL A, R7	MUL A, @RW7 + d8	MULW A, RW7	MULW A, @RW7 + d8	DIVU A, R7	DIVU A, @RW7 + d8	DIVUW A, RW7	DIVUW A, @RW7 + d8	DIV A, R7	DIV A, @RW7 + d8	DIVW A, RW7	DIVW A, @RW7 + d8
+8	MULU A, @RW0	MULU A, @RW0 + d16	MULUW A, @RW0	MULUW A, @RW0 + d16	MUL A, @RW0	MUL A, @RW0 + d16	MULW A, @RW0	MULW A, @RW0 + d16	DIVU A, @RW0	DIVU A, @RW0 + d16	DIVUW A, @RW0	DIVUW A, @RW0 + d16	DIV A, @RW0	DIV A, @RW0 + d16	DIVW A, @RW0	DIVW A, @RW0 + d16
+9	MULU A, @RW1	MULU A, @RW1 + d16	MULUW A, @RW1	MULUW A, @RW1 + d16	MUL A, @RW1	MUL A, @RW1 + d16	MULW A, @RW1	MULW A, @RW1 + d16	DIVU A, @RW1	DIVU A, @RW1 + d16	DIVUW A, @RW1	DIVUW A, @RW1 + d16	DIV A, @RW1	DIV A, @RW1 + d16	DIVW A, @RW1	DIVW A, @RW1 + d16
+A	MULU A, @RW2	MULU A, @RW2 + d16	MULUW A, @RW2	MULUW A, @RW2 + d16	MUL A, @RW2	MUL A, @RW2 + d16	MULW A, @RW2	MULW A, @RW2 + d16	DIVU A, @RW2	DIVU A, @RW2 + d16	DIVUW A, @RW2	DIVUW A, @RW2 + d16	DIV A, @RW2	DIV A, @RW2 + d16	DIVW A, @RW2	DIVW A, @RW2 + d16
+B	MULU A, @RW3	MULU A, @RW3 + d16	MULUW A, @RW3	MULUW A, @RW3 + d16	MUL A, @RW3	MUL A, @RW3 + d16	MULW A, @RW3	MULW A, @RW3 + d16	DIVU A, @RW3	DIVU A, @RW3 + d16	DIVUW A, @RW3	DIVUW A, @RW3 + d16	DIV A, @RW3	DIV A, @RW3 + d16	DIVW A, @RW3	DIVW A, @RW3 + d16
+C	MULU A, @RW0 +	MULU A, @RW0 + RW7	MULUW A, @RW0 +	MULUW A, @RW0 + RW7	MUL A, @RW0 +	MUL A, @RW0 + RW7	MULW A, @RW0 +	MULW A, @RW0 + RW7	DIVU A, @RW0 +	DIVU A, @RW0 + RW7	DIVUW A, @RW0 +	DIVUW A, @RW0 + RW7	DIV A, @RW0 +	DIV A, @RW0 + RW7	DIVW A, @RW0 +	DIVW A, @RW0 + RW7
+D	MULU A, @RW1 +	MULU A, @RW1 + RW7	MULUW A, @RW1 +	MULUW A, @RW1 + RW7	MUL A, @RW1 +	MUL A, @RW1 + RW7	MULW A, @RW1 +	MULW A, @RW1 + RW7	DIVU A, @RW1 +	DIVU A, @RW1 + RW7	DIVUW A, @RW1 +	DIVUW A, @RW1 + RW7	DIV A, @RW1 +	DIV A, @RW1 + RW7	DIVW A, @RW1 +	DIVW A, @RW1 + RW7
+E	MULU A, @RW2 +	MULU A, @PC + d16	MULUW A, @RW2 +	MULUW A, @PC + d16	MUL A, @RW2 +	MUL A, @PC + d16	MULW A, @RW2 +	MULW A, @PC + d16	DIVU A, @RW2 +	DIVU A, @PC + d16	DIVUW A, @RW2 +	DIVUW A, @PC + d16	DIV A, @RW2 +	DIV A, @PC + d16	DIVW A, @RW2 +	DIVW A, @PC + d16
+F	MULU A, @RW3 +	MULU A, addr16	MULUW A, @RW3 +	MULUW A, addr16	MUL A, @RW3 +	MUL A, addr16	MULW A, @RW3 +	MULW A, addr16	DIVU A, @RW3 +	DIVU A, addr16	DIVUW A, @RW3 +	DIVUW A, addr16	DIV A, @RW3 +	DIV A, addr16	DIVW A, @RW3 +	DIVW A, addr16

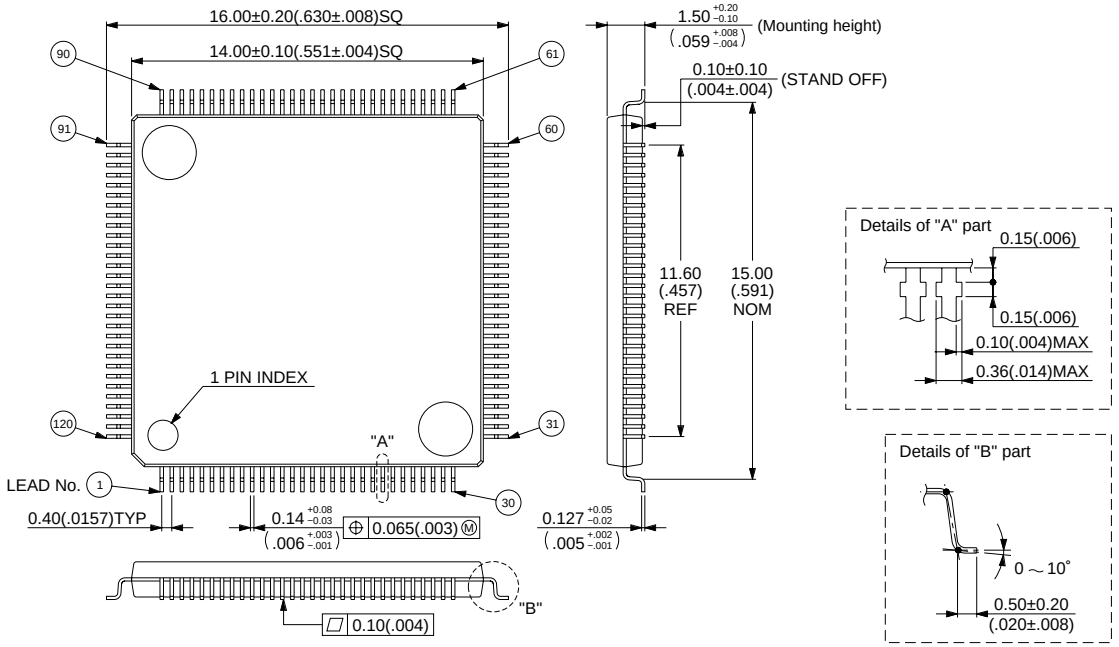
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90523PFF-G MB90522PFF-G MB90F523PFF-G	120-pin Plastic LQFP (FPT-120P-M05)	
MB90523PFV-G MB90522PFV MB90F523PFV-G	120-pin Plastic QFP (FPT-120P-M13)	

MB90520 Series

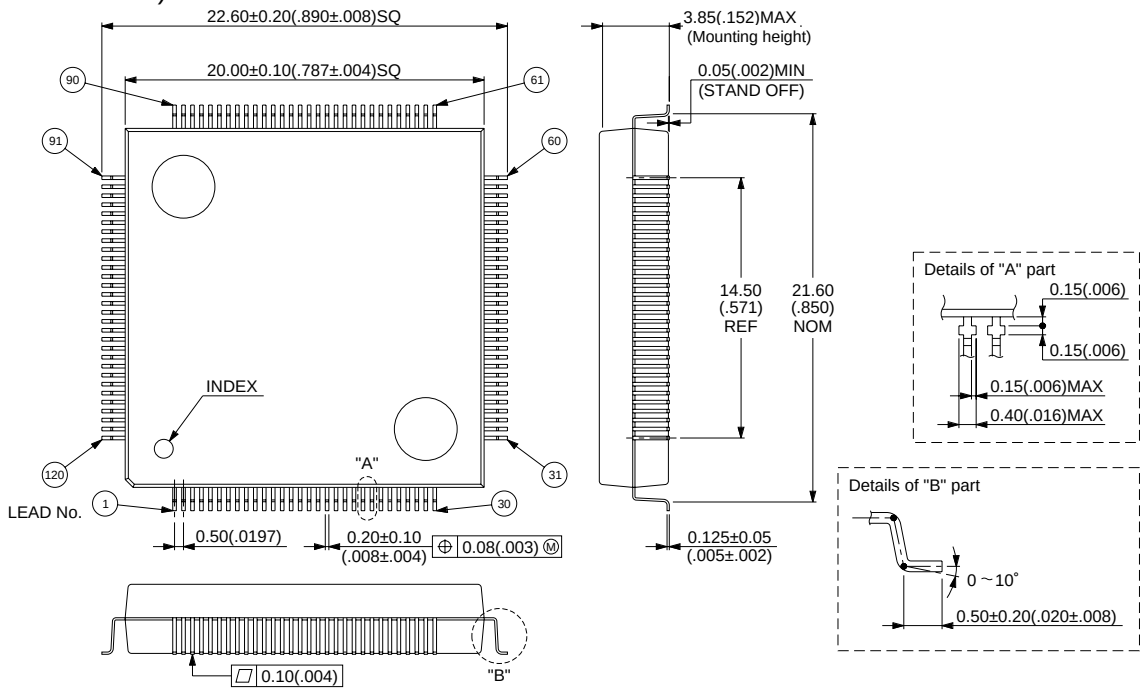
■ PACKAGE DIMENSIONS

120-pin Plastic LQFP
(FPT-120P-M05)



Dimensions in mm (inches)

120-pin Plastic QFP
(FPT-120P-M13)



Dimensions in mm (inches)

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