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#### MPEG Layer 3 Audio Encoder/Decoder

This data sheet applies to MAS 3587F version B2.

Release Note: Revision bars indicate significant changes to the previous edition.

#### 1. Introduction

The MAS 3587F is a single-chip MPEG layer 3 audio encoder/decoder designed for use in memory-based recording/playback applications, e.g. MP3 record/playback equipment. The IC contains a DSP engine with embedded RAM and ROM. It provides flexible digital interfaces for serial and S/PDIF audio data input and output. Also integrated are power management functions and two DC/DC converters for single cell power supply. A high-quality stereo D/A converter and a stereo A/D converter on chip provide the analog functions required in an advanced portable audio player.

In encoding mode, audio data is input via the integrated A/D converter, serial PCM, or S/PDIF interface. The compressed digital data stream is sent via the parallel interface. In decoding mode, compressed digital data streams are accepted in the parallel or serial format. The audio data is output via the high quality D/A converter. A digital output in serial PCM format and/or S/PDIF format is also provided.

Thus, the MAS 3587F provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized memory based music recorders.

Additional functionality is achieved via download software (e.g. Micronas SC4 encoder/decoder). SC4 is a proprietary Micronas speech codec technology based on ADPCM. The codec can be downloaded to the MAS 3587F to allow high quality speech recording and playing back at various sampling rates. (Please contact your local Micronas Sales Representative about availability of SC4 downloads).

In MPEG 1 (ISO 11172-3), three hierarchical layers of compression have been standardized. The most sophisticated and complex, layer 3, allows compression rates of approximately 12:1 for mono and stereo signals while still maintaining CD audio quality.

■ The MAS 3587F is available in the PMQFP64 package.

#### 1.1. Features

#### **Firmware**

- MPEG 1/2 layer 3 encoder
- Encoding with adaptive bit rate up to 192 kbit/s
- MPEG 1/2 layer 2 and layer 3 decoder
- Decoder-extension to MPEG 2 layer 3 for low bit rates ("MPEG 2.5")
- Extraction of MPEG Ancillary Data
- Adaptive bit rates (bit rate switching)
- SDMI-compliant security technology for decoder
- Stereo channel mixer
- Bass, treble and loudness function
- Micronas Dynamic Bass (MDB)
- Automatic Volume Correction (AVC)

#### Interfaces

- 2 serial asynchronous interfaces for bitstreams and uncompressed digital audio
- Parallel handshake bit stream input/output
- Serial audio output via I<sup>2</sup>S and related formats
- S/PDIF audio input
- S/PDIF audio output
- Controlling via I<sup>2</sup>C interface

#### **Hardware Features**

- Two independent embedded DC/DC converters (e.g. for DSP and flash RAM supply)
- Low DC/DC converter start-up voltage (0.9 V)
- DC converter efficiency up to 95%
- Battery voltage monitor
- Low supply voltage (down to 2.5 V for decoder, 3.5 V for encoder)
- Low power dissipation (down to 70 mW for decoder, down to 450 mW for MPEG 1 encoder)
- Hardware power management and power-off functions
- Microphone amplifier
- Stereo A/D converter for FM/AM-radio and speech input
- CD quality stereo D/A converter
- Headphone amplifier
- On-chip crystal oscillator
- External clock or crystal frequency of 13...28 MHz
- Standby current < 10 μA

### 1.2. Application Overview

The following block diagram shows an example application for the MAS 3587F in a portable audio recorder device. Besides a simple controller and the external flash memories, all required components are integrated in the MAS 3587F. By means of the embedded A/D-converter, the MAS 3587F supports both speech and FM radio quality audio encoding. CD-quality encoding/decoding is achieved by using digital inputs/embedded D/A-converter.

Fig. 1–1 depicts a portable audio application that is power optimized. The two embedded DC/DC converters of the MAS 3587F generate optimum power supply voltages for the DSP core and also for state-of-the-art flash memories that typically require 2.7 to 3.3 V supply.

The performance of the DC/DC converters reaches efficiencies up to 95%.

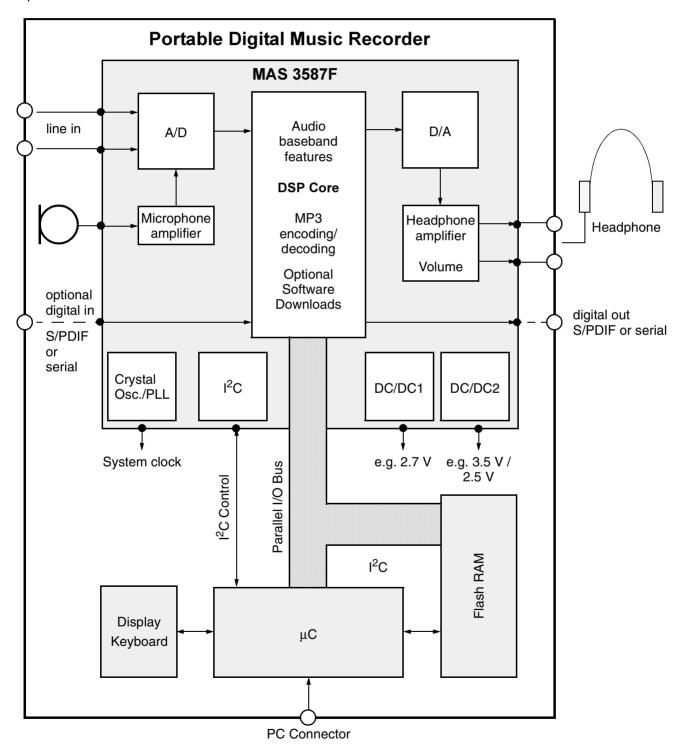


Fig. 1-1: Example application for the MAS 3587F in a portable audio recorder device

#### 2. Functional Description

#### 2.1. Overview

The MAS 3587F is intended for use in consumer audio applications. It encodes analog audio input, PCM data or S/PDIF signals to variable bit rate MPEG 1/2 Layer 3 data streams. The compressed data is stored in an external memory via the parallel port. For playback it receives parallel or serial data streams and decodes MPEG Layer 2 and 3 (including the low sampling frequency extensions).

#### 2.2. Architecture of the MAS 3587F

The hardware of the MAS 3587F consists of a high-performance RISC Digital Signal Processor (DSP), and appropriate interfaces. A hardware overview of the IC is shown in Fig. 2–1.

#### 2.3. DSP Core

The internal processor is a dedicated DSP for advanced audio applications.

#### 2.4. RAM and Registers

The DSP core has access to two RAM banks denoted D0 and D1. All RAM addresses can be accessed in a 20-bit or a 16-bit mode via I<sup>2</sup>C bus. For fast access of internal DSP states the processor core has an address space of 256 data registers which can be accessed by I<sup>2</sup>C bus. For more details please refer to Section 3.3. on page 23.

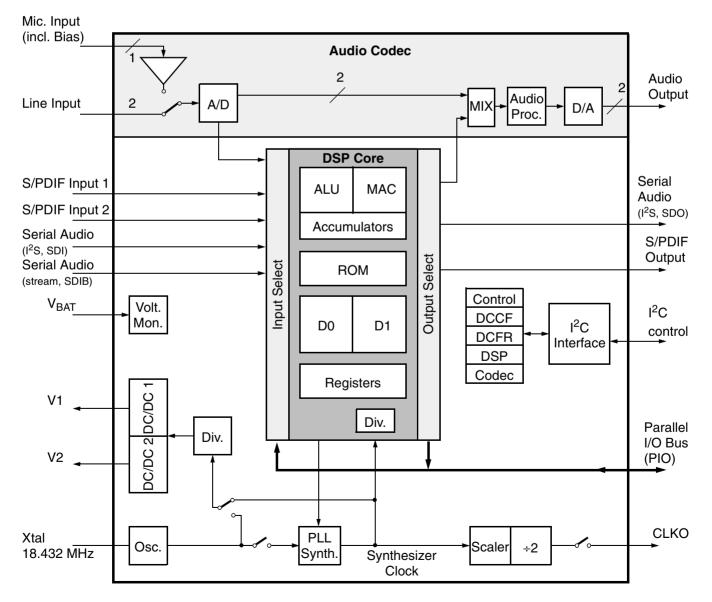


Fig. 2-1: The MAS 3587F architecture

#### 2.5. Firmware and Software

# 2.5.1. Internal Program ROM and Firmware, MPEG-Encoding/Decoding

The firmware implemented in the program ROM of the MAS 3587F provides MPEG 1/2 Layer 3 encoding and decoding of MPEG 1/2 Layer 2 and MPEG 1/2 Layer 3.

The DSP operating system starts the firmware in the "Application Selection Mode". By setting the appropriate bit in the Application Select memory cell (see Table 3–7 on page 28), the MPEG audio encoder or decoder can be activated.

The MPEG decoder provides an automatic standard detection mode. If all MPEG audio decoders are selected, the Layer 2 or Layer 3 bitstream is recognized and decoded automatically.

For general control purposes, the operation system provides a set of I<sup>2</sup>C instructions that give access to internal DSP registers and memory areas.

An auxiliary digital volume control and mixer matrix is applied to the digital stereo audio data. This matrix is capable of performing the balance control and a simple kind of stereo basewidth enhancement. All four factors LL, LR, RL, and RR are adjustable, please refer to Fig. 3–3 on page 39.

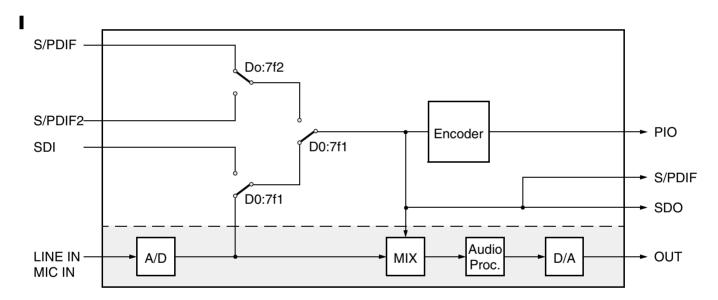


Fig. 2-2: Encoder Signal Flow (Reset setting shown)

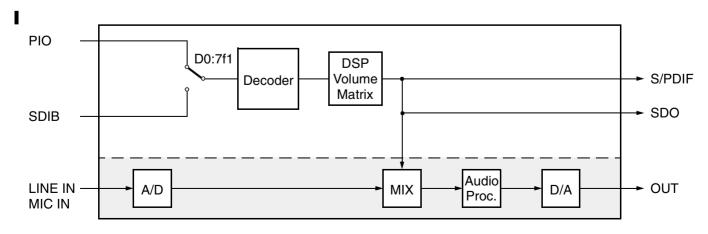


Fig. 2-3: Decoder Signal Flow (Reset setting shown)

#### 2.5.2. Program Download Feature

The standard functions of the MAS 3587F can be extended or substituted by downloading up to 4 kWords (1 Word = 20 bits) of program code and additionally up to 4 kWords of coefficients into the internal RAM.

The code must be downloaded by the *Fast Program Download* command (see Section 3.3.2.10. on page 26) into an area of RAM that is switchable from data memory to program memory. A *Run* command (see Section 3.3.2.1. on page 24) starts the operation.

#### 2.6. Audio Codec

A sophisticated set of audio converters and sound features has been implemented to comply with various kinds of operating environments that range up to highend equipment (see Fig. 2–4).

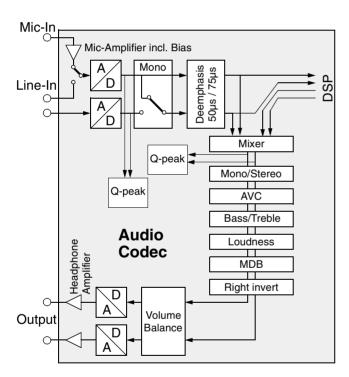


Fig. 2–4: Signal flow block diagram of the Audio Codec

#### 2.7. A/D Converter and Microphone Amplifier

A pair of A/D converters is provided for recording or loop-through purposes. In addition, a microphone amplifier including voltage supply function for an electret type microphone has been integrated.

#### 2.7.1. Baseband Processing

Several baseband functions are applied to the digital audio signal immediately before D/A conversion.

#### 2.7.1.1. Bass, Treble, and Loudness

Standard baseband functions such as bass, treble, and loudness are provided (refer to Table 3–17 for details).

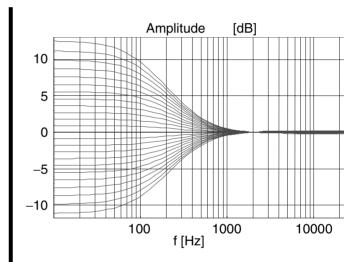


Fig. 2-5: Bass Frequency Response

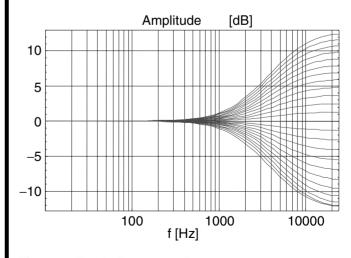


Fig. 2-6: Treble Frequency Response

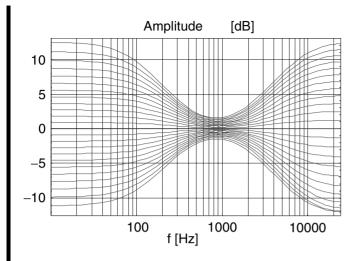


Fig. 2-7: Bass/Treble Frequency Response

#### 2.7.2. Micronas Dynamic Bass (MDB)

The Micronas Dynamic Bass system (MDB) was developed to extend the frequency range of loud-speakers or headphones below the cutoff frequency of the speakers. In addition to dynamically amplifying the low frequency bass signals, the MDB exploits the psychoacoustic phenomenon of the 'missing fundamental'. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental, while at the same time retaining the loudness of the original signal. Due to the parametric implementation of the MDB, it can be customized to create different bass effects and adapted to various loudspeaker characteristics (see Section 3.4.4. on page 46).

### 2.7.2.1. Automatic Volume Correction (AVC)

In a collection of tracks from different sources fairly often the average volume level varies. Especially in a noisy listening environment the user must adjust the volume to achieve a comfortable listening enjoyment. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see Table 3–17).

For input levels of -18 dBr to 0 dBr, the AVC maintains a fixed output level of -9 dBr. Fig. 2-8 shows the AVC output level versus its input level. For volume and baseband registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output.

#### ■ 2.7.2.2. Balance and Volume

To minimize quantization noise, the main volume control is automatically split into a digital and an analog part. The volume range is –114...+12 dB with an additional mute position. A balance function is provided (see Table 3–17).

#### 2.7.3. D/A Converters

A pair of Micronas' unique multibit sigma-delta D/A converters is used to convert the audio data with high linearity and a superior S/N. In order to attenuate high-frequency noise caused by noise-shaping, internal low-pass filters are included. They require additional external capacitors between pins FILTR and OUTR, and FILTL and OUTL respectively (see Section 4.7. on page 81).

#### 2.7.4. Output Amplifiers

The integrated output amplifiers are capable of driving stereo headphones of 16...32  $\Omega$  impedance via 22- $\Omega$  series resistors or built-in loudspeakers of 16  $\Omega$  impedance directly. If more output power is required, the right output signal can be inverted and a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this case the minimum impedance is 32  $\Omega$ , and for optimized power the source should be set to mono.

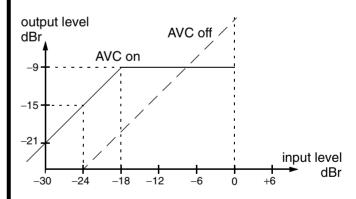


Fig. 2-8: Simplified AVC characteristics

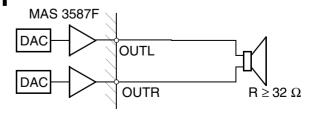


Fig. 2–9: Bridge operation mode

#### 2.8. Clock Management

The MAS 3587F is driven by a single crystal-controlled clock with a frequency of 18.432 MHz. It is possible to drive the MAS 3587F with other reference clocks. In this case, the nominal crystal frequency must be written into memory location D0:7F3. The crystal clock acts as a reference for the embedded synthesizer that generates the internal clock.

For compressed audio data reception, the MAS 3587F may act either as the clock master (Demand Mode) or as a slave (Broadcast Mode) as defined by bit 1 in IOControlMain memory cell (see Table 3–9). In both modes, the output of the clock synthesizer depends on the sample rate of the decoded data stream as shown in Table 2–1.

In the 'Broadcast Mode' (PLL on), the incoming audio data controls the clock synthesizer via a PLL.

In the 'Demand Mode' (PLL off) the MAS 3587F acts as the system master clock, the internal clock. The data transfer is triggered by a demand signal at pin EOD. This mode is used in most applications.

In the encoder application, the MAS 3587F is clock master in case of  $I^2S$  audio input. For S/PDIF input, the MAS 3587F synchronizes the clock to the incoming S/PDIF signal.

**Table 2–1:** Settings of bits 8 and 17 in OutClkConfig and resulting CLKO output frequencies

	Output Frequency at CLKO/MHz									
f <sub>s</sub> /kHz	Synth. Clock bit 8=1		er On bit 17=0		r Plus Division bit 17=1					
48	24.576	E40.f	24.576	0504	12.288					
44.1	22.5792	512·f <sub>s</sub>	22.5792	256·f <sub>s</sub>	11.2896					
32	04.570	768·f <sub>s</sub>	24.576	384·f <sub>s</sub>	12.288					
24	24.576	540.6	12.288	0504	6.144					
22.05	22.5792	512⋅f <sub>s</sub>	11.2896	256·f <sub>s</sub>	5.6448					
16	04.570	768·f <sub>s</sub>	12.288	384·f <sub>s</sub>	6.144					
12	24.576	E40 (	6.144	0501	3.072					
11.025	22.5792	512⋅f <sub>s</sub>	5.6448	256·f <sub>s</sub>	2.8224					
8	24.576	768·f <sub>s</sub>	6.144	384·f <sub>s</sub>	3.072					

#### 2.8.1. DSP Clock

The DSP clock has a separate divider. For power conservation it is set to the lowest acceptable rate of the synthesizer clock which is capable to allow the processor core to perform all tasks.

#### 2.8.2. Clock Output at CLKO

If the DSP or audio codec functions are enabled (bits 11 or 10 in the CONTROL Register at  $I^2C$  subaddress  $6A_{\text{hex}}$ ), the reference clock at pin CLKO is derived from the synthesizer clock.

Dependent on the sample rate of the decoded signal a scaler is applied which automatically divides the clock-out by 1, 2, or 4, as shown in Table 2–1. An additional division by 2 may be selected by setting bit 17 of the Output Clock Configuration memory cell, OutClkConfig (see Table 3–9 on page 30). The scaler can be disabled by setting bit 8 of this cell.

The controlling at OutClkConfig is only possible as long as the DSP is operational (bit 10 of the CONTROL Register). Settings remain valid if the DSP is disabled by clearing bit 10.

#### 2.9. Power Supply Concept

The MAS 3587F has been designed for minimal power dissipation. In order to optimize the battery management in portable players, two DC/DC converters have been implemented to supply the complete portable audio player with regulated voltages.

#### 2.9.1. Power Supply Regions

The MAS 3587F has five power supply regions.

The VDD/VSS pin pair supplies all digital parts including the DSP core, the XVDD/XVSS pin pair is connected to the digital signal pin output buffers, the AVDD0/AVSS0 supply is for the analog output amplifiers, AVDD1/AVSS1 for all other analog circuits like clock oscillator, PLL circuits, system clock synthesizer and A/D and D/A converters. The I<sup>2</sup>C interface has an own supply region via pin I2CVDD. Connecting this to the microcontroller supply assures that the I<sup>2</sup>C bus always works as long as the microcontroller is alive so that the operating modes can be selected.

Beside these regions, the DC/DC converters have start-up circuits of their own which get their power via pin VSENSx.

MAS 3587F PRELIMINARY DATA SHEET

#### 2.9.2. DC/DC Converters

The MAS 3587F has two embedded high-performance step-up DC/DC converters with synchronous rectifiers to supply both the DSP core itself and external circuitry such as a controller or flash memory at two different voltage levels. An overview is given in Fig. 2–10 on page 13.

The DC/DC converters are designed to generate an output voltage between 2.0 V and 3.5 V which can be programmed separately for each converter via the I<sup>2</sup>C interface (see Table 3–3 on page 20). Both converters are of the bootstrapped type which allow start up from a voltage down to 0.9 V for use with a single battery or NiCd/NiMH cell. The default output voltages are 3.0 V. Both converters are enabled with a high level at pin DCEN and enabled/disabled by the I<sup>2</sup>C interface.

The MAS 3587F DC/DC converters feature a constant-frequency, low noise pulse width modulation (PWM) mode and a low quiescent current, pulse frequency modulation (PFM) mode for improved efficiencies at low current loads. Both modes – PWM or PFM – can be selected independently for each converter via I<sup>2</sup>C interface. The default mode is PWM.

In the PWM mode, the switching frequency of the power-MOSFET-switches is derived from the crystal oscillator. Switching harmonics generated by constant frequency operation are consistent and predictable. When the audio codec is enabled the switching frequency of the converters is synchronized to the audio codec clock to avoid interferences into the audio band. The actual switching frequency can be selected via the I<sup>2</sup>C-interface between 300 kHz and 580 kHz (for details see DCFR Register in Table 3–3).

In the PFM operation mode, the switching frequency is controlled by the converters themselves, it will be just high enough to service the output load thus resulting in the best possible efficiency at low current loads. PFM mode does not need a clock signal from the crystal oscillator. If both converters do not use the PWM-mode, the crystal clock will be shut down as long it is not needed from other internal blocks.

The synchronous rectifier bypasses the external Schottky diode to reduce losses caused by the diode forward voltage providing up to 5% efficiency improvement. By default, the P-channel synchronous rectifier switch is turned on when the voltage at pin(s) DCSOn exceeds the converter's output voltage at pin(s) VSENSn and turns off when the inductor current drops below a threshold. If one or both converters are disabled, the corresponding P-channel switch will be turned on, connecting the battery voltage to the DC/DC converters output voltage at pin VSENSn.

If both DC/DC-converters are off, a high signal may be applied at pin DCEN. This will start the converters in their default mode (PWM with 3.0 V output voltage). The PUP signal will change from low to high when both converters have reached their nominal output voltage and will return to low when both converters output voltages have dropped 200 mV below their programmed output voltage. The signal at pin PUP can be used to control the reset of an external microcontroller (see Section 2.13.2. on page 16 for details on start up procedure).

If only DC/DC-converter 1 is used, the output of the unused converter 2 (VSENS2) must be connected to the output of converter 1 (VSENS1) to make the PUP signal work properly. Also, if a DC/DC-converter is not used (no inductor connected), the pin DCSO must be left vacant.

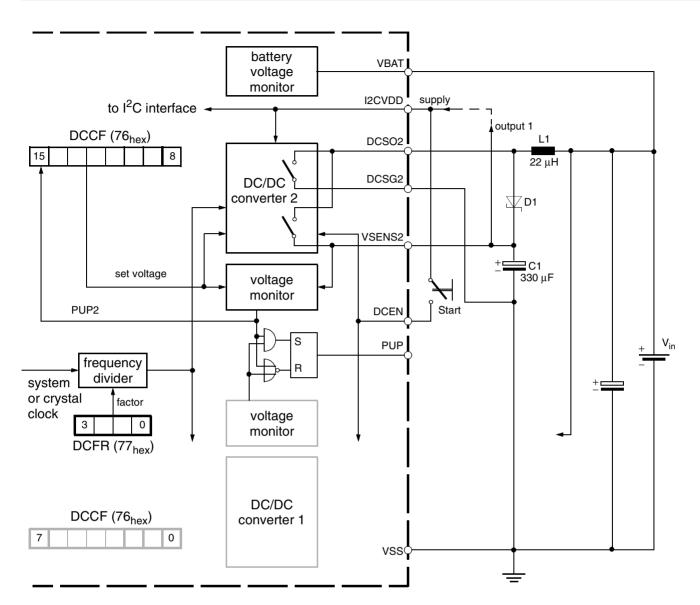


Fig. 2–10: DC/DC converter overview (DCEN input must be connected to pin I2CVDD via the start-up push button)

#### 2.9.3. Power Supply Configurations

One of the following supply configurations may be used:

- Configuration 1: DC/DC 1 (e.g. 2.7 V) supplies controller, flash and MAS 3587F audio parts, DC/DC 2 generates e.g. 2.5 V/3.5 V for the MAS 3587F DSP (see Fig. 2–11).
- Configuration 2: All components are powered by an external source, no DC/DC converter is used (see Fig. 2–12).
- Configuration 3: The external source has a constant voltage of 2.7 V or 3 V, one DC/DC-converter is used to generate the higher DSP-Voltage needed for encoding (see Fig. 2–13)

If DC/DC converter 1 is used, it must supply the analog circuits (pins AVDD0, AVDD1) of the MAS 3587F.

If the DC/DC converters are not used, pin DCEN must be connected to VSS, DCSOx must be left vacant.

# VSENS1 DC/DC1 Flash I<sup>2</sup>CVDD I<sup>2</sup>C μС XVDD DSP VDD VSENS2 DC/DC2 External Supply AVDD0/1 Analog e.g. 3.5 V Parts 2.7 V

Fig. 2-12: Configuration 2: External power supply

#### 2.10. Battery Voltage Supervision

A battery voltage supervision circuit (at pin VBAT) is provided which is independent of the DC/DC converters. It can be programmed to supervise one or two battery cells. The voltage is measured by subsequently setting a series of voltage thresholds and checking the respective comparison result in register 77<sub>hex</sub> (see Table 3–3).

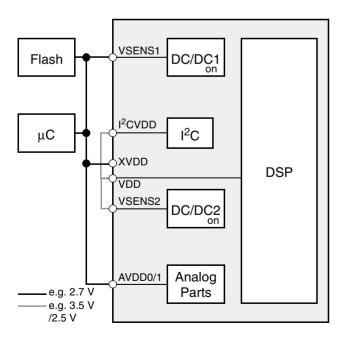


Fig. 2-11: Configuration1: DC/DC-converter supply

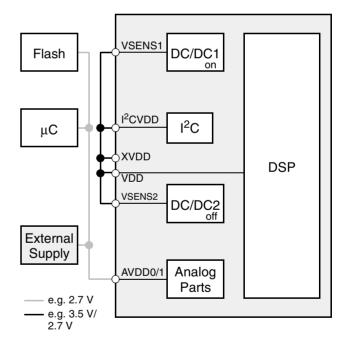


Fig. 2–13: Configuration 3: External constant power supply

#### 2.11. Interfaces

The MAS 3587F uses an I<sup>2</sup>C control interface, a parallel I/O interface (PIO) for MPEG bit streams and digital audio interfaces for the incoming/outgoing audio data (I<sup>2</sup>S or similar). Alternatively, SPDIF input and output interfaces can be used. MPEG bit stream input to the decoder is also possible via a second serial input interface.

#### 2.11.1. I<sup>2</sup>C Control Interface

For controlling and program download purposes, a standard  $I^2C$  slave interface is implemented. A detailed description of all functions can be found in Section 3.

#### 2.11.2. S/PDIF Input Interface

The S/PDIF interface receives a one-wire serial bus signal. In addition to the signal input pin SPDI1/SPDI2, a reference pin SPDIR is provided to support balanced signal sources or twisted pair transmission lines.

The synchronization time on the input signal is < 50 ms.

The S/PDIF input signal can also be switched to the SPDO pin. In this case the analog input circuit of the S/PDIF inputs (see Fig. 4–18 on page 55) restores the S/PDIF input signal to a full swing signal at SPDO.

For controlling details please refer to Table 3-9 on page 30.

# 2.11.3. S/PDIF Output

The S/PDIF output of the baseband audio signals is provided at pin SPDO.

Note that the S/PDIF output is available only for MPEG 1 sampling frequencies (32, 44.1, 48 kHz).

### 2.11.4. Multiline Serial Audio Input (SDI, SDIB)

There are two multiline serial audio input interfaces (SDI, SDIB) each consisting of the three pins SIC, SII, SID, and SIBC, SIBI, SIBD. The firmware supports SDI for audio signals and SDIB for bitstream signals.

The interfaces can be configured as continuous bit stream or word-oriented inputs. For the MPEG bit-streams the word strobe pin SIBI must always be connected to  $V_{SS}$ , bits must be sent MSB first as created by the encoder. During enabling the DSP and its interfaces, it is strongly recommended to hold the SIBC Pin low.

In case of the Demand Mode in decoding applications (see Section 2.8.), the signal clock coming from the data source must be higher than the nominal data transmission rate (e.g. 128 kbit/s). Pin EOD is used to interrupt the data flow whenever the input buffer of the MAS 3587F is filled.

For controlling details please refer to Table 3–9.

# 2.11.5. Multiline Serial Output (SDO)

The serial audio output interface of the MAS 3587F is a standard I<sup>2</sup>S-like interface consisting of the data lines SOD, the word strobe SOI and the clock signal SOC. It is possible to choose between two standard interface configurations (16-bit data words with word strobe time offset or 32-bit data words with inverted SOI-signal).

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default.

### 2.11.6. Parallel Input/Output Interface (PIO)

The parallel interface of the MAS 3587F consists of the 8 data lines PI12...PI19 (MSB) and the control lines PCS, PR, PRTR, PRTW, and EOD. It can be used for data exchange with an external memory and for other special purposes as defined by the DSP software.

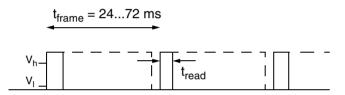
The PIO interface is always used for MPEG-data output. For the handshake protocol please refer to Section 4.6.3.8.

For MPEG-data input, the PIO interface is activated by setting bits 9,8 in D0:7F1 to 01. For the handshake protocol please refer to Section 4.6.3.6.

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#### 2.12. MPEG Synchronization Output

The signal at pin SYNC is set to '1' after the internal decoding for the MPEG header has been finished for one frame. The rising edge of this signal can be used as an interrupt input for the controller that triggers the read out of the control information and ancillary data. As soon as the MAS 3587F has received the SYNC reset command (see Section 3.3.2.8. on page 26), the SYNC signal is cleared. If the controller does not issue a reset command, the SYNC signal returns to '0' as soon as the decoding of the next MPEG frame is started. MPEG status and ancillary data become invalid until the frame is completely decoded and the signal at pin SYNC rises again. The controller must have finished reading all MPEG information before it becomes invalid. The MPEG Layer 2/3 frame lengths are given in Table 2-2.



**Fig. 2–14:** Schematic timing of the signal at pin SYNC. The signal is cleared at t<sub>read</sub> when the controller has issued a Clear SYNC Signal command (see Section 3.3.2.8. on page 26). If no command is issued, the signal returns to '0' just before the decoding of the next MPEG frame.

Table 2-2: Frame length in MPEG Layer 2/3

f <sub>s</sub> /kHz	Frame Length Layer 2	Frame Length Layer 3
48	24 ms	24 ms
44.1	26.12 ms	26.12 ms
32	36 ms	36 ms
24	24 ms	24 ms
22.05	26.12 ms	26.12 ms
16	36 ms	36 ms
12	not available	48 ms
11.025	not available	52.24 ms
8	not available	72 ms

# 2.13. Default Operation

This sections refers to the standard operation mode "Configuration 1" (see Section 2.9.3.).

#### 2.13.1. Stand-by Functions

After applying the battery voltage, the system will remain stand-by, as long as the DCEN pin level is kept low. Due to the low stand-by current of CMOS circuits, the battery may remain connected to DCSOn/VSENSn at all times.

# 2.13.2. Power-Up of the DC/DC Converters and Reset

The battery voltage must be applied to pin DCSOn via the 22  $\mu$ H inductor and, furthermore, to the sense pin VSENSn via a Schottky diode (see Fig. 2–10 on page 13).

For start-up, the pin DCEN must be connected via an external "start" push button to the I2CVDD supply, which is equivalent to the battery supply voltage (> 0.9 V) at start-up.

The supply at DCEN must be applied until the DC/DC converters have started up (signal at pin PUP) and then removed for normal operation.

As soon as the output voltage at VSENSn reaches the default voltage monitor reset level of 3.0 V, the respective internal PUPn bit will be set. When both PUPn bits are set, the signal at pin PUP will go high and can be used to start and reset the microcontroller.

Before transmitting any  $I^2C$  commands, the controller must issue a power-on reset to pin POR. The separate supply pin  $I^2CVDD$  assures that the  $I^2C$  interface works independently of the DSP or the audio codec. Now the desired supply voltage can be programmed at  $I^2C$  subaddress  $76_{hex}$  (see Table 3–3).

The signal at pin PUP will return to low only when both PUPn flags ( $I^2C$  subaddress  $76_{hex}$ ) have returned to zero. Care must be taken when changing both DC/DC output voltages to higher values. In this case, both output voltages are momentarily insufficient to keep the PUPn flags up; the resulting dip in the signal at the PUP pin may in turn reset the microcontroller. To avoid this condition, only one DC/DC output voltage should be changed at a time. Before modifying the second voltage, the microcontroller must wait for the PUPn flag of the first voltage to be set again.

If only DC/DC converter 1 is used, the reference voltage of the second unused should be set to a lower value than that of converter 1 and its pin VSENS2 should be connected to VDD.

The operating mode (pulse width modulation or pulse frequency modulation) are controlled at  $I^2C$  subaddress  $76_{hex}$ , the operating frequency at  $I^2C$  subaddress  $77_{hex}$ .

#### 2.13.3. Control of the Signal Processing

Before starting the DSP, the controller should check for a sufficient voltage supply (respective flag PUPn at  $I^2C$  subaddress  $76_{hex}$ ). The DSP is enabled by setting the appropriate bit in the CONTROL register ( $I^2C$  subaddress  $6A_{hex}$ ). The nominal frequency of the crystal oscillator must be written into D0:7F3. After an initialization phase of 5 ms, the DSP data registers can be accessed via  $I^2C$  (see Table 3–3).

Input and output control is performed via memory location D0:7F1 and D0:7F2. The parallel interface (PIO) is the default setting for compressed data. The decoded audio can be routed to either the S/PDIF, the SDO and the analog outputs. The output clock signal at pin CLKO is defined in D0:7F4. The specific settings for audio encoding are written to memory location D0:7F0.

All changes in the D0-memory cells become effective synchronously upon setting the LSB of Main I/O Control D0:7F1 (see Table 3–9).

The common way to start encoding or decoding is to perform all necessary settings and switch on the application by selecting the desired bit(s) in the Application Selection memory cell (D0:7F6) (see Table 3–9).

The digital volume control (see Table 3–9) is applied to the output signal of the DSP. The decoded audio data is by default available at the S/PDIF output interface (for MPEG 1 sampling frequencies).

The DSP does not have to be started if its functions are not needed, e.g. for routing audio via the A/D and the D/A converters through the codec part of the IC.

#### 2.13.4. Start-up of the Audio Codec

Before enabling the audio codec, the controller should check for a sufficient voltage supply (respective flag PUPn at I<sup>2</sup>C subaddress 76<sub>hex</sub>).

The audio codec is enabled by setting the appropriate bit at the CONTROL register ( $I^2C$  subaddress  $6A_{hex}$ ). After an initialization phase of 5 ms, the DSP data registers can be accessed via  $I^2C$ . The A/D and the D/A converters must be switched on explicitly ( $00~00_{hex}$  at  $I^2C$  subaddress  $6c_{hex}$ ). The D/A converters may either accept data from the A/D converters or the output of the DSP, or a mix of both (register  $00~06_{hex}$  and  $00~07_{hex}$  at  $I^2C$  subaddress  $6C_{hex}$ ). Finally, an appropriate output volume ( $00~10_{hex}$  at  $I^2C$  subaddress  $6C_{hex}$ ) must be selected.

#### 2.13.5. Power-Down

All analog outputs should be muted and the A/D and the D/A converters must be switched off (register  $00\,10_{hex}$  and  $00\,00_{hex}$  at I<sup>2</sup>C subaddress  $6C_{hex}$ ). The DSP and the audio codec must be disabled (clear DSP\_EN and CODEC\_EN bits in the CONTROL register, I<sup>2</sup>C subaddress  $6A_{hex}$ ). By clearing both DC/DC enable flags in the CONTROL register (I<sup>2</sup>C subaddress  $6A_{hex}$ ), the microcontroller can power down the complete system.

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### 3. Controlling

# 3.1. I<sup>2</sup>C Interface

Controlling between the MAS 3587F and the external controller is done via an I<sup>2</sup>C slave interface.

#### 3.1.1. Device Address

The device addresses are  $3\text{C}/3\text{E}_{\text{hex}}$  (device write "DW") and  $3\text{D}/3\text{F}_{\text{hex}}$  (device read, "DR") as shown in Table 3–1. The device address pair  $3\text{C}/3\text{D}_{\text{hex}}$  applies if the DVS pin is connected to VSS, the device address pair  $3\text{E}/3\text{F}_{\text{hex}}$  applies if the DVS pin is connected to I2CVDD.

Table 3-1: I<sup>2</sup>C device address

A7	<b>A6</b>	<b>A</b> 5	<b>A</b> 4	А3	A2	A1	W/R
0	0	1	1	1	1	DVS	0/1

I<sup>2</sup>C clock synchronization is used to slow down the interface if required.

# 3.1.2. I<sup>2</sup>C Registers and Subaddresses

The interface uses one level of subaddresses. The MAS 3587F interface has 7 subaddresses allocated for the corresponding  $\rm I^2C$  registers. The registers can be divided into three categories as shown in Table 3–2.

The address  $6A_{\text{hex}}$  is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 3587F.

The  $I^2C$  registers of the MAS 3587F are 16 bits wide, the MSB is denoted as bit[15]. Transmissions via  $I^2C$  bus have to take place in 16-bit words (two byte transfers, MSB sent first); thus, for each register access, two 8-bit data words must be sent/received via  $I^2C$  bus.

Table 3-2: I<sup>2</sup>C Subaddresses

Sub- address (hex)	I <sup>2</sup> C- Register Name	Function							
Direct Configuration									
6A	CONTROL	Controller writes to MAS 3587F CONTROL register							
76	DCCF	Controller writes to first DC/DC configuration register							
77	DCFR	Controller writes to second DC/DC configuration register							
DSP Core	e Access								
68	data_write	Controller writes to MAS 3587F DSP							
69	data_read	Controller reads from MAS 3587F DSP							
Codec A	ccess								
6C	codec_write	Controller writes to MAS 3587F codec register							
6D	codec_read	Controller reads from MAS 3587F codec regis- ter							

#### 3.1.3. Naming Convention

The description of the various controller commands uses the following formalism:

- **Abbreviations** used in the following descriptions:
  - a address
  - d data value
  - n count value
  - o offset value
  - r register number
  - x don't care
- Memory addresses like D1:89F are always in hexadecimal notation.
- A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.
- Data values in nibbles are always shown in hexadecimal notation.
- A hexadecimal 20-bit number **d** is written, e.g. as  $\mathbf{d} = 17C63_{hex}$ , its five nibbles are  $d0 = 3_{hex}$ ,  $d1 = 6_{hex}$ ,  $d2 = C_{hex}$ ,  $d3 = 7_{hex}$ , and  $d4 = 1_{hex}$ .
- Variables used in the following descriptions:
   I<sup>2</sup>C address:

DW 3C/3E<sub>hex</sub> I<sup>2</sup>C device write DR 3D/3F<sub>hex</sub> I<sup>2</sup>C device read

DSP core:

data\_write 68<sub>hex</sub> DSP data write data\_read 69<sub>hex</sub> DSP data read

Codec:

codec\_write 6C<sub>hex</sub> codec write codec\_read 6D<sub>hex</sub> codec read

#### - Bus signals

S Start P Stop

A ACK = Acknowledge N NAK = Not acknowledge

W Wait =  $I^2C$  clock line is held low

while the MAS 3587F is processing the current I<sup>2</sup>C command

Symbols in the telegram examples

< Start Condition

> Stop
dd data bytes
xx ignore

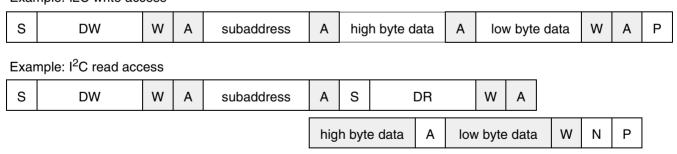
All telegram numbers are hexadecimal, data originating from the MAS 3587F are greyed.

Example:

<DW 68 dd dd > write data to DSP <DW 69 <DR dd dd > read data from DSP

Fig. 3–1 shows I<sup>2</sup>C bus protocols for write and read operations of the interface; the read operations require an extra start condition and repetition of the chip address with the device read command (DR). Fields with signals/data originating from the MAS 3587F are marked by a gray background. Note that in some cases the data reading process must be concluded by a NAK condition.

Example: I2C write access



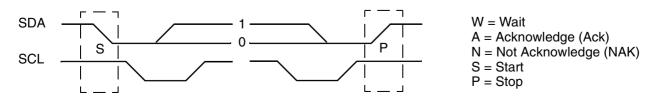


Fig. 3–1: Example of an I<sup>2</sup>C bus protocol for the MAS 3587F (MSB first; data must be stable while clock is high)

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# 3.2. Direct Configuration Registers

The task selection of the DSP and the DC/DC converters are controlled in the direct configuration registers CONTROL, DCCF, and DCFR.

# 3.2.1. Write Direct Configuration Registers

S	DW	W	Α	subaddr.	Α	d3,d2	Α	d1,d0	Α	Р	
---	----	---	---	----------	---	-------	---	-------	---	---	--

The write protocol for the direct configuration registers only consists of device address, subaddress and one 16-bit data word.

# Table 3-3: Direct Configuration Registers

# 3.2.2. Read Direct Configuration Register

S	DW	W	Α	subaddr.	Α	S	D	R	W	Α		
						d3	,d2	Α	d1,	,d0	Ν	Р

To check the PUP1 and PUP2 power-up flags, it is necessary to read back the content of the direct configuration registers.

I <sup>2</sup> C Sub- address (hex)	Function		Name
6A	Control Re	egister (reset value = 3000 <sub>hex</sub> )	CONTROL
	bit[15:14]	Analog supply voltage range	
		Code         AGNDC         recommended for voltage range of AVDD           00         1.1 V         2.0 2.4 V (reset)           01         1.3 V         2.4 3.0 V           10         1.6 V         3.0 3.6 V           11         reserved	
	Higher volta noise ratio.	age ranges permit higher output levels and thus a better signal-to-	
	bit[13] bit[12]	Enable DC/DC 2 (reset = 1) Enable DC/DC 1 (reset = 1)	
	Both DC/D	C converters are switched on by default with DCEN = high (1).	
	bit[11] bit[10]	Enable and reset audio codec Enable and reset DSP core	
	core and th The DSP c the analog	operation (MPEG-decoding and D/A conversion), both, the DSP ne audio codec have to be enabled after the power-up procedure. It is an audio signal is routed from the analog inputs to outputs (set bit[15] in codec register 00 0F <sub>hex</sub> ). The audio codec off if the DSP uses digital inputs and outputs only.	
	bit[9] bit[8]	Reset codec Reset DSP core	
	bit[7]	Enable crystal input clock divider of 1.5 (extended range up to 28 MHz) <sup>1)</sup>	
	bit[6:0]	Reserved, must be set to zero	
	1) refer to T	Table 4–2 on page 58	

Table 3–3: Direct Configuration Registers, continued

I <sup>2</sup> C Sub- address (hex)	ldress					
76	DCCF Reg	DCCF				
	DC/DC Co	nverter 2				]
	bit[15]					
	bit[14:11]	Converter	2 output volta	ge with resp	ect to VREF	
		Code 1111 1110	Nominal output volt. 3.5 V 3.4 V	3.4 V 3.3 V	reset level of PUP2 3.3 V 3.2 V	
		1101 1100 1011 1010 1001	3.3 V 3.2 V 3.1 V 3.0 V 2.9 V	3.2 V 3.1 V 3.0 V 2.9 V 2.8 V	3.1 V 3.0 V 2.9 V 2.8 V (reset) 2.7 V	
		1000 0111 0110 0101 0100 <sup>1)</sup> 0011 <sup>1)</sup>	2.8 V 2.7 V 2.6 V 2.5 V 2.4 V 2.3 V	2.7 V 2.6 V 2.5 V 2.4 V 2.3 V 2.2 V	2.6 V 2.5 V 2.4 V 2.3 V 2.2 V 2.1 V	
	bit[10]	0010 <sup>1)</sup> Mode 1 0	2.2 V  pulse freque pulse width		2.0 V ation (PFM) (PWM) (reset)	
	bit[9:8]	Reserved	, must be set to	o zero	, , ,	
		n the selecte			nus, if the battery voltage is put voltage will exceed the	
	1) refer to S	Section 4.6.2	2. on page 57			
	DC/DC Co	nverter 1				
	bit[7]	PUP1: Vo	Itage monitor 1	l flag (readb	ack)	
	bit[6:3]	Converter (see bits 1		ge at VSEN	S1 with respect to VREF	
	bit[2]	Mode 1 0	pulse freque		ation (PFM) (PWM) (reset)	
	bit[1:0]	Reserved	, must be set to	o zero		
	main refere	ence source	supplied via p	in AVDD1. 7	erter 1 is derived from the herefore, if this DC/DC cone analog supply.	
	The DC/D0 higher than nominal vo					

Table 3-3: Direct Configuration Registers, continued

I <sup>2</sup> C Sub- address (hex)	Function					Name
77	DCFR Reg	<b>jister</b> (reset	= 00 <sub>hex</sub> )			DCFR
	Battery Vo	ltage Monit	or			
	bit[15]					
	bit[14]	Number o 0 1		ls nge 0.81.5 \ ange 1.63.0		
	bit[13:10]	Voltage th  1111 1110 0010 0001 0000	reshold leve 1 cell 1.5 1.45 0.85 0.8 battery ve	2 cells 3.0 V 2.9 V 1.7 V 1.6 V	ision off (reset)	
	bit[9:8]	Reserved	, must be se	t to 0		
		is stable 1 m olds is neglig		oling. The setu	ıp time for switching between	n
					tage monitor should be e measurement is completed	d.
	DC/DC Co					
	bit[7:4]	Reserved	, must be se	t to 0		
	bit[3:0]	Frequency	y of DC/DC	converter		
	address 6A from the cr	A <sub>hex</sub> is zero). ystal freque	315.1 323.4 332.1 341.3 351.1 361.4 372.4 384.0 396.4 409.6 423.7 438.9 455.1 472.6 491.5 512.0 ot enabled (k	or the DC/DC I 18.432 MHz	18.432 MHz 297.3 kHz 307.2 kHz 317.8 kHz 329.1 kHz 341.3 kHz 354.5 kHz 368.6 kHz 384.0 kHz (reset) 400.7 kHz 418.9 kHz 438.9 kHz 460.8 kHz 512.0 kHz 512.0 kHz 576.0 kHz ONTROL register at I <sup>2</sup> C-sub converters is directly derived on the converters of the synthesize e respective column in	t l

#### 3.3. DSP Core

#### 3.3.1. Access Protocol

The I<sup>2</sup>C data register is used to communicate with the internal firmware of the MAS 3506D. It is readable (subaddress "data\_read") and writable (subaddress "data\_write") and also has a length of 16 bits. The data transfer is done with the most significant bit (m) first.

Table 3-4: Data register bit assignment

15	14	13	12	11	10	09	80	07	06	05	04	03	02	01	00
m															-

A special command language is used that allows the controller to access the DSP-registers and RAM-cells and thus monitor internal states, set the parameters for the DSP-firmware, control the hardware, and even provide a download of alternative software modules. The DSP-commands consist of a "Code" which is sent to I<sup>2</sup>C-data register together with additional parameters.



Fig. 3-2: General core access protocol

Table 3–5 on page 24 gives an overview over the different commands which the DSP Core receives via the I<sup>2</sup>C data register. The "Code" is always the first data nibble transmitted after the "data\_write" subaddress byte. A second auxiliary code nibble is used for the short memory (16-bit) access commands.

The MAS 3587F firmware scans the I<sup>2</sup>C interface periodically and checks for pending or new commands.

The commands are then executed by the DSP during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. However, due to some time critical firmware parts, a certain latency time for the response has to be expected at the locations marked with a "W" (= wait). The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms.

Due to the 16-bit width of the  $I^2C$  data register, all actions transmit telegrams with multiples of 16 data bits.

#### 3.3.2. Data Formats

The internal data word size is 20 bits. All RAM-addresses can be accessed in a 20-bit mode via I<sup>2</sup>C-bus. Because of the 16-bit width of the I<sup>2</sup>C-data register the full transfer of all 20 bits requires two 16-bit I<sup>2</sup>C-words. Some commands only access the lower 16 bits of a cell. For fast access of internal DSP-states the processor core also has an address space of 256 data registers.

The internal data format is a 20 bit two's complement denoted "r". If in some cases a fixed point notation "v" is necessary. The conversion between the two forms of notation is done as follows:

 $\begin{array}{l} r = v^*524288.0 + 0.5; \ (-1.0 \le v < 1.0) \\ v = r/524288.0; \ (-524288 < r < 524287) \end{array}$ 

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Table 3-5: Basic controller command codes

Code (hex)	Command	Function
03	Run	Start execution of an internal program. <i>Run</i> with start address 0 means freeze the operating system.
5	Read Ancillary Data	The controller reads a block of MPEG Ancillary Data from the MAS 3587F
6	Fast Program Download	The controller downloads custom software via the PIO interface
7	Read IC Version	The controller reads the version information of the IC
Α	Read from Register	The controller reads an internal register of the MAS 3587F
В	Write to Register	The controller writes an internal register of the MAS 3587F
С	Read D0 Memory	The controller reads a block of the DSP memory
D	Read D1 Memory	The controller reads a block of the DSP memory
Е	Write D0 Memory	The controller writes a block of the DSP memory
F	Write D1 Memory	The controller writes a block of the DSP memory

# 3.3.2.1. Run and Freeze (Codes $0_{\text{hex}}$ to $3_{\text{hex}}$ )

												_
												ı
_	DIM	14/		4-444-		a3,a2		-4 -0	141		_	ı
5	D V V	VV	I A	idata write	A	a3.a2	I A	ı aı.a∪	VV	А	l P	П
_						,		, , , , , , ,				

The *Run* command causes the start of a program part at address  $\mathbf{a} = (a3,a2,a1,a0)$ . Since nibble a3 is also the command code (see Table 3–5), it is restricted to values between 0 and 3. This command is used to start alternate code or downloaded code from a RAM-area that has been configured as program RAM.

If the start address is  $1000_{\text{hex}} \le \mathbf{a} < 3\text{FFF}_{\text{hex}}$  and the respective RAM area has been configured as program RAM (see Table 3–7 on page 28), the MAS 3587F continues execution with a custom program already downloaded to this area.

Example 1: Start program execution at address  $345_{\text{hex}}$ :

<DW 68 03 45>

Example 2: Start execution of a downloaded code at address  $1000_{\text{hex}}$ :

<DW 68 10 00>

Freeze is a special run command with start address 0. It suspends all normal program execution. The operating system will enter an idle loop so that all registers and memory cells can be watched. This state is useful for operations like downloading code or contents of memory cells because the internal program cannot overwrite these values. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 3587F.

Freeze has the following I<sup>2</sup>C protocol:

<DW 68 00 00>

The entry point of the default software will be accessed automatically after a reset, thus issuing a *Run* or *Freeze* command is only necessary for starting downloaded software or special program modules which are not part of the standard set.

# 3.3.2.2. Read Register (Code Ahex)

# 1) send command

S	DW	W	Α	data_	_write	Α	A,	r1	Α	r0	,0	W	Α	Р
2) g	2) get register value													
S	DW	W	Α	data_	_read	Α	s	D	R	W	Α			
	x,x	Α	х,	d4	W	Α	d3,	d2	Α	d1	,d0	W	Ν	Р

The MAS 3587F has an address space of 256 DSPregisters. Some of the registers ( $\mathbf{r} = r1, r0$  in the figure above) are direct control inputs for various hardware blocks, others control the internal program flow. In Table 3-7, the registers of interest are described in detail. In contrast to memory cells, registers cannot be accessed as a block but must always be addressed individually.

# Example:

Read the content of register C8<sub>hex</sub>:

<dw 68<="" th=""><th>ac 80&gt;</th><th>define register</th></dw>	ac 80>	define register
<dw 69<="" td=""><td><dr dd="" xd="" xx=""></dr></td><td>and read</td></dw>	<dr dd="" xd="" xx=""></dr>	and read

# 3.3.2.3. Write Register (Code Bhex)

s	DW	W	Α	data_write	Α	B,r1	Α	r0,d4	W	Α	
						d3,d2	Α	d1,d0	W	Α	Р

The controller writes the 20-bit value ( $\mathbf{d} = d4, d3, d2$ , d1,d0) into the MAS 3587F register ( $\mathbf{r} = r1,r0$ ). A list of registers needed for control purposes is given in Table 3–7.

Example: Writing the value 81234<sub>hex</sub> into the register with the number AA<sub>hex</sub>:

<DW 68 ba a8 12 34>

# 3.3.2.4. Read Memory (Codes C<sub>hex</sub> and D<sub>hex</sub>)

The MAS 3587F has 2 memory areas of 2048 words denoted D0 and D1. The memory areas D0 and D1 can be written by using the codes  $C_{hex}$  and  $D_{hex}$ , respectively.

#### 1) send command (Read D0)

S	DW	W	Α	data_write	Α	<b>C</b> ,0	Α	0,0	W	Α	
						n3,n2	Α	n1,n0	W	Α	
						a3,a2	Α	a1,a0	w	Α	Р
2) g	get regis	ter v	alue	)							

-/ 5	get register value													
s	DW	W	Α	data_read		Α	s	D	R	w	Α			
	x,x	Α	χ,	d4	W	Α	d3	,d2	Α	d1,	d0	W	Α	
				repeat			n da	ıta v	alue	s				
	x,x	Α	χ,	d4	W	Α	d3	,d2	Α	d1,	d0	W	N	Р

The Read D0 Memory command gives the controller access to all 20 bits of the D0/D1 memory cells. The telegram to read 3 words starting at location D1:100 is

# 3.3.2.5. Short Read Memory (Codes C4hex and D4<sub>hex</sub>)

Because most cells in the user interface are only 16 bits wide, it is faster and more convenient to access the memory locations with a special 16 bit mode for reading:

#### 1) send command (e.g. Short Read D0)

s	DW	W	Α	data_write	Α	C,4	Α	0,0	W	Α	
						n3,n2	Α	n1,n0	w	Α	
						a3,a2	Α	a1,a0	W	Α	Р

#### 2) get register value



....repeat for n data values

٠.	Tradia varaco									
	d3,d2	Α	d1,d0	W	N	Р				

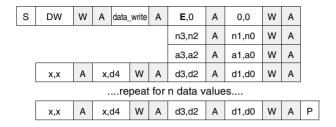
This command is similar to the normal 20 bit read command and uses the same command code  $C_{\text{hex}}$  and D<sub>hex</sub> for D0 and D1-memory, respectively, however it is followed by a  $4_{hex}$  rather than a  $0_{hex}$ .

Example: Read 16 bits of D1:123 has the following I<sup>2</sup>C protocol:

<dw 00<="" 68="" d4="" th=""><th>read 16 bits from D1</th></dw>	read 16 bits from D1
00 01	1 word to be read
01 23	start address
<dw 69="" dr<="" th=""><th>start reading</th></dw>	start reading
dd dd >	and read

# 3.3.2.6. Write Memory (Codes $E_{hex}$ and $F_{hex}$ )

The memory areas D0 and D1 can be written by using the codes  $E_{hex}$  and  $F_{hex}$ , respectively.



With the *Write D0/D1 Memory* command n 20-bit memory cells in D0 can be initialized with new data.

Example: Write 80234<sub>hex</sub> to D1:456 has the following I<sup>2</sup>C protocol:

<3a 68 f0 00	write D1 memory
00 01	1 word to write
04 56	start address
00 08	$value = 80234_{hex}$
02 345	

# 3.3.2.7. Short Write Memory (Codes $E4_{hex}$ and $F4_{hex}$ )

S	DW	W	Α	data_write	Α	E,4	Α	0,0	W	Α	
				"	Α	n3,n2	Α	n1,n0	W	Α	
					Α	a3,a2	Α	a1,a0	W	Α	
					Α	d3,d2	Α	d1,d0	W	Α	
repeat for n data values											
					Α	d3,d2	Α	d1,d0	W	Α	

For faster access only the lower 16 bits of each memory cell are written. The 4 MSBs of the cell are cleared. The command uses the same codes  $E_{\text{hex}}$  and  $F_{\text{hex}}$  for D0/D1 as for the 20-bit command but followed by a 4 rather than a 0.

#### 3.3.2.8. Clear SYNC Signal (Code 5<sub>hex</sub>)

S	DW	w	Δ	data write	Δ	5.0	Δ	0.0	w	Δ	Р
0	D * *	**		data_wiito		3,0	^	0,0	**		٠.

After a successful decoding of an MPEG frame the signal at pin SYNC rises and thus generates an interrupt event for the microcontroller. Issuing this command lets the signal at pin SYNC return to '0'.

#### 3.3.2.9. Default Read

The *Default Read* command is the fastest way to get information from the MAS 3587F. Executing the *Default Read* in a polling loop can be used to detect a special state during decoding.



The *Default Read* command immediately returns the lower 16 bit content of a specific RAM location as defined by the pointer D0:FFB. The pointer must be loaded before the first *Default Read* action occurs. If the MSB of the pointer is set, it points to a memory location in D1 rather than to one in D0.

Example: For watching D1:123 the pointer D0:FFB must be loaded with 8123<sub>hex</sub>:

<dw 6<="" th=""><th>8 e</th><th>00</th><th>write to D0 memory</th></dw>	8 e	00	write to D0 memory
0	0 01	_	1 word to write
0	f fk		start address ffb
0	0 08	3	value = 8
0	1 23	3 >	0123 <sub>hex</sub>

Now the *Default Read* commands can be issued as often as desired:

<dw< th=""><th></th><th></th><th></th><th></th><th></th><th>Default Read command 16 bit content of the</th></dw<>						Default Read command 16 bit content of the
dd dd >					address as defined by the	
						pointer
<dw< td=""><td>69</td><td><dr< td=""><td>dd</td><td>dd</td><td>&gt;</td><td> and do it again</td></dr<></td></dw<>	69	<dr< td=""><td>dd</td><td>dd</td><td>&gt;</td><td> and do it again</td></dr<>	dd	dd	>	and do it again

#### 3.3.2.10. Fast Program Download (Code 6<sub>hex</sub>)

s	DW	W	Α	data_write	Α	<b>6</b> ,n2	Α	n1,n0	W	Α	
						a3,a2	Α	a1,a0	W	Α	Р

The Fast Program Download command introduces a data transfer via the parallel port.  $\mathbf{n} = \text{n2,n1,n0}$  denotes the number of 20-bit data words to be transferred,  $\mathbf{a} = \text{a3,a2,a1,a0}$  gives the start address. The data must be organized in two times five nibbles to get two words of 20-bit length. If the number n of 20-bit data words is odd, the very last word has to be padded with one additional nibble.

The download must be initiated in the following order:

- Issue Freeze command
- Stop all DMA-transfers
- Issue Fast Program Download command
- Download code via PIO-interface
- Switch appropriate memory area to act as program RAM (register ed<sub>hex</sub>)
- Issue a Run command to start program execution at entry point of downloaded code

Example for *Fast Program Download* command: Download 5 words starting at D0:800, then download 4 words starting at D1:200:

<dw< th=""><th>68</th><th>00</th><th>00&gt;</th><th>&gt;</th><th>Freeze</th></dw<>	68	00	00>	>	Freeze
<dw< th=""><th>68</th><th>b3</th><th>b0</th><th>03</th><th>18&gt;Stop all internal transfers</th></dw<>	68	b3	b0	03	18>Stop all internal transfers
<dw< th=""><th>68</th><th>b4</th><th>30</th><th>03</th><th>00&gt;</th></dw<>	68	b4	30	03	00>
<dw< th=""><th>68</th><th>b4</th><th>b0</th><th>00</th><th>00&gt;</th></dw<>	68	b4	b0	00	00>
<dw< th=""><th>68</th><th>b5</th><th>30</th><th>03</th><th>18&gt;</th></dw<>	68	b5	30	03	18>
<DW	68	b6	b0	00	00>
<DW	68	bb	b0	03	18>
<DW	68	bc	30	03	00>
<DW	68	b0	60	00	00>
<dw< th=""><th>68</th><th>60</th><th>05</th><th></th><th>initiate download of 5 words</th></dw<>	68	60	05		initiate download of 5 words
	08	00:	>		start at address D0:800

# Now transfer 5 20-bit words via the parallel PIO-port:

d4,d3	d2,d1	d0,d4	d3,d2	d1,d0	
d4,d3	d2,d1	d0,d4	d3,d2	d1,d0	
d4,d3	d2,d1	d0,x			
<dw 68<="" td=""><td>60 05</td><td>ir</td><td>nitiate dow</td><td>nload of 4 w</td><td>ords</td></dw>	60 05	ir	nitiate dow	nload of 4 w	ords

Now transfer 4 20-bit words via the parallel PIO-port:

82 00>

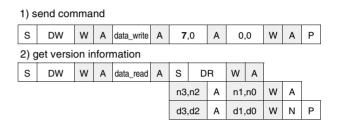
start at address D1:200

d4,d3 d4,d3	d2,d1 d2,d1	d0,d4 d0,d4	d3,d2 d3,d2	d1,d0 d1,d0	
<dw 68<="" td=""><td>b6 bc</td><td></td><td>0:800</td><td>memory ar D0:FFF froi gram usag</td><td>m</td></dw>	b6 bc		0:800	memory ar D0:FFF froi gram usag	m
<dw 68<="" td=""><td>10 0a</td><td></td><td>tart progra</td><td>am executio 0:100a</td><td>on at</td></dw>	10 0a		tart progra	am executio 0:100a	on at

#### 3.3.2.11. Serial Program Download

Program downloads may also be performed via the I<sup>2</sup>C-interface by using the *Write D0/D1 Memory* commands. A similar command sequence as in the Fast Program Download (*Freeze*, stop transfers...) applies.

# 3.3.2.12. Read IC Version (Code 7<sub>hex</sub>)



With this command the version of the IC is read in two 16 bit words. The first word  $\mathbf{n} = n3,n2,n1,n0$  contains the IC's major number (one nibble for each digit). The second word ( $\mathbf{d} = d3,d2,d1,d0$ ) returns the version as shown in Table 3–6.

Table 3-6: Second word of version information

Bit	Nibble	Content
15:12	d3	IC family derivate
11:8	d2	Coded character of order version (add 41 <sub>hex</sub> to the content of d2 to get ASCII)
7:0	d1,d0	Digit of order version

### Example:

Read the version information for MAS 3587F, derivate 0, order version B2:

<dw 00<="" 68="" 70="" th=""><th>send version command</th></dw>	send version command
<dw 69="" <dr<="" th=""><th>and read</th></dw>	and read
35 87	MAS3587
01 02 >	derivate 0, version B2

MAS 3587F PRELIMINARY DATA SHEET

#### 3.3.3. List of DSP Registers

Table 3–7 lists the registers used in the standard firmware (MPEG) and for the download option (Download).

**Note:** Registers not given in the tables must not be written.

# 3.3.4. List of DSP Memory Cells

Among the user interface control memory cells there are some which have a global meaning and some which control application specific parts of the DSP core. In the tables below this is reflected by the mode keywords All, Encoder and Decoder. The operation mode is chosen in the AppSelect cell.

# 3.3.4.1. Application Selection and Application Running

The AppSelect cell is a global user interface configuration cell which has to be written in order to start a specific application. The AppRunning cell is a global user interface status cell, which indicates, which application loop is actually running.

Following steps have to be performed to switch between applications:

- 1. Write "0" to AppSelect
- 2. Check AppRunning for "0"
- 3. For encoder (version B2 only):
- write 98<sub>hex</sub> to register a3<sub>hex</sub>
- write FFFFF<sub>hex</sub> to register 94<sub>hex</sub>
- write 0 to D1:000
- write 90<sub>hex</sub> to register A3<sub>hex</sub>
- 4. Apply necessary/wanted control settings (D0: 7F0..7FF)
- 5. Write value to AppSelect according to Table 3–8 (determines start time of Application program)

Table 3-7: DSP Register Table

Address (hex)	R/W	Function Mode	Default (hex)	Name
6B	R/W	Affected RAM area bit[19] D0:800 D0:BFF bit[18] D0:c00 D0:FFF bit[17] D1:800 D1:BFF bit[16] D1:c00 D1:FFF  This register is used to switch four RAM areas from data to program usage and thus enabling the DSP's program counter to access downloaded program code stored at these locations. For normal operation (firmware in ROM) this register must be kept to zero.  For details of program code download please refer to Section 3.3.2.10. on page 26	0000	PSelect_Shadow
56	R	S/PDIF <sup>1)</sup> Input Channel Status Bits MPEG bit[15:0] channel status bits of incoming signal.  1) IEC 958 Amendment1, "Digital Audio Interface"	0000	SPIChannelStatus

# 3.3.4.2. Application Specific Control

The configuration of the MPEG encoder and decoder firmware is done via the control memory cells described in Table 3–9. The changes applied to any of the control memory cells have to be validated by setting bit[0] of memory cell Main I/O Control except when the application is started by writing the AppSelect memory cell. The validate bit will be reset automatically after the changes have been taken over by the DSP.

The status memory cells are used to read the encoder/decoder status and to get additional MPEG bitstream information.

**Note:** Memory cells not given in the tables must not be written.

Table 3-8: D0 Memory Cells: Mode Selection

Memory Address (hex)	Function	IV	lode	Name			
D0:7F6	Applicatio	on Selection	AII	AppSelect			
	priate bit to ting AppSe feature will	AppSelect is used for selecting an application. This is done by setting the appropriate bit to one. It is principally allowed to set more than one bit to one, e.g. setting AppSelect to 0C <sub>hex</sub> will select all MPEG audio decoders. The auto-detection feature will automatically detect the Layer 2 or Layer 3 data. When bit[0]/bit[1] are asserted, the DSP begins to loop inside the OS loop/Top Level loop respectively.					
		It is recommended to perform the necessary settings for the firmware before the application is started by writing this memory cell.					
	bit[19:7]	Reserved, must be set to zero					
	bit[5:4]	Reserved, must be set to zero					
	bit[6] bit[3] bit[2]	MPEG Layer 3 Encoder MPEG Layer 3 Decoder MPEG Layer 2 Decoder					
	bit[1:0]	Reserved, must be set to zero					
D0:7F7	Applicatio	n Running	All	AppRunning			
	The AppRu application whether the in the confi						
	bit[19:7]	Reserved, must be set to zero					
	bit[5:4]	Reserved, must be set to zero					
	bit[6] bit[3] bit[2]	MPEG Layer 3 Encoder MPEG Layer 3 Decoder MPEG Layer 2 Decoder					
	bit[1:0]	Reserved, must be set to zero					

Table 3-9: D0 Control Memory Cells

Memory Address (hex)	Function				Mode	Name
D0:7F0 <sup>1)</sup>	Encoder Control (reset = A0264 <sub>hex</sub> ) Encoder					EncoderControl
	EncoderCo other option					
	bit[19:17]	000 001 010 011 100	ting (see Section 3.3.7 0 lowest bitrate/quali 1 2 3 4 5 recommended qua 6 7 highest bitrate/qua	lity		
	bit[16:12]	Reserved, ı	must be set to zero			
	bit[11:10]	Sampling F 00 (reset) 01 10 11	requency (kHz)	MPEG 1 44.1 48 32 reserved	MPEG 2 22.05 24 16	
	bit[9] Note that the	MPEG Sele 0 1 (reset) he clock frequ	ection MPEG 2 MPEG 1 ency (bit[3] in D0:7F1)	) must be set ac	cordingly.	
	Bit[11:9] ar	e only evalua	ted for SDI audio input out, MPEG 1 is used a	t (selected in D0	:7F1 <sup>1)</sup> , bit[9:8]). In	
	bit[8]	CRC protect 0 (reset) 1	ction enable CRC protecti disable CRC protecti			
	bit[7:6]	Channel Mo 00 01 (reset) 10 11	ode reserved joint stereo reserved single channel			
	bit[5]	Channel Mo 0 1 (reset)	ode Extension (for join disable MS-Stereo e enable MS-Stereo er	ncoding		
	bit[4]	Reserved, ı	must be set to zero			
	bit[3]	Copyright 0 (reset) 1	(see Section 3.3.5. o bit stream is not copy bit stream is copyrigh	yright protected		
	bit[2]	Copy/Origir 0 1 (reset)	nal (see Section 3.3.5. bit stream is a copy bit stream is an origi			
	bit[1:0]	Emphasis 00 (reset) 01 10 11	none 50/15 μs reserved CCITT J.17			

Table 3-9: D0 Control Memory Cells, continued

Memory Address (hex)	Function	Mode	Name	
D0:7F1 <sup>1)</sup>	Main I/O	IOControlMain		
	IOControl face and t coded aud SDIB. In t			
	bit[15] Reserved, must be set to zero			
	bit[14]	Invert seria 0 (reset) 1	I output clock (SOC) do not invert SOC invert SOC	
	bit[13]	Reserved,	must be set to zero	
	bit[12]	Encoder: A 0 (reset) 1	Add timecode to encoded bitstream no timecode is inserted insert timecode into ancillary data bits	
	The forma	at of the timeco	ode is explained in Section 3.3.7.1. on page 39	
	bit[11]	Serial data 0 (reset) 1	output delay no additional delay (reset) additional delay of data related to word strobe	
	bit[10]	Encoder: L 0 (reset) 1	Low power loop-through mode normal encoder operation audio data loop-through without encoding	
	ing and da	ata transfer to t (audio input/M	ough mode is for monitoring audio signals without encod- the PIO interface. It is controlled just like in normal encod- IPEG mode selection), but power consumption and e as in decoding mode.	
	bit[9:8]	Encoder: A 00 01 (reset) 10 11	Audio input select SDI input with PLL SDI input without PLL S/PDIF input reserved	
		Decoder: [ 00 01 (reset) 10 11	Data input select serial input at interface B parallel input at PIO pins PI[1912] reserved reserved	
	bit[7]	Encoder: I 0 (reset) 1	nvert serial input clock (SIC) do not invert SIC invert SIC	
	bit[6]	Encoder: 5 0 (reset) 1	Serial data input delay no additional delay (reset) additional delay of data related to word strobe	
	bit[5]	SDO Word 0 1 (reset)	strobe invert do not invert invert outgoing word strobe signal	
1) Changes	at this mer	morv address r	must be validated by setting bit[0] of D0:7F1 <sup>1)</sup> .	1

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Table 3-9: D0 Control Memory Cells, continued

Memory Address (hex)	Function		Mode	Name
D0:7F1	Main I/O C			
(continued)	bit[4]	Bits per sar 0 (reset) 1	mple at SDO 32 bits/sample 16 bits/sample	
	bit[3]	Encoder: 0 0 (reset) 1	Clock setting MPEG 1 MPEG 2	
	Please not	e the supply \	oltage restrictions for MPEG 1.	
	0		Serial data input interface B clock invert (pin SIBC) not inverted (data latched at rising clock edge) incoming clock signal is inverted (data latched at falling clock edge)	
		Encoder: 5 0 1 (reset)	SDI word strobe invert do not invert invert incoming word strobe signal	
	bit[1]	Decoder:		
		0 (reset) 1	DEMAND MODE (PLL off, MAS 3587F is clock master) BROADCAST MODE (PLL on, clock of MAS 3587F locks on data stream)	
	bit[0]	Validate 0 (reset) 1	changes in control memory will become effective	
		after the othe	SP has recognized the changes. The controller should r D0 control memory cells have been initialized with the	

Table 3-9: D0 Control Memory Cells, continued

Memory Address (hex)			Mod	e	Name
D0:7F2 <sup>1</sup>	) Interface	Interface Status Control (reset = 05 <sub>hex</sub> )  All  This control cell allows to enable/disable the data I/O interfaces. In addition, the clock of the output data interfaces, S/PDIF and SDO, can be set to a low-impedance mode.			InterfaceControl
	clock of th				
	bit[6]	S/PDIF inpu 0 (reset) 1	ut selection select S/PDIF input 1 select S/PDIF input 2		
	bit[5]	Enable/disa 0 (reset) 1	ble S/PDIF output enable S/PDIF output S/PDIF output invalid		
		S/PDIF audio ( 4.1, and 48 kH;	output is only available for MPEG 1 (sampling frequen- z)		
	bit[4]	bit[4] Reserved, must be set to zero			
	bit[3]	Enable/disa 0 (reset) 1	ble serial data output SDO SDO valid data SDO invalid data		
	bit[2]	Output clock 0 1 (reset)	k characteristic (SDO and S/PDIF outputs) low impedance high impedance		
	bit[1]	reserved, m	oust be set to zero		
	bit[0]	Enable/disa 0 1 (reset)	ble external serial data input SDI <sup>2)</sup> use external audio source (SDI) use internal A/D converter as audio source		
	For details Note.				
	Both digital outputs, S/PDIF and SDO, and the D/A converters may use the outgoing audio independent of each other.				
D0:7F3 <sup>1</sup>	0:7F3 <sup>1)</sup> Oscillator Frequency (reset = 18432 <sub>dec</sub> )		.II	OfreqControl	
	bit[19:0]				
	In order to achieve a correct internal operating frequency of the DSP, the nominal crystal frequency has to be written into this memory cell.				
1) Chang	jes at this men	nory address m	nust be validated by setting bit[0] of D0:7F1 <sup>1)</sup> .		

Changes at this memory address must be validated by setting bit[0] of D0:7F1<sup>1)</sup>.

Note: The pins SIC, SII, SID are switched to output mode if bit[0] = 1 (reset value).

Table 3-9: D0 Control Memory Cells, continued

Memory Address (hex)	Function			Mode	Name
D0:7F4 <sup>1)</sup>	Output Clock Configuration (pin CLKO) (reset = 80000 <sub>hex</sub> ) All				OutClkConfig
	bit[19]	CLKO cont 0 1 (reset)	figuration output clock signal at CLKO CLKO is tristate		
	The CLKC	output pin of	f the MAS 3587F can be disabled via bit [19].		
	bit[18]	Reserved,	must be set to zero		
	bit[17]	Additional 0 (reset) 1	division by 2 if scaler is on (bit[8] cleared) oversampling factor 512/768 oversampling factor 256/384		
	bit[16:9]	Reserved,	must be set to zero		
	bit[8]	Output clod 0 (reset)	ck scaler set output clock according to audio sample rate (see Table 2–1) output clock fixed at 24.576 or 22.5792 MHz		
	For a list of	of output frequ	uencies at pin CLKO please refer to Table 2-1.		
	bit[7:0]	Reserved,	must be set to zero		
D0:7F8	S/PDIF CI	SpdOutBits			
	(see Secti				
D0:7F9 <sup>1)</sup>	Soft Mute (reset = 0 <sub>hex</sub> )			SoftMute	
	bit[2]	Encoder: 0 (reset)	Bitreservoir mode bit reservoir is used bit reservoir is kept empty		
	the MPEG defined fra paste com	ibitstream is ame sizes. If t	ses Variable Bitrate Encoding (VBR), the bit reser used to compensate the differences between the p he reservoir is kept to zero, it is more easy to cut a for audio editing purposes, but bitstreams may gro	ore- and	
	bit[1]	Encoder: 0 (reset) 1	Pause mode normal encoder operation encoding process is paused		
	The encode While in possible when the pause bit ized by the				
	bit[0]	Mute audio 0 (reset)	o output no mute of audio output audio output is muted		

Table 3-9: D0 Control Memory Cells, continued

Memory Address (hex)	Function	Mode	Name			
D0:7FC <sup>1)</sup>	Volume Output Control: Left $\rightarrow$ Left Gain (reset = $80000_{hex}$ )	Decoder	out_LL			
D0:7FD <sup>1)</sup>	Volume Output Control: Left $\rightarrow$ Right Gain (reset = $0_{hex}$ )	Decoder	out_LR			
D0:7FE <sup>1)</sup>	Volume Output Control: Right $\rightarrow$ Left Gain (reset = $0_{hex}$ )	Decoder	out_RL			
D0:7FF <sup>1)</sup>	7FF <sup>1)</sup> Volume Output Control: Right → Right Gain (reset = 80000 <sub>hex</sub> ) Decoder					
1) Changes at this memory address must be validated by setting bit[0] of D0:7F11).						

Table 3-10: D0 Status Memory Cells

Memory Address	Function	Mod	e Name		
D0:FD0	MPEG Frai	II MPEGFrame-			
	bit[19:0]	Count			
	With an inv header is d encoding m	The counter will be incremented with every new frame that is encoded/decoded. With an invalid MPEG bit stream at its input while decoding (e.g. an invalid header is detected), the MAS 3587F resets the MPEGFrameCount to '0'. In encoding mode, the counter is reset on audio data time-outs and after restarting the encoder.			
D0:FD1	MPEG Hea	nder and Status Information A	II MPEGStatus1		
	bit[15]	reserved, must be set to zero			
	bit[14:13]	MPEG ID, bits 12, 11 of the MPEG header 00 MPEG 2.5 (decoding only) 01 reserved 10 MPEG 2 11 MPEG 1			
	bit[12:11]	Bits 14 and 13 of the MPEG header 00 reserved 01 Layer 3 10 Layer 2 (decoding only) 11 Layer 1 (decoding only)			
	bit[10]	CRC protection 0 bitstream protected by CRC 1 bitstream not protected by CRC			
	bit[9:2]	Reserved			
	bit[1]	CRC error (decoding only) 0 no CRC error 1 CRC error			
	bit[0]	Invalid frame (decoding only) 0 no invalid frame 1 invalid frame			
		on contains bits 1511 of the original MPEG header and other status be set each frame directly after the header has been encoded/decode t stream.			

Table 3-10: D0 Status Memory Cells, continued

Memory Address	Function					Mode	Name
D0:FD2	MPEG Hea	der Informa	nation			All	MPEGStatus2
	bit[15:12]	MPEG Lay	er 2/3 Bitrate				
			MPEG1, L2	2 MPEG1, L	3 MPEG2, L2/3		
		0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101	free 32 48 56 64 80 96 112 128 160 192 224 256 320	free 32 40 48 56 64 80 96 112 128 160 192 224 256	free 8 16 24 32 40 48 56 64 80 96 112 128 144		
		1110	384	320	160		
	bit[11:10]	1111 Sampling fr	forbidden requency in F	forbidden	forbidden		
	DIL[11.10]	Sampling ii	MPEG1	MPEG2	MPEG2.5		
		00 01 10 11	44100 48000 32000 reserved	22050 24000 16000 reserved	11025 12000 8000 reserved		
	bit[9]	Padding bit	İ				
	bit[8]	Reserved					
	bit[7:6]	Mode 00 01 10	stereo joint_stered dual chann single chan	el	ereo / m/s stereo)		
	bit[5:4]	Mode exter	nsion (applies	s to joint stere	eo only)		
		00 01 10 11	intensity ste off on off on	ereo	m/s stereo off off on on		
	bit[3]	Copyright p 0 1		ht protected rotected			
	bit[2]	Copy/origir 0/1 1	bitstream is	s a copy s an original			

Table 3-10: D0 Status Memory Cells, continued

Memory Address	Function Mode	Name					
D0:FD2							
(continued)	bit[1:0] Emphasis, indicates the type of emphasis 00 none 01 50/15 µs 10 reserved 11 CCITT J.17						
	This memory cell contains the 16 LSBs of the MPEG header. It will be set directly after synchronizing to the bit stream.						
D0:FD3	MPEG CRC Error Counter Decoder	CRCErrorCount					
	The counter will be increased by each CRC error detected in the MPEG bit- stream. It will not be reset when losing the synchronization.						
D0:FD4	Number of Bits in Ancillary Data Decoder	NumberOfAncil-					
	Number of valid ancillary bits in the current MPEG frame.	laryBits					
D0:FD5	Ancillary Data Decoder	AncillaryData					
 D0:FD1	(see Section 3.3.7. on page 38).						

#### 3.3.5. Copyright Management

The controller software is responsible for the interpretation of the copyright information contained in received bitstreams and the correct setting of the copyright bits in output bitstreams.

Copyright information is included in both, the S/PDIF and the MPEG bitstreams. One bit indicates if the signal is copyright protected at all. The second shows whether the signal was already copied.

In the S/PDIF bitstream the copyright information is carried in the channel status bit area which is part of the S/PDIF signal (see IEC 958: "Digital Audio Interface"). The copyright information (Cp-bit) is located in bit 2 (0 = protected, 1 = no copyright), and the generation information (L-bit) is in bit 15 (0 = copy, 1 = original). The status information of received signals can be read from DSP-register  $56_{\text{hex}}$ , the copyright bits of originating bitstreams are controlled in memory address D0:7F8.

For MPEG bitstreams, this information is located in bit 3 (copyright) and bit 2 (original) of the frame header. The firmware uses the memory cells D0:FD2 for incoming signals, D0:7F0 for outgoing signals.

#### 3.3.5.1. Encoding of Analog or PCM-Audio

In case of analog input or PCM-input at the serial interface SDI, the indication in the originating bitstream has to be set according to the application. If the copyright status is not known, the signal shall be asserted as a copyright protected original.

If the S/PDIF-input is used, the copyright bits have to be evaluated. Table 3–11 gives an example in case of a DAT-Recorder input signal (category code 300<sub>hex</sub>).

As the S/PDIF signal is only looped through the encoder, the copyright indication of the output must be set to the same as that of the input signal. Signals from CD (category code  $100_{\rm hex}$ ) are usually originals and in this case the generation bit at the output must be set to one.

**Table 3–11:** Encoding copyright propagation with a DAT-recorder source

S/PDIF in ch. status (hex)	MPEG copyright bit	MPEG original bit	S/PDIF Out Ch. Status (hex)
0304	0	0	0204
8304	0	0	8204
0300	recording for	orbidden	0200
8300	1	0	8200

#### 3.3.5.2. Decoding

If the S/PDIF output is used, the copyright indication has to be set according to the input bitstream. Table 3–12 gives an example in case of setting the category information in the S/PDIF signal to PCM-encoder/decoder (category code  $200_{hex}$ ).

**Table 3–12:** Decoding copyright propagation (PCM-encoder/deocder)

MPEG Copyright Bit	MPEG Original Bit	S/PDIF Out Channel Status (hex)
0	0	0204
0	1	8204
1	0	0200
1	1	8200

#### 3.3.6. Variable Bitrate Encoding

The encoder uses Variable Bitrate Encoding (VBR) to realize optimal compression of the audio data. The setting of a fixed bitrate is replaced with setting a quality level that preserves audio quality in critical sections and enhances compression otherwise.

The minimum bitrate (in case of digital zero samples) is 32 kbit/s for MPEG 1 and 8 kbit/s for MPEG 2. The maximum bitrate is 192 kbit/s for MPEG 1 and 160 kbit/s for MPEG 2. This theoretically holds for all quality settings, but experience shows that the maximum rate does not vary too much from the average bitrate.

Table 3–13 gives an overview on the average encoding bitrate that can be expected for common audio signals at different quality settings and sample rates.

Table 3-13: Quality setting vs. average bitrate

Quality	Average bitrate in kbit/s for fs/kHz								
Setting "q" in D0:7F0	44.1 stereo	22.05 stereo	44.1 mono	22.05 mono					
0	75	39	65	35					
1	80	41	68	38					
2	90	45	73	40					
3	100	50	80	45					
4	120	60	90	50					
5	140	80	105	60					
6	160	110	125	75					
7	170	130	140	90					

## 3.3.7. Ancillary Data

The memory fields D0:FD5...D0:FF1 contain the ancillary data. It is organized in 28 words of 16 bit each. The last ancillary bit of a frame is placed at bit 0 in D0:FD5. The position of the first ancillary data bit received can be located via the content of NumberO-fAncillaryBits because

int[(NumberOfAncillaryBits-1)/16] + 1

of memory words are used.

Example:

First get the content of 'NumberOfAncillaryBits'

```
<DW 68 c4 00 00 01 0f d4> 
<DW 69 <DR dd dd >
```

Assume that the MAS 3587F has received 19 ancillary data bits. Therefore, it is necessary to read two 16-bit words:

The first bit received from the MPEG source is at position 2 of D0:fd6; the last bit received is at the LSB of D0:FD5.

Table 3-14: Content of D0:fd5 after reception of 19 ancillary bits.

D0:fd5	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Ancillary Data	4th bit	5th bit	6th bit											17th bit	18th bit	last bit

**Table 3–15:** Content of D0:fd6 after reception of 19 ancillary bits.

D0:fd6	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Ancillary Data	х	x	х	x	x	x	x	x	x	x	x	x	x	first bit	2nd bit	3rd bit

#### 3.3.7.1. Timecode Information

As the encoder uses VBR encoding, it is quite difficult to calculate the actual elapsed time in the MPEG bitstream. Therefore the encoder provides an option to insert timecodes into the MPEG bitstream.

The timecode is the number of frames processed from the start of encoding. It occupies 3 bytes at the end of the ancillary data region in each MPEG frame and contains of the tag nibble  $5_{\text{hex}}$  followed by a 20 bit number  $(5_{\text{hex}}, \text{d4}, \text{d3}, \text{d2}, \text{d1}, \text{d0})$ .

A frame number can be translated to the absolute time in seconds by the following formulas:

MPEG 1: time[s] = frame\*1152/sampling freq [Hz] MPEG 2: time[s] = frame\*576/sampling freq [Hz]

While decoding, the controller can check the presence/validity of the timecode information by first reading the NumberOfAncillaryBits. If the number is greater than or equal to 24 bits, two words of the ancillary data bits have to be read. D0:FD5 contains the 16 LSBs of the timecode (d3,d2,d1,d0) and D0:FD6 contains the tag nibble and the 4 MSBs (x,x,5<sub>hex</sub>,d4). If the tag nibble does not match, the timecode is not valid.

As the ancillary data may contain any kind of information, it is advisable to check several successive timecodes for validity and the sequence of numbers before accepting it.

#### 3.3.8. DSP Volume Control

The digital baseband volume matrix is used for controlling the digital gain of the decoder as shown in Fig. 3—3. This volume control is effective on both, the digital audio output and the data stream to the D/A converters. The values are in 20-bit 2's complement notation.

Table 3–16 shows the proposed settings for the 4 volume matrix coefficients for stereo, left and right mono. The gain factors are given in fixed point notation as described in Section 3.3.2.

The DSP volume control is available in Decoder Mode only.

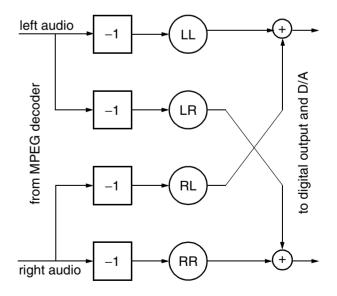


Fig. 3-3: Digital volume matrix

**Table 3–16:** Settings for the digital volume matrix.  $-1.0 \times 2^{19} = 80000_{hex}$ 

Memory	D0:7FC	D0:7FD	D0:7FE	D0:7FF	
Name	LL	LR	RL	RR	
Stereo (default)	-1.0	0	0	-1.0	
Mono left	-1.0	-1.0	0	0	
Mono right	0	0	-1.0	-1.0	

If channels are mixed, care must be taken to prevent clipping at high amplitudes. Therefore the sum of the absolute values of coefficients for one output channel must be less than or equal to 1.0.

For normal operating conditions it is recommended to use the main volume control of the audio codec instead (register 00 10<sub>hex</sub> of the audio codec).

#### 3.4. Audio Codec Access Protocol

The MAS 3587F has 16-bit wide registers for the control of the audio codec. These registers are accessed via the  $\rm I^2C$  subaddresses codec\_write (6C<sub>hex</sub>) and codec\_read (6D<sub>hex</sub>).

### 3.4.1. Write Codec Register

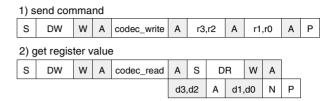
s	DW	W	Α	codec_write	Α	r3,r2	Α	r1,r0	Α	
						d3,d2	Α	d1,d0	Α	Р

The controller writes the 16-bit value ( $\mathbf{d} = d3,d2,d1,d0$ ) into the MAS 3587F codec register ( $\mathbf{r} = r3,r2,r1,r0$ ). A list of registers is given in Table 3–17.

Example: Writing the value 1234<sub>hex</sub> into the codec register with the number 00 1B<sub>hex</sub>:

<DW 6c 00 1b 12 34>

#### 3.4.2. Read Codec Register



Reading the codec registers also needs a set-up for the register address and an additional start condition during the actual read cycle. A list of status registers is given in Table 3–18.

# 3.4.3. Codec Registers

Table 3–17: Codec control registers on I<sup>2</sup>C subaddress 6C<sub>hex</sub>

Register Address (hex)	Function		Name
CONVERT	ER CONFIG	URATION	
00 00	Audio Co	dec Configuration	CONV_CONF
		ated to the D/A full-scale output voltage fer to Section 4.6.4. on page 72)	
	bit[15:12]	A/D converter left amplifier gain = n*1.5-3 [dB]	
	bit[11:8]	A/D converter right amplifier gain = n*1.5-3 [dB] 1111 +19.5 dB 1110 +18.0 dB	
		0011 +1.5 dB 0010 0.0 dB 0001 -1.5 dB 0000 - 3.0 dB	
	bit[7:4]	Microphone amplifier gain = $n*1.5+21$ [dB] 1111 +43.5 dB 1110 +42.0 dB	
		0001 +22.5 dB 0000 +21.0 dB	
	bit[3]	Input selection for left A/D converter channel 0 line-in 1 microphone	
	bit[2]	Enable left A/D converter	
	bit[1]	Enable right A/D converter	
	bit[0]	Enable D/A converter <sup>1)</sup>	
	also contro at pin AGN	eration of the internal DC reference voltage for the D/A converter is olled with this bit. In order to avoid click noise, the reference voltage IDC should have reached a near ground potential before repower-A converter after a short down phase.	
	set during	ly at least one of the A/D converters (bits [2] or [1]) should remain short power-down phases of the D/A. Then the DC reference voltation for the D/A converter will not be interrupted.	
INPUT MO	DE SELECT		
00 08	Input Mod	e Setting	ADC_IN_MODE
	bit[15]	Mono switch  O stereo input mode  1 left channel is copied into the right channel	
	bit[14:2]	Reserved, must be set to 0	
	bit[1:0]	Deemphasis select 0 deemphasis off 1 deemphasis 50 μs 2 deemphasis 75 μs	

**Table 3–17:** Codec control registers on I<sup>2</sup>C subaddress 6C<sub>hex</sub>, continued

Register Address (hex)	Function			Name			
OUTPUT I	MODE SELE	СТ					
	D/A Conve	erter Source N	<b>l</b> ixer				
00 06	MIX ADC	scale		DAC_IN_ADC			
00 07	MIX DSP s	scale		DAC_IN_DSP			
	bit[15:8]	00 <sub>hex</sub> 7F <sub>h</sub>	ex Linear scaling factor				
	Example:	20 <sub>hex</sub> 40 <sub>hex</sub>	off 50% (-6 dB gain) 100% (0 dB gain) 200% (+6 dB gain)				
		of both mixing dio processing	inputs exceeds 100%, clipping may occur in the suc-				
00 0E	D/A Conve	erter Output M		DAC_OUT_MODE			
	bit[15]		stereo through mono matrix applied				
	bit[14]	Invert right c 0 1	channel through right channel is inverted				
	bit[13:0]	Reserved, m	nust be set to 0				
		between pins	output power a single loudspeaker can be connected OUTL and OUTR. In this mode bit[15] and bit[14]				
BASEBAN	ID FEATURE	:S					
00 14	Bass			BASS			
	bit[15:8]	58 <sub>hex</sub>	+12 dB +11 dB +1 dB				
		00 <sub>hex</sub>	0 dB -1 dB				
			-11 dB -12 dB				
	Higher reso	Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB.					
	With positive it is not recurrence would resur						
	The setting	gs require: max	c (bass, treble) + loudness + volume ≤ 0 dB				
	bit[7:0]	Not used, m	ust be set to 0				

**Table 3–17:** Codec control registers on I<sup>2</sup>C subaddress 6C<sub>hex</sub>, continued

Register Address (hex)	Function	Name
00 15	Treble	TREBLE
	bit[15:8] Treble range $60_{\text{hex}}$ +12 dB $58_{\text{hex}}$ +11 dB	
	08 <sub>hex</sub> +1 dB 00 <sub>hex</sub> 0 dB F8 <sub>hex</sub> -1 dB	
	A8 <sub>hex</sub> -11 dB A0 <sub>hex</sub> -12 dB	
	Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB.	
	With positive treble settings, clipping of the output signal may occur. There fore, it is not recommended to set treble to a value that, in conjunction with loudness and volume, would result in an overall positive gain.	
	The settings require: max (bass, treble) + loudness + volume ≤ 0 dB	
	bit[7:0] Not used, must be set to 0	
00 1E	Loudness	LOUDNESS
	bit[15:8] Loudness gain  44 <sub>hex</sub> +17 dB  40 <sub>hex</sub> +16 dB	
	04 <sub>hex</sub> +1 dB 00 <sub>hex</sub> 0 dB	
	bit[7:0] Loudness mode 00 <sub>hex</sub> normal (constant volume at 1 kHz) 04 <sub>hex</sub> Super Bass (constant volume at 2 kHz)	
	Higher resolution of loudness gain is possible: An LSB step results in a gastep of about 1/4 dB.	ain
	Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness value that, in conjunction with volume, would result in an overall positive gain.	to a
	The settings should be: max (bass, treble) + loudness gain + volume $\leq$ 0 of	dB
	The corner frequency for bass amplification can be set to two different values in Super Bass mode, the corner frequency is shifted up. The point of construction of shifted from 1 kHz to 2 kHz.	

**Table 3–17:** Codec control registers on I<sup>2</sup>C subaddress 6C<sub>hex</sub>, continued

Register Address (hex)	Function			Name
Micronas	Dynamic Bas	ss (MDB)		
00 22	MDB Effec	t Strength		MDB_STR
	bit[15:8]	00 <sub>hex</sub> 7F <sub>hex</sub>	MDB off (default) maximum MDB	
		ffect strength lium MDB eff	n can be adjusted in 1dB steps. A value of 40 <sub>hex</sub> will rect.	
00 23	MDB Harm	onics		MDB_HAR
	bit[15:8]	00 <sub>hex</sub> 40 <sub>hex</sub> 7F <sub>hex</sub>	no harmonics are added (default) 50% fundamentals + 50% harmonics 100% harmonics	
	tal by creati bandpass fi that are bel	sychoacoustic phenomenon of the 'missing fundamens of the frequencies below the center frequency of the C). This enables a loudspeaker to display frequencies frequency. The Variable MDB_HAR describes the owards the original signal.		
00 24	MDB Cente	MDB_FC		
	bit[15:8]	2 3	20 Hz 30 Hz	
		30	300 Hz	
	The MDB C pass filter (s mately mate loudspeake 90 Hz			
00 21	MDB Shap	е		MDB_SHAPE
	bit[15:8]	530	corner frequency in 10-Hz steps (range: 50300 Hz)	
	With a second bandpass of frequency of (MDB_FC) the harder to 1.5 × MDB_			
	MDB Switc	h		MDB_SWITCH
	bit[7:2]		reserved, must be set to zero	
	bit[1]	0	MDB switch MDB off MDB on	
	bit [0]		reserved, must be set to zero	

**Table 3–17:** Codec control registers on I<sup>2</sup>C subaddress 6C<sub>hex</sub>, continued

Register Address (hex)	Function			Name
VOLUME				
00 10	Volume Co	VOLUME		
	bit[15:8]	7F <sub>hex</sub> 7E <sub>hex</sub>	ole with 1 dB step size +12 dB (maximum volume) +11 dB	
		74 <sub>hex</sub> 73 <sub>hex</sub> 72 <sub>hex</sub>	+1 dB 0 dB –1 dB	
		02 <sub>hex</sub> 01 <sub>hex</sub> 00 <sub>hex</sub>	-113 dB -114 dB mute (reset)	
	bit[7:0]	Not used, r	must be set to 0	
	between a	digital and ar	ol is applied to the analog outputs only. It is split analog function. In order to avoid noise due to large the actual setting is internally low-pass filtered.	
	With large sping.	scale input si	gnals, positive volume settings may lead to signal clip-	
00 11	Balance			BALANCE
	bit[15:8]	Balance ra 7F <sub>hex</sub> 7E <sub>hex</sub>	nge left –127 dB, right 0 dB left –126 dB, right 0 dB	
		01 <sub>hex</sub> 00 <sub>hex</sub> FF <sub>hex</sub>	left –1 dB, right 0 dB left 0 dB, right 0 dB left 0 dB, right –1 dB	
		81 <sub>hex</sub> 80 <sub>hex</sub>	left 0 dB, right –127 dB left 0 dB, right –128 dB	
		egative settin	s reduce the left channel without affecting the right gs reduce the right channel leaving the left channel	
00 12	Automatic	Volume Co	rrection (AVC) Loudspeaker Channel	AVC
	bit[15:12]	0 <sub>hex</sub> 8 <sub>hex</sub>	AVC off (and reset internal variables) AVC on	
	bit[11:8]	8 <sub>hex</sub> 4 <sub>hex</sub> 2 <sub>hex</sub> 1 <sub>hex</sub>	8 s decay time 4 s decay time 2 s decay time 20 ms decay time (intended for quick adaptation to the average volume level after track or source change)	
	on again du		nal variables, the AVC should be switched off and then ck or source change. For standard applications, the ne is 4 s.	

Table 3–18: Codec status registers on I<sup>2</sup>C subaddress 6D<sub>hex</sub>

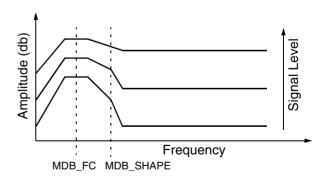
Register Address (hex)	Function	Name
INPUT QU	ASI-PEAK	
00 0A	A/D Converter Quasi-Peak Detector Readout Left	QPEAK_L
	bit[14:0] Positive 15-bit value, linear scale	
	For example: 0000 0% 2000 25% (-12 dBFS) 4000 50% (-6 dBFS) 7FFF 100% (0 dBFS)	
00 0B	A/D Converter Quasi-Peak Detector Readout Right	QPEAK_R
	bit[14:0] Positive 15-bit value, linear scale	
OUTPUT (	QUASI-PEAK	
00 0C	Audio Processing Input Quasi-Peak Detector Readout Left	DQPEAK_L
	bit[14:0] Positive 15-bit value, linear scale	
00 0D	Audio Processing Input Quasi-Peak Detector Readout Right	DQPEAK_R
	bit[14:0] Positive 15-bit value, linear scale	

#### 3.4.4. Basic MDB Configuration

With the parameters described in Table 3–17, the Micronas Dynamic Bass system (MDB) can be customized to create different bass effects as well as to fit the MDB to various loudspeaker characteristics. The easiest way to find a good set of parameter is by selecting one of the settings below, listening to music with strong bass content and adjusting the MDB parameters:

- MDB\_STR: Increase/decrease the strength of the MDB effect
- MDB\_HAR: Increase/decrease the content of low frequency harmonics
- MDB\_FC: Shift the MDB effect to lower/higher frequencies

 MDB\_SHAPE: Widen/narrow MDB frequency range (which results in a softer/harder bass sound), turn on/off the MDB



**Fig. 3–4:** Micronas Dynamic Bass (MDB): Bass boost in relation to input signal leve

Table 3-19: Suggested MDB settings (all addresses and values are in hexadecimal notation)

Function (Address)	MDB_STR (00 22)	MDB_HAR (00 23)	MDB_FC (00 24)	MDB_SHAPE (00 21)
MDB off	xxxx	xxxx	xxxx	0000
Low end headphones, medium effect	5000	3000	0600	0902

## 4. Specifications

## 4.1. Outline Dimensions

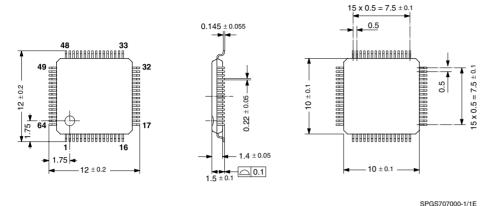


Fig. 4–1:
64-Pin Plastic Low-Profile Quad Flat Pack
(PLQFP64)
Weight approximately 0.35 g
Dimensions in mm

■ (not usable for new design)

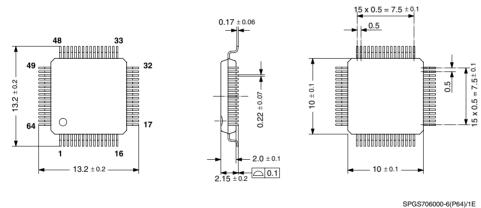


Fig. 4–2: 64-Pin Plastic Metric Quad Flat Pack (PMQFP64) Weight approximately 0.4 g Dimensions in mm

## 4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant

LV If not used, leave vacant

X obligatory, pin must be connected as described

in application information (see Fig. 4–34 on page 81)

VDD connect to positive supply

VSS connect to ground

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Туре	Default Connection (if not used)	Short Description
1	AGNDC		Х	Analog reference voltage
2	MICIN	IN	LV	Input for internal microphone amplifier
3	MICBI	IN	LV	Bias for internal microphone
4	INL	IN	LV	Left A/D input
5	INR	IN	LV	Right A/D input
6	TE	IN	Х	Test enable
7	XTI	IN	Х	Crystal oscillator (ext. clock) input
8	ХТО	OUT	LV	Crystal oscillator output
9	POR	IN	Х	Power on reset, active low
10	VSS	SUPPLY	Х	DSP supply ground
11	XVSS	SUPPLY	Х	Digital output supply ground
12	VDD	SUPPLY	Х	DSP supply
13	XVDD	SUPPLY	Х	Digital output supply
14	I2CVDD	SUPPLY	Х	I <sup>2</sup> C supply
15	DVS	IN	Х	I <sup>2</sup> C device address selector
16	VSENS1	IN/OUT	VDD	Sense input and power output of DC/DC converter 1
17	DCSO1	SUPPLY	LV	DC/DC 1 switch output
18	DCSG1	SUPPLY	VSS	DC/DC 1 switch ground
19	DCSG2	SUPPLY	VSS	DC/DC 2 switch ground
20	DCSO2	SUPPLY	LV	DC/DC 2 switch output
21	VSENS2	IN/OUT	VDD	Sense input and power output of DC/DC converter 2
22	DCEN	IN	VSS	DC/DC enable (both converters)
23	CLKO	OUT	LV	Clock output
24	I2CC	IN/OUT	Х	I <sup>2</sup> C clock

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Туре	Default Connection (if not used)	Short Description
25	I2CD	IN/OUT	Х	I <sup>2</sup> C data
26	SYNC	OUT	LV	Sync output
27	VBAT	IN	LV	Battery voltage monitor input
28	PUP	OUT	LV	DC Converters Power-Up Signal
29	EOD	OUT	LV	PIO end of DMA, active low
30	PRTR	OUT	LV	PIO ready to read, active low
31	PRTW	OUT	LV	PIO ready to write, active low
32	PR	IN	VDD	PIO DMA request, active high
33	PCS	IN	VSS	PIO chip select, active low
34	PI19	IN/OUT	LV	PIO data bit[7] (MSB)
35	PI18	IN/OUT	LV	PIO data bit[6]
36	PI17	IN/OUT	LV	PIO data bit[5]
37	PI16	IN/OUT	LV	PIO data bit[4]
38	PI15	IN/OUT	LV	PIO data bit[3]
39	PI14	IN/OUT	LV	PIO data bit[2]
40	PI13	IN/OUT	LV	PIO data bit[1]
41	PI12	IN/OUT	LV	PIO data bit[0] (LSB)
42	SOD	OUT	LV	Serial output data
43	SOI	OUT	LV	Serial output word identification
44	SOC	OUT	LV	Serial output clock
45	SID	IN/OUT	Х	Serial input data, interface A
46	SII	IN/OUT	Х	Serial input word identification, interface A
47	SIC	IN/OUT	Х	Serial input clock, interface A
48	SPDO	OUT	LV	S/PDIF output interface
49	SIBD	IN	VSS	Serial input data, interface B
50	SIBC	IN	VSS	Serial input clock, interface B
51	SIBI	IN	VSS	Serial input word identification, interface B
52	SPDI2	IN	LV	Active differential S/PDIF input 2
53	SPDI1	IN	LV	Active differential S/PDIF input 1

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Туре	Default Connection (if not used)	Short Description
54	SPDIR	IN	LV	Reference differential S/PDIF inputs 1 and 2
55	FILTL	IN	х	Feedback input for left amplifier
56	AVDD0	SUPPLY	х	Analog supply for output amplifiers
57	OUTL	OUT	LV	Left analog output
58	OUTR	OUT	LV	Right analog output
59	AVSS0	SUPPLY	Х	Analog ground for output amplifiers
60	FILTR	IN	Х	Feedback for right output amplifier
61	AVSS1	SUPPLY	Х	Analog ground
62	VREF		Х	Analog reference ground
63	PVDD	SUPPLY	Х	Internal power supply
64	AVDD1	SUPPLY	Х	Analog supply

PRELIMINARY DATA SHEET MAS 3587F

#### 4.3. Pin Descriptions

#### 4.3.1. Power Supply Pins

The use of all power supply pins is mandatory to achieve correct function of the MAS 3587F.

VDD, VSS SUPPLY

Digital supply pins.

XVDD, XVSS SUPPLY

Supply for digital output pins.

I2CVDD SUPPLY

Supply for I<sup>2</sup>C interface circuitry. This net uses VSS or XVSS as the ground return line.

PVDD SUPPLY

Auxiliary pin for analog circuitry. This pin has to be connected via a 3-nF capacitor to AVDD1. Extra care should be taken to achieve a low inductance PCB line.

AVDD0/AVSS0 SUPPLY

Supply for analog output amplifier (output stage).

AVDD1/AVSS1 SUPPLY

Supply for internal analog circuits (A/D, D/A converters, clock, PLL, S/PDIF input).

AVDD0/AVSS0 and AVDD1/AVSS1 should receive the same supply voltages.

#### 4.3.2. Analog Reference Pins

#### **AGNDC**

Internal analog reference voltage. This pin serves as the internal ground connection for the analog circuitry.

#### **VREF**

Analog reference ground. All analog inputs and outputs should drive their return currents using separate traces to a ground starpoint close to this pin. Connect to AVSS1. This reference pin should be as noise free as possible.

#### 4.3.3. DC/DC Converters and Battery Voltage Supervision

DCSG1/DCSG2 SUPPLY

DC/DC converters switch ground. Connect using separate wide trace to negative pole of battery cell. Connect also to AVSS0/1 and VSS/XVSS, VREF.

DCSO1/DCSO2 SUPPLY

DC/DC converter switch connection. If the respective DC/DC converter is not used, this pin must be left vacant.

#### VSENS1/VSENS2

IN

Sense input and power output of DC/DC converters. If the respective DC/DC converter is not used, this pin should be connected to a supply to enable proper function of the PUP-signals.

DCEN IN

Enable signal for both DC/DC converters. If none of the DC/DC converters is used, this pin must be connected to VSS.

PUP OUT

Power-up. This signal is set when the required voltages are available at both DC/DC converter output pins VSENS1 and VSENS2. The signal is cleared when both voltages have dropped below the level is set in the DCCF Register.

VBAT IN

Analog input for battery voltage supervision.

#### 4.3.4. Oscillator Pins and Clocking

XTI IN XTO OUT

The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Each pin should be directly connected to the crystal and to a ground-connected capacitor (see application diagram).

CLKO OUT

The CLKO can drive an output clock line.

#### 4.3.5. Control Lines

I2CC SCL IN/OUT I2CD SDA IN/OUT

Standard I<sup>2</sup>C control lines.

DVS IN

I<sup>2</sup>C device address selector. Connect this pin either to VDD (I<sup>2</sup>C device address: 3E/3F<sub>hex</sub>) or VSS (I<sup>2</sup>C device address: 3C/3D<sub>hex</sub>) to select a proper I<sup>2</sup>C device address (see also Table 3–1 on page 18).

### 4.3.6. Parallel Interface Lines

PI12..PI19 IN/OUT

The PIO input pins PI12..PI19 are used as 8-bit I/O interface to a microcontroller in order to transfer compressed and uncompressed data. PI12 is the LSB, PI19 the MSB.

#### 4.3.6.1. PIO Handshake Lines

PCS IN

The PIO chip select PCS must be set to '0' to activate the PIO in operation mode.

PR IN

Pin PR must be set to '1' when ready to send/receive data to/from MAS 3587F PIO pins.

PRTR OUT

Ready to read. This signal indicates that the MAS 3587F is able to receive data in PIO input mode.

PRTW OUT

Ready to write. This pin indicates that MAS 3587F has data available in PIO output mode.

<u>EOD</u> OUT

EOD indicates the end of an DMA cycle in the IC's PIO input/output mode. In 'serial' input mode it is used as Demand signal, that indicates that new input data are required.

#### 4.3.7. Serial Input Interface (SDI)

SID	DATA	IN/OUT
SII	WORD STROBE	IN/OUT
SIC	CLOCK	IN/OUT

I<sup>2</sup>S compatible serial interface A for digital audio data. In the standard firmware this interface is not used. Note: Please refer to Interface Status Register (D0:7f2) bit[0] (Table 3–9).

#### 4.3.8. Serial Input Interface B (SDIB)

SIBD	DATA	IN
SIBI	WORD STROBE	IN
SIBC	CLOCK	IN

The serial interface B is used as bitstream input interface. The SIBI line must be connected to VSS in the serial decoder application.

#### 4.3.9. Serial Output Interface (SDO)

SOD	DATA	OUT
SOI	WORD STROBE	OUT
SOC	CLOCK	IN/OUT

Data, Frame Indication, and Clock line of the serial output interface. The SDO is reconfigurable and can be adapted to several I<sup>2</sup>S compliant modes.

#### 4.3.10. S/PDIF Input Interface

SPDI1 IN SPDI2 IN SPDIR IN

SPDI1 and SPDI2 are alternative input pins for S/PDIF sources according to the IEC 958 consumer specification. A switch at D0:7F2 selects one of these pins at a time. The SPDIR pin is a common reference for both input lines (see Fig. 4–34 on page 81).

#### 4.3.11. S/PDIF Output Interface

SPDO OUT

The SPDO pin provides an digital output with standard CMOS level that is compliant to the IEC 958 consumer specification.

#### 4.3.12. Analog Input Interfaces

In the standard MPEG-decoding DSP firmware the analog inputs are not used. However, they can be selected as a source for the D/A converters (set MIX ADC scale of the D/A Converter Source Mixer, Register 00  $06_{\rm hex}$  in Table 3–15 on page 39).

MICIN IN MICBI IN

The MICIN input may be directly used as electret microphone input, which should be connected as described in application information (see Fig. 4–34 on page 81). The MICBI signal provides the supply voltage for these microphones.

INL IN IN IN

INL and INR are analog line-in input lines. They are connected to the embedded stereo A/D converter of the MAS 3587F. The sources should be AC coupled. The reference ground for these analog input pins is the VREF pin.

#### 4.3.13. Analog Output Interfaces

OUTL OUT OUT

OUTL and OUTR are left and right analog outputs, that may be directly connected to a pair of 16  $\Omega$  loudspeakers, to one 32  $\Omega$  loudspeaker in a bridge mode (see Section 2.7.4. on page 10), or via 22  $\Omega$  series resistance to the headphones as described in the application information (see Fig. 4–34 on page 81).

FILTL IN FILTR IN

Connection to input terminal of output amplifier. Can be used to connect capacitors from OUTL to FILTL and from OUTR to FILTR and thus implement low pass fil-

ters to reduce the out-of-band noise of the D/A converters.

#### 4.3.14. Miscellaneous

SYNC OUT

The SYNC signal indicates the detection of a frame start in the input data of MAS 3587F. Usually this signal generates an interrupt in the controller.

#### POR

IN

The Power-On Reset pin completely resets the MAS 3587F. The POR is an active-low signal (see Fig. 4–34 on page 81).

TE IN

The TE pin is for production test only and must be connected with VSS in all applications.

## 4.4. Pin Configurations

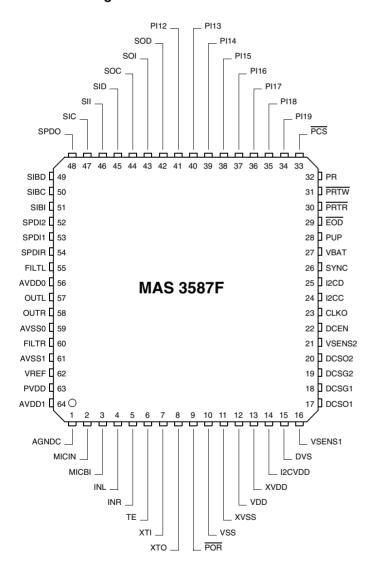


Fig. 4-3: PLQFP64/PMQFP64 package (Top view)

#### 4.5. Internal Pin Circuits

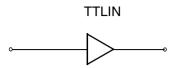


Fig. 4–4: Input pins PCS, PR

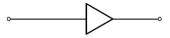


Fig. 4–5: Input pin TE, DVS, POR

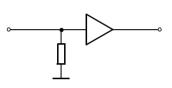
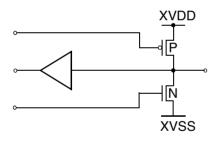


Fig. 4-6: Input pin DCEN



**Fig. 4–7:** Input/output pins SOC, SOI, SOD, PI12...PI19, SPDO

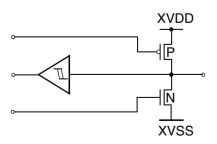


Fig. 4-8: Input pins SI(B)C, SI(B)I, SI(B)D

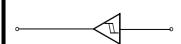


Fig. 4-9: Input pins SIBC, SIBI, SIBD

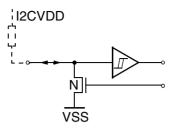


Fig. 4-10: Input/output pins I2CC, I2CD

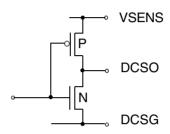


Fig. 4–11: Input/output pins DCSO1/2, DCSG1/2, VSENS1/2

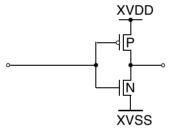


Fig. 4–12: Output pins  $\overline{\text{PRTW}}$ ,  $\overline{\text{EOD}}$ ,  $\overline{\text{PRTR}}$ , CLKO, SYNC, PUP

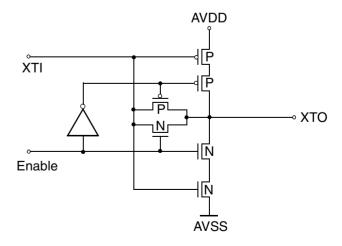


Fig. 4-13: Clock oscillator XTI, XTO

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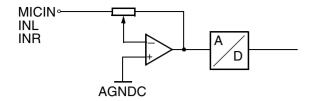


Fig. 4-14: Analog input pins MICIN, INL, INR

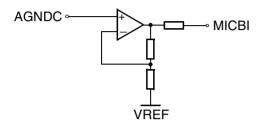
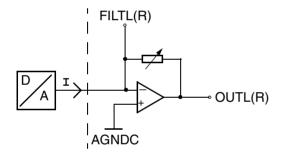
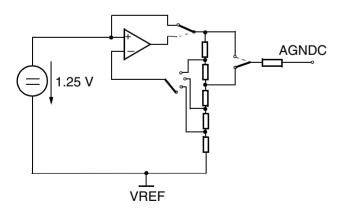


Fig. 4-15: Microphone bias pin (MICBI)



**Fig. 4–16:** Analog outputs OUTL(R) and connections for filter capacitors FILTL(R)



**Fig. 4–17:** Analog ground generation with pin to connect external capacitor

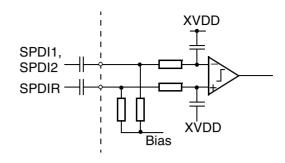


Fig. 4-18: S/PDIF inputs

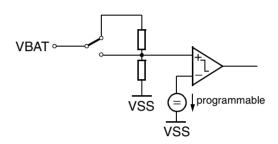


Fig. 4–19: Battery voltage monitor VBAT

#### 4.6. Electrical Characteristics

## 4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T <sub>A</sub>	Ambient operating temperature				
	- operating conditions - extended temperature range <sup>1)</sup>		0 -40	70 70	°C °C
$T_{C\_LQFP}$	Case temperature PLQFP64		-40	80	°C
$T_{C\_MQFP}$	Case temperature PMQFP64		-40	TBD	°C
T <sub>S</sub>	Storage Temperature		-40	125	°C
P <sub>TOT</sub>	Power dissipation	VDD, XVDD, AVDD0/1, I2CVDD		650	mW
V <sub>SUP</sub>	Supply voltage	VDD, XVDD, I2CVDD AVDD0/1 <sup>2)</sup>	-0.3	6	V
V <sub>II2C</sub>	Input voltage, I <sup>2</sup> C-Pins	I2CC, I2CD	-0.3	6	V
$V_{\text{Idig}}$	Input voltage, all digital inputs		-0.3	V <sub>SUP</sub> +0.3	V
I <sub>Idig</sub>	Input current, all digital inputs		-20	+20	mA
V <sub>lana</sub>	Input voltage, all analog inputs		-0.3	V <sub>SUP</sub> + 0.3	٧
I <sub>lana</sub>	Input current, all analog inputs		-5	+5	mA
I <sub>Oaudio</sub>	Output current, audio output <sup>3)</sup>	OUTL/R	-0.2	0.2	Α
l <sub>Odig</sub>	Output current, all digital outputs <sup>4)</sup>		-50	+50	mA
I <sub>Odcdc1</sub>	Output current DCDC converter 1	DCSO1		1.5	Α
I <sub>Odcdc2</sub>	Output current DCDC converter 2	DCSO2	_	1.5	Α

<sup>1)</sup> The functionality of the device in the "extended temperature range" was checked by electrical characterization on sample base. Data sheet parameters are valid for "operating conditions" only.

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions/Characteristics" of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

<sup>2)</sup> Both AVDD0 and AVDD1 have to be connected together!

<sup>3)</sup> These pins are not short-circuit proof!

<sup>4)</sup> Total chip power dissipation must not exceed absolute maximum rating

## 4.6.2. Recommended Operating Conditions

## ■ Table 4–1: Temperature range and supply voltages

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit
T <sub>A</sub>	Ambient operating temperature					
	<ul> <li>operating conditions</li> <li>extended temperature range<sup>1)</sup></li> </ul>		0 -40		70 70	°C °C
V <sub>SUPD1</sub>	Digital supply voltage (MPEG decoder)	VDD, XVDD	2.5	2.7	3.9	٧
V <sub>SUPD2</sub>	Digital supply voltage (MPEG 1 encoder)					
	48, 32 kHz 44.1 kHz		3.5 3.3	3.7 3.5	3.9 3.9	
	Digital supply voltage (MPEG 2 encoder)		2.7	2.9	3.9	
V <sub>SUPI2C</sub>	I <sup>2</sup> C bus supply voltage	I2CVDD	V <sub>SUPDn</sub> <sup>2)</sup> at VDD		3.9	V
V <sub>SUPA</sub>	Analog audio supply voltage	AVDD0/1	2.2	2.7	3.9	V
	Analog audio supply voltage in relation to the digital supply voltage		0.62		1.6	V <sub>SUPDn</sub>
V <sub>SUPx</sub>	PIN supply voltage	XVDD	2.5		3.9	V
	PIN supply voltage in relation to digital supply voltage		0.62		1.6	V <sub>SUPDn</sub>

<sup>1)</sup> The functionality of the device in the "extended temperature range" was checked by electrical characterization on sample base. Data sheet parameters are valid for "operating conditions" only.

 $<sup>^{2}</sup>$ ) n = 1,2

**Table 4–2:** Reference frequency generation and crystal recommendation

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit
External Cl	ock Input Recommendations					
f <sub>CLK</sub>	Clock frequency	XTI, XTO	13.0 <sup>2)</sup>	18.432	20.0 <sup>1)</sup>	MHz
V <sub>CLKI</sub>	Clock amplitude of external clock fed into XTI at V <sub>SUPA</sub> = 2.2 V	ХТІ	0.7		1.05	V <sub>PP</sub>
	Clock amplitude of external clock fed into XTI at V <sub>SUPA</sub> = 2.7 V		0.55		1.5	
	Clock amplitude of external clock fed into XTI at V <sub>SUPA</sub> = 3.3 V		0.45		1.75	
	Clock amplitude of external clock fed into XTO at V <sub>SUPA</sub> = 2.2 V	хто	1.25		2.2	
	Clock amplitude of external clock fed into XTO at V <sub>SUPA</sub> = 2.7 V		0.75		2.7	
	Clock amplitude of external clock fed into XTO at V <sub>SUPA</sub> = 3.3 V		0.55		3.3	
	Duty cycle	XTI, XTO	45	50	55	%
Crystal Rec	commendations					
T <sub>A</sub>	Ambient operating temperature		-40		70	°C
f <sub>P</sub>	Load resonance frequency at C <sub>I</sub> = 20 pF	XTI, XTO		18.432		MHz
Δf/f <sub>S</sub>	Accuracy of frequency adjust- ment		-50		50	ppm
Δf/f <sub>S</sub>	Frequency variation vs. temperature		-50		50	ppm
R <sub>EQ</sub>	Equivalent series resistance			12	30	Ω
C <sub>0</sub>	Shunt (parallel) capacitance			3	5	pF
1) extended	to 28 MHz by divider 1/1.5 (refer to Ta	able 3–3 on page	20)	1	ı	

<sup>&</sup>lt;sup>1)</sup> extended to 28 MHz by divider 1/1.5 (refer to Table 3–3 on page 20) <sup>2)</sup> depending on mode (refer to Table 4–3)

Table 4–3: Input clock frequency

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit
f <sub>CLK</sub>	MPEG 1 Encoder MPEG Decoder	XTI	11.0			MHz
	MPEG 2 Encoder		13.7			MHz

Table 4-4: Input levels

	Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit
	I <sub>IL</sub>	Input low voltage at V <sub>SUPI2C</sub> = 2.53.9 V	I2CC, I2CD			0.3	V
	I <sub>IH</sub>	Input high voltage at V <sub>SUPI2C</sub> = 2.53.9 V		1.4			V
I	I <sub>IL</sub>	Input low voltage at V <sub>SUPI2C</sub> = 2.53.9 V	POR, DCEN			0.2	V
I	I <sub>IH</sub>	Input high voltage at V <sub>SUPI2C</sub> = 2.53.9 V		0.9			V
	I <sub>ILD</sub>	Input low voltage	PI <i>,</i>			0.3	V
	I <sub>IHD</sub>	Input high voltage	SI(B)I, SI(B)C, <u>SI(B</u> )D, PR, PCS, TE, DVS	V <sub>SUPD</sub> -0.5			V

Table 4–5: Analog input and output recommendations

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit			
Analog Refer	rence								
C <sub>AGNDC1</sub>	Analog filter capacitor	AGNDC	1.0	3.3		μF			
C <sub>AGNDC2</sub>	Ceramic capacitor in parallel			10		nF			
C <sub>PVDD</sub>	Capacitor for analog circuitry	PVDD	3			nF			
Analog Audio	Analog Audio Inputs								
C <sub>inAD</sub>	DC-decoupling capacitor at A/D-converter inputs	INL/R		390		nF			
C <sub>inMI</sub>	DC-decoupling capacitor at microphone-input	MICIN		390		nF			
C <sub>LMICBI</sub>	Minimum-Capacitance at micro- phone bias	MICBI	3.3			nF			
Analog Audio	Analog Audio Filter Outputs								
C <sub>FILT</sub>	Filter capacitor for headphone amplifier high-Q type, NP0 or C0G material	FILTL/R OUTL/R	-20%	470	+20%	pF			
Analog Audio	Output								
Z <sub>AOL_HP</sub>	Analog output load with stereo	OUTL/R	16			Ω			
	headphones			100		pF			
DC/DC-Conv	erter External Circuitry (please re	fer to application	example)						
C <sub>1</sub>	VSENS blocking (<100 mΩ ESR)	VSENS1/2		330		μF			
V <sub>TH</sub>	Schottky diode threshold voltage	DCSO1/2 VSENS1/2		0.39		V			
L	Ferrite core coil inductance	DCSO1/2		22		μH			
S/PDIF Interf	ace Analog Input								
C <sub>SPI</sub>	S/PDIF coupling capacitor	SPDI1/2 SPDIR		100		nF			

# 4.6.3. Digital Characteristics

at T =  $T_A$ ,  $V_{SUPDn}$ ,  $V_{SUPA}$ ,  $V_{SUPX}$  = 2.5 ... 3.6 V,  $f_{Crystal}$  = 18.432 MHz, Typ. values for  $T_A$  = 25 °C, in PMQFP64/PLQFP64 package

	Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
	Digital Sup	ply Voltage						
	I <sub>SUPD1</sub>	Current consumption (MPEG decoding)	VDD, XVDD, I2CVDD		35		mA	2.5 V, sampling frequency ≥ 32 kHz
I			120 V D D		18			2.5 V, sampling frequency ≤ 24 kHz
					10			2.5 V, sampling frequency ≤ 12 kHz
ı	I <sub>SUPD2</sub>	Current consumption (MPEG encoding)			130			3.5 V, sampling frequency ≥ 32 kHz
					63			2.7 V, sampling frequency ≤ 24 kHz
	I <sub>STANDBY</sub>	Total current at stand-by				10	μΑ	DSP off, Codec off, DC /DC off, A/D and D/A off, no I <sup>2</sup> C access
•	Digital Outp	outs and Inputs						
	O <sub>DigL</sub>	Output low voltage	Pl <i>,</i>			0.3	V	I <sub>load</sub> = 2 mA
	O <sub>DigH</sub>	Output low voltage	SOI, SOC, SOD, EOD, PRTR, PRTW, CLKO, SYNC, PUP, SPDO	V <sub>SUPD</sub> -0.3			V	I <sub>load</sub> = −2 mA
ľ	Z <sub>DigI</sub>	Input impedance	all digital Inputs			7	pF	
	I <sub>DLeak</sub>	Digital input leakage current		-1		1	μΑ	0 V < V <sub>pin</sub> < V <sub>SUPD</sub>

# 4.6.3.1. I<sup>2</sup>C Characteristics

at T = 25°C, V<sub>SUPI2C</sub> = 2.5...3.6 V, in PMQFP64/PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions				
I <sup>2</sup> C Input S	<sup>2</sup> C Input Specifications										
f <sub>I2C</sub>	Upper limit I <sup>2</sup> C bus frequency operation	I2CC	400			kHz					
t <sub>I2C1</sub>	I <sup>2</sup> C START condition setup time	I2CC, I2CD	300			ns					
t <sub>I2C2</sub>	I <sup>2</sup> C STOP condition setup time	I2CC, I2CD	300			ns					
t <sub>I2C3</sub>	I <sup>2</sup> C clock low pulse time	I2CC	1250			ns					
t <sub>I2C4</sub>	I <sup>2</sup> C clock high pulse time	I2CC	1250			ns					
t <sub>I2C5</sub>	I <sup>2</sup> C data setup time before rising edge of clock	I2CC	80			ns					
t <sub>I2C6</sub>	I <sup>2</sup> C data hold time after falling edge of clock	I2CC	80			ns					
V <sub>I2COL</sub>	I <sup>2</sup> C output low voltage	I2CC, I2CD			0.4	٧	I <sub>load</sub> = 3 mA				
I <sub>I2COH</sub>	I <sup>2</sup> C output high leakage current	I2CC, I2CD			1	μΑ					
t <sub>I2COL1</sub>	I <sup>2</sup> C data output hold time after falling edge of clock	I2CC, I2CD	20			ns					
t <sub>I2COL2</sub>	I <sup>2</sup> C data output setup time before rising edge of clock	I2CC, I2CD	250			ns	f <sub>I2C</sub> = 400 kHz				
V <sub>I2CIL</sub>	I <sup>2</sup> C input low voltage	I2CC; I2CD			0.3	V <sub>SUPI2C</sub>					
V <sub>I2CIH</sub>	I <sup>2</sup> C input high voltage	I2CC, I2CD	0.6			V <sub>SUPI2C</sub>					
t <sub>W</sub>	Wait time	I2CC, I2CD	0	0.5	4	ms					

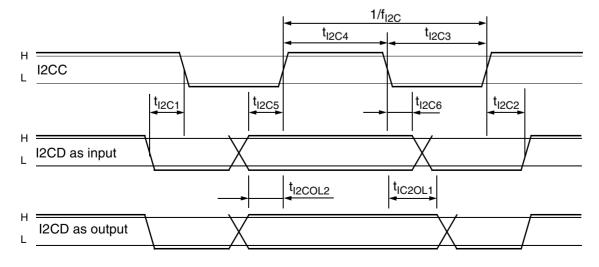


Fig. 4–20: I<sup>2</sup>C timing diagram

PRELIMINARY DATA SHEET MAS 3587F

# 4.6.3.2. Serial (I<sup>2</sup>S) Input Interface Characteristics (SDI, SDIB)

at T =  $T_A$ ,  $V_{SUPDn}$ ,  $V_{SUPX}$  = 2.5 ... 3.6 V,  $f_{Crystal}$  = 18.432 MHz, Typ. values for  $T_A$  = 25 °C, in PMQFP64/ PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
<sup>t</sup> siclk	I <sup>2</sup> S clock input clock period	SI(B)C		325		ns	f <sub>S</sub> = 48 kHz Stereo, 32 bits per sample (for demand mode see Table 4–6 on page 64)
t <sub>SIDS</sub>	I <sup>2</sup> S data setup time before rising edge of clock (for continuous data stream: falling edge)	SI(B)C, SI(B)D	50			ns	
t <sub>SIDH</sub>	I <sup>2</sup> S data hold time	SI(B)D	50			ns	
t <sub>SIIS</sub>	I <sup>2</sup> S ident setup time before rising edge of clock (for continuous data stream: falling edge)	SI(B)C, SI(B)I	50			ns	
t <sub>SIIH</sub>	I <sup>2</sup> S ident hold time	SI(B)I	50			ns	
t <sub>bw</sub>	Burst wait time	SI(B)C, SI(B)D	480				

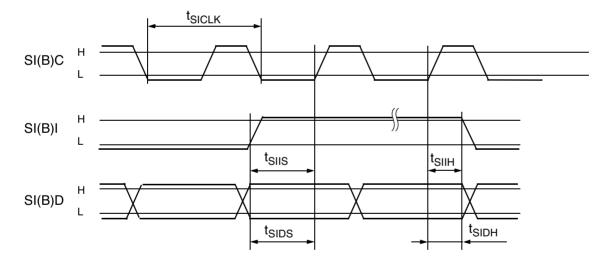


Fig. 4–21: Serial input of I<sup>2</sup>S signal

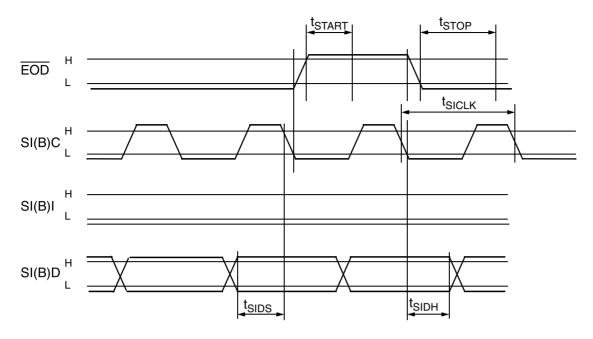


Fig. 4–22: Continuous data stream at serial input A or B. In this mode, the word strobe SI(B)I is not used and the data are read at the falling edge of the clock (bit 2 in D0:7F1 is set).

**Table 4–6:** Maximum allowed sample clock frequency in Demand Mode

f <sub>Sample</sub> (kHz)	f <sub>C</sub> max (MHz)	min. t <sub>SICLK</sub> (ns)
48, 32	6.144	162
44.1	5.6448	177
24, 16	3.072	325

**Table 4–6:** Maximum allowed sample clock frequency in Demand Mode

f <sub>Sample</sub> (kHz)	f <sub>C</sub> max (MHz)	min. t <sub>SICLK</sub> (ns)
22.05	2.8224	354
12, 8	1.536	651
11.025	1.4112	708

Micronas Micronas

Table 4-7: Allowed transmission delays of external data source

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
t <sub>START48-320</sub>	Allowed delay time before start of serial data	EOD			3.1	ms	48 kHz/s, 320 kbit/s
t <sub>START48-64</sub>	transmission after assertion				5.7	ms	48 kHz/s, 64 kbit/s
t <sub>START24-320</sub>	of signal at EOD				4.2	ms	24 kHz/s, 320 kbit/s
t <sub>START24-32</sub>					9.2	ms	24 kHz/s, 32 kbit/s
t <sub>START12-64</sub>					23.1	ms	12 kHz/s, 64 kbit/s
t <sub>START12-16</sub>					25.6	ms	12 kHz/s, 16 kbit/s
t <sub>START8-64</sub>					34.8	ms	8 kHz/s, 64 kbit/s
t <sub>START8-8</sub>					38.4	ms	8 kHz/s, 8 kbit/s
t <sub>STOP</sub>	Allowed delay time before stop of serial data transmission after deassertion of signal at EOD	EOD			1.3	ms	Clock rate of input data 1 Mbit/s

# 4.6.3.3. Serial Output Interface Characteristics (SDO)

at T =  $T_A$ ,  $V_{SUPDn}$ ,  $V_{SUPX}$  = 2.5 ... 3.6 V,  $f_{Crystal}$  = 18.432 MHz, Typ. values for  $T_A$  = 25 °C, in PMQFP64/ PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
tsoclk	I <sup>2</sup> S clock output frequency	soc		325		ns	f <sub>S</sub> = 48 kHz Stereo 32 bits per sample
t <sub>SOISS</sub>	I <sup>2</sup> S word strobe delay time after falling edge of clock	SOC, SOI	0			ns	
t <sub>SOODC</sub>	I <sup>2</sup> S data delay time after falling edge of clock	SOC, SOD	0			ns	

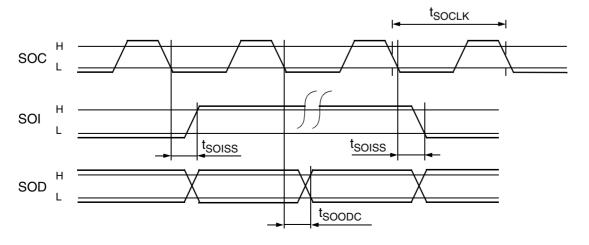
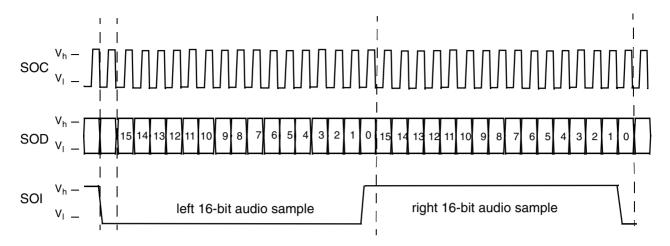
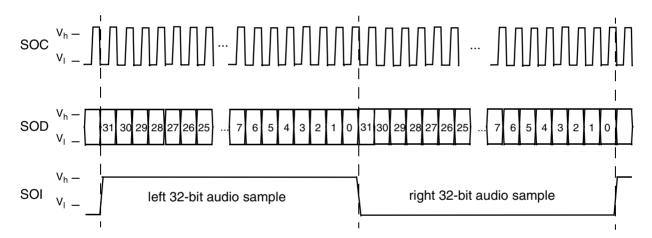


Fig. 4–23: Serial output interface timing.



**Fig. 4–24:** Sample timing of the SDO interface in 16 bit/sample mode. D0:7F1 settings are: Bit 14 = 0 (SOC not inverted), bit 11 = 1 (SOI delay), bit 5 = 0 (word strobe not inverted), bit 4 = 1 (16 bits/sample).



**Fig. 4–25:** Sample timing of the SDO interface in 32 bit/sample mode. D0:7F1 settings are: Bit 14 = 0 (SOC not inverted), bit 11 = 0 (no SOI delay), bit 5 = 1 (word strobe inverted), bit 4 = 0 (32 bits/sample).

## 4.6.3.4. S/PDIF Input Characteristics

at T =  $T_A$ ,  $V_{SUPDn}$ ,  $V_{SUPA}$ ,  $V_{SUPX}$  = 2.5 ... 3.6 V,  $f_{Crystal}$  = 18.432 MHz, Typ. values for  $T_A$  = 25 °C, in PMQFP64/PLQFP64 package.

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
V <sub>S</sub>	Signal amplitude	SPDI1, SPDI2, SPDIR	200	500	1000	mV <sub>pp</sub>	
f <sub>s1</sub>	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.048		MHz	±1000 ppm, f <sub>s</sub> = 48 kHz
f <sub>s2</sub>	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.822		MHz	±1000 ppm, f <sub>s</sub> = 44.1 kHz
f <sub>s3</sub>	Bi-phase frequency	SPDI1, SPDI2, SPDIR		3.072		MHz	$\pm 1000$ ppm, f <sub>s</sub> = 32 kHz
t <sub>P</sub>	Bi-phase period	SPDI1, SPDI2, SPDIR		326		ns	at f <sub>s</sub> = 48 kHz, (highest sampling rate)
t <sub>R</sub>	Rise time	SPDI1, SPDI2, SPDIR	0		65	ns	at f <sub>s</sub> = 48 kHz, (highest sampling rate)
t <sub>F</sub>	Fall time	SPDI1, SPDI2, SPDIR	0		65	ns	at f <sub>s</sub> = 48 kHz, (highest sampling rate)
	Duty cycle	SPDI	40	50	60	%	at bit value = 1 and $f_s = 48 \text{ kHz}$
t <sub>H1,L1</sub>		SPDI	81		163	ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f <sub>s</sub> = 48 kHz
t <sub>H0,L0</sub>		SPDI	163		244	ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f <sub>s</sub> = 48 kHz

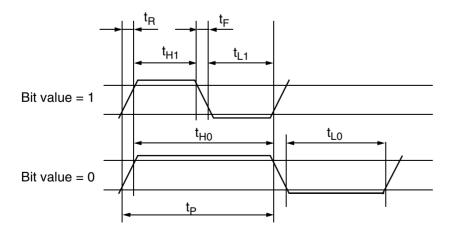


Fig. 4–26: Timing of the S/PDIF input

## 4.6.3.5. S/PDIF Output Characteristics

at T =  $T_A$ ,  $V_{SUPDn}$ ,  $V_{SUPA}$ ,  $V_{SUPx}$  = 2.5 ... 3.6 V,  $f_{Crystal}$  = 18.432 MHz, Typ. values for  $T_A$  = 25 °C, in PMQFP64/PLQFP64 package.

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
f <sub>s1</sub>	Bi-phase frequency	SPDO		3.072		MHz	f <sub>s</sub> = 48 kHz
f <sub>s2</sub>	Bi-phase frequency	SPDO		2.822		MHz	f <sub>s</sub> = 44.1 kHz
f <sub>s3</sub>	Bi-phase frequency	SPDO		2.048		MHz	f <sub>s</sub> = 32 kHz
t <sub>P</sub>	Bi-phase period	SPDO		326		ns	at f <sub>s</sub> = 48 kHz, (highest sampling rate)
t <sub>R</sub>	Rise time	SPDO	0		2	ns	C <sub>load</sub> = 10 pF
t <sub>F</sub>	Fall time	SPDO	0		2	ns	C <sub>load</sub> = 10 pF
	Duty cycle	SPDO		50		%	
t <sub>H1,L1</sub>		SPDO		163		ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f <sub>s</sub> = 48 kHz
t <sub>H0,L0</sub>		SPDO		326		ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f <sub>s</sub> = 48 kHz
V <sub>S</sub>	Signal amplitude	SPDO		V <sub>SUPD</sub>			

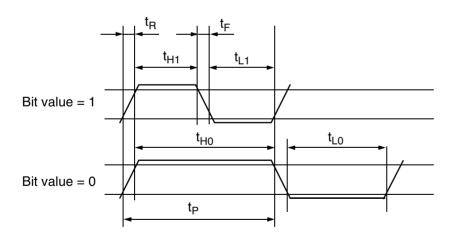


Fig. 4-27: Timing of the S/PDIF output

### 4.6.3.6. PIO as Parallel Input Interface: DMA Mode

In decoding mode, the data transfer can be started after the EOD pin of the MAS 3587F is set to "high". After verifying this, the controller signalizes the sending of data by activating the PR line. The MAS 3587F responds by setting the RTR line to the "low" level and reads the data at PI[19:12]. After RTR is set to high again, the controller sets PR to low. The next data word write operation will be initialized again by setting the PR line via the controller. Please refer to Figure 4–28 for the exact timing

The procedure above will be repeated until the MAS 3587F sets the EOD signal to "0" which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to "0", wait until EOD rises again and then repeat the procedure to send the next block of data. The DMA buffer is 30 bytes long.

Table 4-8: DMA input timing

Symbol	Pin Name	Min.	Max.	Unit
t <sub>st</sub>	PR, EOD	OD 0.010 2000		μs
t <sub>r</sub>	PR, RTR	R 40 160		ns
t <sub>pd</sub>	PR, PI[19:12]	120	480	ns
t <sub>set</sub>	PI[19:12]	160		ns
t <sub>h</sub>	PI[19:12]	160		ns
t <sub>rtrq</sub>	RTR	200	30000	ns
t <sub>pr</sub>	PR	480		ns
t <sub>rpr</sub>	PR, RTR	160	160	
t <sub>eod</sub>	PR, EOD	40 160		ns
t <sub>eodq</sub>	EOD	2.5 500		μs

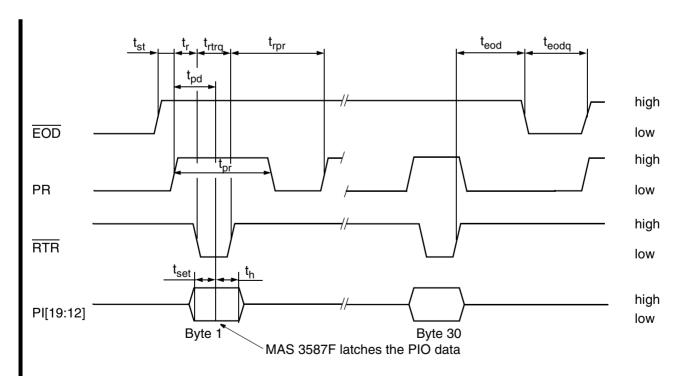


Fig. 4-28: Handshake protocol for writing MPEG data to the PIO-DMA

# 4.6.3.7. PIO As Parallel Input Interface: Program Download Mode

Handshaking for PIO input in Program Download Mode is accomplished through the RTR, PCS, and PI12..PI19 signal lines (see Fig. 4–29). The PR line should be set to low level.

The MAS 3587F will drive RTR low as soon as it is ready to receive a byte and RTR will stay low until one byte has been written. Writing of a byte is performed with a PCS pulse, driven by the microcontroller. The MAS 3587F reads data after the falling edge of PCS and will finish the cycle by setting RTR to high level after the rising edge of PCS. The next data transfer initialized by the MAS 3587F by driving the RTR line.

Table 4-9: PIO Program Download Mode timing

Symbol	Pin Name	Min.	Max.	Unit
t <sub>0</sub>	RTR, PCS	0		μs
t <sub>1</sub>	PCS	150	50	
t <sub>2</sub>	PCS, RTR	0	30	ns
t <sub>3</sub>	RTR	0.4	5	μs
t <sub>4</sub>	PI	50		ns
t <sub>5</sub>	PI	50		ns

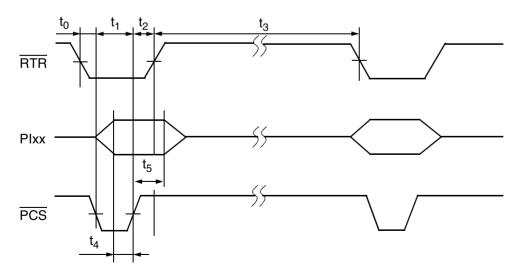


Fig. 4-29: Input timing for Program Download Mode

# 4.6.3.8. PIO as Parallel Output Interface: DMA Mode

In encoding mode, the MAS 3587F signals available data by setting the EOD pin to "high". After verifying this, the controller signalizes its capability to receive one byte of data by activating the PR line. The MAS 3587F responds by setting the RTW line to the "low" level when the actual byte is set on the data lines PI[19:12]. After PR is set to "low" level, the RTW line is set to "high" again. The next data word write operation will be initialized again by setting the PR line via the controller. Please refer to Figure 4–30 for the exact timing.

The procedure above will be repeated until the MAS 3587F sets the EOD signal to "0" which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to "0", wait until EOD rises again and then repeat the procedure to receive the next block of data. The DMA buffer is currently 30 bytes long.

In order to transfer the worst case data rate of 192 kbit/s, the controller must react sufficiently fast. The mean response times (t0, t3, t5) must be faster than 10 ms. Due to internal buffering in the MAS 3587F, this time can be expanded up to 4.8 ms once within each frame (see Table 2–2 on page 16) in any case.

Table 4–10: PIO output mode timing

Symbol	Pin Name	Min.	Max.	Unit
t <sub>0</sub>	EOD, PR	0.010	2000	μs
t <sub>1</sub>	PR, PI	110	310	ns
t <sub>2</sub>	PI, RTW	18	55	ns
t <sub>3</sub>	RTW, PR	18		ns
t <sub>4</sub>	PR, RTW	90	260	ns
t <sub>5</sub>	RTW, PR	35		ns
t <sub>eod</sub>		140	8000	ns
t <sub>eodq</sub>		2.5		μs

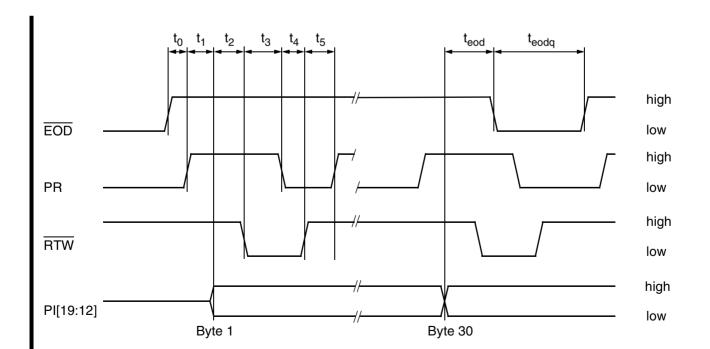


Fig. 4-30: Handshake protocol for reading MPEG data from the PIO-DMA

# 4.6.4. Analog Characteristics

at T =  $T_A$   $V_{SUPDn}$ ,  $V_{SUPx}$  = 2.5...3.6 V,  $V_{SUPA}$  = 2.2 ... 3.6 V,  $f_{Crystal}$  = 13...20 MHz, typical values at  $T_A$  = 25 °C and  $f_{CRYSTAL}$  = 18.432 MHz, in PMQFP64/PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Co	nditions
Analog Su	oply							
I <sub>AVDD</sub>	Current consumption analog audio	AVDD0/1		5		mA	V <sub>SUPA</sub> = 2.2 V, Mute	
I <sub>QOSC</sub>	Current consumption crystal oscillator	AVDD0/1		200		μΑ	Codec = off DSP = off DC/DC = on	
I <sub>STANDBY</sub>					10		Codec = DSP = o DC/DC =	ff
Crystal Os	cillator							
V <sub>DCCLK</sub>	DC voltage at oscillator pins	XTI, XTO		0.5		V <sub>SUPA</sub>		
V <sub>ACLK</sub>	Clock amplitude		0.5		V <sub>SUPA</sub> -0.5	V <sub>PP</sub>	if crystal is used	
C <sub>IN</sub>	Input capacitance			3		pF		
R <sub>OUT</sub>	Output resistance	хто		220		Ω	V <sub>SUPA</sub> =	2.2 V
				125			V <sub>SUPA</sub> = 2.7 V	
				94			V <sub>SUPA</sub> =	3.3 V
Analog Ref	ferences							
V <sub>AGNDC</sub>	Analog Reference Voltage	AGNDC				V	R <sub>L</sub> >> 10 referred	$0\mathrm{M}\Omega,$ to VREF
							V <sub>SUPA</sub>	Bits 15, 14 in Reg. 6A <sub>hex</sub>
				1.1			>2.2 V	00
				1.3			>2.4 V	01
				1.6			>3.0 V	10
V <sub>MICBI</sub>	Bias voltage for microphone	MICBI					V <sub>SUPA</sub>	Bits 15, 14 in Reg. 6A <sub>hex</sub>
				1.8			>2.2 V	00
				2.13			>2.4 V	01
				2.62			>3.0 V	10
R <sub>MICBI</sub>	Source resistance	MICBI		180		Ω		
I <sub>MAX</sub>	Maximum current microphone bias	MICBI				μΑ	V <sub>SUPA</sub>	Bits 15, 14 in Reg. 6A <sub>hex</sub>
				300			>2.2 V	00

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions		
Analog Au	idio Inputs	•					•		
V <sub>AI</sub>	Analog line input clipping level (at minimum analog input gain,i.e. –3 dB)	INL/R				V <sub>pp</sub>	V <sub>SUPA</sub>	Bits 15, 14 in Reg. 6A <sub>hex</sub>	
				2.2			>2.2 V	00	
				2.6			>2.4 V	01	
				3.2			>3.0 V	10	
V <sub>MI</sub>	Microphone input clipping level (at minimum analog	MICIN				mV <sub>pp</sub>	V <sub>SUPA</sub>	Bits 15,14 in Reg. 6A <sub>hex</sub>	
	input gain, i.e. +21 dB)			141			>2.0 V	00	
				167			>2.4 V	01	
				282			>3.0 V	10	
R <sub>inAl</sub>	Analog line input resistance	INL/R		97		kΩ	at minim gain, i.e.	um analog input –3 dB	
				20				num analog input +19.5 dB	
				67			not selec	eted	
R <sub>inMI</sub>	Microphone input resistance	MICIN		94		kΩ	at minim gain, i.e.	um analog input –21 dB	
				8				num analog input +43.5 dB	
				94			not selec	eted	
SNR <sub>AI</sub>	Signal-to-noise ratio of line input	INL/R		74		dB(A)	BW = 20 Hz20 kHz, analog gain = 0 dB, input 1 kHz at V <sub>AI</sub> –20 dB		
SNR <sub>MI</sub>	Signal-to-noise ratio of microphone input	MICIN		73		dB(A)	analog g	Hz20 kHz, ain = +21 dB, Hz at V <sub>MI</sub> –20 dB	
THD <sub>AI</sub>	Total harmonic distortion of analog inputs	INL/R MICIN		0.01	0.02	%	analog g resp. 24 input 1 k	Hz at 5 = V <sub>AI</sub> –6 dB	
XTALK <sub>AI</sub>	Crosstalk attenuation left/right channel (analog inputs)	INL/R MICIN		80		dB		z, sine wave, ain = 0 dB, ·3 dBFS	
PSRR <sub>AI</sub>	Power supply rejection ratio for analog audio inputs	AVDD0/1, INL/R MICIN		45		dB	1 kHz sir	ne at 100 mV <sub>rms</sub>	
				20		dB	≤100 kH: 100 mV <sub>ri</sub>		

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
Audio Out	out			•		•	<u> </u>
V <sub>AO1</sub>	Analog output voltage AC	OUTL/R					$\begin{aligned} &R_L{\ge}1 \text{ k}\Omega\\ &\text{Input} = 0 \text{ dBFS digital}\\ &V_{SUPA} &\text{Bits 15, 14}\\ &\text{in Reg } 6A_{\text{hex}} \end{aligned}$
	at 0 dB output gain			1.56		V <sub>pp</sub>	>2.2 V 00
				1.84			>2.4 V 01
				2.27			>3.0 V 10
	at +3 dB output gain			2.20		V <sub>pp</sub>	>2.2 V 00
				2.60			>2.6 V 01
				3.20			>3.2 V 10
dV <sub>AO1</sub>	Deviation of DC-level at analog output for AGNDC-voltage	OUTL/R	-20		20	mV	
V <sub>AO2</sub>	Analog output voltage AC	OUTL/R					$R_L$ is 16 $\Omega$ Headphone and 22 $\Omega$ series resistor Input = 0 dBFS digital
							(see Fig. 4–34 on page 81)
							V <sub>SUPA</sub> Bits 15, 14 in Reg 6A <sub>hex</sub>
	at 0 dB output gain			1.56		V <sub>pp</sub>	>2.2 V 00
				1.84			>2.4 V 01
				2.27			>3.0 V 10
	at +3 dB output gain			2.00		V <sub>pp</sub>	>2.2 V 00
				2.40			>2.6 V 01
				3.00			>3.2 V 10
R <sub>outAO</sub>	Analog output resistance	OUTL/R			6	Ω	analog gain = +3 dB, Input = 0 dBFS digital
SNR <sub>AO</sub>	Signal-to-noise ratio of analog output	OUTL/R		94		dB(A)	$R_L$ ≥16 Ω BW = 20 Hz20 kHz, analog gain = 0 dB input = −20 dBFS
THD <sub>AO</sub>	Total harmonic distortion (headphone)	OUTL/R		0.03	0.05	%	for R <sub>L</sub> $\geq$ 16 $\Omega$ plus 22 $\Omega$ series resistor (see Fig. 4–34 on page 81)
				0.003	0.01	%	for R <sub>L</sub> ≥1 kΩ
Lev <sub>MuteAO</sub>	Mute level	OUTL/R		-113		dBV	A-weighted BW = 20 Hz22 kHz , no digital input signal, analog gain = mute

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
XTALK <sub>AO</sub>	Crosstalk attenuation left/right channel (headphone)	OUTLR		80		dB	f=1 kHz, sine wave, OUTL/R: $R_L \ge 16 \Omega$ (see Fig. 4–34 on page 81) analog gain = 0 dB input = -3 dBFS
PSRR <sub>AO</sub>	Power supply rejection ratio for analog audio outputs	AVDD0/1 OUTL/R		70		dB	1 kHz sine at 100 mV <sub>rms</sub>
				35		dB	≤100 kHz sine at 100 mV <sub>rms</sub>

#### 4.6.5. DC/DC Converter Characteristics

at T =  $T_A$ ,  $V_{in}$  = 1.2 V,  $V_{outn}$  = 3.0 V,  $f_{clk}$  = 18.432 MHz,  $f_{sw}$  = 384 kHz, PWM-mode, L = 22  $\mu$ H, in PMQFP64/PLQFP64 package (unless otherwise noted) Typ. values for  $T_A$  = 25 °C

Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
V <sub>IN</sub>	Minimum start-up input voltage	*		0.9		V	I <sub>LOAD</sub> ≤ 1 mA, DCCF = 5050 <sub>hex</sub> (reset)
V <sub>IN</sub>	Minimum operating input voltage						1)
	DC1 DC2			0.7 0.8		V	I <sub>LOAD</sub> = 50 mA, DCCF = 5050 <sub>hex</sub> (reset)
	DC1 DC2			1.1 1.2		V	I <sub>LOAD</sub> = 200 mA, DCCF = 5050 <sub>hex</sub> (reset)
V <sub>OUT</sub>	Programmable output voltage range	VSENSn	2.0		3.5	V	Voltage settings in DCCF register (I <sup>2</sup> C subaddress 76 <sub>hex</sub> )
V <sub>OTOL</sub>	Output voltage tolerance	VSENSn	-4		4	%	$I_{LOAD} = 20 \text{ mA}$ $T_A = 25 ^{\circ}\text{C}^{2)}$
I <sub>LOAD1</sub>	Output current 1 battery cell	VSENSn			200	mA	V <sub>IN</sub> = 0.91.5 V, 330 μF
I <sub>LOAD2</sub>	Output current 2 battery cells				600	mA	V <sub>IN</sub> = 1.83.0 V, 330 μF
dV <sub>OUT</sub> / dV <sub>IN</sub> /V <sub>OUT</sub>	Line regulation	VSENSn		0.7		%/V	I <sub>LOAD</sub> = 20 mA
dV <sub>OUT</sub> / V <sub>OUT</sub>	Load regulation	VSENSn		-1.8		%	I <sub>LOAD</sub> = 20200 mA
h <sub>max</sub>	Maximum efficiency			95		%	V <sub>IN</sub> = 2.4 V, V <sub>OUT</sub> = 3.5 V
f <sub>switch</sub>	Switching frequency	DCSOn	297	384	576	kHz	(see Section 2.9.2. on page 12), (see Table 3–3 on page 20)
f <sub>startup</sub>	Switching frequency during start-up	DCSOn		250		kHz	VSENSn < 1.9 V
I <sub>supPFM1</sub>	Supply current in PFM mode	VSENS1		75		μΑ	3)
I <sub>supPFM2</sub>		VSENS2		135			
I <sub>supPWM1</sub>	Supply current in PWM mode	VSENS1		265		μΑ	VSENSn
I <sub>supPWM2</sub>		VSENS2		325			4)
I <sub>Inmax</sub>	NMOS switch current limit (low side switch)	DCSOn, DCSGn		1		A	PWM-mode
				0.4			PFM-mode
I <sub>lptoff</sub>	PMOS switch turnoff current (rectifier switch)	DCSOn, VSENSn		70		mA	
R <sub>ON</sub>	NMOS switch on resistance (low side switch)	DCSO1, DCSG1		170		mΩ	
		DCSO2, DCSG2		280			

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Symbol	Parameter	Pin Name	Min.	Тур.	Max.	Unit	Test Conditions
I <sub>LEAK</sub>	Leakage current	DCSOn, DCSGn		0.1		μΑ	Converters off, no load

<sup>1)</sup> Since the regulators are bootstrapped, once started they will operate down to 0.7 V input voltage 2) PFM-mode regulates aprox. 1% higher 3) Current into VSENSn Pin. VIN > VOUT+0.4 V; no DC/DC-Converter switching action present 4) Add. current of oscillator at PIN AVDD0/1, (see Section 4.6.4. on page 72)

#### 4.6.6. Typical Performance Characteristics

## **Efficiency vs. Load Current** DCDC1 (V<sub>OUT</sub> = 3.5 V) 100 80 Efficiency (%) 60 V<sub>IN</sub>: 40 1.8 V **PFM** 20

# 100 80 Efficiency (%) 60 40 20 $10^{-4}$ $10^{-4}$ $10^{-3}$ $10^{-2}$ $10^{-1}$ Load Current (A)

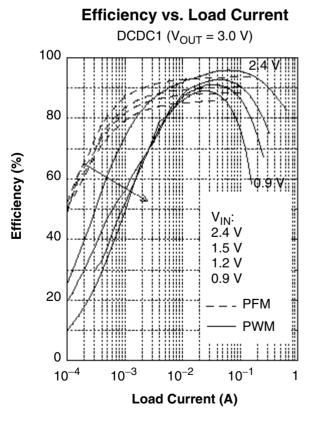
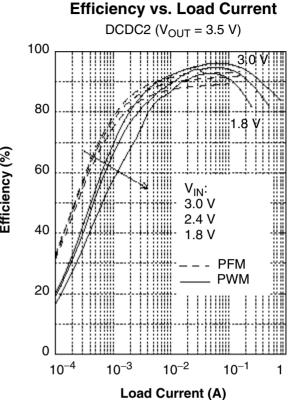
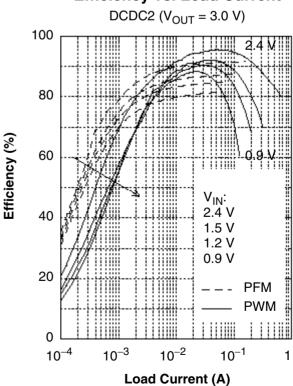
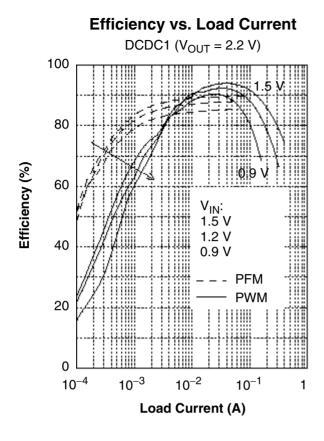


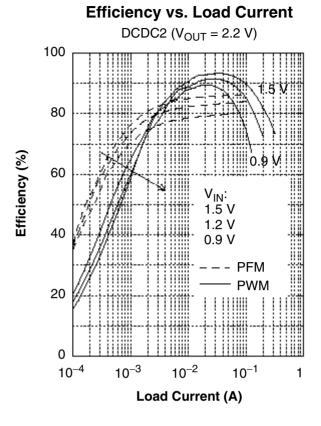
Fig. 4-31: Efficiency vs. Load Current

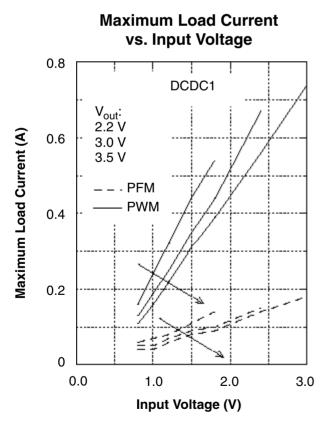


### **Efficiency vs. Load Current**









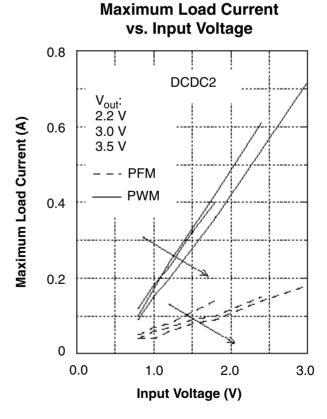
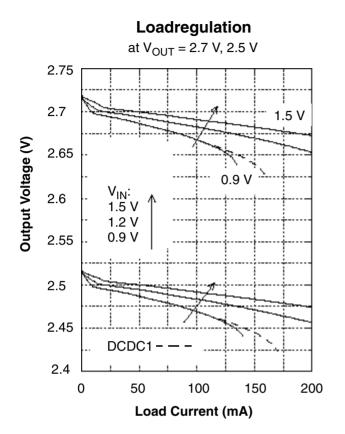


Fig. 4-32: Maximum Load Current vs. Input Voltage

**Note**: Efficiency is measured as  $V_{SENSn} \times I_{LOAD} / (V_{in} \times I_{in})$ .  $I_{AVDD}$  is not included (Oscillator current)



### Loadregulation at $V_{OUT} = 3.0 \text{ V}, 3.5 \text{ V}$ 3.55 3.5 1.5 V Output Voltage (V) 3.45 0.9 V V<sub>IN</sub>: 1.5 V 3.4 1.2 V 0.9 V 3.05 3.0 2.95 2.9 0 50 100 150 200 Load Current (mA)

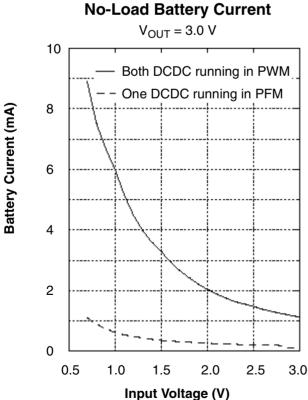
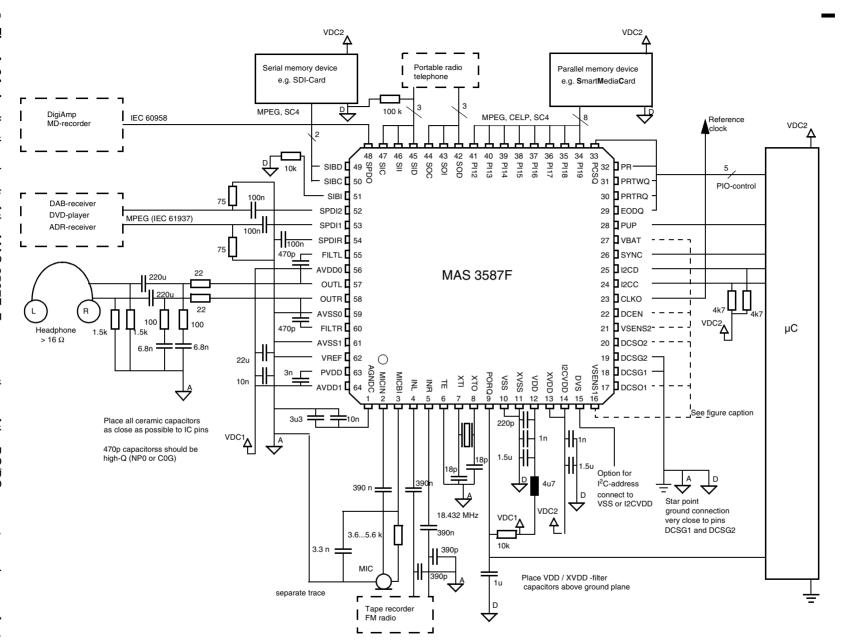


Fig. 4-33: Loadregulation

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# Typical Application in a Portable Player

- MMC/SDI-Card or SMC/CF2+ used as storage media Dashed lines show optional (external) devices



**Fig. 4–34:** Application circuit of the MAS 3587F. For connections of the DC/DC converters, please refer to Fig. 4–35 on page 82. page

#### 4.8. Recommended DC/DC Converter Application Circuit

Configuration 1 (see Fig. 2-11 on page 14)

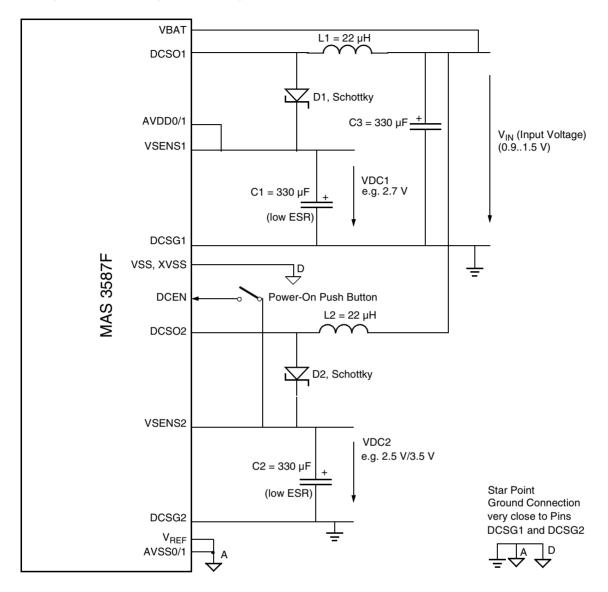


Fig. 4-35: External circuitry for the DC/DC converters

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#### 5. Data Sheet History

- 1. Preliminary data sheet: "MAS 3587F MPEG Layer 3 Audio Encoder/Decoder", July 9, 2001, 6251-542-1PD. First release of the preliminary data sheet.
- 2. Preliminary data sheet: "MAS 3587F MPEG Layer 3 Audio Encoder/Decoder", Nov. 7, 2001, 6251-542-2PD. Second release of the preliminary data sheet. Major changes:
- definition of ambient operating temperature range  $T_{\text{A}}$  specified

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