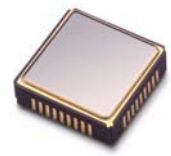
GENERAL DESCRIPTION

The M2040 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for clock protection, frequency translation and jitter attenuation in fault tolerant computing applications. It features dual differential inputs with two modes of input selection: manual and automatic upon clock failure. The clock multiplication ratios and output divider ratio are pin selectable. External loop components allow the tailoring of PLL loop response.



FEATURES

- **Integrated SAW (surface acoustic wave) delay line; VCSO frequency of 400.00 or 533.3334 MHz;* outputs VCSO frequency or half; pin-configurable dividers**
- **Loss of Lock (LOL) indicator output**
- **Narrow Bandwidth control input (NBW Pin); Initialization (INIT) input overrides NBW at power-up**
- **Dual reference clock inputs support LVDS, LVPECL, LVCMOS, LVTTL**
- **Automatic (non-revertive) reference clock reselection upon clock failure; controlled PLL slew rate ensures normal system operation during reference reselection**
- **Acknowledge pin indicates the actively selected reference input**
- **Dual differential LVPECL outputs**
- **Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Industrial temperature available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

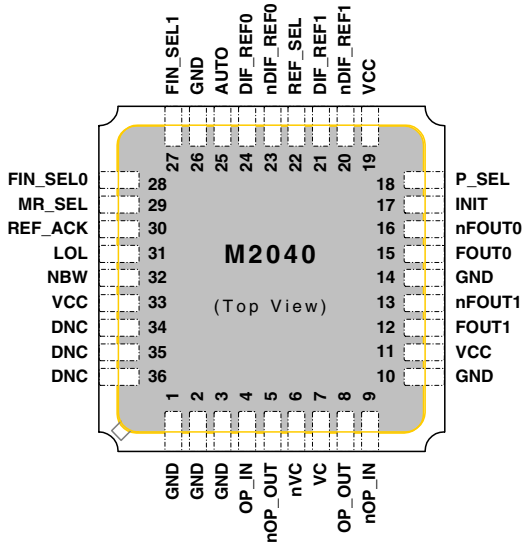


Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input (MHz)	VCSO * (MHz)	Output (MHz)
200.0000	400.0000	200.0000
213.3333		400.0000
266.6667	533.3334	266.6667
284.4444		533.3334

Table 1: Example Input / Output Frequency Combinations

* Specify VCSO center frequency at time of order.

SIMPLIFIED BLOCK DIAGRAM

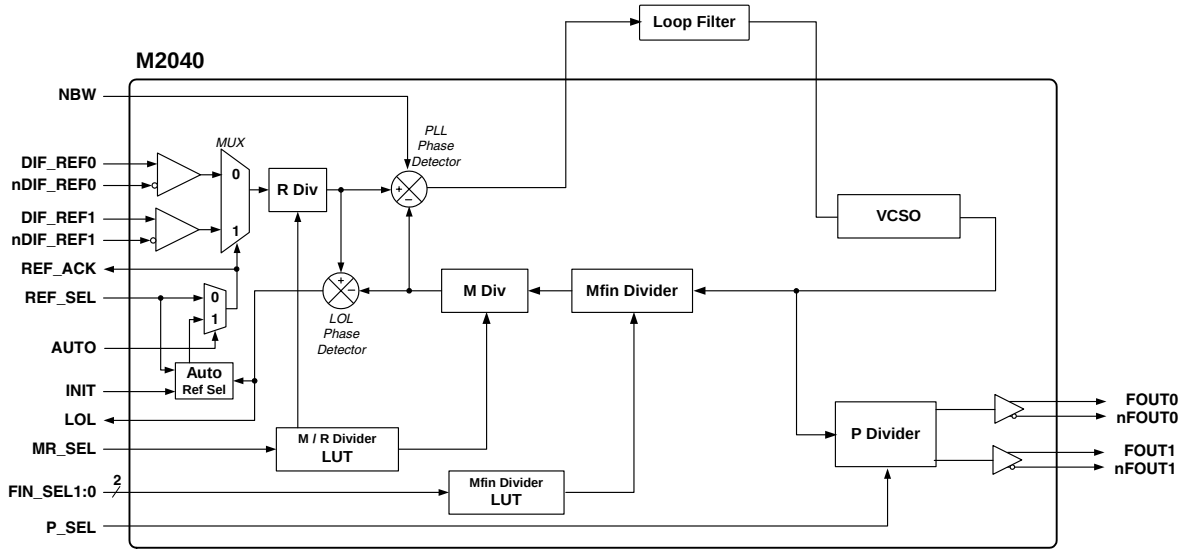


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 7.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT1 nFOUT1	Output	No internal terminator	Clock output pair 1. Differential LVPECL.
15 16	FOUT0 nFOUT0	Output	No internal terminator	Clock output pair 0. Differential LVPECL.
17	INIT	Input	Internal pull-UP resistor[1]	Power-on Initialization; LVCMOS/LVTTL: Logic 1 allows device to enter narrow mode if selected (in addition must have 8 LOL=0 counts) Logic 0 forced device into wide bandwidth mode.
18	P_SEL		Internal pull-down[1]	Post-PLL , P divider selection. LVCMOS/LVTTL. See Table 5, P Divider Selector Values and Frequencies, on pg. 3.
20	nDIF_REF1	Input	Biased to Vcc/2 [2]	Reference clock input pair 1. Differential LVPECL/ LVDS
21	DIF_REF1		Internal pull-down resistor[1]	Reference clock input pair 1. Differential LVPECL/ LVDS, or single ended LVCMOS/ LVTTL
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL. Logic 1 selects DIF_REF1/nDIF_REF1 inputs Logic 0 selects DIF_REF0/nDIF_REF0 inputs
23	nDIF_REF0	Input	Biased to Vcc/2 [2]	Reference clock input pair 0. Differential LVPECL/ LVDS
24	DIF_REF0		Internal pull-down resistor[1]	Reference clock input pair 0. Differential LVPECL/ LVDS, or single ended LVCMOS/ LVTTL
25	AUTO	Input	Internal pull-down resistor[1]	Automatic/manual reselection mode for clock input: Logic 1 automatic reselection upon clock failure (non-revertive) Logic 0 manual selection only (using REF_SEL)
27 28	FIN_SEL1 FIN_SEL0	Input	Internal pull-UP resistor[1]	Input clock frequency selection. LVCMOS/LVTTL. (For FIN_SEL1:0, see Table 3 on pg. 3.)
29	MR_SEL	Input	Internal pull-UP resistor[1]	M & R PLL divider ratio selection. LVCMOS/ LVTTL. (For MR_SEL, see Table 4 on pg. 3.)
30	REF_ACK	Output		Reference Acknowledgement pin for input mux state; outputs the currently selected reference input pair: Logic 1 indicates nDIF_REF1, DIF_REF1 Logic 0 indicates nDIF_REF0, DIF_REF0
31	LOL	Output		Loss of Lock indicator output. [3] Logic 1 indicates loss of lock. Logic 0 indicates locked condition.
32	NBW	Input	Internal pull-UP resistor[1]	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, R_{IN} = 2100kΩ Logic 0 - Wide (normal) bandwidth, R_{IN} = 100kΩ
34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see **DC Characteristics** on pg. 8.
Note 2: Biased to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. Float if using DIF_REF1 as LVCMOS input. See **DC Characteristics** on pg. 8.
Note 3: See LVCMOS Outputs in DC Characteristics on pg. 8.

DETAILED BLOCK DIAGRAM

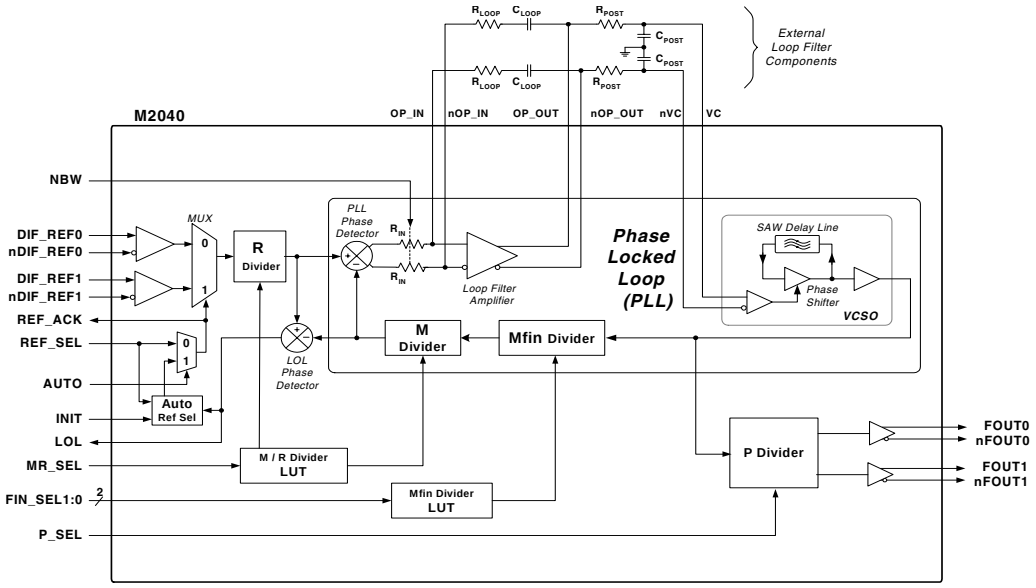


Figure 3: Detailed Block Diagram

PLL DIVIDER SELECTION TABLES

Mfin (Frequency Input) Divider Look-Up Table (LUT)

The FIN_SEL1:0 pins select the feedback divider value ("Mfin").

FIN_SEL1:0	Mfin Value
1 1	1
1 0	4
0 1	8
0 0	32

Table 3: Mfin (Frequency Input) Divider Look-Up Table (LUT)

M / R Divider Ratio Look-up Table (LUT)

The MR_SEL pin selects the feedback and reference divider values M and R, respectively.

MR_SEL	M R	Description
0	32 16	Used when Fin = 32/16 = 1/2 Fvcso (e.g., Fin=266.6667MHz, Fvcso= 533.3334MHz[1])
1	30 16	Used when Fin = 30/16 = 0.53334 Fvcso (e.g., Fin=284.444MHz, Fvcso= 533.3334 MHz [1])

Table 4: M / R Divider Ratio Look-up Table (LUT)

Note 1: Fvcso= Example 533.3334MHz in M2040-01-533.3334.

Post-PLL Divider

The M2040 also features a post-PLL (P) divider for the output clocks. It divides the VCSO frequency to produce one of two selectable output frequencies (1/2 or 1/1 of the VCSO frequency). That selected frequency appears on both clock output pairs. The P_SEL pin selects the value for the P divider.

P_SEL	P Value	Example: M2040-533.3334 Output Frequency (MHz)
1	2	266.6667
0	1	533.3334

Table 5: P Divider Selector Values and Frequencies

FUNCTIONAL DESCRIPTION

The M2040 is a PLL (Phase Locked Loop) based clock generator that generates two output clocks synchronized to one of two selectable input reference clocks. An internal high “Q” SAW delay line provides a low jitter clock output.

The device is pin-configured for feedback divider and output divider values. Output is LVPECL compatible. External loop filter component values set the PLL bandwidth to optimize jitter attenuation characteristics.

The device features dual differential inputs with two input selection modes: manual and automatic upon clock failure. (The differential inputs are internally configured for easy single-ended operation.)

The M2040 includes: a Loss of Lock (LOL) indicator, a reference mux state acknowledge pin (REF_ACK), a Narrow Bandwidth control input pin (NBW pin), and a Power-on Initialization (INIT) input (which overrides NBW=0 to facilitate acquisition of phase lock).

Hitless Switching (HS) is an optional feature that provides a controlled output clock phase change during a reference clock reselection. HS is triggered by a Loss of Lock detection by the PLL.

Input Reference Clocks

Two clock reference inputs and a selection mux are provided. Either reference clock input can accept a differential clock signal (such as LVPECL or LVDS) or a single-ended clock input (LVCMOS or LVTTL on the non-inverting input).

A single-ended reference clock on the unselected reference input can cause an increase in output clock jitter. For this reason, differential reference inputs are preferred; interference from a differential input on the non-selected input is minimal.

Configuration of a single-ended input has been facilitated by biasing nDIF_REF0 and nDEF_REF1 to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. The input clock structure, and how it is used with either LVCMOS/LVTTL inputs or a DC- coupled LVPECL clock, is shown in Figure 4.

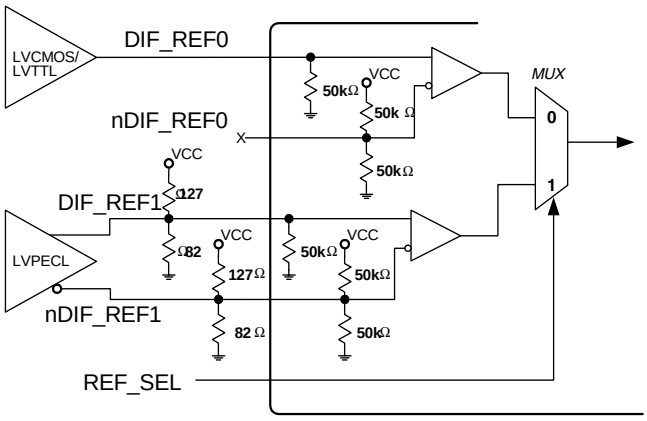


Figure 4: Input Reference Clocks

Differential Inputs

Differential LVPECL inputs are connected to both reference input pins in the usual manner. The external load termination resistors shown in Figure 4 (the 127Ω and 82Ω resistors) is ideally suited for both AC and DC coupled LVPECL reference clock lines. These provide the 50Ω load termination and the VTT bias voltage.

Single-ended Inputs

Single-ended inputs (LVCMOS or LVTTL) are connected to the non-inverting reference input pin (DIF_REF0 or DIF_REF1). The inverting reference input pin (nDIF_REF0 or nDIF_REF1) must be left unconnected.

In single-ended operation, when the unused inverting input pin (nDIF_REF0 or nDEF_REF1) is left floating (not connected), the input will self-bias at VCC/2.

PLL Operation

The M2040 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The “M” divider (and the “Mfin” divider) divides the VCSO output frequency, feeding the result into the plus input of the phase detector.

The frequency input (“Mfin”) divider gives the device the capability to be adapted for use with other input frequencies.

The output of the “R” divider is fed into the minus input of the phase detector. The phase detector compares its two inputs. The phase detector output, filtered externally, causes the VCSO to increase or decrease in frequency as needed to phase- and frequency-lock the VCSO to the reference input.

The value of M plus Mfin directly affects closed loop bandwidth.

The relationship between the nominal VCSO center frequency (Fvcso), the M divider, and the input reference frequency (Fref_clk) is:

$$Fvcso = Fref\_clk \times \frac{M \times Mfin}{R}$$

The M, R, and Mfin dividers can be set by pin configuration using the input pins MR_SEL, FIN_SEL1, and FIN_SEL0.

P Divider and Outputs

The M2040 provides two differential LVPECL output pairs: FOUT0 and FOUT1. One output divider (the “P” divider) is used for both the FOUT0 and FOUT1 output pairs. By using the P divider, the output frequency can be the VCSO frequency (Fvcso) or 1/2 Fvcso.

The P_SEL pin selects the value for the P divider: logic 1 sets P to divide-by-2, logic 0 sets P to divide-by-1.

See Table 5, P Divider Selector Values and Frequencies, on pg. 3.

When the P divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{P} = Fref\_clk \times \frac{M \times Mfin}{R \times P}$$

Loss of Lock Indicator Output Pin

Under normal device operation, when the PLL is locked, LOL remains at logic 0. Under circumstances when the VCSO cannot lock to the input (as measured by a greater than 4 ns discrepancy between the feedback and reference clock rising edges at the phase detector) the LOL output goes to logic 1. The LOL pin will return back to logic 0 when the phase detector error is less than 2 ns. The loss of lock indicator is a low current CMOS output.

Narrow Loop Bandwidth Control Pin (NBW Pin)

A Narrow Loop Bandwidth control pin (NBW pin) is included to adjust the PLL loop bandwidth. In normal (wide) bandwidth mode (NBW=0), the internal resistor Rin is 100kΩ. With the NBW pin asserted, the internal resistor Rin is changed to 2100kΩ. This lowers the loop bandwidth by a factor of about 21 (2100 / 100) and lowers the damping factor by about 4.6 (the square root of 21), assuming the same loop filter components.

Automatic Reference Clock Reselection

This device offers an automatic reference clock reselection feature for switching input reference clocks upon a reference clock failure. With the AUTO input pin set to high and the LOL output low, the device is placed into automatic reselection (AutoSwitch) mode.

Once in AutoSwitch mode, when LOL then goes high (due to a reference clock fault), the input clock reference is automatically reselected internally, as indicated by the state change of the REF_ACK output. Automatic clock reselection is made only once (it is non-revertive). Re-arming of automatic mode requires placing the device into manual selection (Manual Select) mode (AUTO pin low) before returning to AutoSwitch mode (AUTO pin high).

Using the AutoSwitch Feature

See also Table 6, Example AutoSwitch Sequence.

In application, the system is powered up with the device in Manual Select mode (AUTO pin is set low), allowing sufficient time for the reference clock and device PLL to settle. The REF_SEL input selects the reference clock to be used in Manual Select mode and the initial reference clock used in AutoSwitch mode. The REF_SEL input state must be maintained when switching to AutoSwitch mode (AUTO pin high) and must still be maintained until a reference fault occurs.

Once a reference fault occurs, the LOL output goes high and the input reference is automatically reselected. The REF_ACK output always indicates the reference selection status and the LOL output always indicates the PLL lock status.

A successful automatic reselection is indicated by a change of state of the REF_ACK output and a momentary level high of the LOL output (minimum high time is 10ns).

If an automatic reselection is made to a non-valid reference clock (one to which the PLL cannot lock), the REF_ACK *output will change state but the* LOL *output will remain high.*

No further automatic reselection is made; only one reselection is made each time the AutoSwitch mode is armed. AutoSwitch mode is re-armed by placing the device into Manual Select mode (AUTO pin low) and then into AutoSwitch mode again (AUTO pin high).

Following an automatic reselection and prior to selecting Manual Select mode (AUTO pin low), the REF_SEL pin has no control of reference selection. To prevent an unintential reference reselection, AutoSwitch mode must not be re-enabled until the desired state of the REF_SEL pin is set and the LOL output is low. It is recommended to delay the re-arming of AutoSwitch mode, following an automatic reselection, to ensure the PLL is fully locked on the new reference. In most system configurations, where loop bandwidth is in the range of 100-1000 Hz and damping factor below 10, a delay of 500 ms should be sufficient. Until the PLL is fully locked intermittent LOL pulses may occur.

Example AutoSwitch Sequence

0 = Low; 1 = High. Example with REF_SEL initially set to 0 (*i.e.,* DIF_REF0 selected)

REF_SEL Input	Selected Clock Input	REF_ACK Output	AUTO Input	LOL Output	Conditions
					Initialization
0	DIF_REF0	0	0	1	Device power-up. Manual Select mode. DIF_REF0 input selected reference, not yet locked to.
0	DIF_REF0	0	0	**-0-**	LOL to 0: Device locked to reference (may get intermittent LOL pulses until fully locked).
0	DIF_REF0	0	**-1-**	0	AUTO set to 1: Device placed in AutoSwitch mode (with DIF_REF0 as initial reference clock).
					Operation & Activation
0	DIF_REF0	0	1	0	Normal operation with AutoSwitch mode armed, with DIF_REF0 as initial reference clock.
0	DIF_REF0	0	1	**-1-**	LOL to 1: Clock fault on DIF_REF0, loss of lock indicated by LOL pin, ...
0	**-DIF_REF1-**	**-1-**	1	1	... and immediate automatic reselection to DIF_REF1 (indicated by REF_ACK pin).
0	DIF_REF1	1	1	**-0-**	LOL to 0: Device locks to DIF_REF1 (assuming valid clock on DIF_REF1).
					Re-initialization
-1-	DIF_REF1	1	1	0	REF_SEL set to 1: Prepares for Manual Selection of DIF_REF1 before then re-arming AutoSwitch.
1	DIF_REF1	1	**-0-**	0	AUTO set to 0: Manual Select mode entered briefly, manually selecting DIF_REF1 as reference.
1	DIF_REF1	1	**-1-**	0	AUTO set to 1: Device is placed in AutoSwitch mode (delay recommended to ensure device fully locked), re-initializing AutoSwitch with DIF_REF1 now specified as the initial reference clock.

Table 6: Example AutoSwitch Sequence

Hitless Switching Option

Hitless Switching is a device option that can be specified at time of order. (Please contact ICS.) The M2040-01 remains in wide bandwidth mode if NBW = 0.

When NBW = 0, placing the device into wide bandwidth operation, the optional Hitless Switching (HS) function will automatically place the device into narrow bandwidth operation during reference reselection. This provides a controlled output clock phase change while the PLL is acquiring phase lock to a new reference clock phase. The HS function is trigged by a loss of lock event. Wide bandwidth is resumed once the PLL relocks to the input reference. (When the NBW pin = 1, the device operates in narrow bandwidth continually and hence the HS mode does not apply).

The HS function is armed after the device locks to the input clock reference (8 successive phase detector clock cycles with LOL low). Once armed, HS is triggered by detection at the phase detector of a single phase error greater than 4 ns (rising edges).

Once triggered, the HS function narrows the loop bandwidth until the PLL is locked to the selected reference (8 successive phase detector clock cycles with LOL low).

When pin AUTO = 1 (automatic reference reselection mode) HS is used in conjunction with input reselection. When AUTO = 0 (manual mode), HS will still occur upon an input phase transient, however the clock input is not reselected (this enables hitless switching when using an external MUX for clock selection).

Power-Up Initialization Function (INIT Pin)

The initialization function provides a short-term override of the narrow bandwidth mode when the device is powered up in order to facilitate phase locking.

When INIT is set to logic 1, initialization is enabled. With NBW set to logic 1 (narrow bandwidth mode), the initialization function puts the PLL into wide bandwidth mode until eight consecutive phase detector cycles occur without a single LOL event. Once the eight valid PLL locked states have occurred, the PLL bandwidth is automatically reduced to narrow bandwidth mode.

When INIT is logic 0, the device is forced into wide bandwidth mode unconditionally.

External Loop Filter

The M2040 requires the use of an external loop filter components. These are connected to the provided filter pins (see Figure 5).

Because of the differential signal path design, the implementation consists of two identical complementary RC filters as shown in Figure 5, below.

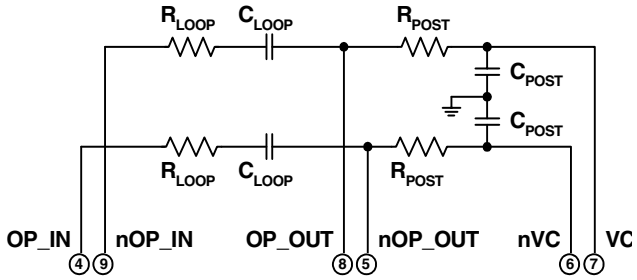


Figure 5: External Loop Filter

PLL bandwidth is affected by the total "M" (feedback divider) value, loop filter component values, and other device parameters. See Table 7, External Loop Filter Component Values, below.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

External Loop Filter Component Values [1]

VCSO Parameters: K_{VCO} = 800kHz/V, VCO Bandwidth = 700kHz. See AC Characteristics on pg. 9 for PLL Loop Constants.

Device Configuration			External Loop Filter Component Values				NBW Mode[2]	Nominal Performance Using These Values		
F_{VCSO} (MHz)		M Divider Value	R loop	C loop	R post	C post		PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
533.333		30, 32	30kΩ	1.0µF	33kΩ	100pF	1	110 Hz	2.2	0.35
							0	3 kHz	10	0.02

Table 7: External Loop Filter Component Values

Note 1: Recommended values for hitless switching. For PLL Simulator software, go to www.icst.com.

Note 2: NBW mode 1 = Narrow Bandwidth, where R_{IN} = 2100 kΩ. NBW mode 0 = Wide Bandwidth, where R_{IN} = 100 kΩ

Note 3: This table does not apply to the 400 MHz VCSO option since the Kvco value is different.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 8: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 9: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = 400-534, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			175	225	mA	
Differential Input: LVDS / LVPECL	V_{P-P}	Peak to Peak Input Voltage [1]	DIF_REF, nDIF_REF	0.15			V	
	V_{CMR}	Common Mode Input [1]		0.5		V_{cc} - 0.85	V	
LVCMOS / LVTTL Input	V_{IH}	Input High Voltage	REF_SEL, MR_SEL	2		V_{cc} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		1.3	V	
Inputs with Pull-down	I_{IH}	Input High Current	DIF_REF1, DIF_REF0			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ	
Inputs with Pull-up	I_{IH}	Input High Current	FIN_SEL1, FIN_SEL0, INIT, MR_SEL			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current		-150			µA	
	R_{pullup}	Internal Pull-up Resistor			51		kΩ	
Inputs biased to Vcc/2 [2]			nDIF_REF1, nDIF_REF0		(Note 2)			
All Inputs	C_{IN}	Input Capacitance	All Inputs			4	pF	
Differential Outputs	V_{OH}	Output High Voltage	FOUT1, nFOUT1 FOUT0, nFOUT0	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [3]		0.4		0.85	V	
LVCMOS Outputs	V_{OH}	Output High Voltage, Lock	LOL , REF_ACK	2.4		V_{CC}	V	I_{OH}= 1mA
	V_{OL}	Output Low Voltage, Lock		GND		0.4	V	I_{OL}= 1mA

Table 10: DC Characteristics

Note 1: Single-ended measurement. See Figure 7, Differential Input Level on pg. 10.
Note 2: Biased to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground.
Note 3: Single-ended measurement. See Figure 6, Input and Output Rise and Fall Time on pg. 10.

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = 400-534, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF1, nDIF_REF1, DIF_REF0, nDIF_REF0	200		285	MHz	
	F_{OUT}	Output Frequency	FOUT1, nFOUT1, FOUT0, nFOUT0	200		534	MHz	
	APR	VCSO Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain	M2040-xx-400.0000		1600		kHz/V	
			M2040-xx-533.3334		800		kHz/V	
	R_{IN}	Internal Loop Resistor	NBW = 0		100		kΩ	
			NBW = 1		2100		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-72		dBc/Hz	
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms)	12kHz to 20MHz		0.25	0.5	ps	
			50kHz to 80MHz		0.25	0.5	ps	
	odc	Output Duty Cycle [2]	F_{OUT} =200-285MHz P = 2 (P_SEL = 1)	45	50	55	%	
			F_{OUT}= 400-534MHz P = 1 (P_SEL = 0)	40	50	60	%	
	t_R	Output Rise Time [2] for FOUT1, nFOUT1, FOUT0, nFOUT0	F_{OUT} =200-285MHz P = 2 (P_SEL = 1)	325	425	500	ps	20% to 80%
			F_{OUT}= 400-534MHz P = 1 (P_SEL = 0)	200	275	350	ps	
	t_F	Output Fall Time [2] for FOUT1, nFOUT1, FOUT0, nFOUT0	F_{OUT} =200-285MHz P = 2 (P_SEL = 1)	325	425	500	ps	20% to 80%
			F_{OUT}= 400-534MHz P = 1 (P_SEL = 0)	200	275	350	ps	
	t_{LOCK}	PLL Lock Time				100	ms	

Table 11: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 7, External Loop Filter Component Values, on pg. 7.
Note 2: See Parameter Measurement Information on pg. 10.

PARAMETER MEASUREMENT INFORMATION

Input and Output Rise and Fall Time

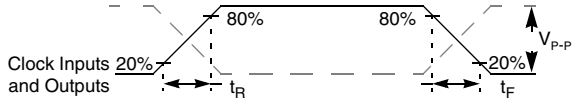


Figure 6: Input and Output Rise and Fall Time

Differential Input Level

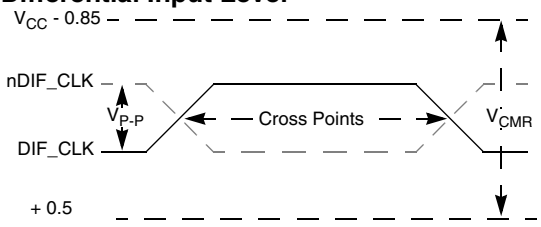
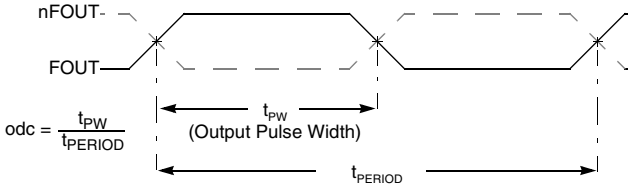


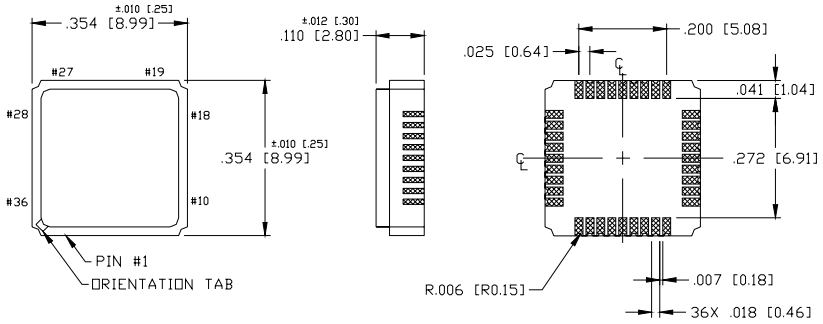
Figure 7: Differential Input Level

Output Duty Cycle



DEVICE PACKAGE - 9 x 9mm SMT CERAMIC

Mechanical Dimensions:



Refer to the M2040 product web page at www.icst.com/products/summary/m2040.htm for links to recommended PCB footprint, solder mask, furnace profile, and related information.

NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

Figure 9: Device Package - 9 x 9mm SMT Ceramic

ORDERING INFORMATION

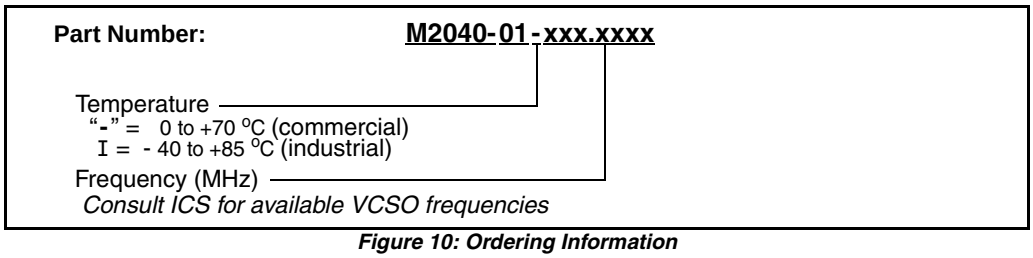


Figure 10: Ordering Information

Example Part Numbers

VCSO Freq (MHz)	Temperature	Part Number
400.0000	commercial	**M2040-01- 400.0000**
	industrial	**M2040-01I 400.0000**
533.3334	commercial	**M2040-01- 533.3334**
	industrial	**M2040-01I 533.3334**

Table 12: Example Part Numbers

Consult ICS for the availability of other VCSO frequencies.